

# DRV8143-Q1 Automotive Half Bridge Driver with Integrated Current Sense and Diagnostics

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- 4.5-V to 35-V (40-V abs. max) operating range
- SPI(S) or HW(H) variant in VQFN-HR package:  $R_{ON\_LS} + R_{ON\_HS}$ : 42m $\Omega$
- SPI(P) variant in HVSSOP package:  $R_{ON\_LS} + R_{ON\_HS}$ : 49m $\Omega$
- $I_{OUT\ Max} = 20\text{A}$
- PWM frequency operation up to 125KHz with automatic dead time assertion
- Configurable slew rate and spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated current sense (eliminates shunt resistor)
- Proportional load current output on IPROPI pin
- Configurable current regulation
- Protection and diagnostic features with configurable fault reaction (latched or retry)
  - Load diagnostics in both the off-state and on-state to detect open load and short circuit
  - Voltage monitoring on supply (VM) and charge pump (VCP)
  - Over current protection
  - Over temperature protection
  - Fault indication on nFAULT pin
- Supports 3.3V, 5V logic inputs
- Low sleep current - 1 $\mu\text{A}$  typical at 25 $^{\circ}\text{C}$
- [Device family comparison table](#)

## 2 Applications

- [Automotive brushed DC motors, Solenoids](#)
- [Door modules and seat modules](#)
- [Body control module \(BCM\)](#)
- [Fuel, water, oil pumps](#)
- [On board charger](#)

## 3 Description

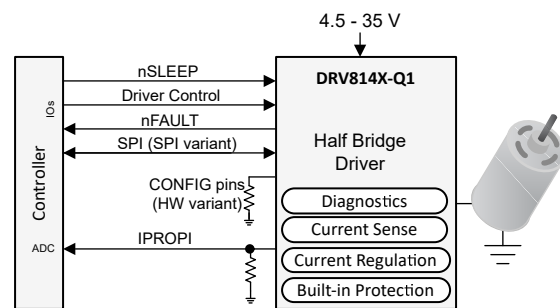
The DRV814x-Q1 family of devices is a fully integrated half-bridge driver intended for a wide range of automotive applications. Designed in a BiCMOS high power process technology node, this monolithic family of devices in a power package offer excellent power handling and thermal capability while providing compact package size, ease of layout, EMI control, accurate current sense, robustness, and diagnostic capability. This family provides an identical pin function with scalable  $R_{ON}$  (current capability) to support different loads.

The devices integrate a N-channel half-bridge, charge pump regulator, high-side current sensing with regulation, current proportional output, and protection circuitry. A low-power sleep mode is provided to achieve low quiescent current. The devices offer voltage monitoring and load diagnostics as well as protection features against over current and over temperature. Fault conditions are indicated on nFAULT pin. DRV8143 and DRV8145 are available in three variants - hardwired interface: HW (H) and two SPI interface variants: SPI(P) and SPI(S), with SPI (P) for externally supplied logic supply and SPI (S) for internally generated logic supply. DRV8144 is available only in two variants: SPI(S) and HW(H). The SPI interface variants offer more flexibility in device configuration and fault observability.

### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE      | BODY SIZE (nominal) |
|-------------|--------------|---------------------|
| DRV8143-Q1  | VQFN-HR (14) | 3mm X 4.5mm         |
| DRV8143-Q1  | HVSSOP (28)  | 3mm X 7.3mm         |

- (1) For all available packages, see the orderable addendum at the end of the data sheet



**Simplified Schematic**

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## 4 Device Comparison

Table 4-1 summarizes the  $R_{ON}$  and package differences between devices in the DRV814x-Q1 family.

**Table 4-1. Device Comparison**

| PART NUMBER <sup>(1)</sup> | (LS + HS) $R_{ON}$ | $I_{OUT\ MAX}$ | PACKAGE      | BODY SIZE (nominal) | Variants        |
|----------------------------|--------------------|----------------|--------------|---------------------|-----------------|
| DRV8143-Q1                 | 42m $\Omega$       | 20A            | VQFN-HR (14) | 3mm X 4.5mm         | HW (H), SPI (S) |
| DRV8143-Q1                 | 49m $\Omega$       | 20A            | HVSSOP (28)  | 3mm X 7.3mm         | HW (H), SPI (P) |
| DRV8144-Q1                 | 23.6m $\Omega$     | 30A            | VQFN-HR (16) | 3mm X 6mm           | HW (H), SPI (S) |
| DRV8145-Q1                 | 16m $\Omega$       | 46A            | VQFN-HR (16) | 3.5mm X 5.5mm       | HW (H), SPI (S) |
| DRV8145-Q1                 | 19m $\Omega$       | 46A            | HTSSOP (28)  | 4.4mm X 9.7mm       | SPI (P)         |

(1) This is the product datasheet for the DRV8143-Q1. Please reference other device variant data sheets for additional information.

Table 4-2 summarizes the feature differences between the SPI and HW interface variants in the DRV814x-Q1 family. In general, the SPI variant offers more configurability, bridge control options, diagnostic feedback, redundant driver shutoff, improved Pin FMEA, and additional features.

In addition, the SPI variant has two options - **SPI (S) variant and SPI (P) variant**. The SPI (P) variant supports an external, low voltage 5V supply to the device through the VDD pin for the device logic, whereas in the SPI (S) variant, this supply is internally derived from the VM pin. With this external logic supply, the SPI (P) variant avoids device brown out (reset of device) during VM under voltage transients.

### Note

DRV8144-Q1 is NOT available in SPI(P) variant.

**Table 4-2. SPI Variant vs HW Variant Comparison**

| FUNCTION  | HW (H) Variant                                 | SPI (S) Variant  | SPI (P) Variant           |
|---|--|--|---------------------------|
| Bridge control  | Pin only                                       | Individual pin "and/or" register bit with pin status indication (Refer Register Pin control) |                           |
| Sleep function  | Available through nSLEEP pin                   |  | Not available             |
| External logic supply to the device                                       | Not supported                                  | Not supported  | Supported through VDD pin |
| Clear fault command   | Reset pulse on nSLEEP pin                      | SPI CLR_FAULT command  |                           |
| Slew rate   | 6 levels                                       | 8 levels   |                           |
| Over current protection (OCP)   | Fixed at the highest setting                   | 3 choices for thresholds, 4 choices for filter time  |                           |
| ITRIP regulation  | 5 levels with disable & fixed TOFF time        | 7 levels with disable & indication, with programmable TOFF time                              |                           |
| Individual fault reaction configuration between retry or latched behavior | Not supported, either all latched or all retry | Supported  |                           |
| Detailed fault logging and device status feedback                         | Not supported, nFAULT pin monitoring necessary | Supported, nFAULT pin monitoring optional  |                           |
| VM over voltage   | Fixed  | 4 threshold choices  |                           |
| On-state (Active) diagnostics   | Not supported                                  | Supported for high-side loads  |                           |
| Spread spectrum clocking (SSC)  | Not supported                                  | Supported  |                           |

**Table 4-3. Differentiating between devices in the family**

| Device      | Package Symbolization | DEVICE_ID Register |
|-------------|-----------------------|--------------------|
| DRV8143H-Q1 | 8143H                 | Not applicable     |
| DRV8144H-Q1 | 8144H                 | Not applicable     |
| DRV8145H-Q1 | 8145H                 | Not applicable     |
| DRV8143S-Q1 | 8143S                 | 0 x BA             |
| DRV8144S-Q1 | 8144S                 | 0 x CA             |

**Table 4-3. Differentiating between devices in the family (continued)**

| Device      | Package Symbolization | DEVICE_ID Register |
|-------------|-----------------------|--------------------|
| DRV8145S-Q1 | 8145S                 | 0 x DA             |
| DRV8143P-Q1 | 8143P                 | 0 x BE             |
| DRV8145P-Q1 | 8145P                 | 0 x DE             |

## 5 Pin Configuration and Functions

### 5.1 HW Variant

#### 5.1.1 VQFN-HR (14) package

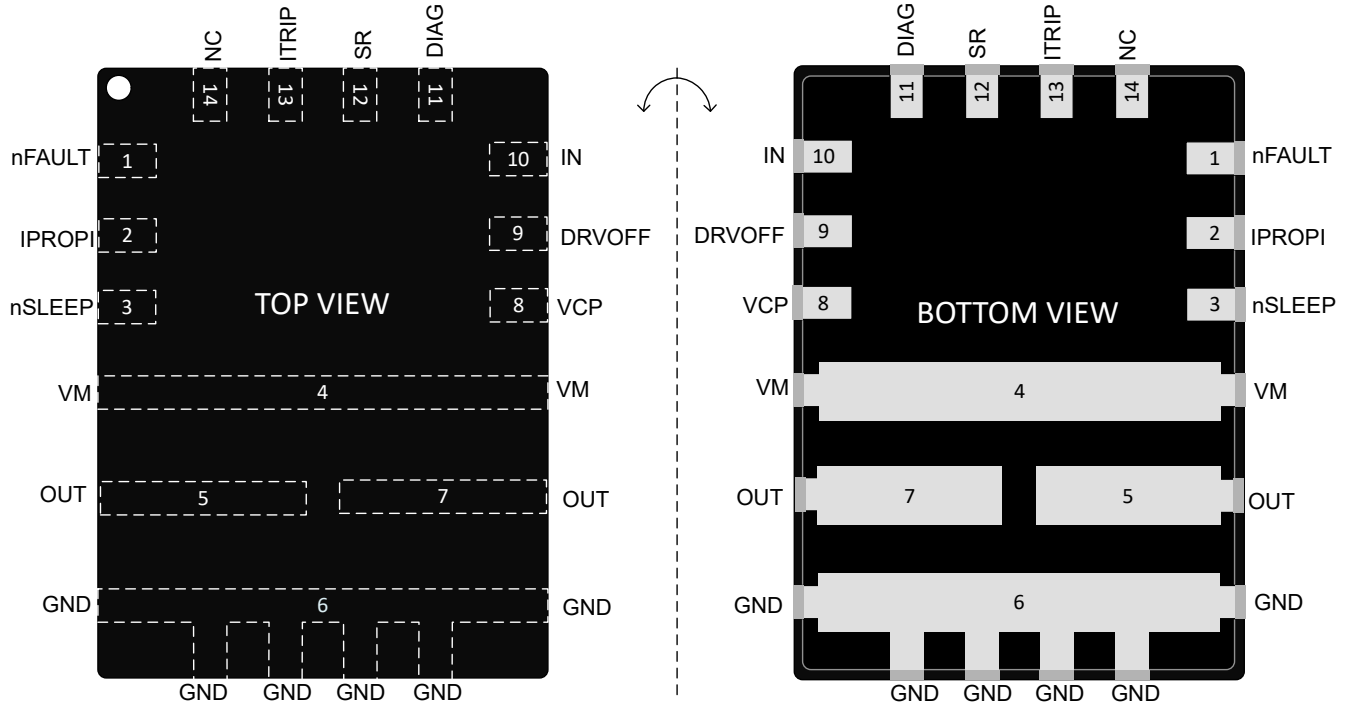


Figure not drawn to scale

**Figure 5-1. DRV8143H-Q1 HW variant in VQFN-HR (14) package**

**Table 5-1. Pin Functions**

| PIN |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|--------|---------------------|--|
| NO. | NAME   |                     |  |
| 1   | nFAULT | OD                  | Fault indication to the controller. For details, refer to <b>nFAULT</b> in the <a href="#">Device Configuration section</a> .                                      |
| 2   | IPROPI | I/O                 | Driver load current analog feedback. For details, refer to <b>IPROPI</b> in the <a href="#">Device Configuration section</a> .                                     |
| 3   | nSLEEP | I                   | Controller input pin for SLEEP. For details, see the <a href="#">Bridge Control section</a> .  |
| 4   | VM     | P                   | Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1- $\mu$ F ceramic capacitor and a bulk capacitor.                             |
| 5,7 | OUT    | P                   | Half-bridge output. Connect this pin to the motor or load. Must combine with the other OUT pin to support device current capability.                               |
| 6   | GND    | G                   | Ground pin   |
| 8   | VCP    | P                   | Charge Pump pin for storage cap. Connect a 6.3V, 1 $\mu$ F capacitor to VM supply.   |
| 9   | DRVOFF | I                   | Controller input pin for bridge Hi-Z. For details, see the <a href="#">Bridge Control section</a> .  |
| 10  | IN     | I                   | Controller input pin for bridge operation. For details, see the <a href="#">Bridge Control section</a> .   |
| 11  | DIAG   | I                   | Device configuration pin for load type indication. For details, refer to <b>DIAG</b> in the <a href="#">Device Configuration section</a>                           |
| 12  | SR     | I                   | Device configuration pin for Slew Rate control . For details, refer to <a href="#">Slew Rate</a> in the <a href="#">Device Configuration section</a> .             |
| 13  | ITRIP  | I                   | Device configuration pin for ITRIP level for high-side current limiting . For details, refer to <b>ITRIP</b> in the <a href="#">Device Configuration section</a> . |

**Table 5-1. Pin Functions (continued)**

| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION |
|-----|------|---------------------|-------------|
| NO. | NAME |                     |             |
| 14  | NC   | I                   | No connect  |

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

**5.1.2 HVSSOP (28) package**

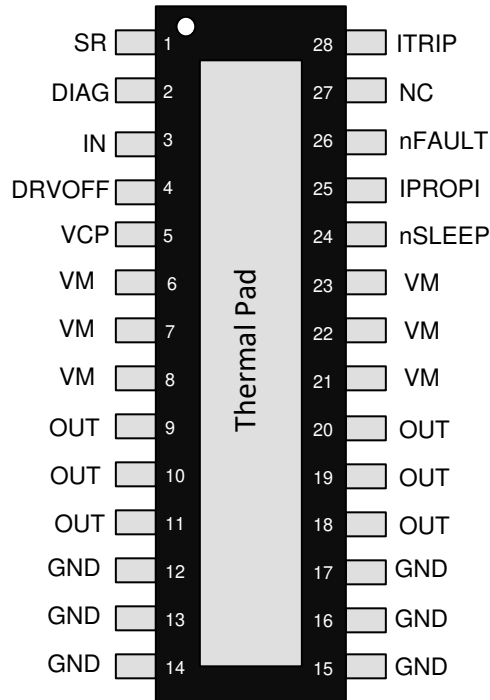


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**Figure 5-2. DRV8143H -Q1 HW variant in HVSSOP (28) package**

**Table 5-2. Pin Functions**

| PIN                    |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|------------------------|--------|---------------------|--|
| NO.                    | NAME   |                     |  |
| 1                      | SR     | I                   | Device configuration pin for Slew Rate control. For details, refer to <a href="#">Slew Rate</a> in the <a href="#">Device Configuration</a> section.   |
| 2                      | DIAG   | I                   | Device configuration pin for load type indication. For details, refer to <a href="#">DIAG</a> in the <a href="#">Device Configuration</a> section.   |
| 3                      | IN     | I                   | Controller input pin for bridge operation. For details, see the <a href="#">Bridge Control</a> section.  |
| 4                      | DRVOFF | I                   | Controller input pin for bridge Hi-Z. For details, see the <a href="#">Bridge Control</a> section.   |
| 5                      | VCP    | P                   | Charge Pump pin for storage cap. Connect a 6.3V, 1µF capacitor to VM supply.   |
| 6, 7, 8, 21, 22, 23    | VM     | P                   | Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor. |
| 9, 10, 11, 18, 19, 20  | OUT    | P                   | Half-bridge output. Connect this pin to the motor or load. Must combine with the rest of OUT pins (6 total) to support device current capability.  |
| 12, 13, 14, 15, 16, 17 | GND    | G                   | Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.   |
| 24                     | nSLEEP | I                   | Controller input pin for SLEEP. For details, see the <a href="#">Bridge Control</a> section.   |
| 25                     | IPROPI | O                   | Driver load current analog feedback. For details, refer to <a href="#">IPROPI</a> in the <a href="#">Device Configuration</a> section.   |

**Table 5-2. Pin Functions (continued)**

| PIN |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|--------|---------------------|--|
| NO. | NAME   |                     |  |
| 26  | nFAULT | OD                  | Fault indication to the controller. For details, refer to nFAULT in the <a href="#">Device Configuration section</a> .                                     |
| 27  | NC     | I                   | No connect   |
| 28  | ITRIP  | I/O                 | Device configuration pin for ITRIP level for high-side current limiting. For details, refer to ITRIP in the <a href="#">Device Configuration section</a> . |

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

## 5.2 SPI Variant

### 5.2.1 HVSSOP (28) package

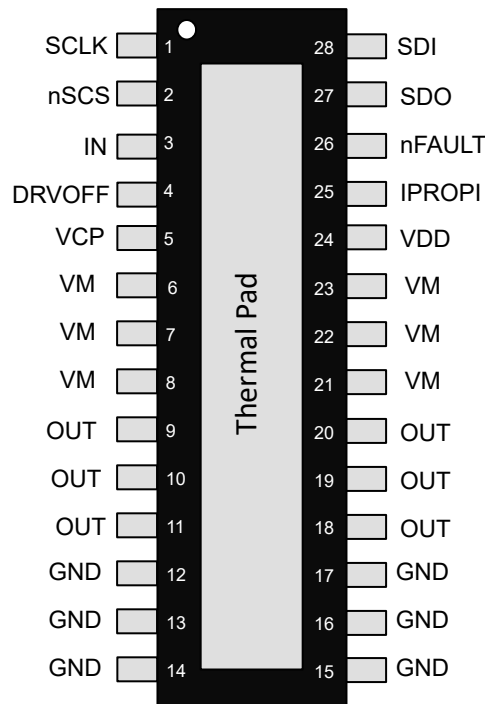


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SPI (P) variant

**Figure 5-3. DRV8143P-Q1 SPI(P) variant in HVSSOP (28) package**

**Table 5-3. Pin Functions**

| PIN                   |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----------------------|--------|---------------------|--|
| NO.                   | NAME   |                     |  |
| 1                     | SCLK   | I                   | SPI - Serial Clock input.  |
| 2                     | nSCS   | I                   | SPI - Chip Select. An active low on this pin enables the serial interface communication.   |
| 3                     | IN     | I                   | Controller input pin for bridge operation. For details, see the <a href="#">Bridge Control section</a> .   |
| 4                     | DRVOFF | I                   | Controller input pin for bridge Hi-Z. For details, see the <a href="#">Bridge Control section</a> .  |
| 5                     | VCP    | P                   | Charge Pump pin for storage cap. Connect a 6.3V, 1µF capacitor to VM supply.   |
| 6, 7, 8, 21, 22, 23   | VM     | P                   | Power supply. This pin is the motor supply voltage. Must combine with the rest of VM pins (6 total) to support device current capability. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor. |
| 9, 10, 11, 18, 19, 20 | OUT    | P                   | Half-bridge output. Connect this pin to the motor or load. Must combine with the rest of OUT pins (6 total) to support device current capability.  |

**Table 5-3. Pin Functions (continued)**

| PIN                       |        | TYPE <sup>(1)</sup> | DESCRIPTION   |
|---------------------------|--------|---------------------|---|
| NO.                       | NAME   |                     |   |
| 12, 13, 14,<br>15, 16, 17 | GND    | G                   | Ground pin. Must combine with the rest of GND pins (6 total) to support device current capability.                      |
| 24                        | VDD    | P                   | Logic power supply to the device.   |
| 25                        | IPROPI | I/O                 | Driver load current analog feedback. For details, refer to IPROPI in the <a href="#">Device Configuration section</a> . |
| 26                        | nFAULT | OD                  | Fault indication to the controller. For details, refer to nFAULT in the <a href="#">Device Configuration section</a> .  |
| 27                        | SDO    | PP                  | SPI - Serial Data Output. Data is updated at the rising edge of SCLK.   |
| 28                        | SDI    | I                   | SPI - Serial Data Input. Data is captured at the falling edge of SCLK.  |

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

### 5.2.2 VQFN-HR (14) package

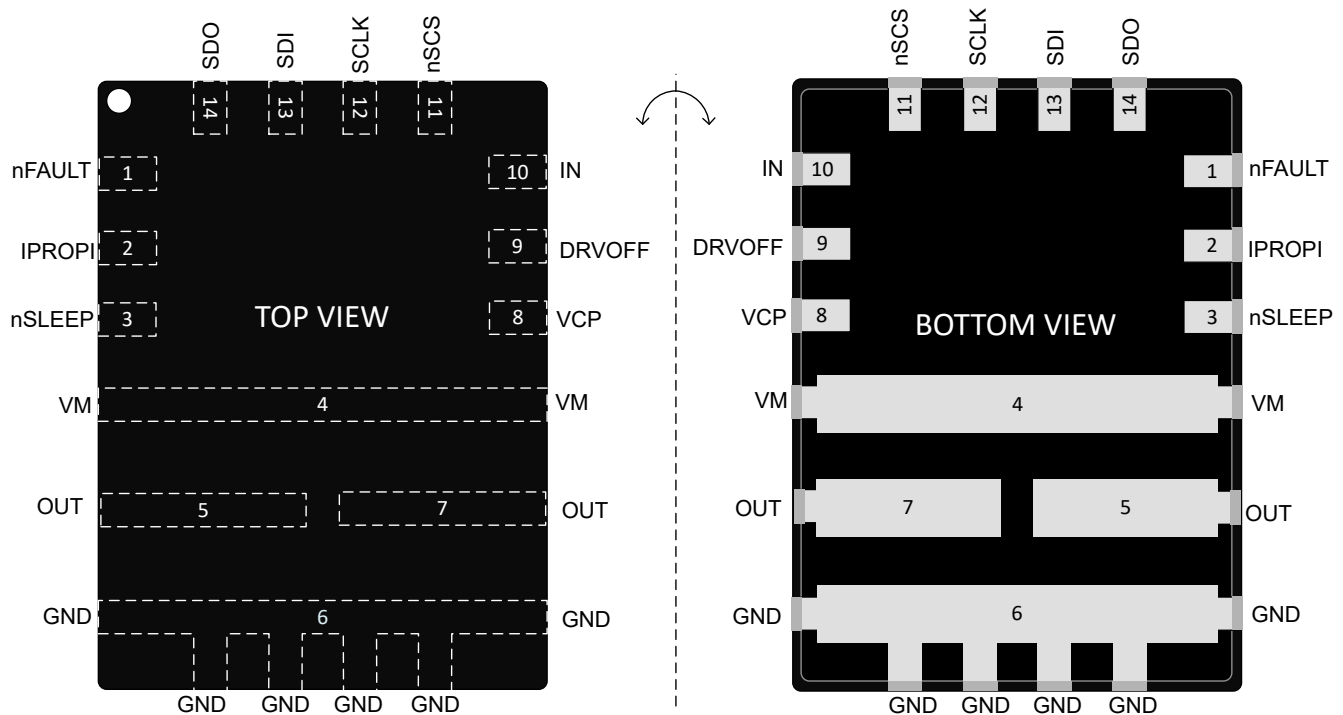


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**Figure 5-4. DRV8143S-Q1 SPI(S) variant in VQFN-HR (14) package**

**Table 5-4. Pin Functions**

| PIN |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|--------|---------------------|--|
| NO. | NAME   |                     |  |
| 1   | nFAULT | OD                  | Fault indication to the controller. For details, refer to nFAULT in the <a href="#">Device Configuration section</a> .                 |
| 2   | IPROPI | I/O                 | Driver load current analog feedback. For details, refer to IPROPI in the <a href="#">Device Configuration section</a> .                |
| 3   | nSLEEP | I                   | Controller input pin for SLEEP. For details, see the <a href="#">Bridge Control section</a> .  |
| 4   | VM     | P                   | Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1- $\mu$ F ceramic capacitor and a bulk capacitor. |
| 5,7 | OUT    | P                   | Half-bridge output. Connect this pin to the motor or load. Must combine with the other OUT pin to support device current capability.   |



**Table 5-4. Pin Functions (continued)**

| PIN |        | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|--------|---------------------|--|
| NO. | NAME   |                     |  |
| 6   | GND    | G                   | Ground pin   |
| 8   | VCP    | P                   | Charge Pump pin for storage cap. Connect a 6.3V, 1µF capacitor to VM supply.                             |
| 9   | DRVOFF | I                   | Controller input pin for bridge Hi-Z. For details, see the <a href="#">Bridge Control section</a> .      |
| 10  | IN     | I                   | Controller input pin for bridge operation. For details, see the <a href="#">Bridge Control section</a> . |
| 11  | nSCS   | I                   | SPI - Chip Select. An active low on this pin enables the serial interface communication.                 |
| 12  | SCLK   | I                   | SPI - Serial Clock input.  |
| 13  | SDI    | I                   | SPI - Serial Data Input. Data is captured at the falling edge of SCLK. Also VIO logic level for SDO.     |
| 14  | SDO    | PP                  | SPI - Serial Data Output. Data is updated at the rising edge of SCLK.                                    |

(1) I = input, O = output, I/O = input/output, G = ground, P = power, OD = open-drain output, PP = push-pull output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)<sup>(1)</sup>

|  |                      | MIN                               | MAX            | UNIT |
|--|----------------------|-----------------------------------|----------------|------|
| Power supply pin voltage                               | VM                   | -0.3 <sup>(3)</sup>               | 40             | V    |
| Power supply transient voltage ramp                    | VM                   |                                   | 2              | V/μs |
| Charge pump pin voltage                                | VCP                  | $V_{VM} - 0.3$                    | $V_{VM} + 7$   | V    |
| Output pin voltage                                     | OUT                  | -0.9                              | $V_{VM} + 0.9$ | V    |
| Output pin current                                     | OUT                  | Internally limited <sup>(2)</sup> |                | A    |
| Driver disable pin voltage                             | DRVOFF               | -0.3                              | 40             | V    |
| Logic I/O voltage                                      | IN, nFAULT           | -0.3                              | 5.75           | V    |
| HW variant - Configuration pins voltage                | ITRIP, SR, DIAG      | -0.3                              | 5.75           | V    |
| Analog feedback pin voltage                            | IPROPI               | -0.3                              | 5.75           | V    |
| Sleep pin voltage (Not applicable for SPI (P) variant) | nSLEEP               | -0.3                              | 40             | V    |
| SPI I/O voltage - SPI variant                          | SDI, SDO, nSCS, SCLK | -0.3                              | 5.75           | V    |
| SPI (P) variant - Logic supply                         | VDD                  | -0.3                              | 5.75           | V    |
| SPI (P) variant - Logic supply transient voltage ramp  | VDD                  |                                   | 5              | V/μs |
| Ambient temperature, $T_A$                             |                      | -40                               | 125            | °C   |
| Junction temperature, $T_J$                            |                      | -40                               | 150            | °C   |
| Storage temperature, $T_{stg}$                         |                      | -65                               | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Limited by the over current and over temperature protection functions of the device
- (3) With external component support, short duration violation of this limit can be tolerated during ISO 7637 transient pulse testing

### 6.2 ESD Ratings

|             |                         |   | VALUE          | UNIT  |   |
|-------------|-------------------------|---|----------------|-------|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup><br>HBM ESD Classification Level 2 | VM, OUT, GND   | ±4000 | V |
|             |                         |   | All other pins | ±2000 |   |
|             |                         | Charged device model (CDM), per AEC Q100-011<br>CDM ESD Classification Level C4B          | Corner pins    | ±750  |   |
|             |                         |   | Other pins     | ±500  |   |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

|                |  |                            | MIN      | MAX                | UNIT |
|----------------|--|----------------------------|----------|--------------------|------|
| $V_{VM}$       | Power supply voltage                   | VM                         | 4.5      | 35 <sup>(1)</sup>  | V    |
| $V_{VDD}$      | SPI (P) variant - Logic supply voltage | VDD                        | 4.5      | 5.5                | V    |
| $V_{VCP}$      | Charge pump pin voltage                | VCP                        | $V_{VM}$ | $V_{VM}+5.5$       | V    |
| $V_{LOGIC}$    | Logic pin voltage                      | IN, nSLEEP, DRVOFF, nFAULT | 0        | 5.5                | V    |
| $f_{PWM}$      | PWM frequency                          | IN                         | 0        | 125                | KHz  |
| $V_{CONFIG}$   | HW variant - Configuration pin voltage | ITRIP, SR, DIAG            | 0        | 5.5                | V    |
| $V_{IPROPI}$   | Analog feedback voltage                | IPROPI                     | 0        | 5.5                | V    |
| $V_{SPL\_IOS}$ | SPI (S) variant - SPI pin voltage      | SDI, SDO, nSCS, SCLK       | 0        | $V_{nSLEEP} + 0.5$ | V    |
|                | SPI (P) variant - SPI pin voltage      | SDI, SDO, nSCS, SCLK       | 0        | $V_{VDD} + 0.5$    | V    |
| $T_A$          | Operating ambient temperature          |                            | -40      | 125                | °C   |
| $T_J$          | Operating junction temperature         |                            | -40      | 150                | °C   |

(1) The over current protection function does not support short on OUT to VM or GND above 28 V for short inductance < 1  $\mu$ H.

### 6.4 Thermal Information

Refer [Transient thermal impedance](#) table for application related use case.

| THERMAL METRIC <sup>(1)</sup> |  | HVSSOP package | VQFN-HR package | UNIT |
|-------------------------------|--|----------------|-----------------|------|
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 31.0           | 48.4            | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case(top) thermal resistance     | 29.1           | 22.3            | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 9.3            | 8.1             | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.4            | 0.5             | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 9.3            | 7.9             | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case(bottom) thermal resistance  | 1.3            | N/A             | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Electrical Characteristics

4.5 V (falling)  $\leq V_{VM} \leq 35$  V,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$  (unless otherwise noted)

For SPI (P) variant only: 4.5 V  $\leq V_{VDD} \leq 5.5$  V (unless otherwise noted)

#### 6.5.1 Power Supply & Initialization

Refer [wake up transient](#) waveforms

| PARAMETER     | TEST CONDITIONS                           | MIN  | TYP | MAX | UNIT          |
|---------------|---|--|-----|-----|---------------|
| $V_{VM\_REV}$ | Supply pin voltage during reverse current |  | 1.4 |     | V             |
| $I_{VMQ}$     | VM current in SLEEP state                 | $V_{VM} = 13.5\text{V}$ , $V_{nSLEEP} = 0\text{V}$ or $V_{VDD} < \text{POR}_{VDD\_FALL}$ , $T_A = 25^\circ\text{C}$  | 1   |     | $\mu\text{A}$ |
|               |   | $V_{VM} = 13.5\text{V}$ , $V_{nSLEEP} = 0\text{V}$ or $V_{VDD} < \text{POR}_{VDD\_FALL}$ , $T_A = 125^\circ\text{C}$ |     | 5.8 | $\mu\text{A}$ |
| $I_{VMS}$     | VM current in STANDBY state               |  | 3   | 5   | mA            |
| $I_{VDD}$     | VDD current in ACTIVE state               |  |     | 10  | mA            |
| $t_{RESET}$   | RESET pulse filter time                   |  | 5   | 20  | $\mu\text{s}$ |
| $t_{SLEEP}$   | SLEEP command filter time                 |  | 40  | 120 | $\mu\text{s}$ |

| PARAMETER              |  | TEST CONDITIONS  | MIN | TYP                | MAX | UNIT |
|------------------------|--|--|-----|--------------------|-----|------|
| t <sub>SLEEP_SPI</sub> | SLEEP command filter time  | Sleep signal on nSLEEP pin for SPI (S) variant   | 5   |                    | 20  | μs   |
| t <sub>WAKEUP</sub>    | Wake-up command filter time  | Wake-up signal on nSLEEP pin for HW (H) and SPI (S) variants   |     | 10                 |     | μs   |
| t <sub>COM</sub>       | Time for communication to be available after wake-up or power-up through VM or VDD supply pin                | Wake-up signal on nSLEEP pin or power cycle - V <sub>VM</sub> > V <sub>VM_POR_RISE</sub> or V <sub>VDD</sub> > V <sub>VDD_POR_RISE</sub>                       |     |                    | 400 | μs   |
| t <sub>READY</sub>     | Time for driver ready to be driven after wake-up through nSLEEP pin or power-up through VM or VDD supply pin | Wake-up signal on nSLEEP pin or power cycle - V <sub>VM</sub> > V <sub>VM_POR_RISE</sub> or V <sub>VDD</sub> > V <sub>VDD_POR_RISE</sub> , 1 μF cap on VCP pin |     |                    | 3.5 | ms   |
| V <sub>VCP</sub>       | Charge pump regulator voltage  | V <sub>VM</sub> > 7 V  |     | V <sub>VM</sub> +5 |     | V    |
| f <sub>VCP</sub>       | Average Charge pump switching frequency  |  |     | 20                 |     | MHz  |

### 6.5.2 Logic I/Os

| PARAMETER                |  | TEST CONDITIONS                       | MIN  | TYP | MAX  | UNIT |
|--------------------------|--|---------------------------------------|------|-----|------|------|
| V <sub>IL_nSLEEP</sub>   | Input logic low voltage  | nSLEEP pin                            |      |     | 0.65 | V    |
| V <sub>IH_nSLEEP</sub>   | Input logic high voltage   | nSLEEP pin                            | 1.55 |     |      | V    |
| V <sub>IHYS_nSLEEP</sub> | Input hysteresis   | nSLEEP pin                            |      | 200 |      | mV   |
| V <sub>IL</sub>          | Input logic low voltage  | DRVOFF, IN pins                       |      |     | 0.7  | V    |
| V <sub>IH</sub>          | Input logic high voltage   | DRVOFF, IN pins                       | 1.5  |     |      | V    |
| V <sub>IHYS</sub>        | Input hysteresis   | DRVOFF, IN pins                       |      | 100 |      | mV   |
| R <sub>PD_nSLEEP</sub>   | Internal pull-down resistance on nSLEEP to GND                         | Measured at min V <sub>IL</sub> level | 100  |     | 400  | KΩ   |
| R <sub>PU</sub>          | Internal pull-up resistance to VDD (reverse current blocked) on DRVOFF | Measured at min V <sub>IH</sub> level | 200  |     | 550  | KΩ   |
| R <sub>PD</sub>          | Internal pull-down resistance to GND on IN                             | Measured at max V <sub>IL</sub> level | 200  |     | 500  | KΩ   |
| I <sub>nFAULT_PD</sub>   | Sink current to GND on nFAULT pin when asserted low                    | V <sub>nFAULT</sub> = 0.3 V           | 5    |     |      | mA   |

### 6.5.3 SPI I/Os

| PARAMETER            |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|----------------------|--|--|-----|-----|-----|------|
| R <sub>PU_nSCS</sub> | Internal pull-up resistance to VDD (reverse current blocked) on nSCS | Measured at min V <sub>IH</sub> level                                      | 200 |     | 500 | KΩ   |
| R <sub>PD_SPI</sub>  | Internal pull-down resistance to GND on SDI, SCLK                    | Measured at max V <sub>IL</sub> level                                      | 150 |     | 500 | KΩ   |
| V <sub>IL</sub>      | Input logic low voltage  | SDI, SCLK, nSCS pins   |     |     | 0.7 | V    |
| V <sub>IH</sub>      | Input logic high voltage   | SDI, SCLK, nSCS pins   | 1.5 |     |     | V    |
| V <sub>IHYS</sub>    | Input hysteresis   | SDI, SCLK, nSCS pins   |     | 100 |     | mV   |
| V <sub>OL_SDO</sub>  | Output logic low voltage   | 0.5 mA sink into SDO   |     |     | 0.4 | V    |
| V <sub>OH_SDO</sub>  | Output logic high voltage for SPI (S) variant                        | 0.5 mA source from SDO, V <sub>nSLEEP</sub> = 5 V, V <sub>VM</sub> > 7 V   | 4.1 |     |     | V    |
|                      |  | 0.5 mA source from SDO, V <sub>nSLEEP</sub> = 3.3 V, V <sub>VM</sub> > 5 V | 2.7 |     |     | V    |
|                      | Output logic high voltage for SPI (P) variant                        | 0.5 mA source from SDO, V <sub>VDD</sub> = 5 V                             | 4.5 |     |     | V    |

| PARAMETER              |   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|------------------------|---|---|-----|-----|-----|------|
| V <sub>OH_SDO_NL</sub> | Output logic high voltage at no load on SDO, valid only for SPI (S) variant | No current from SDO, V <sub>nSLEEP</sub> = 5 V, V <sub>VM</sub> > 7 V   |     |     | 5.5 | V    |
|                        |   | No current from SDO, V <sub>nSLEEP</sub> = 3.3 V, V <sub>VM</sub> > 5 V |     |     | 3.8 | V    |

### 6.5.4 Configuration Pins - HW Variant Only

| PARAMETER                                     |              | TEST CONDITIONS         | MIN  | TYP | MAX  | UNIT |
|---|--------------|-------------------------|------|-----|------|------|
| <i>6 level setting for ITRIP, SR and DIAG</i> |              |                         |      |     |      |      |
| R <sub>LVL10F6</sub>                          | Level 1 of 6 | Connect to GND          |      |     | 10   | Ω    |
| R <sub>LVL20F6</sub>                          | Level 2 of 6 | +/- 10% resistor to GND | 7.4  | 8.2 | 9    | KΩ   |
| R <sub>LVL30F6</sub>                          | Level 3 of 6 | +/- 10% resistor to GND | 19.8 | 22  | 24.2 | KΩ   |
| R <sub>LVL40F6</sub>                          | Level 4 of 6 | +/- 10% resistor to GND | 42.3 | 47  | 51.7 | KΩ   |
| R <sub>LVL50F6</sub>                          | Level 5 of 6 | +/- 10% resistor to GND | 90   | 100 | 110  | KΩ   |
| R <sub>LVL60F6</sub>                          | Level 6 of 6 | Hi-Z (no connect)       | 250  |     |      | KΩ   |

### 6.5.5 Power FET Parameters

Measured at V<sub>VM</sub> = 13.5 V

| PARAMETER          |   | TEST CONDITIONS                                | MIN | TYP  | MAX  | UNIT |
|--------------------|---|--|-----|------|------|------|
| R <sub>HS_ON</sub> | High-side FET on resistance, HVSSOP package                                     | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 25°C  |     | 24.5 |      | mΩ   |
|                    |   | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 150°C |     |      | 46.6 | mΩ   |
|                    | High-side FET on resistance, VQFN-HR package                                    | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 25°C  |     | 21   |      | mΩ   |
|                    |   | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 150°C |     |      | 39.9 | mΩ   |
| R <sub>LS_ON</sub> | Low-side FET on resistance, HVSSOP package                                      | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 25°C  |     | 24.5 |      | mΩ   |
|                    |   | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 150°C |     |      | 46.6 | mΩ   |
|                    | Low-side FET on resistance, VQFN-HR package                                     | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 25°C  |     | 21   |      | mΩ   |
|                    |   | I <sub>OUT</sub> = 6 A, T <sub>J</sub> = 150°C |     |      | 39.9 | mΩ   |
| V <sub>SD</sub>    | Low-side & High-side FET source-drain voltage when body diode is forward biased | I <sub>OUT</sub> = +/- 6 A(both directions)    | 0.4 | 0.9  | 1.5  | V    |
| R <sub>Hi-Z</sub>  | OUT resistance to GND in SLEEP or STANDBY state                                 | V <sub>OUTx</sub> = V <sub>VM</sub> = 13.5 V   | 1.4 |      | 64   | KΩ   |

### 6.5.6 Switching Parameters with High-Side Recirculation

Load = 1.5mH / 4.7 Ohm, V<sub>VM</sub> = 13.5 V, refer [high-side recirculation waveform](#)

| PARAMETER           |                                     | TEST CONDITIONS        | MIN | TYP  | MAX | UNIT |
|---------------------|-------------------------------------|------------------------|-----|------|-----|------|
| SR <sub>LSOFF</sub> | Output voltage rise time, 10% - 90% | SR = 3'b000 or LVL2    |     | 1.7  |     | V/μs |
|                     |                                     | SR = 3'b001 (SPI only) |     | 4.8  |     | V/μs |
|                     |                                     | SR = 3'b010 (SPI only) |     | 8.1  |     | V/μs |
|                     |                                     | SR = 3'b011 or LVL3    |     | 14   |     | V/μs |
|                     |                                     | SR = 3'b100 or LVL4    |     | 19.9 |     | V/μs |
|                     |                                     | SR = 3'b101 or LVL1    |     | 25.7 |     | V/μs |
|                     |                                     | SR = 3'b110 or LVL6    |     | 36.4 |     | V/μs |
|                     |                                     | SR = 3'b111 or LVL5    |     | 45.8 |     | V/μs |

| PARAMETER               |   | TEST CONDITIONS                     | MIN | TYP  | MAX | UNIT |
|-------------------------|---|-------------------------------------|-----|------|-----|------|
| t <sub>PD_LSOFF</sub>   | Propagation time during output voltage rise     | SR = 3'b000 or LVL2                 |     | 1.2  |     | μs   |
|                         |   | SR = 3'b001 (SPI only)              |     | 0.9  |     | μs   |
|                         |   | SR = 3'b010 (SPI only)              |     | 0.8  |     | μs   |
|                         |   | SR = 3'b011 or LVL3                 |     | 0.7  |     | μs   |
|                         |   | SR = 3'b100 & 3'b101 or LVL4 & LVL1 |     | 0.5  |     | μs   |
|                         |   | SR = 3'b110 & 3'b111 or LVL6 & LVL5 |     | 0.4  |     | μs   |
| t <sub>DEAD_LSOFF</sub> | Dead time during output voltage rise            | All SRs                             |     | 0.9  |     | μs   |
| SR <sub>LSON</sub>      | Output voltage fall time, 90% - 10%             | SR = 3'b000 or LVL2                 |     | 1.7  |     | V/μs |
|                         |   | SR = 3'b001 (SPI only)              |     | 4.8  |     | V/μs |
|                         |   | SR = 3'b010 (SPI only)              |     | 8.1  |     | V/μs |
|                         |   | SR = 3'b011 or LVL3                 |     | 14   |     | V/μs |
|                         |   | SR = 3'b100 or LVL4                 |     | 19.9 |     | V/μs |
|                         |   | SR = 3'b101 or LVL1                 |     | 25.7 |     | V/μs |
|                         |   | SR = 3'b110 or LVL6                 |     | 36.4 |     | V/μs |
|                         |   | SR = 3'b111 or LVL5                 |     | 45.8 |     | V/μs |
| t <sub>PD_LSON</sub>    | Propagation time during output voltage fall     | SR = 3'b000 or LVL2                 |     | 1.5  |     | μs   |
|                         |   | SR = 3'b001 (SPI only)              |     | 0.9  |     | μs   |
|                         |   | SR = 3'b010 (SPI only)              |     | 0.6  |     | μs   |
|                         |   | SR = 3'b011 or LVL3                 |     | 0.5  |     | μs   |
|                         |   | SR = 3'b100 or LVL4                 |     | 0.4  |     | μs   |
|                         |   | SR = 3'b101 or LVL1                 |     | 0.35 |     | μs   |
|                         |   | SR = 3'b110 & 3'b111 or LVL6 & LVL5 |     | 0.3  |     | μs   |
| t <sub>DEAD_LSON</sub>  | Dead time during output voltage fall            | SR = 3'b000 or LVL2                 |     | 2.2  |     | μs   |
|                         |   | SR = 3'b001 (SPI only)              |     | 1    |     | μs   |
|                         |   | SR = 3'b010 (SPI only)              |     | 1    |     | μs   |
|                         |   | SR = 3'b011 or LVL3                 |     | 0.7  |     | μs   |
|                         |   | All other SRs                       |     | 0.6  |     | μs   |
| Match <sub>SRLS</sub>   | Output voltage rise and fall slew rate matching | All SRs                             | -20 |      | +20 | %    |

### 6.5.7 Switching Parameters with Low-Side Recirculation

Load = 1.5 mH / 4.7 Ohm,  $V_{VM} = 13.5\text{ V}$ , refer [low-side recirculation](#) waveform

| PARAMETER               |   | TEST CONDITIONS                  | MIN | TYP  | MAX | UNIT |
|-------------------------|---|----------------------------------|-----|------|-----|------|
| SR <sub>HSON</sub>      | Output voltage rise time, 10% - 90%   | SR = 3'b000 or LVL2              |     | 1.8  |     | V/μs |
|                         |   | SR = 3'b001 (SPI only)           |     | 5.7  |     | V/μs |
|                         |   | SR = 3'b010 (SPI only)           |     | 3.1  |     | V/μs |
|                         |   | SR = 3'b011 or LVL3              |     | 8.7  |     | V/μs |
|                         |   | SR = 3'b100 or LVL4              |     | 14.4 |     | V/μs |
|                         |   | SR = 3'b101 or LVL1              |     | 20.1 |     | V/μs |
|                         |   | SR = 3'b110 or LVL6              |     | 30.7 |     | V/μs |
|                         |   | SR = 3'b111 or LVL5              |     | 40.3 |     | V/μs |
| t <sub>PD_HSON</sub>    | Propagation time during output voltage rise   | SR = 3'b000 or LVL2              |     | 3.2  |     | μs   |
|                         |   | SR = 3'b001 (SPI only)           |     | 1.7  |     | μs   |
|                         |   | SR = 3'b010 (SPI only)           |     | 1.2  |     | μs   |
|                         |   | SR = 3'b011 or LVL3              |     | 1    |     | μs   |
|                         |   | All other SRs                    |     | 0.9  |     | μs   |
| t <sub>DEAD_HSON</sub>  | Dead time during output voltage rise  | SR = 3'b000 or LVL2              |     | 2.4  |     | μs   |
|                         |   | SR = 3'b001 (SPI only)           |     | 5.1  |     | μs   |
|                         |   | SR = 3'b010 (SPI only)           |     | 1.2  |     | μs   |
|                         |   | All other SRs                    |     | 0.5  |     | μs   |
| SR <sub>HSOFF</sub>     | Output voltage fall time, 90% - 10%   | SR = 3'b000 or LVL2              |     | 2.5  |     | V/μs |
|                         |   | SR = 3'b001 (SPI only)           |     | 5.7  |     | V/μs |
|                         |   | SR = 3'b010 (SPI only)           |     | 8.6  |     | V/μs |
|                         |   | SR = 3'b011 or LVL3              |     | 14.1 |     | V/μs |
|                         |   | SR = 3'b100 or LVL4              |     | 19.7 |     | V/μs |
|                         |   | SR = 3'b101 or LVL1              |     | 25.1 |     | V/μs |
|                         |   | SR = 3'b110 or LVL6              |     | 35   |     | V/μs |
|                         |   | SR = 3'b111 or LVL5              |     | 43.6 |     | V/μs |
| t <sub>PD_HSOFF</sub>   | Propagation time during output voltage fall   | All SRs                          |     | 0.25 |     | μs   |
| t <sub>DEAD_HSOFF</sub> | Dead time during output voltage fall  | All SRs                          |     | 0.3  |     | μs   |
| t <sub>BLANK</sub>      | Current regulation blanking time after OUT slewing for current sense output to settle (Valid for only for LS recirculation) | SR = 3'b000 or LVL2              |     | 10.8 |     | μs   |
|                         |   | SR = 3'b001 or 3'b010 (SPI only) |     | 3.5  |     | μs   |
|                         |   | All other SRs                    |     | 2.5  |     | μs   |

### 6.5.8 IPROPI & ITRIP Regulation

| PARAMETER                           |  | TEST CONDITIONS                        | MIN  | TYP  | MAX  | UNIT |
|-------------------------------------|--|--|------|------|------|------|
| A <sub>I<sub>PROPI</sub></sub>      | Current scaling factor, HVSSOP package   |  |      | 3040 |      | A/A  |
|                                     | Current scaling factor, VQFN-HR package  |  |      | 3050 |      | A/A  |
| A <sub>I<sub>ERR</sub></sub>        | Current scaling factor   | 1.6 A < I <sub>OUT</sub> < 8.6 A       | -5   |      | +5   | %    |
|                                     |  | 0.4 A < I <sub>OUT</sub> ≤ 1.6 A       | -20  |      | +20  | %    |
|                                     |  | 0.2 A < I <sub>OUT</sub> ≤ 0.4 A       | -50  |      | +50  | %    |
| Offset <sub>I<sub>PROPI</sub></sub> | Offset current on IPROPI at no load current  | I <sub>OUT</sub> = 0 A                 |      |      | 15   | μA   |
| BW <sub>I<sub>PROPI</sub></sub>     | Bandwidth of the IPROPI internal sense circuit   | No external capacitor on IPROPI.       | 400  |      |      | KHz  |
| V <sub>I<sub>PROPI</sub>_LIM</sub>  | Internal clamping voltage on IPROPI  |  | 4.5  |      | 5.5  | V    |
| V <sub>I<sub>TRIP</sub>_LVL</sub>   | Voltage limit on V <sub>I<sub>PROPI</sub></sub> to trigger TOFF cycle for ITRIP regulation | ITRIP = 3'b001 or LVL2                 | 1.06 | 1.18 | 1.3  | V    |
|                                     |  | ITRIP = 3'b010 (SPI only)              | 1.27 | 1.41 | 1.55 | V    |
|                                     |  | ITRIP = 3'b011 (SPI only)              | 1.49 | 1.65 | 1.82 | V    |
|                                     |  | ITRIP = 3'b100 or LVL3                 | 1.78 | 1.98 | 2.18 | V    |
|                                     |  | ITRIP = 3'b101 or LVL4                 | 2.08 | 2.31 | 2.54 | V    |
|                                     |  | ITRIP = 3'b110 or LVL5                 | 2.38 | 2.64 | 2.9  | V    |
|                                     |  | ITRIP = 3'b111 or LVL6                 | 2.67 | 2.97 | 3.27 | V    |
| t <sub>OFF</sub>                    | ITRIP regulation - off time  | TOFF = 2'b00 (SPI only)                | 16   | 20   | 25   | μs   |
|                                     |  | TOFF = 2'b01 (SPI). Only choice for HW | 24   | 30   | 36   | μs   |
|                                     |  | TOFF = 2'b10 (SPI only)                | 33   | 40   | 48   | μs   |
|                                     |  | TOFF = 2'b11 (SPI only)                | 41   | 50   | 61   | μs   |

### 6.5.9 Over Current Protection (OCP)

| PARAMETER           |  | TEST CONDITIONS                            | MIN  | TYP | MAX | UNIT |
|---------------------|--|--|------|-----|-----|------|
| I <sub>OCP_HS</sub> | Over current protection threshold on the high side | OCP_SEL = 2'b00 (SPI), Only choice for HW  | 24   |     | 48  | A    |
|                     |  | OCP_SEL = 2'b10 (SPI only)                 | 18   |     | 36  | A    |
|                     |  | OCP_SEL = 2'b01 (SPI only)                 | 12   |     | 28  | A    |
| I <sub>OCP_LS</sub> | Over current protection threshold on the low side  | OCP_SEL = 2'b00 (SPI), Only choice for HW  | 24   |     | 48  | A    |
|                     |  | OCP_SEL = 2'b10 (SPI only)                 | 18   |     | 36  | A    |
|                     |  | OCP_SEL = 2'b01 (SPI only)                 | 12   |     | 28  | A    |
| t <sub>OCP</sub>    | Over current protection deglitch time              | TOCP_SEL = 2'b00 (SPI), Only choice for HW | 4.5  | 6   | 7.3 | μs   |
|                     | Over current protection deglitch time              | TOCP_SEL = 2'b01 (SPI only)                | 2.2  | 3   | 4.1 | μs   |
|                     | Over current protection deglitch time              | TOCP_SEL = 2'b10 (SPI only)                | 1.1  | 1.5 | 2.3 | μs   |
|                     | Over current protection deglitch time              | TOCP_SEL = 2'b11 (SPI only)                | 0.15 | 0.2 | 0.4 | μs   |

### 6.5.10 Over Temperature Protection (TSD)

| PARAMETER        |                                | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--------------------------------|-----------------|-----|-----|-----|------|
| T <sub>TSD</sub> | Thermal shutdown temperature   |                 | 155 | 170 | 185 | °C   |
| T <sub>HYS</sub> | Thermal shutdown hysteresis    |                 |     | 30  |     | °C   |
| t <sub>TSD</sub> | Thermal shutdown deglitch time |                 | 10  | 12  | 19  | μs   |



### 6.5.11 Voltage Monitoring

| PARAMETER               |   | TEST CONDITIONS                                   | MIN  | TYP                  | MAX | UNIT |
|-------------------------|---|---|------|----------------------|-----|------|
| V <sub>VMOV</sub>       | VM over voltage threshold while rising            | VMOV_SEL = 2'b00 (SPI), Only choice in HW variant | 33.6 |                      | 37  | V    |
|                         |   | VMOV_SEL = 2'b01 (SPI only)                       | 28   |                      | 31  | V    |
|                         |   | VMOV_SEL = 2'b10 (SPI only)                       | 18   |                      | 21  | V    |
| V <sub>VMOV_HYS</sub>   | VM over voltage hysteresis                        |   | 0.6  |                      | V   |      |
| t <sub>VMOV</sub>       | VM over voltage deglitch time                     |   | 10   | 12                   | 19  | µs   |
| V <sub>VMUV</sub>       | VM under voltage threshold while falling          |   | 4.2  |                      | 4.5 | V    |
| V <sub>VMUV_HYS</sub>   | VM under voltage hysteresis                       |   |      | 200                  |     | mV   |
| t <sub>VMUV</sub>       | VM under voltage deglitch time                    |   | 8    | 12                   | 19  | µs   |
| VM <sub>POR_FALL</sub>  | VM voltage at which device goes into POR          | Applicable for HW & SPI (S) variant               |      |                      | 3.6 | V    |
| VM <sub>POR_RISE</sub>  | VM voltage at which device comes out of POR       | Applicable for HW & SPI (S) variant               |      |                      | 3.9 | V    |
| VDD <sub>POR_FALL</sub> | VDD voltage at which device goes into POR         | Applicable for SPI (P) variant                    |      |                      | 3.5 | V    |
| VDD <sub>POR_RISE</sub> | VDD voltage at which device comes out of POR      | Applicable for SPI (P) variant                    |      |                      | 3.8 | V    |
| V <sub>CPUV</sub>       | Charge pump under-voltage threshold while falling |   |      | V <sub>VM</sub> +2.5 |     | V    |
| t <sub>CPUV</sub>       | Charge pump deglitch time                         |   | 10   | 12                   | 19  | µs   |

### 6.5.12 Load Monitoring

| PARAMETER  |   | TEST CONDITIONS                                    | MIN | TYP  | MAX | UNIT |
|--|---|--|-----|------|-----|------|
| <i>Off-state diagnostics (OLP)</i>                   |   |  |     |      |     |      |
| R <sub>S_GND</sub>                                   | Resistance on OUT to GND that will be detected as short                         |  |     |      | 1   | KΩ   |
| R <sub>S_VM</sub>                                    | Resistance on OUT to VM that will be detected as short                          |  |     |      | 1   | KΩ   |
| R <sub>OPEN_LS</sub>                                 | Resistance on OUT to GND that will be detected as open                          | Valid for low-side load                            | 2   |      |     | KΩ   |
| R <sub>OPEN_HS</sub>                                 | Resistance on OUT to VM that will be detected as open                           | Valid for high-side load, V <sub>VM</sub> = 13.5 V | 10  |      |     | KΩ   |
| V <sub>OLP_REFH</sub>                                | OLP Comparator Reference High   |  |     | 2.65 |     | V    |
| V <sub>OLP_REFL</sub>                                | OLP Comparator Reference Low  |  |     | 2    |     | V    |
| R <sub>OLP_PU</sub>                                  | Internal pull-up resistance on OUT to VDD during OLP                            | V <sub>OUTx</sub> = V <sub>OLP_REFH</sub> + 0.1V   |     | 1    |     | KΩ   |
| R <sub>OLP_PD</sub>                                  | Internal pull-down resistance on OUT to GND during OLP                          | V <sub>OUTx</sub> = V <sub>OLP_REFL</sub> - 0.1V   |     | 1    |     | KΩ   |
| <i>SPI variant only - On-state diagnostics (OLA)</i> |   |  |     |      |     |      |
| I <sub>PD_OLA</sub>                                  | Internal sink current on OUT to GND during dead-time in high-side recirculation |  | 0.1 |      | 10  | mA   |
| V <sub>OLA_REF</sub>                                 | Comparator Reference with respect to VM used for OLA                            |  |     | 0.25 |     | V    |

### 6.5.13 Fault Retry Setting

Refer to [retry setting waveform](#)

| PARAMETER          |                             | TEST CONDITIONS             | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|-----------------------------|-----|-----|-----|------|
| t <sub>RETRY</sub> | Automatic driver retry time | Fault reaction set to RETRY | 4.1 | 5   | 6.1 | ms   |

| PARAMETER              |   | TEST CONDITIONS             | MIN | TYP | MAX | UNIT |
|------------------------|---|-----------------------------|-----|-----|-----|------|
| t <sub>CLEAR</sub>     | Fault free operation time to auto-clear from over current event     | Fault reaction set to RETRY | 85  |     | 200 | µs   |
| t <sub>CLEAR_TSD</sub> | Fault free operation time to auto-clear from over temperature event | Fault reaction set to RETRY | 4.2 |     | 6.7 | ms   |

### 6.5.14 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

**Table 6-1. Transient Thermal Impedance (R<sub>θJA</sub>) and Current Capability - half-bridge**

| PART NUMBER | PACKAGE | R <sub>θJA</sub> [°C/W] <sup>(1)</sup> |       |        |      | Current [A] <sup>(2)</sup> |       |        |     |                         |     |
|-------------|---------|--|-------|--------|------|----------------------------|-------|--------|-----|-------------------------|-----|
|             |         |  |       |        |      | without PWM <sup>(3)</sup> |       |        |     | with PWM <sup>(4)</sup> |     |
|             |         | 0.1 sec                                | 1 sec | 10 sec | DC   | 0.1 sec                    | 1 sec | 10 sec | DC  | 10 sec                  | DC  |
| DRV8143-Q1  | VQFN-HR | 6.6                                    | 12.4  | 16.9   | 33.4 | 15.7                       | 11.5  | 9.8    | 7.0 | 8.0                     | 5.3 |
| DRV8143-Q1  | HVSSOP  | 5.0                                    | 9.8   | 14.7   | 31.7 | 16.7                       | 11.9  | 9.7    | 6.6 | 8.2                     | 5.2 |

- (1) Based on thermal simulations using 40 mm x 40 mm x 1.6 mm 4 layer PCB – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes with 0.3 mm thermal via drill diameter, 0.025 mm Cu plating, 1 minimum mm via pitch.
- (2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C
- (3) Only conduction losses (I<sup>2</sup>R) considered
- (4) Switching loss roughly estimated by the following equation:

$$P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times V_{VM}/SR, \text{ where } V_{VM} = 13.5 \text{ V, } f_{PWM} = 20 \text{ KHz, } SR = 23 \text{ V}/\mu\text{s} \quad (1)$$

### 6.6 SPI Timing Requirements

|                      |                                       | MIN | TYP | MAX | UNIT |
|----------------------|---------------------------------------|-----|-----|-----|------|
| t <sub>SCLK</sub>    | SCLK minimum period <sup>(1)</sup>    | 100 |     |     | ns   |
| t <sub>SCLKH</sub>   | SCLK minimum high time                | 50  |     |     | ns   |
| t <sub>SCLKL</sub>   | SCLK minimum low time                 | 50  |     |     | ns   |
| t <sub>HI_nSCS</sub> | nSCS minimum high time                | 300 |     |     | ns   |
| t <sub>SU_nSCS</sub> | nSCS input setup time                 | 25  |     |     | ns   |
| t <sub>H_nSCS</sub>  | nSCS input hold time                  | 25  |     |     | ns   |
| t <sub>SU_SDI</sub>  | SDI input data setup time             | 25  |     |     | ns   |
| t <sub>H_SDI</sub>   | SDI input data hold time              | 25  |     |     | ns   |
| t <sub>EN_SDO</sub>  | SDO enable delay time <sup>(1)</sup>  |     |     | 35  | ns   |
| t <sub>DIS_SDO</sub> | SDO disable delay time <sup>(1)</sup> |     |     | 100 | ns   |

- (1) SPI (S) variant: SDO delay times are valid only with SDO external load of 5 pF. With a 20 pF load on SDO, there is an additional delay on SDO, which results in a 25% increase in SCLK minimum time, limiting the SCLK to a maximum of 8 MHz. There is NO such limitation for the SPI (P) variant.

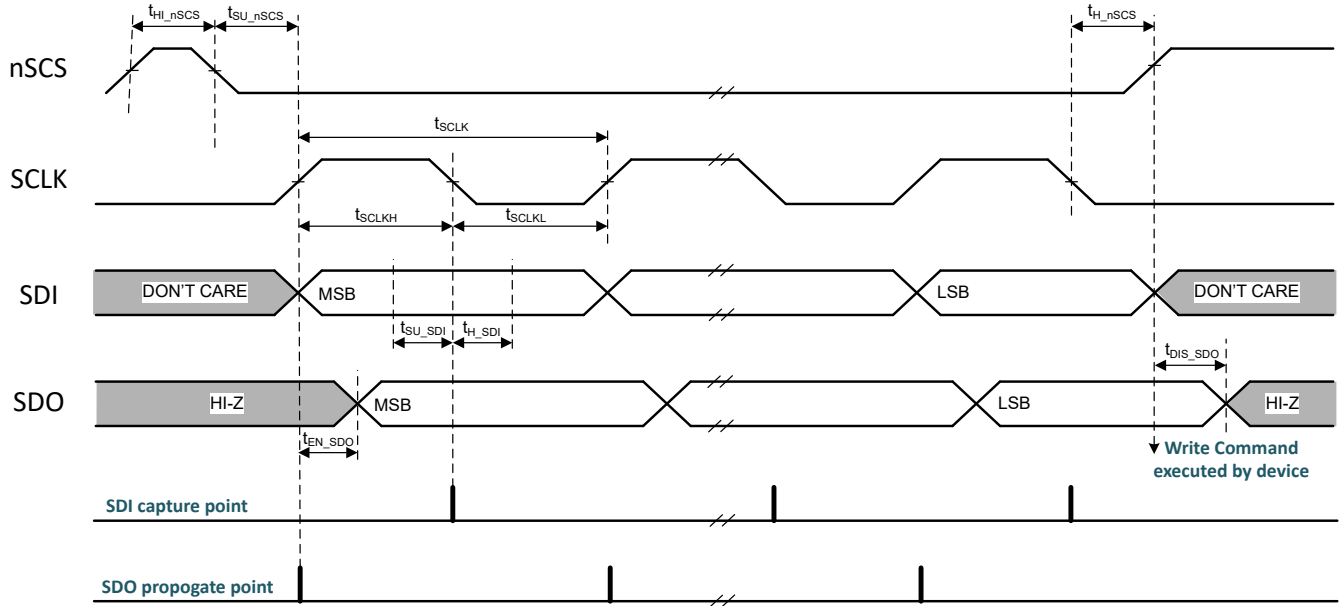


Figure 6-1. SPI Peripheral-Mode Timing Definition

## 6.7 Switching Waveforms

This section illustrates the switching transients for an inductive load due to external PWM or internal ITRIP regulation.

### 6.7.1.1 High-Side Recirculation

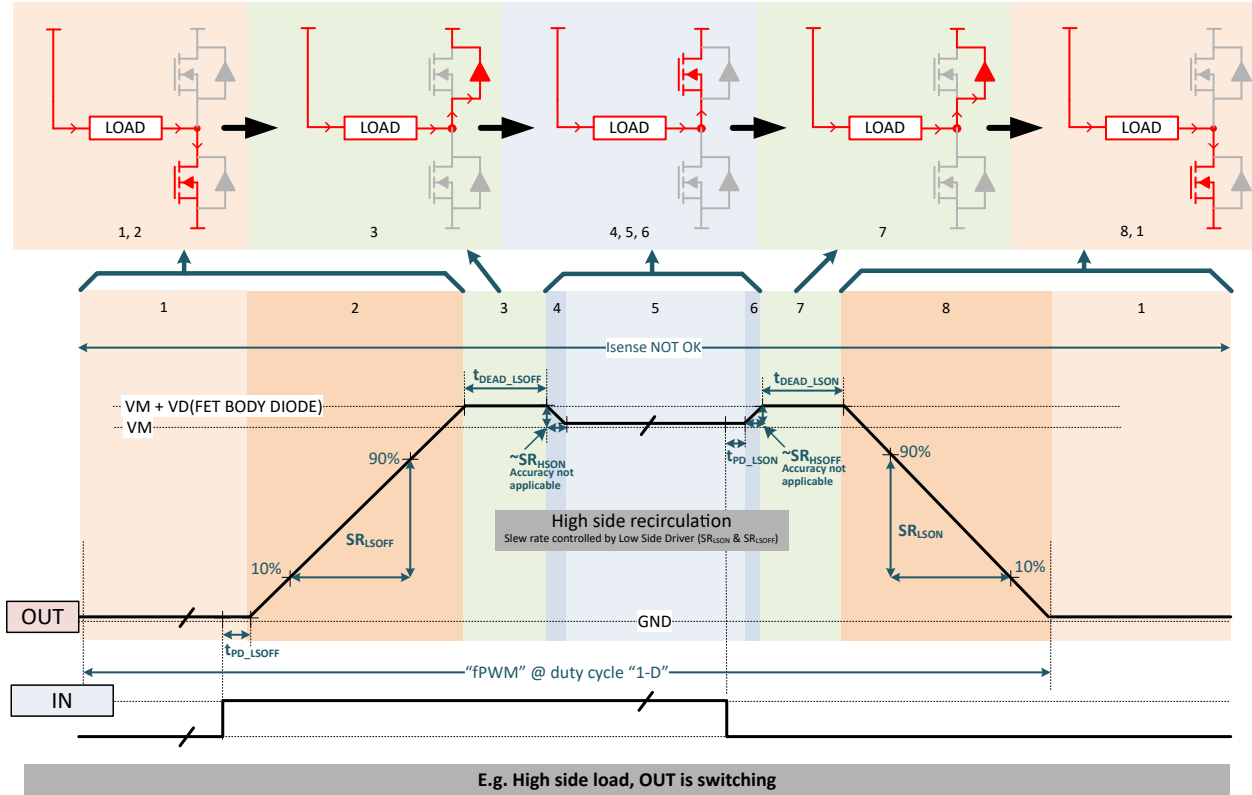


Figure 6-2. Output Switching Transients with High-Side Recirculation

### 6.7.1.2 Low-Side Recirculation

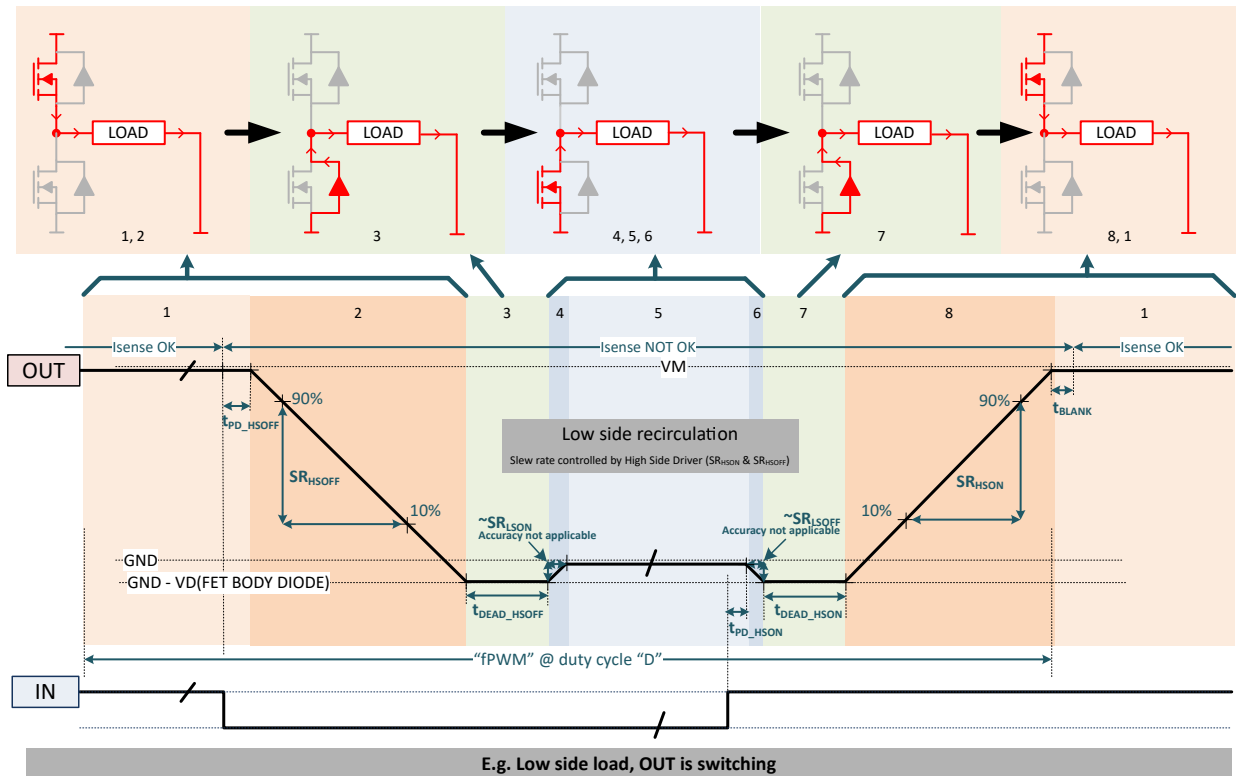


Figure 6-3. Output Switching Transients with Low-Side Recirculation

### 6.7.2 Wake-up Transients

#### 6.7.2.1 HW Variant

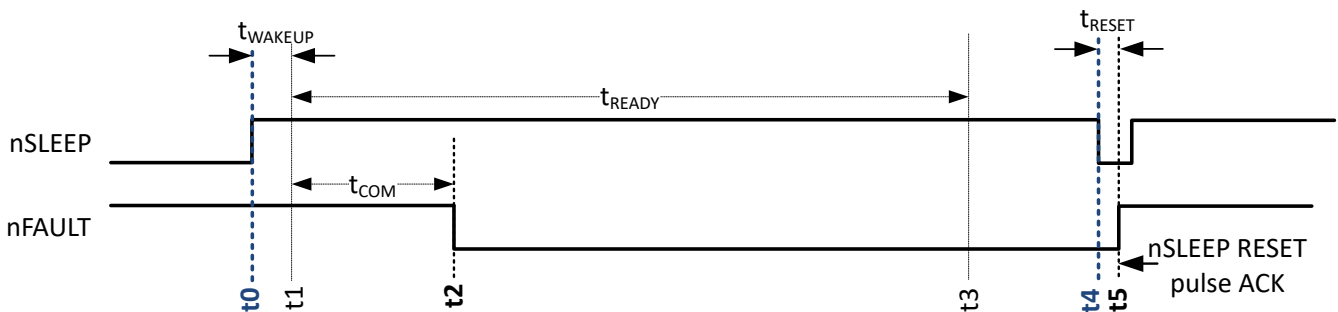


Figure 6-4. Wake-up from SLEEP State to STANDBY State Transition for HW Variant

Hand shake between controller and device during wake-up as follows:

- t0: Controller - nSLEEP asserted high to initiate device wake-up
- t1: Device internal state - Wake-up command registered by device (end of Sleep state)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (any time after t2): **Controller – Issue nSLEEP reset pulse** to acknowledge device wake-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

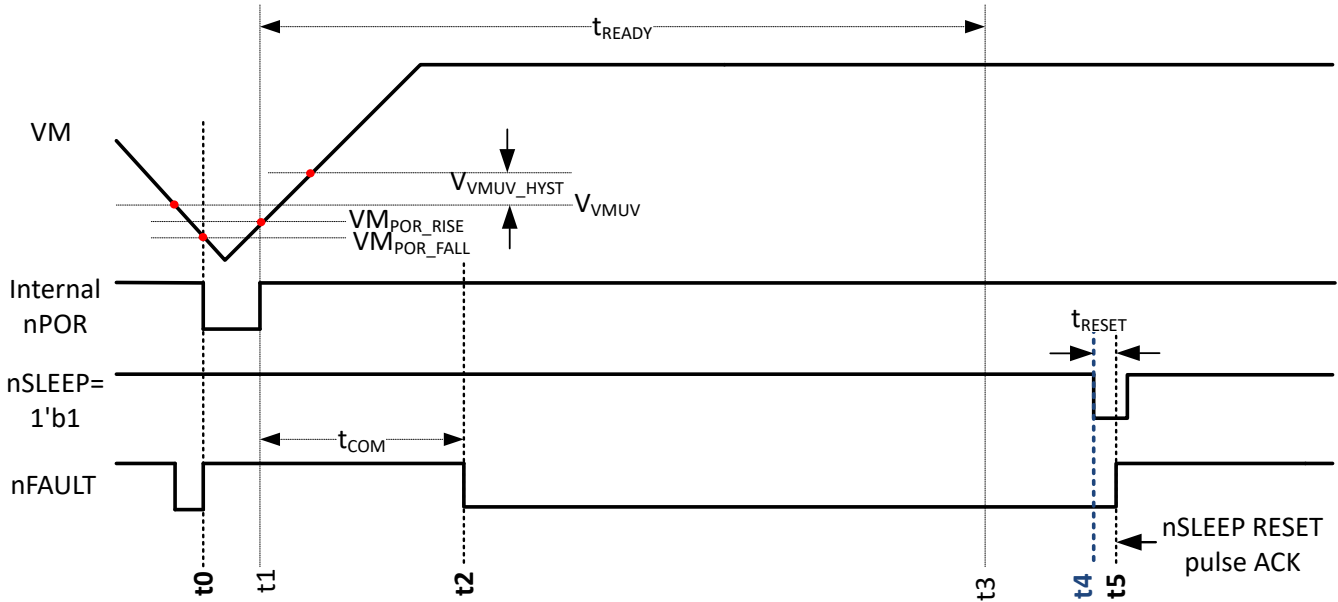


Figure 6-5. Power-up to STANDBY State Transition for HW Variant

Hand shake between controller and device during power-up as follows:

- t<sub>0</sub>: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t<sub>1</sub>: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t<sub>2</sub>: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t<sub>3</sub>: Device internal state - Initialization complete
- t<sub>4</sub> (any time after t<sub>2</sub>): **Controller – Issue nSLEEP reset pulse** to acknowledge device power-up
- t<sub>5</sub>: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

### 6.7.2.2 SPI Variant

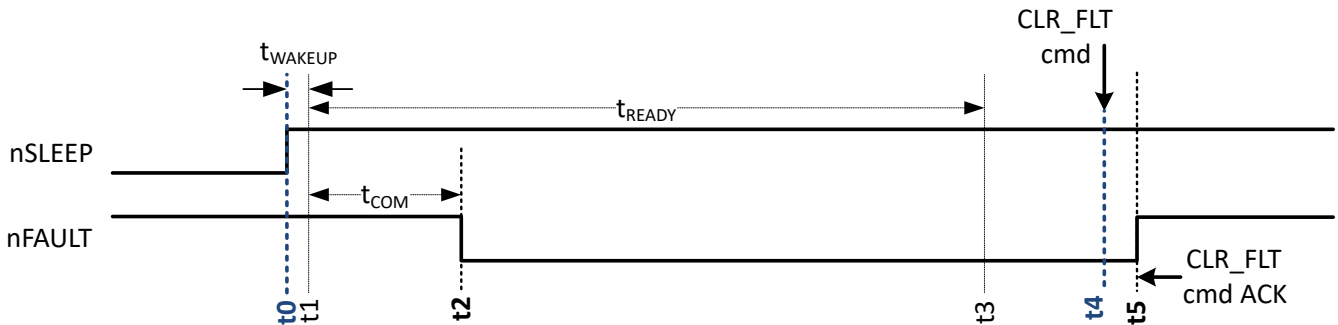


Figure 6-6. Wake-up from SLEEP State to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during a wake-up transient as follows:

- t<sub>0</sub>: Controller - nSLEEP asserted high to initiate device wake-up
- t<sub>1</sub>: Device internal state - Wake-up command registered by device (end of Sleep state)
- t<sub>2</sub>: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t<sub>3</sub>: Device internal state - Initialization complete
- t<sub>4</sub> (Any time after t<sub>2</sub>): **Controller – Issue CLR\_FLT command** through SPI to acknowledge device wake-up
- t<sub>5</sub>: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

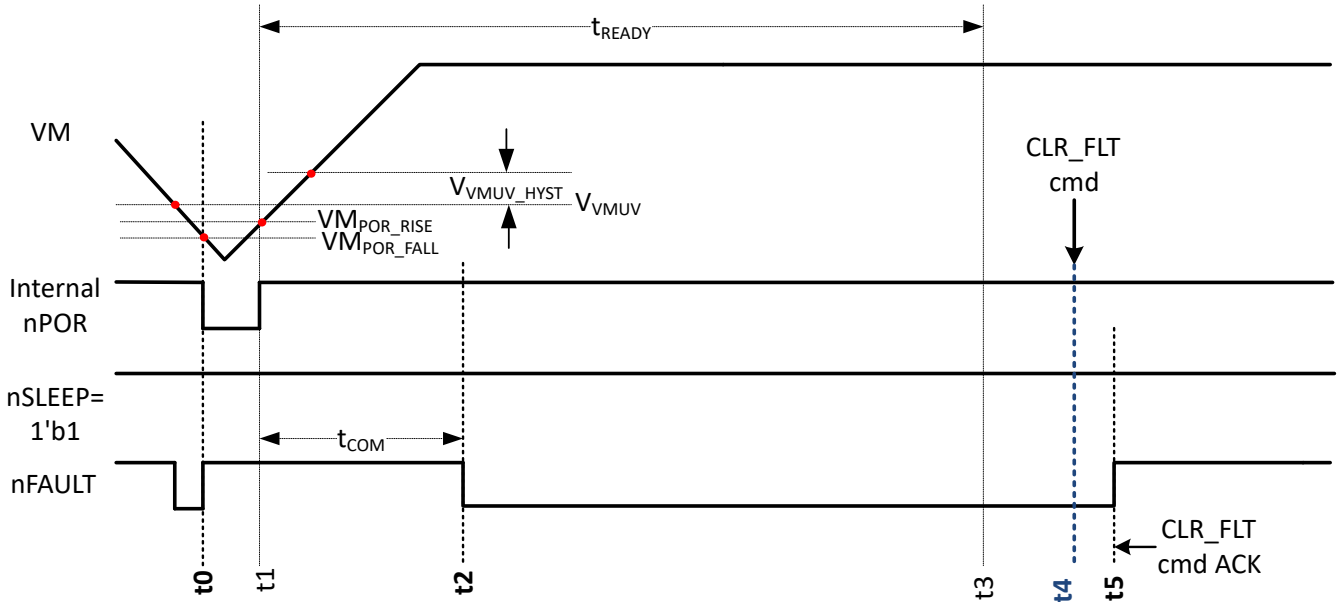


Figure 6-7. Power-up to STANDBY State Transition for SPI (S) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage of internal LDO (VM dependent)
- t1: Device internal state – POR de-asserted based on recovery of internal LDO voltage
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR\_FLT command** through SPI to acknowledge device power-up
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state

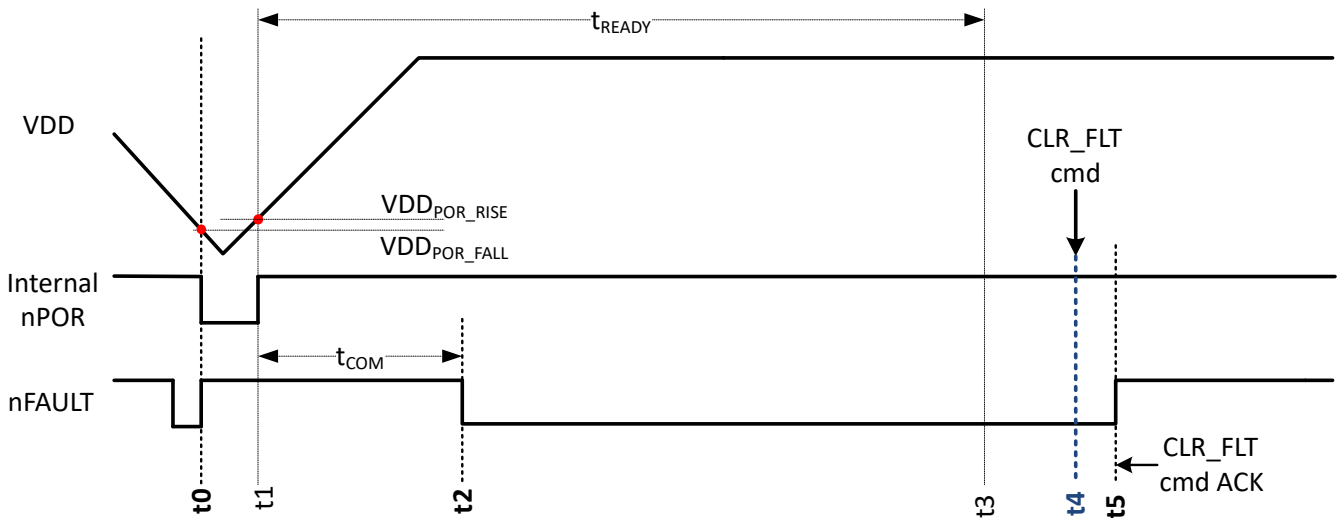


Figure 6-8. Power-up to STANDBY State Transition for SPI (P) Variant

Hand shake between controller and device during power-up as follows:

- t0: Device internal state - POR asserted based on under voltage on VDD (external supply)
- t1: Device internal state – POR de-asserted based on recovery of voltage on VDD (external supply)
- t2: Device – nFAULT asserted low to acknowledge wake-up and indicate device ready for communication
- t3: Device internal state - Initialization complete
- t4 (Any time after t2): **Controller – Issue CLR\_FLT command** through SPI to acknowledge device power-up

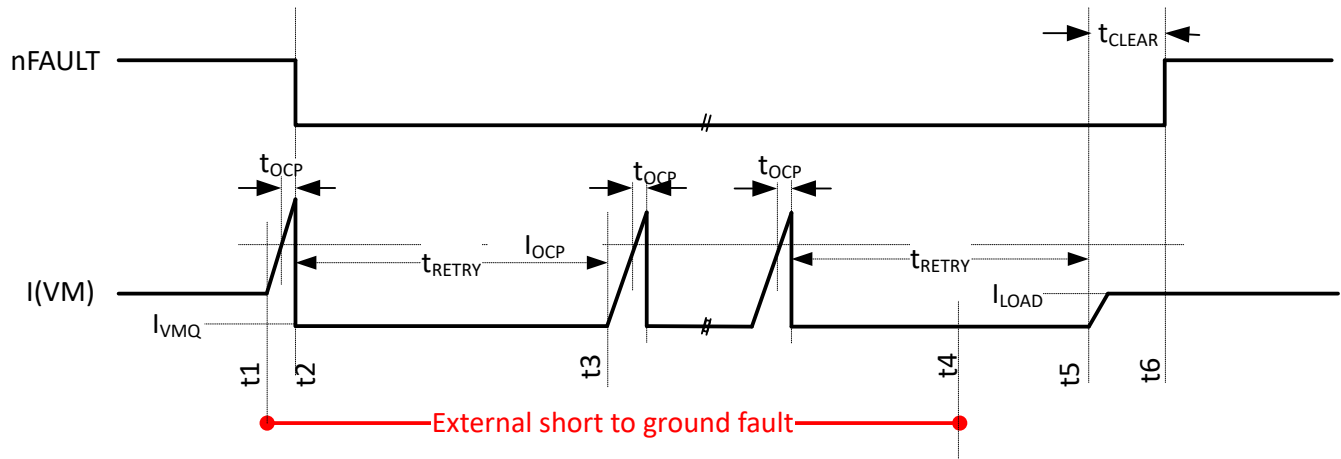
- t5: Device - nFAULT de-asserted as an acknowledgment of nSLEEP reset pulse. Device in STANDBY state



## 6.7.3 Fault Reaction Transients

### 6.7.3.1 Retry setting

Valid for both SPI and HW variants



**Figure 6-9. Fault reaction with RETRY setting (shown for OCP occurrence on high-side when OUT is shorted to ground)**

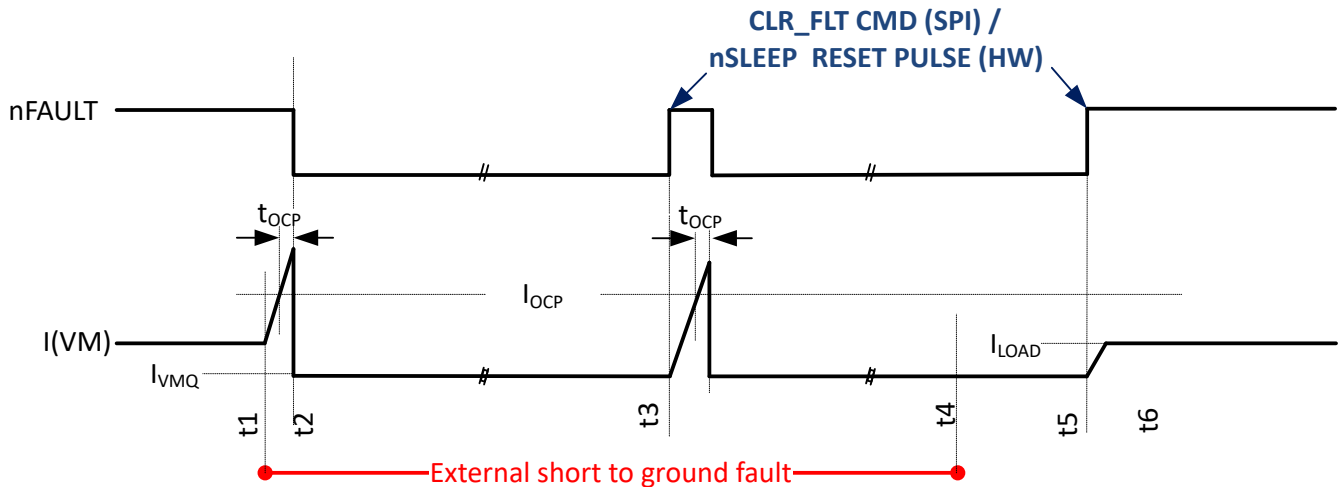
Short occurrence and recovery scenario with RETRY setting:

- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after  $t_{OCP}$ , output disabled, nFAULT asserted low to indicate fault.
- t3: Device automatically attempts retry (auto retry) after  $t_{RETRY}$ . Each time output is briefly turned on to confirm short occurrence and then immediately disabled after  $t_{OCP}$ . nFAULT remains asserted low through out. Cycle repeats till driver is disabled by the user or external short is removed, as illustrated further. Note that, in case of a TSD (Thermal Shut Down) event, automatic retry time depends on the cool off based on thermal hysteresis.
- t4: The external short is removed.
- t5: Device attempts auto retry. But this time, no fault occurs and device continues to keep the output enabled.
- t6: After a fault free operation for a period of  $t_{CLEAR}$  is confirmed, nFAULT is de-asserted.
- SPI variant only – Fault status remains latched till a CLR\_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to  $V_{IPROPI\_LIM}$  voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

### 6.7.3.2 Latch setting

Valid for both SPI and HW variants



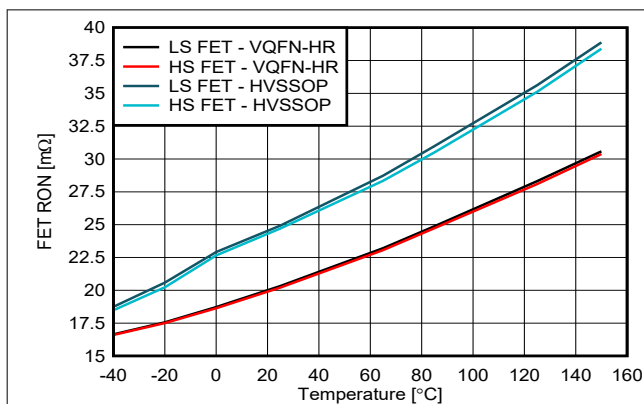
**Figure 6-10. Fault reaction with Latch setting (shown for OCP occurrence on high-side when OUT is shorted to ground)**

Short occurrence and recovery scenario with LATCH setting:

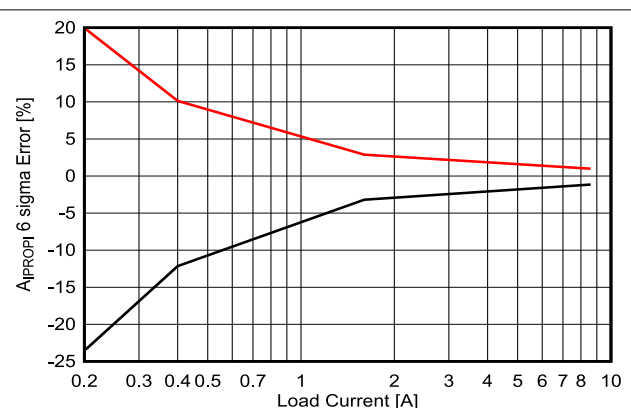
- t1: An external short occurs.
- t2: OCP (Over Current Protection) fault confirmed after  $t_{OCP}$ , output disabled, nFAULT asserted low to indicate fault.
- t3: A CLR\_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. OCP fault is detected again and output is disabled with nFAULT asserted low.
- t4: The external short is removed.
- t5: A CLR\_FLT command (SPI variant) or nSLEEP RESET Pulse (HW variant) issued by controller. nFAULT is de-asserted and output is enabled. Normal operation resumes.
- SPI variant only – Fault status remains latched till a CLR\_FLT command is issued.

Note that, in the event of an output short to ground causing the high-side OCP fault detection, IPROPI pin will continue to be pulled up to  $V_{IPROPI\_LIM}$  voltage to indicate this type of short, while the output is disabled. This is especially useful for the HW (H) variant to differentiate the indication of a short to ground fault from the other faults.

### 6.8 Typical Characteristics



**Figure 6-11.  $R_{HS\_ON}$  &  $R_{LS\_ON}$  vs Temperature at  $V_{VM} = 13.5$  V**



**Figure 6-12.  $A_{IPROPI}$  Gain Error vs Load Current at  $V_{VM} = 13.5$  V**

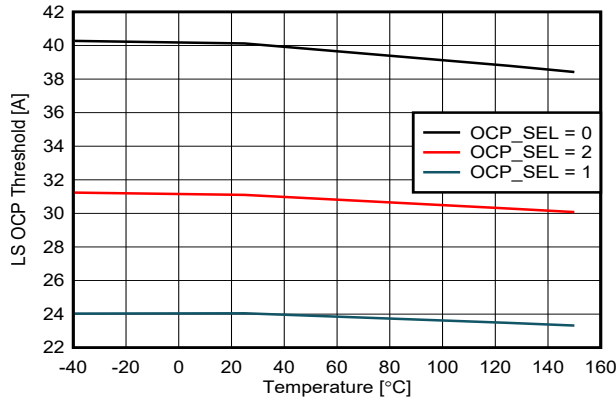


Figure 6-13. LS OCP Threshold vs Temperature at  $V_{VM} = 13.5\text{ V}$

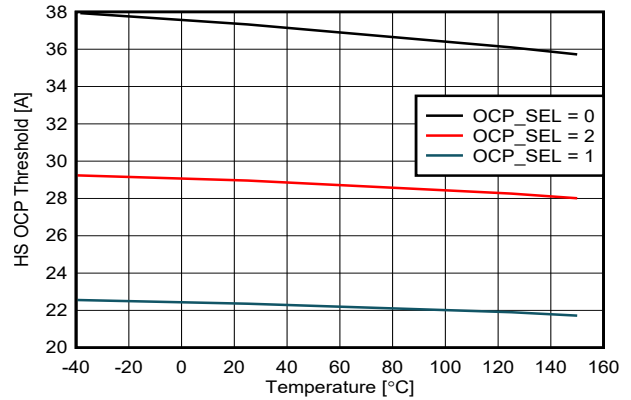


Figure 6-14. HS OCP Threshold vs Temperature at  $V_{VM} = 13.5\text{ V}$

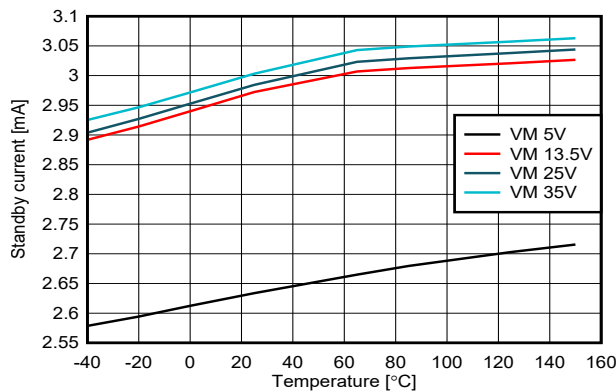


Figure 6-15. Current on VM in STANDBY state vs Temperature

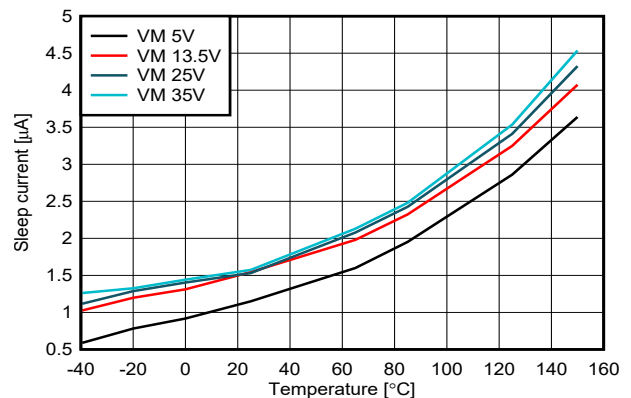


Figure 6-16. Current on VM in SLEEP state vs Temperature

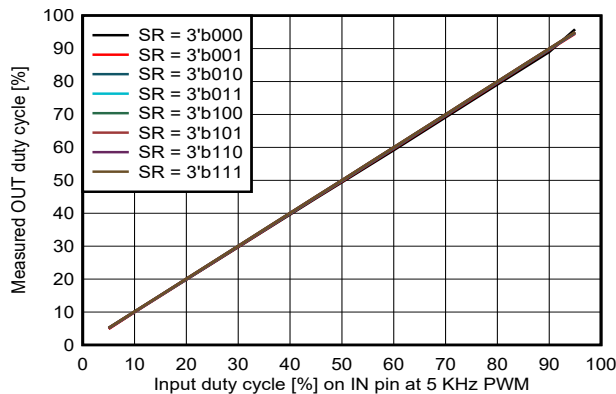


Figure 6-17. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 5 KHz at  $V_{VM} = 13.5\text{ V}$  for HS recirculation

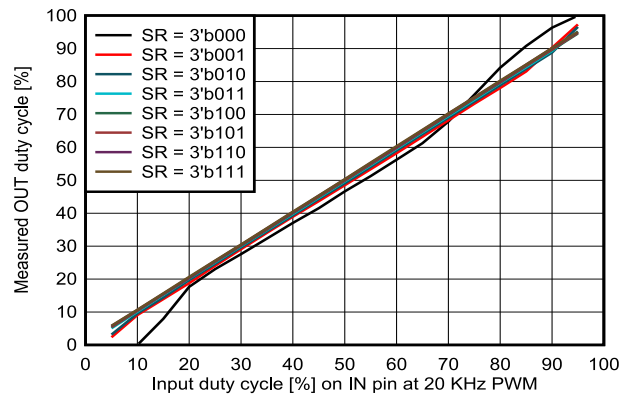
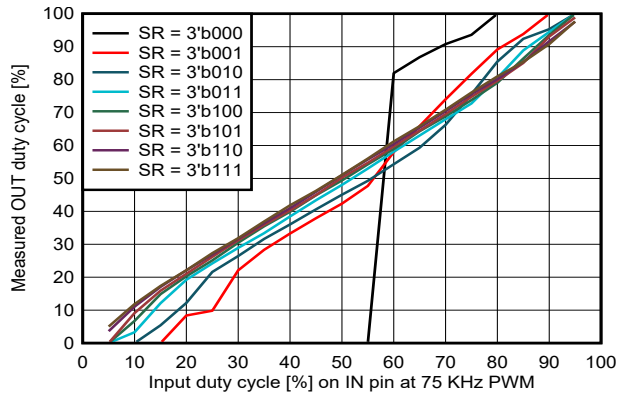
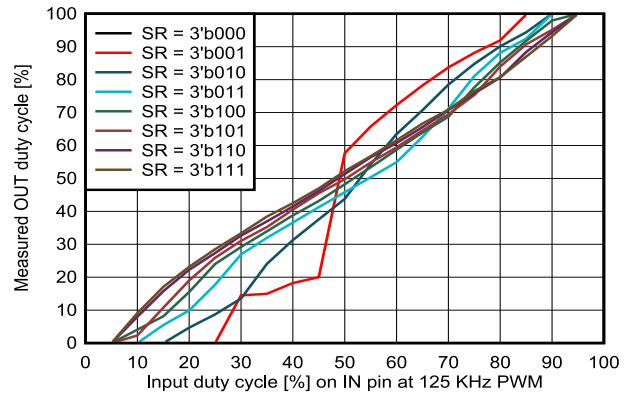


Figure 6-18. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 20 KHz at  $V_{VM} = 13.5\text{ V}$  for HS recirculation



**Figure 6-19. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 75 KHz at  $V_{VM} = 13.5$  V for HS recirculation**



**Figure 6-20. Measured Duty Cycle vs Input Duty Cycle at PWM frequency of 125 KHz at  $V_{VM} = 13.5$  V for HS recirculation**

## 7 Detailed Description

### 7.1 Overview

The DRV814x-Q1 family of devices are brushed DC motor drivers that operate from 4.5 to 35-V supporting a wide range of output load currents for various types of motors and loads. The devices integrate a charge pump regulator to support efficient high-side N-channel MOSFETs with 100% duty cycle operation. The devices operate from a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The devices also provide a low power mode to minimize current draw during system inactivity.

The devices are available in two interface variants -

1. HW variant - Hardwired interface variant is available for easy device configuration. Due to the limited number of available pins in the device, this variant offers fewer configuration and fault reporting capability compared to the SPI variant.
2. SPI variant - A standard 4-wire serial peripheral interface (SPI) with daisy chain capability allows flexible device configuration and detailed fault reporting to an external controller. The feature differences of the SPI and HW variants can be found in the [device comparison](#) section. The SPI interface is available in two device variant choices, as stated below:
  - a. SPI (S) variant - The power supply for the digital block is provided by an internal LDO regulator sourced from VM supply. The nSLEEP pin is a high impedance input pin.
  - b. SPI (P) variant (N/A for DRV8144-Q1) - This allows for an external supply input to the digital block of the device through a VDD pin. The nSLEEP pin is replaced by this VDD supply pin. This prevents device reset (brown out) during a VM under voltage condition.

The DRV814x family of devices provide a load current sense output using current mirrors on the high-side power MOSFETs. The IPROPI pin sources a small current that is proportional to the current in the high-side MOSFETs (current sourced out of the OUTx pin). This current can be converted to a proportional voltage using an external resistor ( $R_{IPROPI}$ ). Additionally, the devices also support a fixed off-time PWM chopping scheme for limiting current to the load. The current regulation level can be configured through the ITRIP function.

A variety of protection features and diagnostic functions are integrated into the device. These include supply voltage monitors (VMOV & VMUV), charge pump undervoltage (CPUV), off-state (Passive) diagnostics (OLP), on-state (Active) diagnostics (OLA) - SPI variant only, overcurrent protection (OCP) for each power FET and over-temperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin. The SPI variant has additional communication protection features such as frame errors and lock features for configuration register bits and driver control bits.

## 7.2 Functional Block Diagram

### 7.2.1 HW Variant

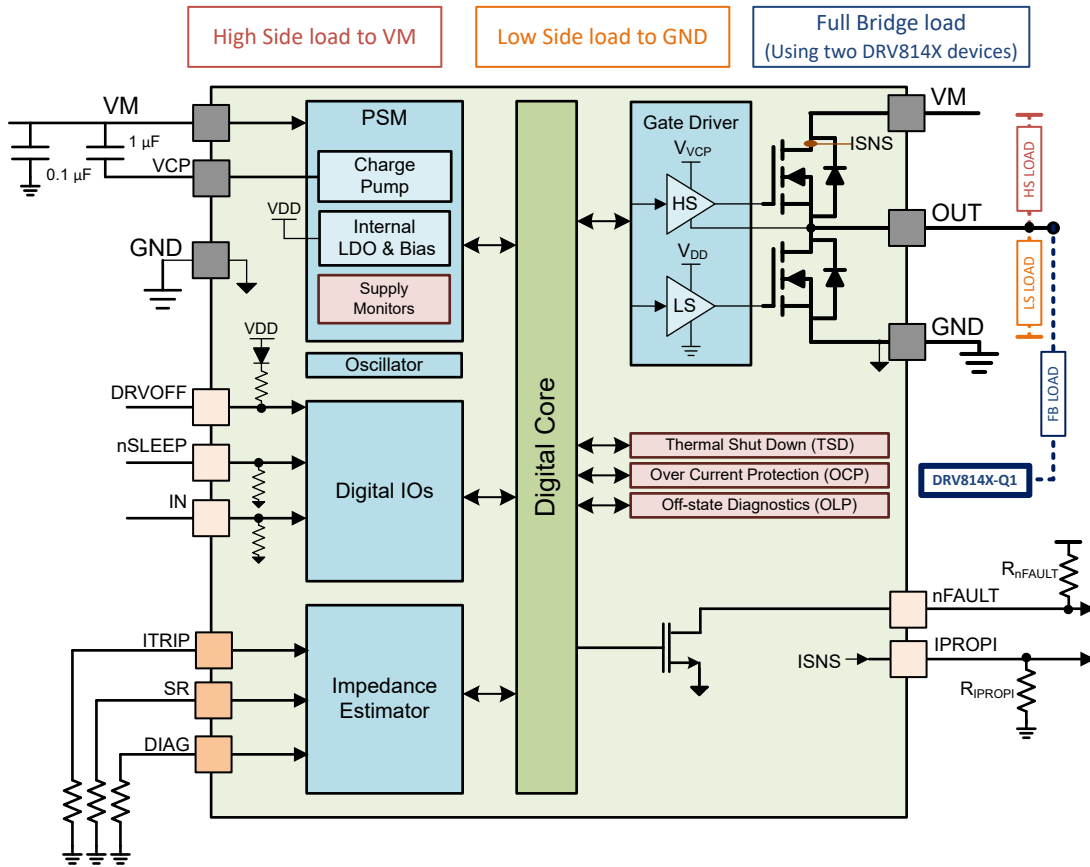


Figure 7-1. Functional Block Diagram - HW Variant

### 7.2.2 SPI Variant

There are two variants for the SPI interface - SPI (S) variant and SPI (P) variant as shown below.

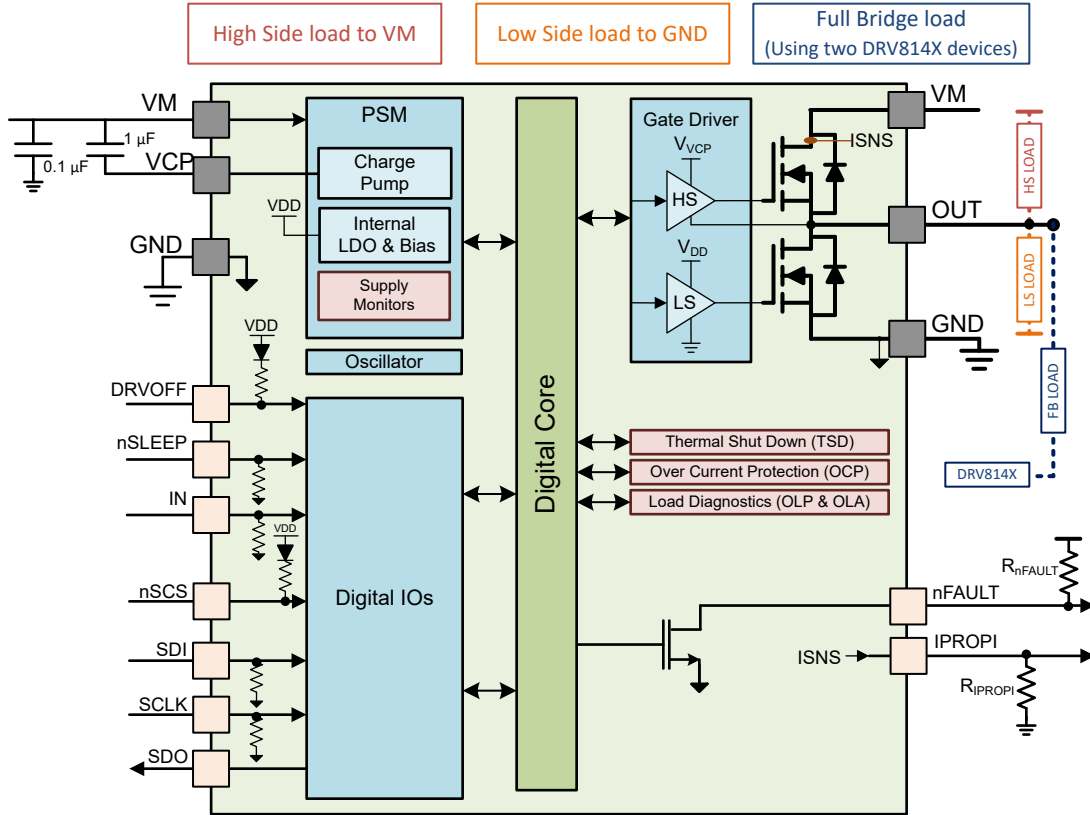


Figure 7-2. Functional Block Diagram - SPI (S) Variant

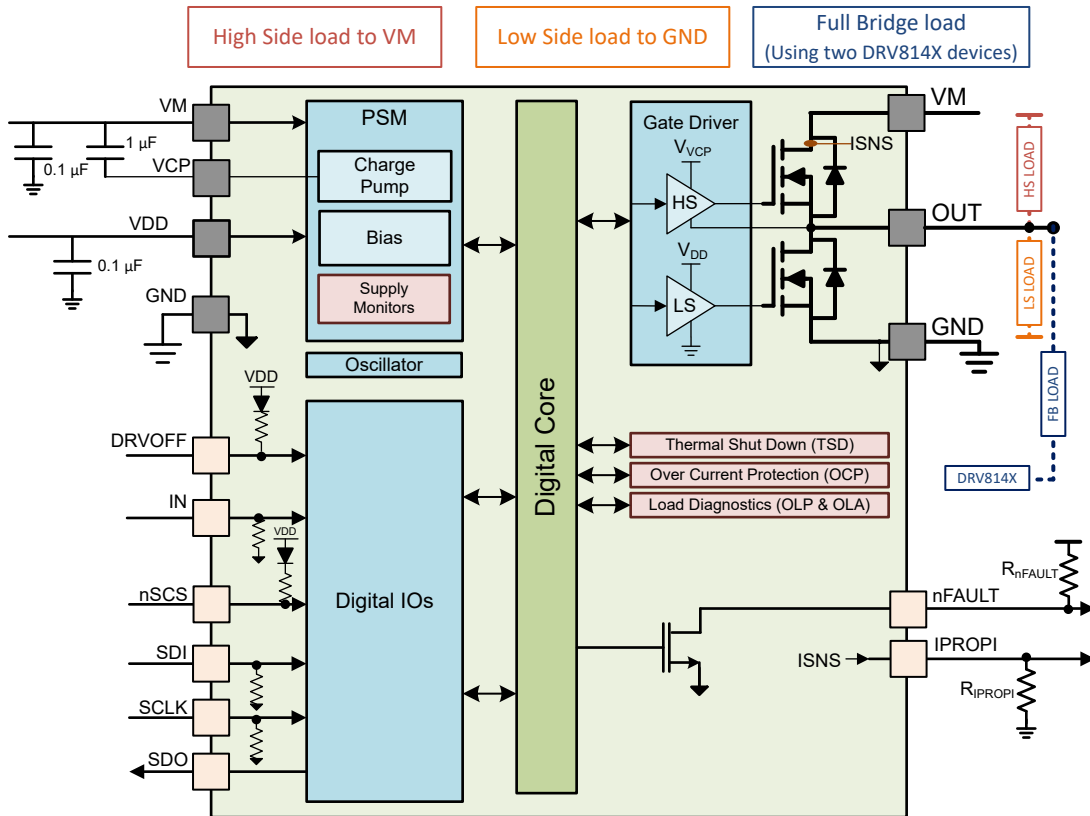


Figure 7-3. Functional Block Diagram - SPI (P) variant

## 7.3 Feature Description

### 7.3.1 External Components

Section 7.3.1.1 and Section 7.3.1.2 contain the recommended external components for the device.

#### 7.3.1.1 HW Variant

**Table 7-1. External Components Table for HW Variant**

| Component           | PIN    | Recommendation  |
|---------------------|--------|---|
| C <sub>VM1</sub>    | VM     | 0.1 $\mu$ F, low ESR ceramic capacitor to GND rated for VM  |
| C <sub>VM2</sub>    | VM     | Local bulk capacitor to GND, 10 $\mu$ F or higher, rated for VM to handle load transients. Refer the section on <a href="#">bulk capacitor sizing</a> .                     |
| C <sub>VCP</sub>    | VCP    | 1 $\mu$ F, 6.3 V low ESR ceramic capacitor to VM  |
| R <sub>IPROPI</sub> | IPROPI | Typically 500 - 5000 $\Omega$ 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed. |
| C <sub>IPROPI</sub> | IPROPI | Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer <a href="#">Over Current Protection (OCP) section</a> .                           |
| R <sub>nFAULT</sub> | nFAULT | Typically 1K $\Omega$ - 10 K $\Omega$ , 0.063 W pull-up resistor to controller supply.  |
| R <sub>SR</sub>     | SR     | Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer <a href="#">SR section</a> .  |
| R <sub>ITRIP</sub>  | ITRIP  | Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer <a href="#">ITRIP table</a> .   |
| R <sub>DIAG</sub>   | DIAG   | Open or short to GND or 0.063 W 10% resistor to GND depending on setting. Refer <a href="#">DIAG section</a> .  |

#### 7.3.1.2 SPI Variant

**Table 7-2. External Components Table for SPI Variant**

| Component           | PIN    | Recommendation  |
|---------------------|--------|---|
| C <sub>VM1</sub>    | VM     | 0.1 $\mu$ F, low ESR ceramic capacitor to GND rated for VM  |
| C <sub>VM2</sub>    | VM     | Local bulk capacitor to GND, 10 $\mu$ F or higher, rated for VM to handle load transients. Refer the section on <a href="#">bulk capacitor sizing</a> .                     |
| C <sub>VCP</sub>    | VCP    | 1 $\mu$ F, 6.3 V low ESR ceramic capacitor to VM  |
| R <sub>IPROPI</sub> | IPROPI | Typically 500 - 5000 $\Omega$ 0.063 W resistor to GND, depending on the controller ADC dynamic range. Pin can be shorted to GND if ITRIP and IPROPI function is not needed. |
| C <sub>IPROPI</sub> | IPROPI | Optional 10 - 100nF, 6.3 V capacitor to GND to slow down the ITRIP regulation loop. Refer <a href="#">Over Current Protection (OCP) section</a> .                           |
| R <sub>nFAULT</sub> | nFAULT | Typically 1K $\Omega$ - 10 K $\Omega$ , 0.063 W pull-up resistor to controller supply. If nFAULT signaling is not used, this pin can be short to GND or left open.          |
| C <sub>VDD</sub>    | VDD    | 0.1 $\mu$ F, 6.3 V, low ESR ceramic capacitor to GND. This is applicable for the SPI (P) variant only.  |

### 7.3.2 Bridge Control

The DRV814x-Q1 family of devices provides a simple two pin control of the output through the pins, DRVOFF and IN.

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied. By default, the nSLEEP and DRVOFF pins have an internal pull-down and pull-up resistor respectively, to ensure the outputs are Hi-Z if no inputs are present. The IN pin also has an internal pull down resistor.

The device automatically generates the optimal dead-time needed during transitioning between the high-side and low-side FET on the switching half-bridge. This timing is based on internal FET gate-source voltage feedback. No external timing is required. This scheme ensures minimum dead time, while guaranteeing no shoot-through current.



**Note**

1. The SPI variant also provides additional control through the SPI\_IN register bits. Refer to - [Register - Pin control](#).
2. For the SPI (P) variant, ignore the nSLEEP column in the control table as there is no nSLEEP pin. Internally, nSLEEP = 1, always. The control table is valid when VDD > VDD<sub>POR</sub> level.

The table below shows the logic table for bridge control. For load illustration, refer the [Load Summary section](#).

**Table 7-3. Control table**

| nSLEEP | DRVOFF | IN | OUT   | IPROPI              | Device State |
|--------|--------|----|---|---------------------|--------------|
| 0      | X      | X  | Hi-Z  | No current          | SLEEP        |
| 1      | 1      | 0  | Hi-Z  | No current          | STANDBY      |
| 1      | 1      | 1  | Refer <a href="#">Off-state diagnostics table</a> | No current          | STANDBY      |
| 1      | 0      | 0  | L   | No current          | ACTIVE       |
| 1      | 0      | 1  | H <sup>(2)</sup>                                  | ISNS <sup>(1)</sup> | ACTIVE       |

(1) Current sourcing out of device (VM → OUTx → Load)

(2) If internal ITRIP regulation is enabled and ITRIP level is reached, then OUTx is forced "L" for a fixed time

**7.3.2.1 Register - Pin Control - SPI Variant Only**

The SPI variant allows control of the bridge through the specific register bits, S\_DRVOFF, S\_IN in the [SPI\\_IN](#) register, provided the **SPI\_IN register has been unlocked**. The user can unlock this register by writing the right combination to the SPI\_IN\_LOCK bits in the [COMMAND](#) register.

Additionally, the user can configure between an AND / OR logic combination of each of external input pin with their equivalent register bit in the SPI\_IN register. This logical configuration is done through the equivalent selects bits in the [CONFIG4](#) register:

- DRVOFF\_SEL and IN\_SEL

The control of the output is similar to the truth tables described in the section before, but with these logically combined inputs. These combined inputs are listed as follows:

- Combined input = Pin input **OR** equivalent SPI\_IN register bit, if equivalent CONFIG4 select bit = 1'b0
- Combined input = Pin input **AND** equivalent SPI\_IN register bit, if equivalent CONFIG4 select bit = 1'b1

Note that external nSLEEP pin is still needed for sleep function.

This logical combination offers more configurability to the user as shown in the table below.

**Table 7-4. Register - Pin Control Examples**

| Example                     | CONFIG4: xxx_SEL Bit | PIN status                 | SPI_IN Bit Status | Comment   |
|-----------------------------|----------------------|----------------------------|-------------------|---|
| DRVOFF as redundant shutoff | DRVOFF_SEL = 1'b0    | DRVOFF active              | S_DRVOFF active   | Either DRVOFF pin = 1 or S_DRVOFF bit = 1 will shutoff the output |
| Pin only control            | DRVOFF_SEL = 1'b1    | DRVOFF active              | S_DRVOFF = 1'b1   | Only DRVOFF pin function is available                             |
| Register only control       | IN_SEL = 1'b0        | IN - short to GND or float | S_IN active       | IN function will be controlled by the register bit alone          |

**7.3.3 Device Configuration**

This section describes the various device configurations to enable the user to configure the device to suit their use case.

### 7.3.3.1 Slew Rate (SR)

The SR pin (HW variant) or S\_SR bits in the [CONFIG3](#) register (SPI variant) determines the voltage slew rate of the driver output. This enables the user to optimize the PWM switching losses while meeting the EM conformance requirements. For the HW variant, SR is a **6-level setting**, while the SPI variant has 8 settings. For an inductive load, the slew rate control of the device depends on whether the recirculation path is through the high-side path to VM or through the low-side path to GND. Depending on the use-case, refer to the switching parameters table for either [high-side recirculation](#) or [low-side recirculation](#) in the Electrical Characteristics section for the slew rate range and values.

---

#### Note

The SPI variant also offers an **optional** spread spectrum clocking (SSC) feature that spreads the internal oscillator frequency +/- 12% around its mean with a period triangular function of ~1.3MHz to reduce emissions at higher frequencies. There is **no** spread spectrum clocking (SSC) feature in the HW variant.

---

In the HW variant, the SR pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

In the SPI variant, the slew rate setting can be changed at any time when SPI communication is available by writing to the S\_SR bits. This change is immediately reflected.

### 7.3.3.2 IPROPI

The device integrates a current sensing feature with a proportional analog current output on the IPROPI pin that can be used for load current regulation. This eliminates the need of an external sense resistor or sense circuitry reducing system size, cost, and complexity.

The device senses the load current by using a shunt-less high-side current mirror topology. This way the device can only sense an uni-directional high-side current from VM → OUT → Load through the high-side FET when it is fully turned ON (linear mode). The IPROPI pin outputs an analog current proportional to this sensed current scaled by  $A_{IPROPI}$  as follows:

$$I_{IPROPI} = I_{HS} [A] / A_{IPROPI}$$

The IPROPI pin must be connected to an external resistor ( $R_{IPROPI}$ ) to ground in order to generate a proportional voltage  $V_{IPROPI}$ . This allows for the load current to be measured as a voltage-drop across the  $R_{IPROPI}$  resistor with an analog to digital converter (ADC). The  $R_{IPROPI}$  resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized.

### 7.3.3.3 ITRIP Regulation

The device offers an optional internal load current regulation feature using fixed TOFF time method. This is done by comparing the voltage on the IPROPI pin against a reference voltage determined by ITRIP setting. TOFF time is fixed at 30µsec for HW variant, while it is configurable between or 20 to 50µsec for the SPI variant using TOFF\_SEL bits in the [CONFIG3](#) register.

The ITRIP regulation, when enabled, comes into action only when the HS FET is enabled and current sensing is possible. In this scenario, when the voltage on the IPROPI pin exceeds the reference voltage set by the ITRIP setting, the internal current regulation loop forces the following action:

- OUT = L for a fixed TOFF time

---

#### Note

The user inputs always takes **precedence** over the internal control. That means that if the inputs change during the TOFF time, the remainder of the TOFF time is ignored and the outputs will follow the inputs as commanded.

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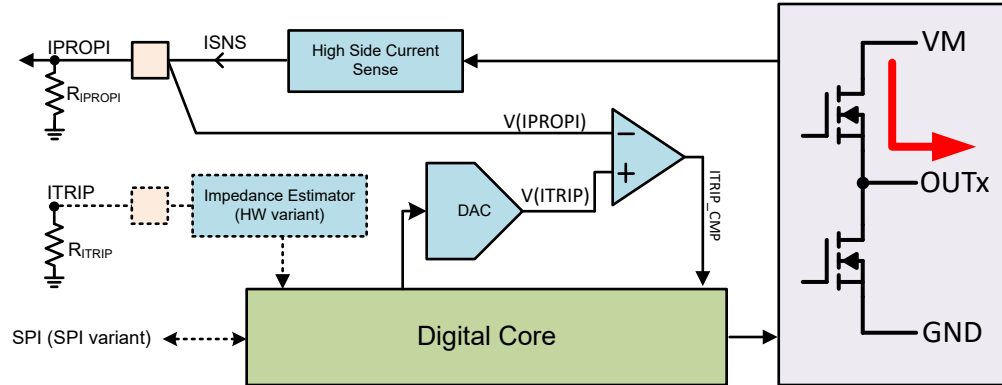


Figure 7-4. ITRIP Implementation

Current limit is set by the following equation:

$$\text{ITRIP regulation level} = (V_{ITRIP} / R_{IPROPI}) \times A_{IPROPI} \quad (2)$$

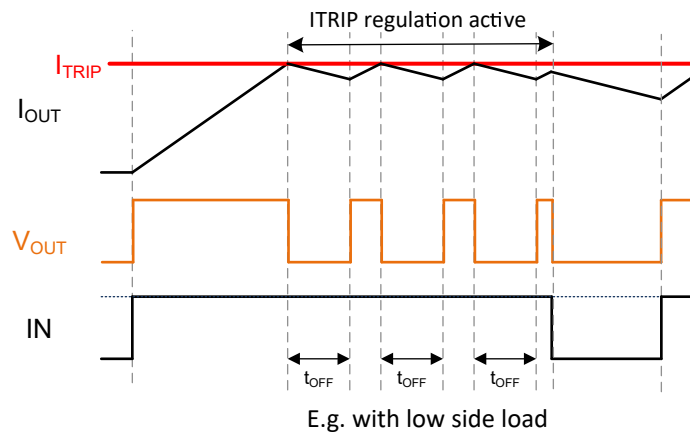


Figure 7-5. Fixed TOFF ITRIP Current Regulation

The ITRIP comparator output (ITRIP\_CMP) is ignored during output slewing to avoid false triggering of the comparator output due to current spikes from the load capacitance. Additionally, in the event of transition from low-side recirculation, an additional blanking time  $t_{BLANK}$  is needed for the sense loop to stabilize before the ITRIP comparator output is valid.

ITRIP is a **6-level setting** for the HW variant. The SPI variant offers two more settings. This is summarized in the table below:

Table 7-5. ITRIP Table

| ITRIP Pin            | S_ITRIP Register Bits | $V_{ITRIP}$ [V]     |
|----------------------|-----------------------|---------------------|
| R <sub>LVL10F6</sub> | 3'b000                | Regulation Disabled |
| R <sub>LVL20F6</sub> | 3'b001                | 1.18                |
| Not available        | 3'b010                | 1.41                |
| Not available        | 3'b011                | 1.65                |
| R <sub>LVL30F6</sub> | 3'b100                | 1.98                |
| R <sub>LVL40F6</sub> | 3'b101                | 2.31                |
| R <sub>LVL50F6</sub> | 3'b110                | 2.64                |
| R <sub>LVL60F6</sub> | 3'b111                | 2.97                |

In the HW variant of the device, the ITRIP pin changes are **transparent** and changes are reflected immediately.

In the SPI variant of the device, the ITRIP setting can be changed at any time when SPI communication is available by writing to the S\_ITRIP bits. This change is immediately reflected in the device behavior.

SPI variant only - If the ITRIP regulation levels are reached, the ITRIP\_CMP bit in the [STATUS1](#) register is set. There is no nFAULT pin indication. This bit can be cleared with a CLR\_FLT command.

#### Note

If the application requires a linear ITRIP control with multiple steps beyond the choices provided by the device, an external DAC can be used to force the voltage on the bottom side of the IPROPI resistor, instead of terminating it to GND. With this modification, the ITRIP current can be controlled by the external DAC setting as follows:

$$\text{ITRIP regulation level} = [(V_{\text{ITRIP}} - V_{\text{DAC}}) / R_{\text{IPROPI}}] \times A_{\text{IPROPI}} \quad (3)$$

### 7.3.3.4 DIAG

The DIAG is a pin (HW variant) or register (SPI variant) setting that is used in both ACTIVE and STANDBY operation of the device, as follows:

- STANDBY state
  - Enable or disable [Off-state diagnostics \(OLP\)](#), as well as select the OLP combinations when enabled. Refer to the tables in the [Off-state diagnostics \(OLP\)](#) section for details on this.
- ACTIVE state
  - Mask ITRIP regulation function if the load type is indicated as high-side load.
  - SPI variant only - Mask active open load detection (OLA) if the load type is indicated as low-side. load
  - HW variant only - Configure fault reaction between retry and latch settings

#### 7.3.3.4.1 HW variant

For the HW variant, the DIAG pin is a [6-level setting](#). Depending on the mode, its configurations are summarized in the table below.

**Table 7-6. DIAG table for HW variant**

| DIAG pin             | STANDBY state          | ACTIVE state   |                |                        |
|----------------------|------------------------|----------------|----------------|------------------------|
|                      | Off-state diagnostics  | Fault reaction | IPROPI / ITRIP | Comment                |
| R <sub>LVL10F6</sub> | Disabled               | Retry          | Available      | Use for low-side load  |
| R <sub>LVL20F6</sub> | Enabled <sup>(1)</sup> | Latch          | Available      |                        |
| R <sub>LVL30F6</sub> | Enabled <sup>(1)</sup> | Latch          | Disabled       | Use for high-side load |
| R <sub>LVL40F6</sub> | Enabled <sup>(1)</sup> | Retry          | Disabled       |                        |
| R <sub>LVL50F6</sub> | Disabled               | Latch          | Available      | Use for low-side load  |
| R <sub>LVL60F6</sub> | Enabled <sup>(1)</sup> | Retry          | Available      |                        |

(1) Refer to the tables in the [Off-state diagnostics \(OLP\)](#) section for combination details

#### Note

HW variant only - Option to disable off-state diagnostics for a high-side load use case is not supported. In this case, setting DRVOFF pin high and IN pin low is only way to disable off-state diagnostics.

In the HW variant, the DIAG pin is **latched** during device initialization following power-up or wake-up from sleep. Update during operation is blocked.

#### 7.3.3.4.2 SPI variant

For the SPI variant, S\_DIAG is a 2-bit setting in the [CONFIG2](#) register. Depending on the mode, its configurations are summarized in the table below.

**Table 7-7. DIAG table for the SPI variant**

| S_DIAG bits | STANDBY state          |                      | ACTIVE state   |  | Comment                |
|-------------|------------------------|----------------------|----------------|--|------------------------|
|             | Off-state diagnostics  | On-state diagnostics | IPROPI / ITRIP |  |                        |
| 2'b00       | Disabled               | Disabled             | Available      |  | Use for low-side load  |
| 2'b01       | Enabled <sup>(1)</sup> | Disabled             | Available      |  |                        |
| 2'b10       | Disabled               | Available            | Disabled       |  | Use for high-side load |
| 2'b11       | Enabled <sup>(1)</sup> | Available            | Disabled       |  |                        |

(1) Refer to the tables in the [Off-state diagnostics \(OLP\)](#) section for combination details

In the SPI variant of the device, the settings can be changed anytime when SPI communication is available by writing to the S\_DIAG bits. This change is immediately reflected.

### 7.3.4 Protection and Diagnostics

The driver is protected against over-current and over-temperature events to ensure device robustness. Additionally, the device also offers load monitoring (on-state and off-state), over/ under voltage monitoring on VM pin as well as under voltage monitoring on the VCP pin to signal any unexpected voltage conditions. Fault signaling is done through a low-side open drain nFAULT pin which gets pulled to GND by  $I_{nFAULT\_PD}$  current on detection of a fault condition. Transition to SLEEP state automatically de-asserts nFAULT.

#### Note

In the SPI variant, nFAULT pin logic level is the inverted copy of the FAULT bit in the [FAULT SUMMARY](#) register. Only exception is when off-state diagnostics are enabled and SPI\_IN register is locked (Refer [OLP section](#)).

For the SPI variant, whenever nFAULT is asserted low, the device logs the fault into the FAULT SUMMARY and STATUS registers. These registers can be cleared only by

- CLR FLT command or
- SLEEP command through the nSLEEP pin

It is possible to get all the useful diagnostic information for periodic software monitoring in a single 16 bit SPI frame by:

- Reading the STATUS1 register during ACTIVE state
- Reading the STATUS2 register during STANDBY state

All the diagnosable fault events can be uniquely identified by reading the STATUS registers.

#### 7.3.4.1 Over Current Protection (OCP)

- Device state: ACTIVE
- Mechanism & thresholds: An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold,  $I_{OCP}$ , for longer than  $t_{OCP}$ , then an over current fault is detected.
- Action:
  - nFAULT pin is asserted low
  - OUT is Hi-Z
  - For a short to GND fault (over current detected on the high-side FET), the IPROPI pin continues to be pulled up to  $V_{IPROPI\_LIM}$  even if the FET has been disabled. For the HW variant, this helps differentiate a short to GND fault during ACTIVE state from other fault types, as the IPROPI pin is pulled high while the nFAULT pin is asserted low.
- Reaction configurable between latch setting and retry setting based on  $t_{RETRY}$  and  $t_{CLEAR}$
- User can add a capacitor in the range of 10nF to 100nF on the IPROPI pin to ensure OCP detection in case of a load short condition when internal ITRIP regulation is enabled. This is especially true where there is enough inductance in the short that causes ITRIP regulation to trigger ahead of the OCP detection, resulting in the device missing the short detection. To ensure that OCP detection wins this race condition, a small

capacitance added on the IPROPI pin slows down the ITRIP regulation loop enough to allow the OCP detection circuit to work as intended.

The SPI variant offers configurable  $I_{OCP}$  levels and  $t_{OCP}$  filter times. Refer [CONFIG4](#) register for these settings.

#### 7.3.4.2 Over Temperature Protection (TSD)

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: The device has several temperature sensors spread around the die. If any of the sensors detect an over temperature event, set by  $T_{TSD}$  for a time greater than  $t_{TSD}$ , then an over temperature fault is detected.
- Action:
  - nFAULT pin is asserted low
  - OUT is Hi-Z
  - IPROPI pin is Hi-Z
- Reaction configurable between latch setting and retry setting based on  $T_{HYS}$  and  $t_{CLEAR\_TSD}$

#### 7.3.4.3 Off-State Diagnostics (OLP)

The user can determine the impedence on the OUT node using off-state diagnostics in the STANDBY state when the power FETs are off. With this diagnostics, it is possible to detect the following fault conditions passively in the STANDBY state:

- Output short to VM or GND < 100 $\Omega$
- Open load > 1K $\Omega$  for low-side load
- Open load > 10K $\Omega$  for high-side load, VM = 13.5V

---

#### Note

It is NOT possible to detect a **load short** with this diagnostic. However, the user can deduce this logically if an over current fault (OCP) occurs during ACTIVE operation, but OLP diagnostics do not report any fault in the STANDBY state. Occurrence of both OCP in the ACTIVE state and OLP in the STANDBY state would imply a terminal short (short on OUT node).

---

- The user can configure the following combinations
  - Internal pull up resistor ( $R_{OLP\_PU}$ ) on OUT
  - Internal pull down resistor ( $R_{OLP\_PD}$ ) on OUT
  - Comparator reference level
- This combination is determined by the controller inputs (pins only for the HW variant) or equivalent bits in the [SPI\\_IN](#) register for the SPI variant if the SPI\_IN register has been unlocked.
- HW variant - When off-state diagnostics are enabled, comparator output (OLP\_CMP) is available on nFAULT pin.
- SPI variant - The off-state diagnostics comparator output (OLP\_CMP) is available on OLP\_CMP bit in [STATUS2](#) register. Additionally, if the SPI\_IN register has been locked, this comparator output is also available on the nFAULT pin when off-state diagnostics are enabled.
- The user is expected to toggle through all the combinations and record the comparator output after its output is settled.
- Based on the input combinations and comparator output, the user can determine if there is a fault on the output.

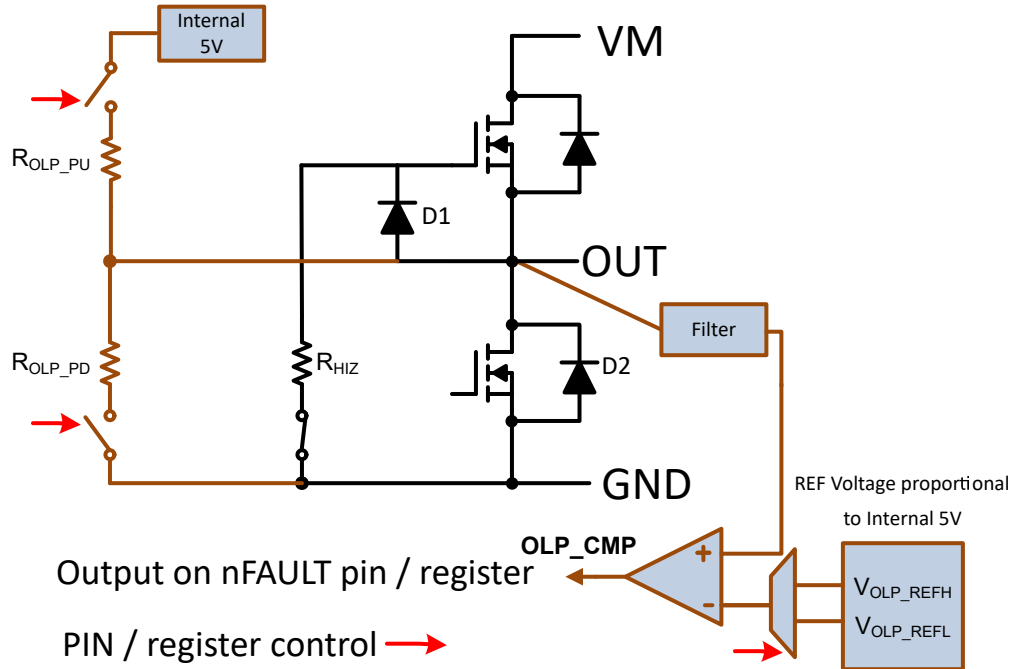


Figure 7-6. Off-State (Passive) Diagnostics

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a low-side load is shown in Table 7-8.

Table 7-8. Off-State Diagnostics Table for a Low-Side Load

| User Inputs |             |        |        |    | OLP Set-Up          |                       | OLP_CMP Output |      |       |
|-------------|-------------|--------|--------|----|---------------------|-----------------------|----------------|------|-------|
| DIAG Pin    | S_DIAG Bits | nSLEEP | DRVOFF | IN | OUT                 | CMP REF               | Normal         | Open | Short |
| LVL2, LVL6  | 2'b01       | 1      | 1      | 1  | R <sub>OLP_PU</sub> | V <sub>OLP_REFH</sub> | L              | H    | H     |
| LVL3, LVL4  | 2'b11       | 1      | 1      | 1  | R <sub>OLP_PD</sub> | V <sub>OLP_REFL</sub> | L              | L    | H     |

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a high-side load is shown in Table 7-9.

Table 7-9. Off-State Diagnostics Table for a High-Side Load

| User Inputs |             |        |        |    | OLP Set-Up          |                       | OLP_CMP Output |      |       |
|-------------|-------------|--------|--------|----|---------------------|-----------------------|----------------|------|-------|
| DIAG Pin    | S_DIAG Bits | nSLEEP | DRVOFF | IN | OUT                 | CMP REF               | Normal         | Open | Short |
| LVL2, LVL6  | 2'b01       | 1      | 1      | 1  | R <sub>OLP_PU</sub> | V <sub>OLP_REFH</sub> | H              | H    | L     |
| LVL3, LVL4  | 2'b11       | 1      | 1      | 1  | R <sub>OLP_PD</sub> | V <sub>OLP_REFL</sub> | H              | L    | L     |

#### 7.3.4.4 On-State Diagnostics (OLA) - SPI Variant Only

- Device state: ACTIVE - high-side recirculation
- Mechanism and threshold: On-state diagnostics (OLA) can detect an open load detection in the ACTIVE state during high-side recirculation. This includes high-side load connected directly to VM or through a high-side FET on the other half-bridge. During a PWM switching transition, the inductive load current re-circulates into VM through the HS body diode when the LS FET is turned OFF. The device looks for a voltage spike on OUTx above VM during the brief dead time, before the HS FET is turned ON. To observe the voltage spike, this load current needs to be higher than the pull down current (I<sub>PD\_OLA</sub>) on the output asserted by the FET

driver. Absence of this voltage spike for "3" consecutive re-circulation switching cycles indicates a loss of load inductance or increase in load resistance and is detected as an OLA fault.

- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between latch setting and retry setting. In retry setting, OLA fault is automatically cleared with the detection of "3" consecutive voltage spikes during re-circulation switching cycles.

This monitoring is optional and can be disabled.

#### Note

1. OLA is not supported for low-side loads (low-side recirculation).

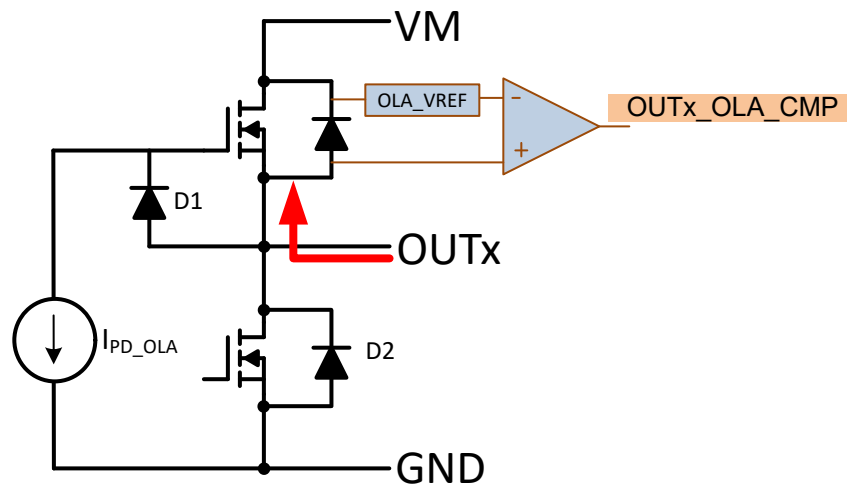


Figure 7-7. On-State Diagnostics

#### 7.3.4.5 VM Over Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin exceeds the threshold, set by  $V_{VMOV}$  for a time greater than  $t_{VMOV}$ , then an VM over voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained
  - IPROPI pin - normal function maintained
- Reaction configurable between retry and latch setting

In the SPI variant, this monitoring is optional and can be disabled. Also the thresholds are configurable. Refer [CONFIG1](#) register.

#### 7.3.4.6 VM Under Voltage Monitor

- Device state: STANDBY, ACTIVE
- Mechanism & thresholds: If the supply voltage on the VM pin drops below the threshold, set by  $V_{VMUV}$  for a time greater than  $t_{VMUV}$ , then an VM under voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - OUT is Hi-Z
  - IPROPI pin is Hi-Z



- HW and SPI (S) variant: Reaction fixed to retry setting
- Only for SPI (P) variant: Reaction configurable between retry and latch setting
- Note that retry time is only dependent on recovery of VM under voltage condition and is independent of  $t_{RETRY}$  /  $t_{CLEAR}$  times

#### 7.3.4.7 Charge pump under voltage monitor

- Device state: ACTIVE
- Mechanism & thresholds: If the voltage on the VCP pin falls below the threshold, set by  $V_{VCPUV}$  for a time greater than  $t_{VCPUV}$ , then a VCP under voltage fault is detected.
- Action:
  - nFAULT pin is asserted low
  - Output - normal function maintained. However, the high-side FET between VM and OUT becomes resistive in this charge pump under voltage condition to a point where it may even appear to Hi-Z due to lack of voltage headroom.
  - IPROPI pin - normal function maintained. However, current sense is affected in this charge pump voltage condition to a point where it may even appear to be Hi-Z due to lack of voltage headroom.
- Reaction fixed to retry based on  $V_{VCPUV\_HYS}$

#### 7.3.4.8 Power On Reset (POR)

- Device state: ALL
- Mechanism & thresholds: If logic supply drops below  $VDD_{POR\_FALL}$  for a time greater than  $t_{POR}$ , then a power on reset will occur that will hard reset the device.
- Action:
  - nFAULT pin is de-asserted
  - OUT is Hi-Z
  - IPROPI pin is Hi-Z.
  - When this supply recovers above the  $VDD_{POR\_RISE}$  level, the device will go through a wake-up initialization and nFAULT pin will be asserted low to notify the user on this reset (Refer [Wake-up transients](#)).
- HW and SPI (S) variant: These thresholds translate to  $VM_{POR\_FALL}$  and  $VM_{POR\_RISE}$  as the logic supply is internally derived from the VM supply
- Only for SPI (P) variant: These thresholds directly map to the VDD pin voltage ( $VDD_{POR\_FALL}$  and  $VDD_{POR\_RISE}$ )
- Fault reaction: Always retry, retry time depends on the external supply condition to initiate a device wake-up

#### 7.3.4.9 Event Priority

In the ACTIVE state, in a scenario where two or more events occur simultaneously, the device assigns control of the driver based on the following priority table.

**Table 7-10. Event Priority Table**

| Event   | Priority |
|---|----------|
| User SLEEP command                              | 1        |
| User input: DRVOFF                              | 2        |
| Over temperature detection (TSD)                | 3        |
| Over current detection (OCP) <sup>(1)</sup>     | 4        |
| VM under voltage detection (VMUV)               | 5        |
| Under input: IN                                 | 6        |
| Internal PWM control from ITRIP regulation      | 7        |
| VM over voltage detection (VMOV) <sup>(2)</sup> | 8        |
| Charge pump under voltage (CPUV) <sup>(2)</sup> | 9        |

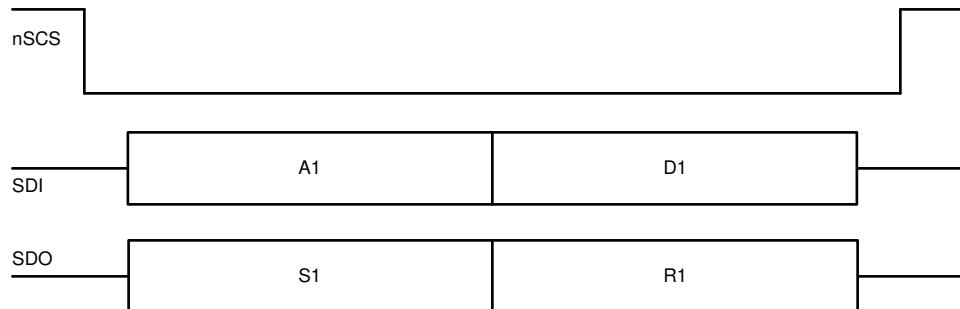
(1) If the device is waiting for an OCP event to be confirmed (waiting for  $t_{OCP}$ ) when any of events with lower priority than OCP occur, then the device may delay servicing the other events up to a maximum time of  $t_{OCP}$  to enable detection of the OCP event.

(2) Priority is "don't care" in this case as this fault event does not cause a change in OUTx

## 7.4 Programming - SPI Variant Only

### 7.4.1 SPI Interface

The SPI variant has full-duplex, 4-wire synchronous communication that is used to set device configurations, operating parameters, and read out diagnostic information from the device. The SPI operates in peripheral mode and connects to a controller. The serial data input (SDI) word consists of a 16-bit word, with an 8-bit command (A1), followed by 8-bit data (D1). The serial data output (SDO) word consists of the FAULT\_SUMMARY byte (S1), followed by a report byte (R1). The report byte is either the register data being accessed by read command or null for a write command. The data sequence between the MCU and the SPI peripheral driver is shown in Figure 7-8.



**Figure 7-8. SPI Data - Standard "16-bit" Frame**

A valid frame must meet the following conditions:

- SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- nSCS pin should be pulled high between words.
- When nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data on SDO from the device is propagated on the rising edge of SCLK, while data on SDI is captured by the device on the subsequent falling edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for a valid transaction for a standard frame, or alternately, for a daisy chain frame with "n" number of peripheral devices, 16 + (n x 16) SCLK cycles must occur for a valid transaction. Else, a frame error (SPI\_ERR) is reported and the data is ignored if it is a WRITE operation.

### 7.4.2 Standard Frame

The SDI input data word is 2 bytes long and consists of the following format:

- Command byte (first byte)
  - MSB bit indicates frame type (bit B15 = 0 for standard frame).
  - Next to MSB bit, W0, indicates read or write operation (bit B14, write = 0, read = 1)
  - Followed by 6 address bits, A[5:0] (bits B13 through B8)
- Data byte (second byte)
  - Second byte indicates data, D[7:0] (bits B7 through B0). For a read operation, these bits are typically set to null values, while for a write operation, these bits have the data value for the addressed register.

**Table 7-11. SDI - Standard Frame Format**

|      | Command Byte |     |     |     |     |     |    |    | Data Byte |    |    |    |    |    |    |    |
|------|--------------|-----|-----|-----|-----|-----|----|----|-----------|----|----|----|----|----|----|----|
| Bit  | B15          | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7        | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Data | 0            | W0  | A5  | A4  | A3  | A2  | A1 | A0 | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

The SDO output data word is 2 bytes long and consists of the following format:

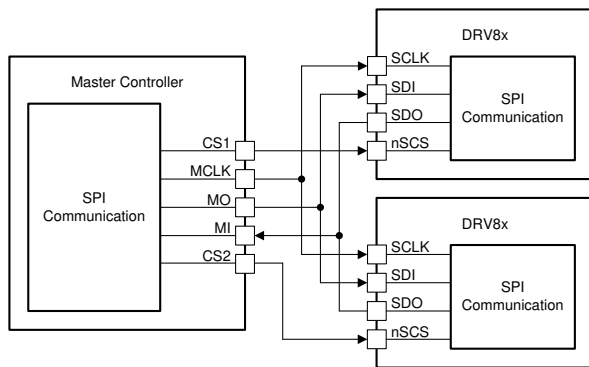
- Status byte (first byte)
  - 2 MSB bits are forced high (B15, B14 = 1)
  - Following 6 bits are from the FAULT SUMMARY register (B13:B8)
- Report byte (second byte)
  - The second byte (B7:B0) is either the data currently in the register being read for a read operation (W0 = 1), or, existing data in the register being written to for a write command (W0 = 0)

**Table 7-12. SDO - Standard Frame Format**

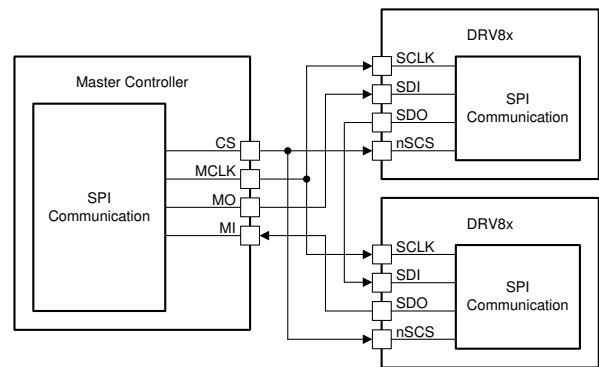
| Bit  | Status Byte |     |       |      |      |     |     |         | Report Byte |    |    |    |    |    |    |    |
|------|-------------|-----|-------|------|------|-----|-----|---------|-------------|----|----|----|----|----|----|----|
|      | B15         | B14 | B13   | B12  | B11  | B10 | B9  | B8      | B7          | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Data | 1           | 1   | FAULT | VMOV | VMUV | OCF | TSD | SPI_ERR | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### 7.4.3 SPI Interface for Multiple Peripherals

Multiple devices can be connected to the controller with and without the daisy chain. For connecting a 'n' number of devices to a controller without using a daisy chain, 'n' number of I/O resources from controller has to be utilized for nSCS pins as shown in Figure 7-9. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple devices. Figure 7-10



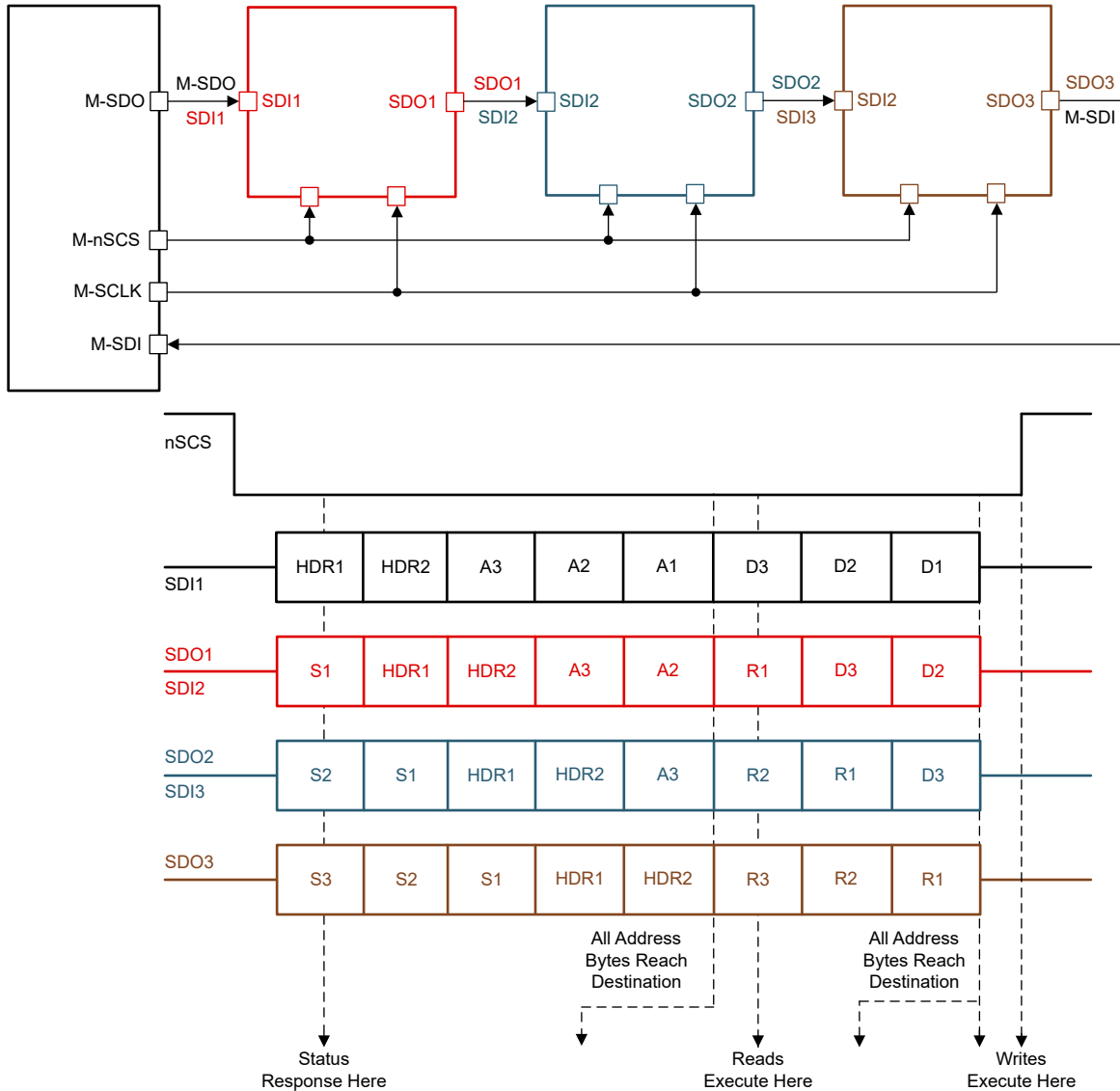
**Figure 7-9. SPI Operation Without Daisy Chain**



**Figure 7-10. SPI Operation With Daisy Chain**

### 7.4.3.1 Daisy Chain Frame for Multiple Peripherals

The device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 7-11 shows the topology with waveforms, where, number of peripherals connected in a daisy chain "n" is set to 3. A maximum of up to 63 devices can be connected in this manner.



**Figure 7-11. Daisy Chain SPI Operation**

The SDI sent by the controller in this case would be in the following format (see SDI1 in Figure 7-11 ):

- 2 bytes of header (HDR1, HDR2)
- "n" bytes of **command byte** starting with furthest peripheral in the chain (for this example, this is A3, A2, A1)
- "n" bytes of **data byte** starting with furthest peripheral in the chain (for this example, this is D3, D2, D1)
- Total of 2 x "n" + 2 bytes

While the data is being transmitted through the chain, the controller receives it in the following format (see SDO3 in Figure 7-11):

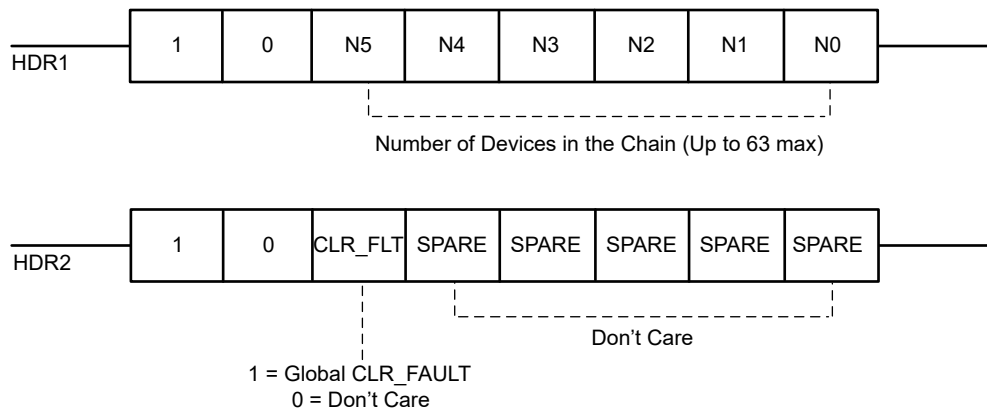
- 3 bytes of **status byte** starting with furthest peripheral in the chain (for this example, this is S3, S2, S1)
- 2 bytes of header that were transmitted before (HDR1, HDR2)

- 3 bytes of [report byte](#) starting with furthest peripheral in the chain (for this example, this is R3, R2, R1)

The Header bytes are special bytes asserted at the beginning of a daisy chain SPI communication. **Header bytes must start with 1 and 0 for the two leading bits.**

The first header byte (HDR1) contains information of the total number of peripheral devices in the daisy chain. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in [Figure 7-12](#). Up to 63 devices can be connected in series per daisy chain connection. Number of peripheral = 0 is not permitted and will result in a SPI\_ERR flag.

The second header byte (HDR2) contains a global [CLR\\_FAULT](#) command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. The 5 trailing bits of the HDR2 register are marked as SPARE (don't care bits). These can be used by the MCU to determine integrity of the daisy chain connection.



**Figure 7-12. Header bytes**

In addition, the device recognizes bytes that start with 1 and 1 for the two leading bits as a "pass" byte. These "pass" bytes are NOT processed by the device, but they are simply transmitted out on SDO in the following byte.

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two status bytes before receiving the two header bytes.

From the two status bytes it knows that its position is second in the chain, and from HDR1 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The command, data, status and report bytes remain the same as described in the [standard frame format](#).

## 8 Register Map - SPI Variant Only

This section describes the user configurable registers in the device.

---

### Note

While the device allows register writes at any time SPI communication is available, it is recommended to exercise caution while updating registers in the ACTIVE state while the load is being driven. This is especially important for settings such as S\_DIAG which control the critical device configuration. In order to prevent accidental register writes, the device offers a locking mechanism through the REG\_LOCK bits in the [COMMAND](#) register to lock the contents of all configurable registers. Best practice would be to write all the configurable registers during initialization and then lock these settings. Run-time register writes for output control are handled by the [SPI\\_IN](#) register, which offers its own separate locking mechanism through the SPI\_IN\_LOCK bits.

---

## 8.1 User Registers

The following table lists all the registers that can be accessed by the user. All register addresses NOT listed in this table should be considered as "reserved" locations and access is blocked to this space. Accessing them will cause a SPI\_ERR.

**Table 8-1. User Registers**

| Name          | Bit 7                  | Bit 6                  | Bit 5              | Bit 4                  | Bit 3                            | Bit 2                               | Bit 1                | Bit 0                      | Type <sup>(2)</sup> | Addr |
|---------------|------------------------|------------------------|--------------------|------------------------|----------------------------------|-------------------------------------|----------------------|----------------------------|---------------------|------|
| DEVICE_ID     | DEV_ID[5]              | DEV_ID[4]              | DEV_ID[3]          | DEV_ID[2]              | DEV_ID[1]                        | DEV_ID[0]                           | REV_ID[1]            | REV_ID[0]                  | R                   | 00h  |
| FAULT_SUMMARY | SPI_ERR <sup>(3)</sup> | POR                    | FAULT              | VMOV                   | VMUV                             | OCP                                 | TSD                  | VCPUV <sup>(3)</sup>       | R                   | 01h  |
| STATUS1       | OLA <sup>(6)</sup>     | OLA <sup>(6)</sup>     | ITRIP_CMP          | ACTIVE                 | OCP_H <sup>(7)</sup>             | OCP_L <sup>(8)</sup>                | OCP_H <sup>(7)</sup> | OCP_L <sup>(8)</sup>       | R                   | 02h  |
| STATUS2       | DRVOFF_STAT            | N/A <sup>(4)</sup>     | N/A <sup>(4)</sup> | ACTIVE                 | N/A <sup>(4)</sup>               | N/A <sup>(4)</sup>                  | N/A <sup>(4)</sup>   | OLP_CMP                    | R                   | 03h  |
| COMMAND       | CLR_FLT                | N/A <sup>(4)</sup>     | N/A <sup>(4)</sup> | SPI_IN_LOCK[1]         | SPI_IN_LOCK[0]<br><sup>(1)</sup> | N/A <sup>(4)</sup>                  | REG_LOCK[1]          | REG_LOCK[0] <sup>(1)</sup> | R/W                 | 08h  |
| SPI_IN        | N/A <sup>(4)</sup>     | N/A <sup>(4)</sup>     | N/A <sup>(4)</sup> | N/A <sup>(4)</sup>     | S_DRVOFF <sup>(1)</sup>          | SPARE <sup>(5)</sup> <sup>(1)</sup> | SPARE <sup>(5)</sup> | S_IN                       | R/W                 | 09h  |
| CONFIG1       | EN_OLA                 | VMOV_SEL[1]            | VMOV_SEL[0]        | SSC_DIS <sup>(1)</sup> | OCP_RETRY                        | TSD_RETRY                           | VMOV_RETRY           | OLA_RETRY                  | R/W                 | 0Ah  |
| CONFIG2       | SPARE <sup>(5)</sup>   | S_DIAG[1]              | S_DIAG[0]          | N/A <sup>(4)</sup>     | N/A <sup>(4)</sup>               | S_ITRIP[2]                          | S_ITRIP[1]           | S_ITRIP[0]                 | R/W                 | 0Bh  |
| CONFIG3       | TOFF[1]                | TOFF[0] <sup>(1)</sup> | N/A <sup>(4)</sup> | S_SR[2]                | S_SR[1]                          | S_SR[0]                             | SPARE <sup>(5)</sup> | SPARE <sup>(5)</sup>       | R/W                 | 0Ch  |
| CONFIG4       | TOCP_SEL[1]            | TOCP_SEL[0]            | N/A <sup>(4)</sup> | OCP_SEL[1]             | OCP_SEL[0]                       | DRVOFF_SEL <sup>(1)</sup>           | SPARE <sup>(5)</sup> | IN_SEL                     | R/W                 | 0Dh  |

- (1) Defaulted to 1b on reset, others are defaulted to 0b on reset
- (2) R = Read Only, R/W = Read/Write
- (3) VCPUV replaced by SPI\_ERR in the first SDO byte response, common to all SPI frames. Refer [SDO - Standard frame format](#).
- (4) N/A = Not available (read back of this bit will be 0b)
- (5) SPARE = Don't care bits. These are available to USER as scratch bits.
- (6) OLA is indicated if either of the two OLA bits is set
- (7) OCP\_L is indicated if either of the two OCP\_L bits is set
- (8) OCP\_H is indicated if either of the two OCP\_H bits is set

### 8.1.1 DEVICE\_ID register (Address = 00h)

Return to the [User Register table](#).

| Device      | DEVICE_ID value |
|-------------|-----------------|
| DRV8143S-Q1 | BAh             |
| DRV8144S-Q1 | CAh             |
| DRV8145S-Q1 | DAh             |
| DRV8143P-Q1 | BEh             |
| DRV8145P-Q1 | DEh             |

### 8.1.2 FAULT\_SUMMARY Register (Address = 01h) [reset = 40h]

Return to the [User Register table](#).

| Bit | Field   | Type | Reset | Description  |
|-----|---------|------|-------|--|
| 7   | SPI_ERR | R    | 0b    | 1b indicates that a SPI communication fault has occurred in the previous SPI frame.  |
| 6   | POR     | R    | 1b    | 1b indicates that a power-on-reset has been detected.  |
| 5   | FAULT   | R    | 0b    | Logic OR of SPI_ERR, POR, VMOV, VMUV, OCP, TSD, OLA & VCPUV  |
| 4   | VMOV    | R    | 0b    | 1b indicates that a VM over voltage has been detected. Refer <a href="#">VMOV_SEL</a> to change thresholds or disable diagnostic, <a href="#">VMOV_RETRY</a> to configure fault reaction.  |
| 3   | VMUV    | R    | 0b    | 1b indicates that a VM under voltage has been detected.  |
| 2   | OCP     | R    | 0b    | 1b indicates that an over current has been detected in either one or more power FETs. Refer <a href="#">OCP_SEL</a> , <a href="#">TOCP_SEL</a> to change thresholds & filter times. Refer <a href="#">OCP_RETRY</a> to configure fault reaction. |
| 1   | TSD     | R    | 0b    | 1b indicates that an over temperature has been detected. Refer <a href="#">TSD_RETRY</a> to configure fault reaction.  |
| 0   | VCPUV   | R    | 0b    | 1b indicates that a charge pump under voltage has been detected.   |

### 8.1.3 STATUS1 Register (Address = 02h) [reset = 00h]

Return to the [User Register table](#).

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 7   | OLA       | R    | 0b    | 1b indicates that an open load condition has been detected in the ACTIVE state on OUT |
| 6   | OLA       | R    | 0b    | 1b indicates that an open load condition has been detected in the ACTIVE state on OUT |
| 5   | ITRIP_CMP | R    | 0b    | 1b indicates that load current has reached the ITRIP regulation level.                |
| 4   | ACTIVE    | R    | 0b    | 1b indicates that the device is in the ACTIVE state                                   |



| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--|
| 3   | OCP_H | R    | 0b    | 1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT |
| 2   | OCP_L | R    | 0b    | 1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT   |
| 1   | OCP_H | R    | 0b    | 1b indicates that an over current has been detected on the high-side FET (short to GND) on OUT |
| 0   | OCP_L | R    | 0b    | 1b indicates that an over current has been detected on the low-side FET (short to VM) on OUT   |

#### 8.1.4 STATUS2 Register (Address = 03h) [reset = 80h]

Return to the [User Register table](#).

| Bit     | Field       | Type | Reset | Description   |
|---------|-------------|------|-------|---|
| 7       | DRVOFF_STAT | R    | 1b    | This bit shows the status of the DRVOFF pin. 1b implies the pin status is high. |
| 6, 5    | N/A         | R    | 0b    | Not available   |
| 4       | ACTIVE      | R    | 0b    | 1b indicates that the device is in the ACTIVE state (Copy of bit4 in STATUS1)   |
| 3, 2, 1 | N/A         | R    | 0b    | Not available   |
| 0       | OLP_CMP     | R    | 0b    | This bit is the output of the off-state diagnostics (OLP) comparator.           |

#### 8.1.5 COMMAND Register (Address = 08h) [reset = 09h]

Return to the [User Register table](#).

| Bit | Field       | Type | Reset | Description  |
|-----|-------------|------|-------|--|
| 7   | CLR_FLT     | R/W  | 0b    | Clear Fault command - Write 1b to clear all faults reported in the fault registers and de-assert the nFAULT pin  |
| 6-5 | N/A         | R    | 0b    | Not available  |
| 4-3 | SPI_IN_LOCK | R/W  | 01b   | Write 10b to <b>unlock</b> the SPI_IN register<br>Write 01b or 00b or 11b to <b>lock</b> the SPI_IN register<br>SPI_IN register is <b>locked</b> by default.       |
| 2   | N/A         | R    | 0b    | Not available  |
| 1-0 | REG_LOCK    | R/W  | 01b   | Write 10b to <b>lock</b> the CONFIG registers<br>Write 01b or 00b or 11b to <b>unlock</b> the CONFIG registers<br>CONFIG registers are <b>unlocked</b> by default. |

### 8.1.6 SPI\_IN Register (Address = 09h) [reset = 0Ch]

Return to the [User Register table](#).

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7-4 | N/A      | R    | 0b    | Not available  |
| 3   | S_DRVOFF | R/W  | 1b    | Register bit equivalent of DRVOFF pin when SPI_IN is unlocked. Refer <a href="#">Register Pin control</a> section. |
| 2-1 | N/A      | R    | 10b   | Not available  |
| 0   | S_IN     | R/W  | 0b    | Register bit equivalent of IN pin when SPI_IN is unlocked. Refer <a href="#">Register Pin control</a> section      |

### 8.1.7 CONFIG1 Register (Address = 0Ah) [reset = 10h]

Return to the [User Register table](#).

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7   | EN_OLA     | R/W  | 0b    | Write 1b to enable open load detection in the active state. In Independent mode, OLA is always disabled for low-side load. Refer <a href="#">DIAG</a> section.   |
| 6-5 | VMOV_SEL   | R/W  | 0b    | Determines the thresholds for the VM over voltage diagnostics<br>00b = VM > 35V<br>01b = VM > 28V<br>10b = VM > 18V<br>11b = VMOV disabled   |
| 4   | SSC_DIS    | R/W  | 1b    | 0b: Enables the spread spectrum clocking feature   |
| 3   | OCP_RETRY  | R/W  | 0b    | Write 1b to configure fault reaction to retry setting on the detection of over current, else the fault reaction is latched   |
| 2   | TSD_RETRY  | R/W  | 0b    | Write 1b to configure fault reaction to retry setting on the detection of over temperature, else the fault reaction is latched   |
| 1   | VMOV_RETRY | R/W  | 0b    | Write 1b to configure fault reaction to retry setting on the detection of VMOV, else the fault reaction is latched.<br><br><b>Note</b><br><br>For the SPI (P) variant, this bit also controls the fault reaction for a VM under voltage detection. |
| 0   | OLA_RETRY  | R/W  | 0b    | Write 1b to configure fault reaction to retry setting on the detection of open load during active, else the fault reaction is latched.   |

### 8.1.8 CONFIG2 Register (Address = 0Bh) [reset = 00h]

Return to the [User Register table](#).

| Bit | Field   | Type | Reset | Description   |
|-----|---------|------|-------|---|
| 7   | SPARE   | R/W  | 0b    | Don't care  |
| 6-5 | S_DIAG  | R/W  | 0b    | Load type indication - refer to <a href="#">DIAG table</a>    |
| 4-3 | N/A     | R    | 0b    | Not available   |
| 2-0 | S_ITRIP | R/W  | 0b    | ITRIP level configuration - refer <a href="#">ITRIP table</a> |

### 8.1.9 CONFIG3 Register (Address = 0Ch) [reset = 40h]

Return to the [User Register table](#).

| Bit | Field | Type | Reset | Description   |
|-----|-------|------|-------|---|
| 7-6 | TOFF  | R/W  | 1b    | TOFF time used for ITRIP current regulation<br>00b = 20µsec<br>01b = 30µsec<br>10b = 40µsec<br>11b = 50µsec |
| 5   | N/A   | R    | 0b    | Not available   |
| 4-2 | S_SR  | R/W  | 0b    | Slew Rate configuration - refer to <a href="#">Section 7.3.3.1</a>  |
| 1-0 | SPARE | R/W  | 0b    | Don't care  |

### 8.1.10 CONFIG4 Register (Address = 0Dh) [reset = 04h]

Return to the [User Register table](#).

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7-6 | TOCP_SEL | R/W  | 0b    | Filter time for over current detection configuration<br>00b = 6µsec<br>01b = 3µsec<br>10b = 1.5µsec<br>11b = Minimum (~0.2µsec) |
| 5   | N/A      | R    | 0b    | Not available   |

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 4-3 | OCP_SEL    | R/W  | 0b    | Threshold for over current detection configuration<br>00b = 100% setting<br>01b, 11b = 50% setting<br>10b = 75% setting |
| 2   | DRVOFF_SEL | R/W  | 1b    | DRVOFF <a href="#">pin - register logic combination</a> , when SPI_IN is unlocked<br>0b = OR<br>1b = AND                |
| 1   | SPARE      | R/W  | 0b    | Don't care  |
| 0   | IN_SEL     | R/W  | 0b    | IN <a href="#">pin - register logic combination</a> , when SPI_IN is unlocked<br>0b = OR<br>1b = AND                    |

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The DRV814x-Q1 family of devices can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver and dual unidirectional current control applications requiring two half-bridge drivers.

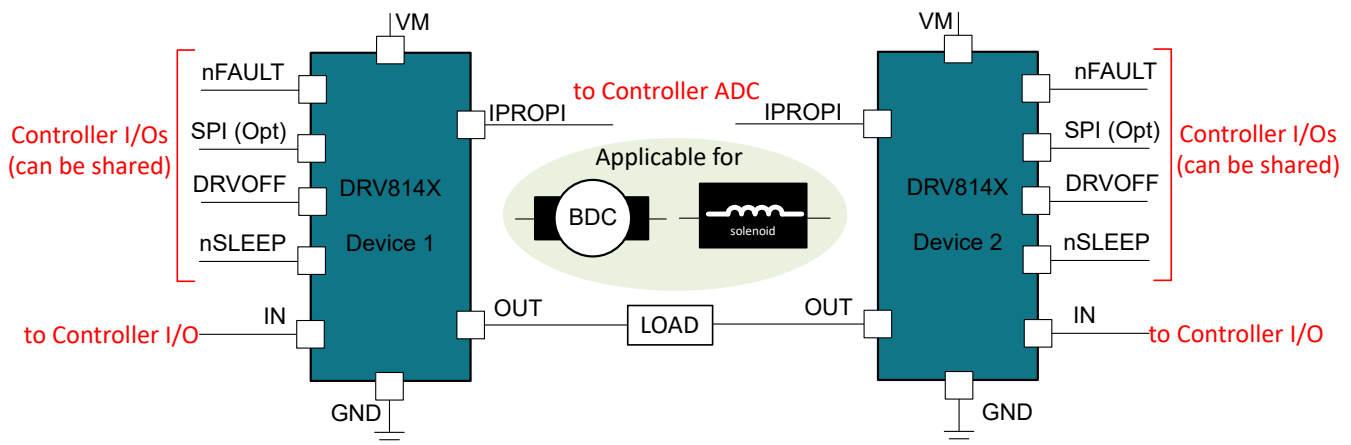
#### 9.1.1 Load Summary

summarizes the utility of the device features for different type of inductive loads.

**Table 9-1. Load Summary Table**

| LOAD   | Configuration                |                    |                   | Device Feature                        |                           |
|--|------------------------------|--------------------|-------------------|---------------------------------------|---------------------------|
|  | Device                       | Recirculation Path | Slew Rate control | Current sense                         | ITRIP regulation          |
| Bi-directional motor or solenoid <sup>(1)</sup>                        | Full-Bridge with two DRV814x | High-side          | Full range        | Continuous                            | Not useful <sup>(3)</sup> |
| Bi-directional motor or solenoid <sup>(1)</sup>                        | Full-Bridge with two DRV814x | Low-side           | Full range        | Discontinuous <sup>(2)</sup>          | Useful                    |
| Uni-directional motor or Low-side solenoid (one side connected to GND) | DRV814x                      | Low-side           | Full range        | Discontinuous <sup>(2)</sup>          | Useful                    |
| High-side solenoid (one side connected to VM)                          | DRV814x                      | High-side          | Full range        | Not available, need external solution |                           |

- (1) Solenoid - clamping or quick demagnetization possible, but clamping level will be VM dependent
- (2) Not sensed during recirculation and during OUT voltage slew times including  $t_{blank}$
- (3) SPI variant - Controller can poll ITRIP\_CMP bit for external coordination between the two Half-Bridges



**Figure 9-1. Illustration Showing a Full-Bridge Topology With Two DRV814X-Q1 Devices**

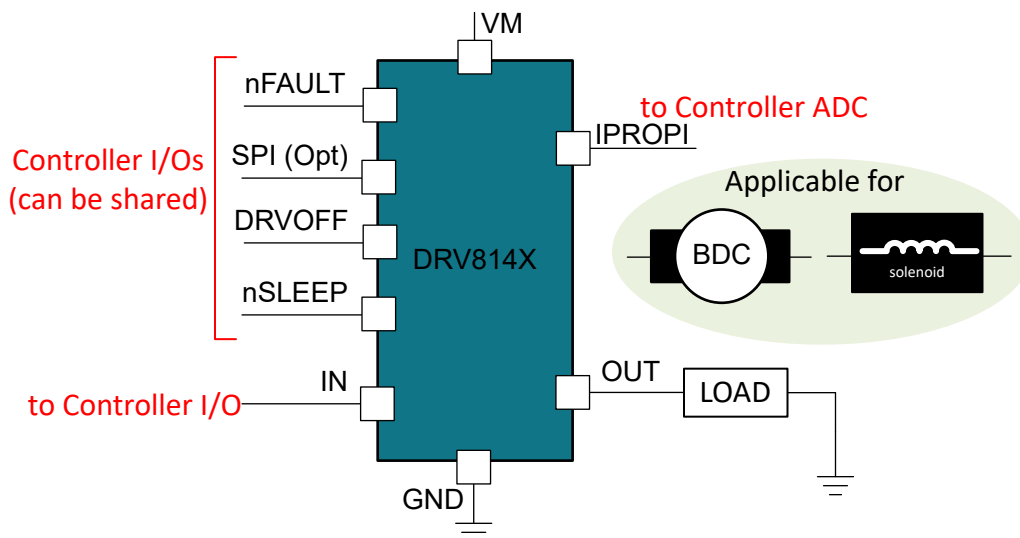


Figure 9-2. Illustration Showing a Half-Bridge Topology to Drive Low-side Load With DRV814X-Q1 Device

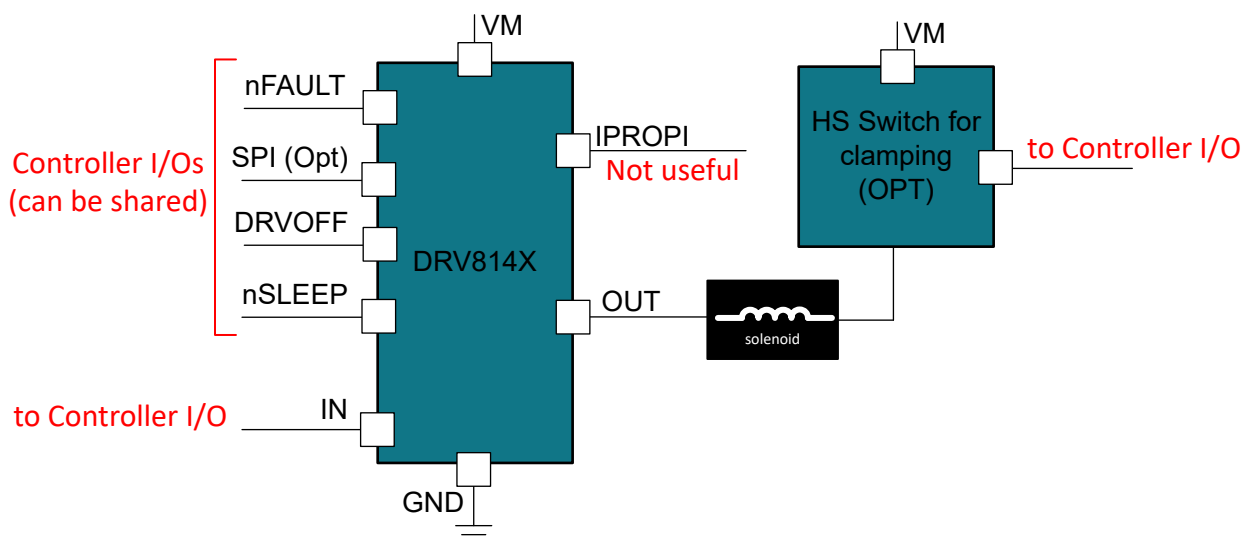


Figure 9-3. Illustration showing a Half-Bridge topology to drive high-side load with DRV814X-Q1 device

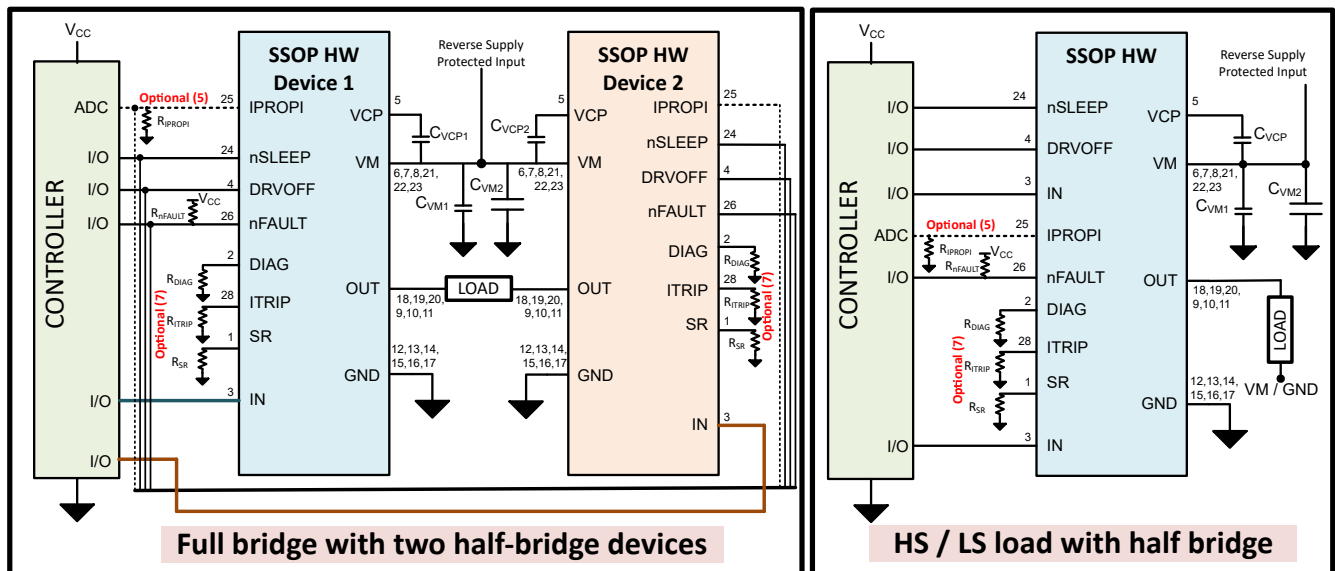
## 9.2 Typical Application

The figures below show the typical application schematic for driving a brushed DC motor or any inductive load. There are several optional connections shown in these schematics, which are listed as follows:

- nSLEEP pin
  - SPI (S) variant - This pin can be tied off high in the application if SLEEP function is not needed.
  - SPI (P) variant - N/A
  - HW (H) variant - Pin control is **mandatory** even if SLEEP function is not needed. The controller needs to issue a reset pulse (typical: 30µsec bounded between  $t_{reset\ max}$  and  $t_{sleep\ min}$ ) during wake-up to acknowledge wake-up or power-up.
- DRVOFF pin
  - Both SPI (P) and SPI (S) variants - This pin can be tied off low in the application if shutoff through **pin** function is not needed. The equivalent register bit can be used.
- IN pin

- Both SPI (P) and SPI (S) variants - This pin can be tied off low or left floating if register only control is needed.
- NC pin
  - All variants - This pin can be left floating or tied off low.
- OUT pin
  - Recommend to add a PCB footprint for capacitor from OUT to GND close to the load for EMC purposes.
- IPROPI pin
  - All variants - Monitoring of this output is optional. Also IPROPI pin can be tied low if ITRIP feature & IPROPI function is not needed. Recommend to add a PCB footprint for a small capacitor (10nF to 100nF) if needed.
- nFAULT pin
  - Both SPI (P) and SPI (S) variants - Monitoring of this output is optional. All diagnostic information can be read from the STATUS registers.
- SPI input pins
  - Both SPI (P) and SPI (S) variants - Inputs (SDI, nSCS, SCLK) are compatible with 3.3V / 5V levels.
- SPI SDO pin
  - SPI (S) variant - SDO tracks the nSLEEP pin voltage.
  - SPI (P) variant - SDO tracks the VDD pin voltage. To interface with a 3.3V level controller input, a level shifter or a current limiting series resistor is recommended.
- CONFIG pins
  - HW (H) variant - Resistor is not needed for short to GND and Hi-Z level selections
    - LVL1 and LVL6 for SR, ITRIP, DIAG pins

**9.2.1 HW Variant**



**Figure 9-4. Typical Application schematic - HW variant in HVSSOP Package**

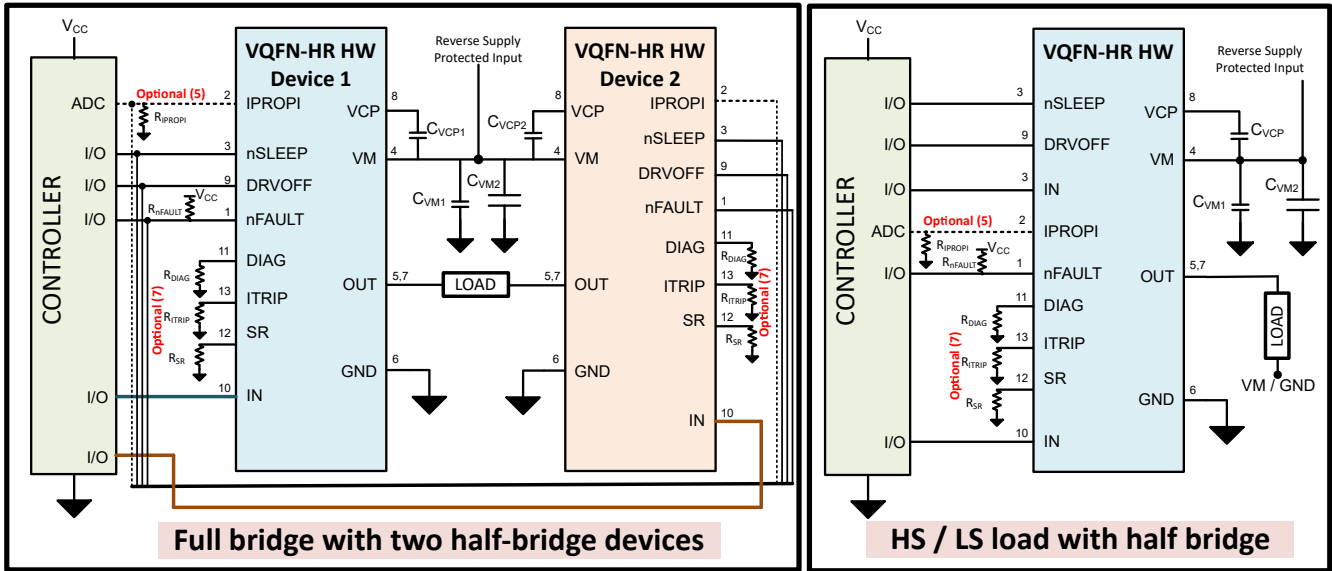


Figure 9-5. Typical Application Schematic - HW Variant in VQFN-HR Package

9.2.2 SPI Variant

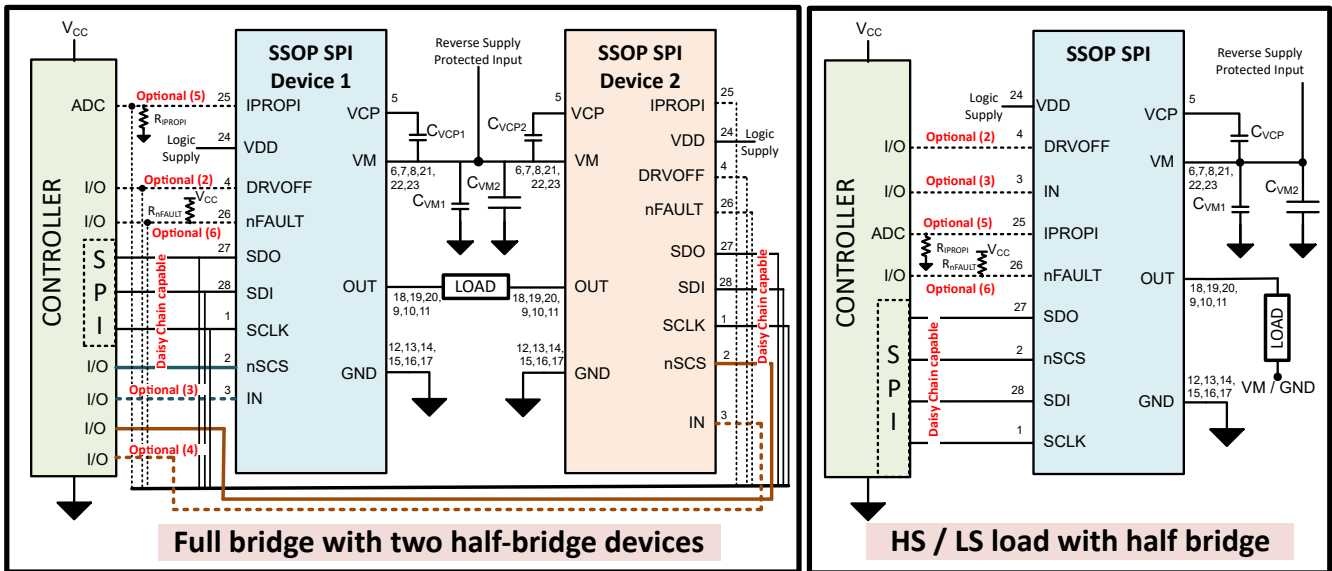


Figure 9-6. Typical Application Schematic - SPI (P) Variant in HVSSOP Package



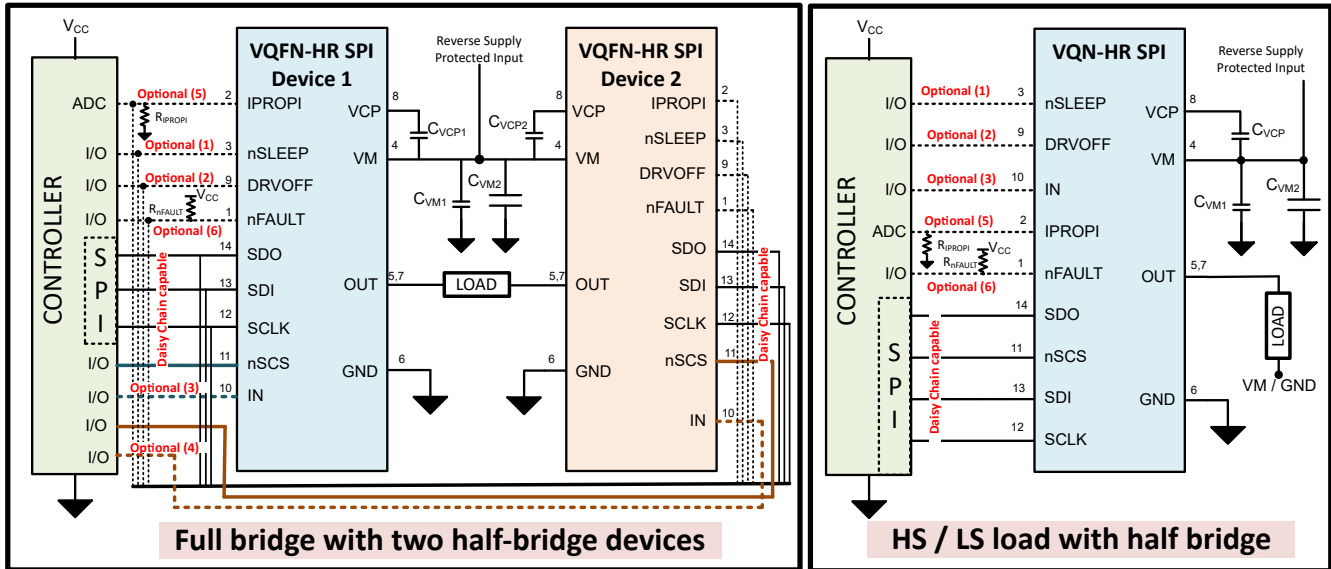


Figure 9-7. Typical Application Schematic - SPI (S) Variant in VQFN-HR Package

### 9.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply (VM) range from 4.5V to 40V. A 0.1- $\mu$ F ceramic capacitor rated for VM must be placed as close to the device as possible. Also, an appropriately sized bulk capacitor must be placed on the VM pin.

#### 9.3.1 Bulk Capacitance Sizing

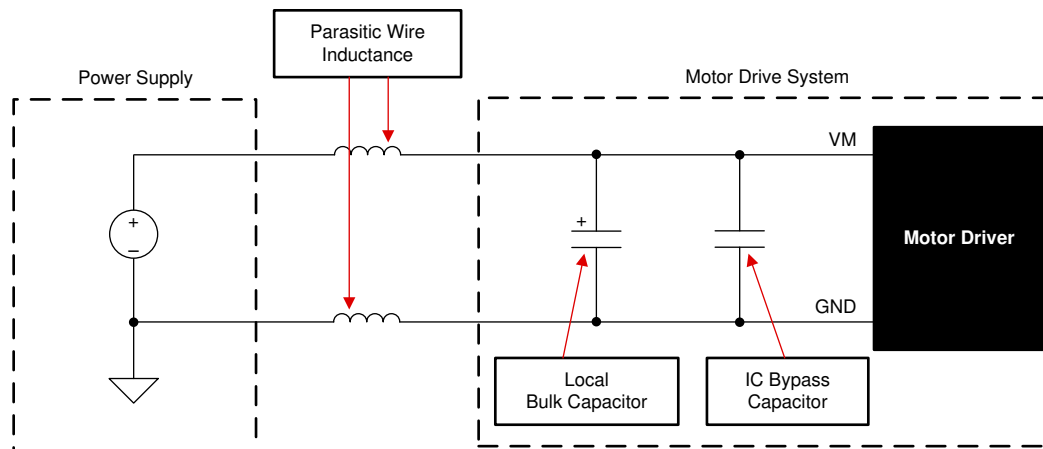
Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.



**Figure 9-8. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

## 9.4 Layout

### 9.4.1 Layout Guidelines

Each VM pin must be bypassed to ground using low-ESR ceramic bypass capacitors with recommended values of 0.1 $\mu$ F rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1 $\mu$ F, rated for 6.3V, and be of type X5R or X7R.

For the SPI (P) device variant, VDD pin may be bypassed to ground using low-ESR ceramic 6.3V bypass capacitor with recommended values of 0.1 $\mu$ F.

### 9.4.2 Layout Example

The following figure shows a layout example for a 4cm X 4cm x 1.6mm, 4 layer PCB for a leaded package device. The 4 layers uses 2oz copper on top/ bottom signal layers and 1oz copper on internal supply layers, with 0.3mm thermal via drill diameter, 0.025mm Cu plating, 1mm minimum via pitch. The same layout can be adopted for the non-leaded VQFN-HR package as well. The [Section 6.5.14](#) for the 4cm X 4cm X 1.6mm is based on a similar layout.

Note: The layout example shown is for a full-bridge topology using DRV814xQ1 device in VQFN-HR package.

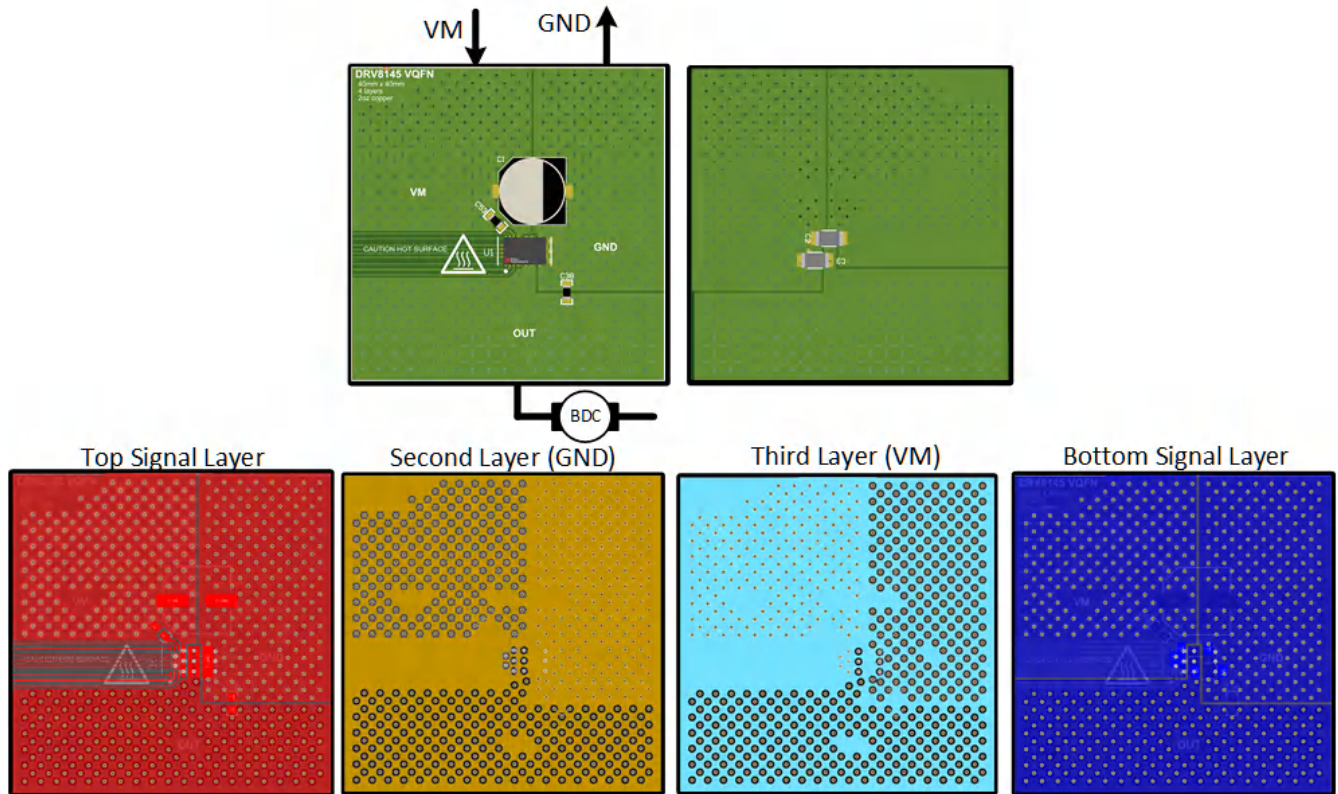


Figure 9-9. Layout example: 4cm x 4 cm x 1.6mm, 4 layer PCB

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Half Bridge Driver Junction Temperature Estimator \(Excel-based worksheet\)](#)
- Texas Instruments, [Calculating Motor Driver Power Dissipation](#) application report
- Texas Instruments, [Current Recirculation and Decay Modes](#) application report
- Texas Instruments, [PowerPAD™ Made Easy](#) application report
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package](#) application report
- Texas Instruments, [Understanding Motor Driver Current Ratings](#) application report
- Texas Instruments, [Best Practices for Board Layout of Motor Drivers](#) application report

#### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.3 Community Resources

#### 10.4 Trademarks

All trademarks are the property of their respective owners.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

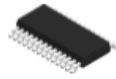
| Changes from Revision * (January 2023) to Revision A (March 2024) | Page |
|---|------|
| • Added HVSSOP device package option for DRV8143H.....            | 3    |
| • Added HVSSOP package option for HW variant.....                 | 55   |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and order-able information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

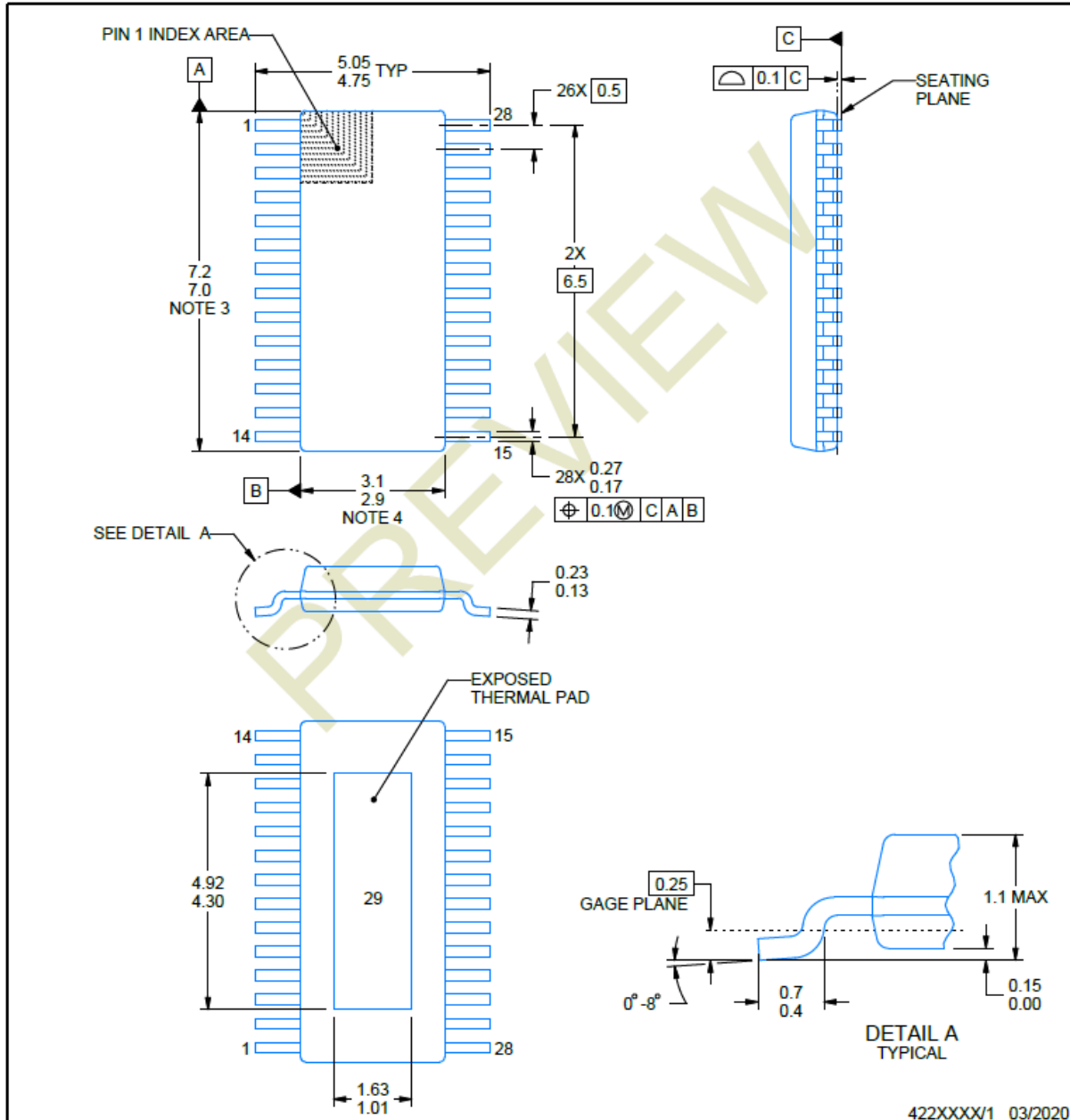
## PACKAGE OUTLINE

**DGQ0028A**



**PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



422XXXX/1 03/2020

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

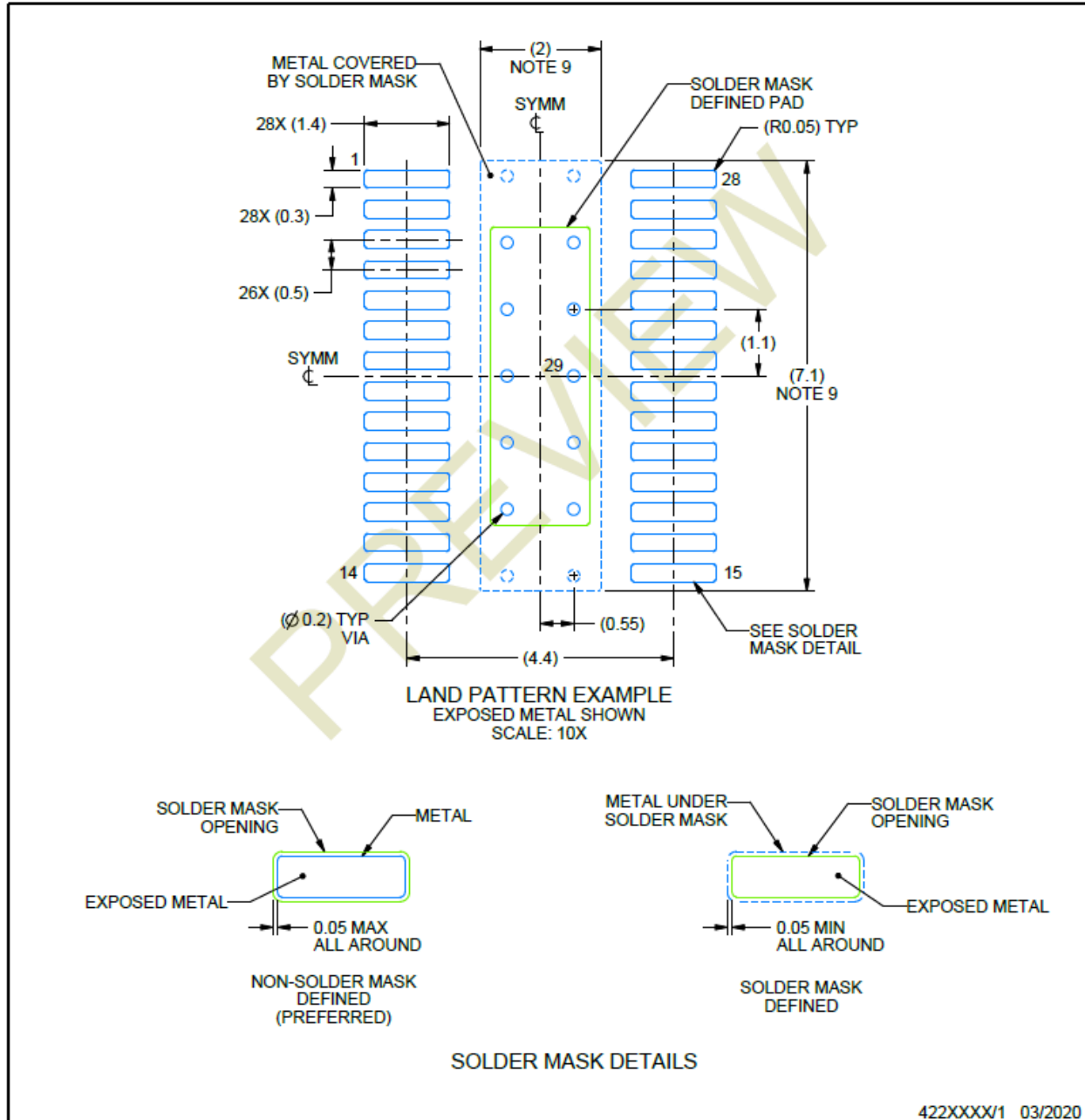
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. No JEDEC registration as of March 2020.

## EXAMPLE BOARD LAYOUT

**DGQ0028A**

**PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

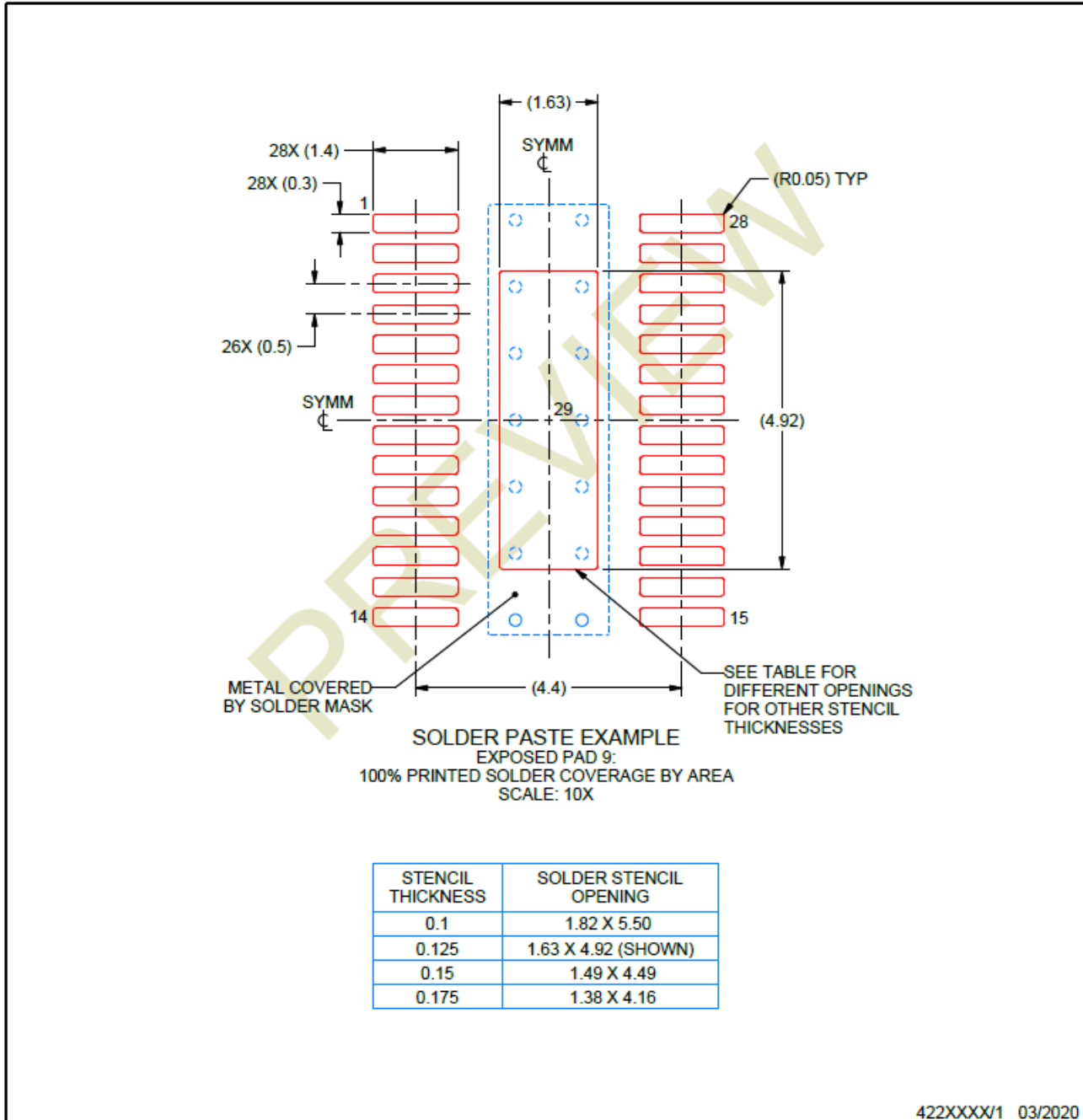
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

## EXAMPLE STENCIL DESIGN

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

Figure 12-1. DGQ28A: HVSSOP(28) Package Drawing



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV8143HQDGQRQ1  | ACTIVE        | HVSSOP       | DGQ             | 28   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | 8143H                   | <a href="#">Samples</a> |
| DRV8143HQRXYRQ1  | ACTIVE        | VQFN-HR      | RXY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | DRV8143H                | <a href="#">Samples</a> |
| DRV8143PQDGQRQ1  | ACTIVE        | HVSSOP       | DGQ             | 28   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | 8143P                   | <a href="#">Samples</a> |
| DRV8143SQRXYRQ1  | ACTIVE        | VQFN-HR      | RXY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | DRV8143S                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8143HQDQGRQ1 | HVSSOP       | DGQ             | 28   | 2500 | 330.0              | 16.4               | 5.5     | 7.4     | 1.45    | 8.0     | 16.0   | Q1            |
| DRV8143HQRXYRQ1 | VQFN-HR      | RXY             | 14   | 3000 | 330.0              | 12.4               | 3.3     | 4.8     | 1.2     | 8.0     | 12.0   | Q1            |
| DRV8143SQRXYRQ1 | VQFN-HR      | RXY             | 14   | 3000 | 330.0              | 12.4               | 3.3     | 4.8     | 1.2     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV8143HQDGQRQ1 | HVSSOP       | DGQ             | 28   | 2500 | 356.0       | 356.0      | 35.0        |
| DRV8143HQRXYRQ1 | VQFN-HR      | RXY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |
| DRV8143SQRXYRQ1 | VQFN-HR      | RXY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

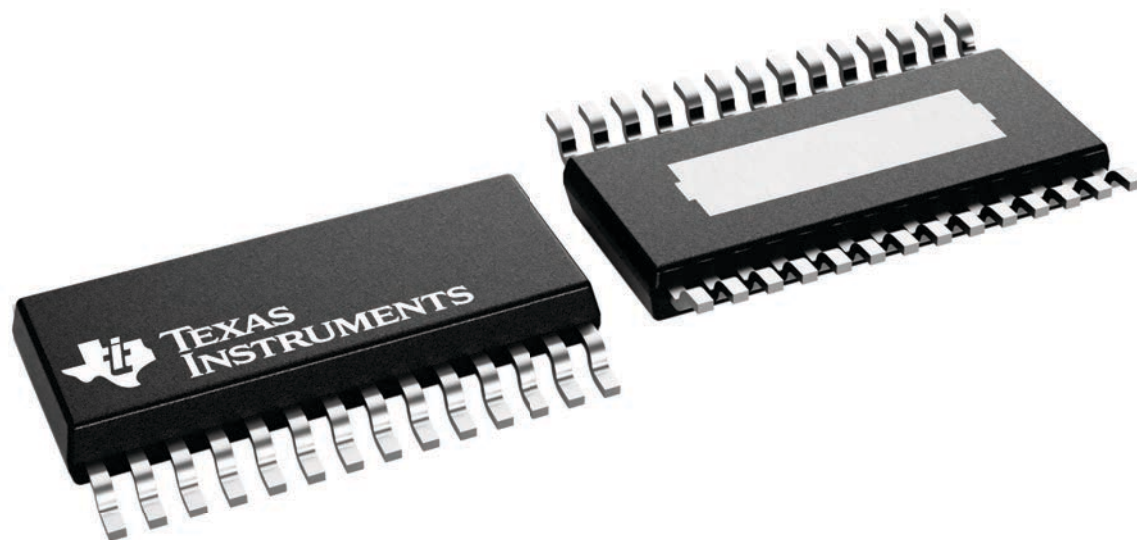
**DGQ 28**

**HVSSOP - 1.1 mm max height**

3 x 7.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226530/A

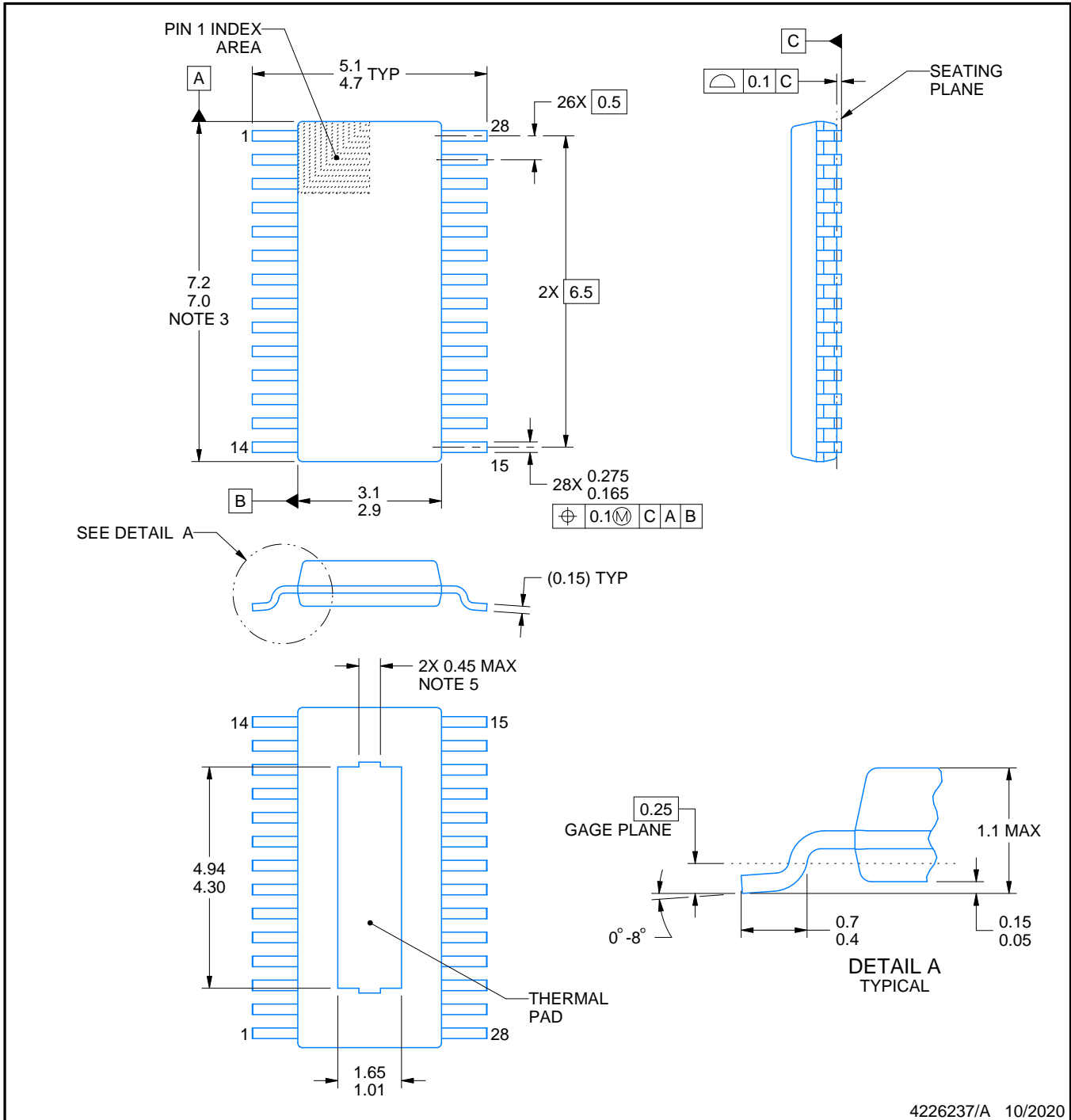
# DGQ0028A



# PACKAGE OUTLINE

## PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226237/A 10/2020

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

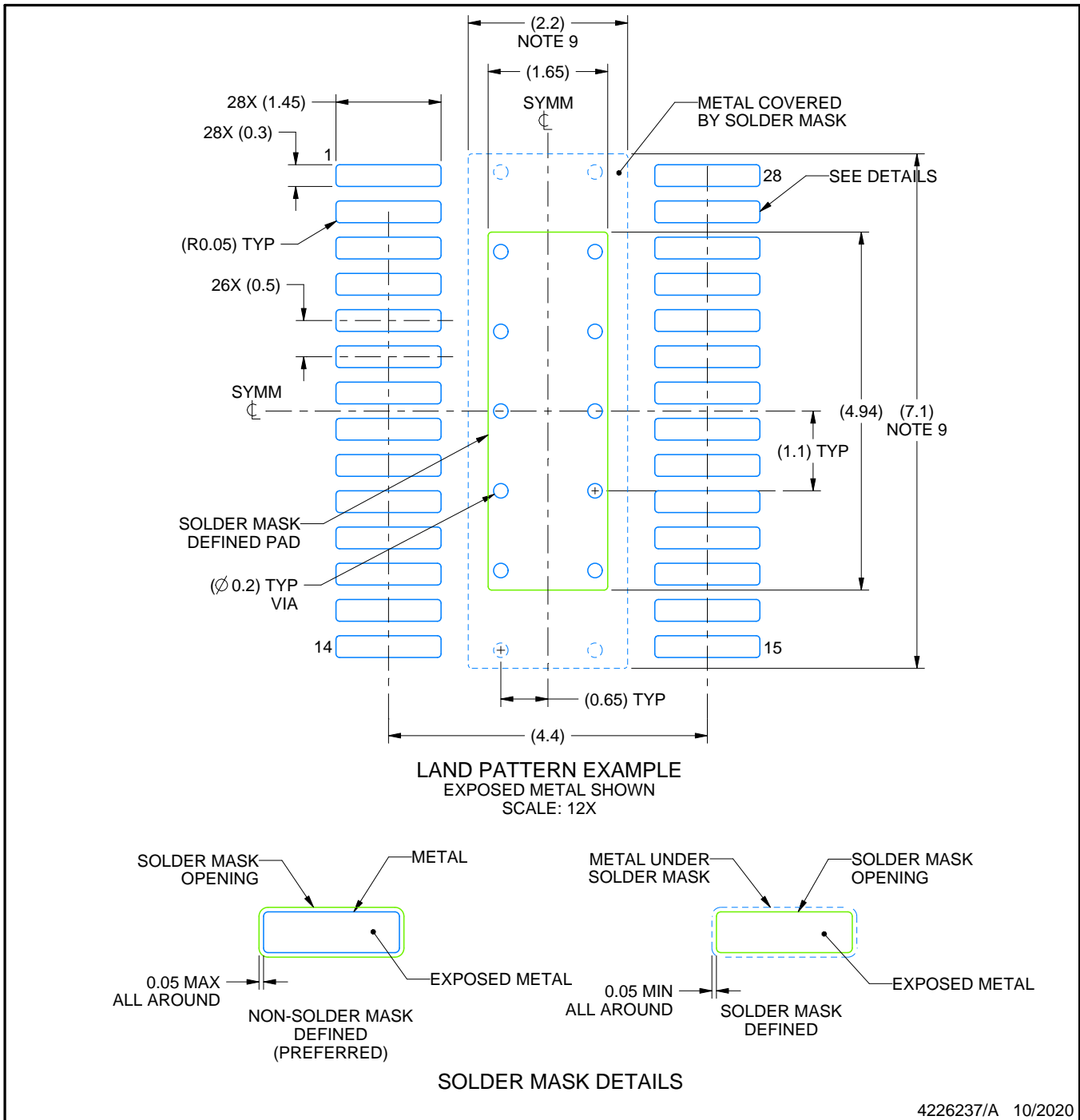
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

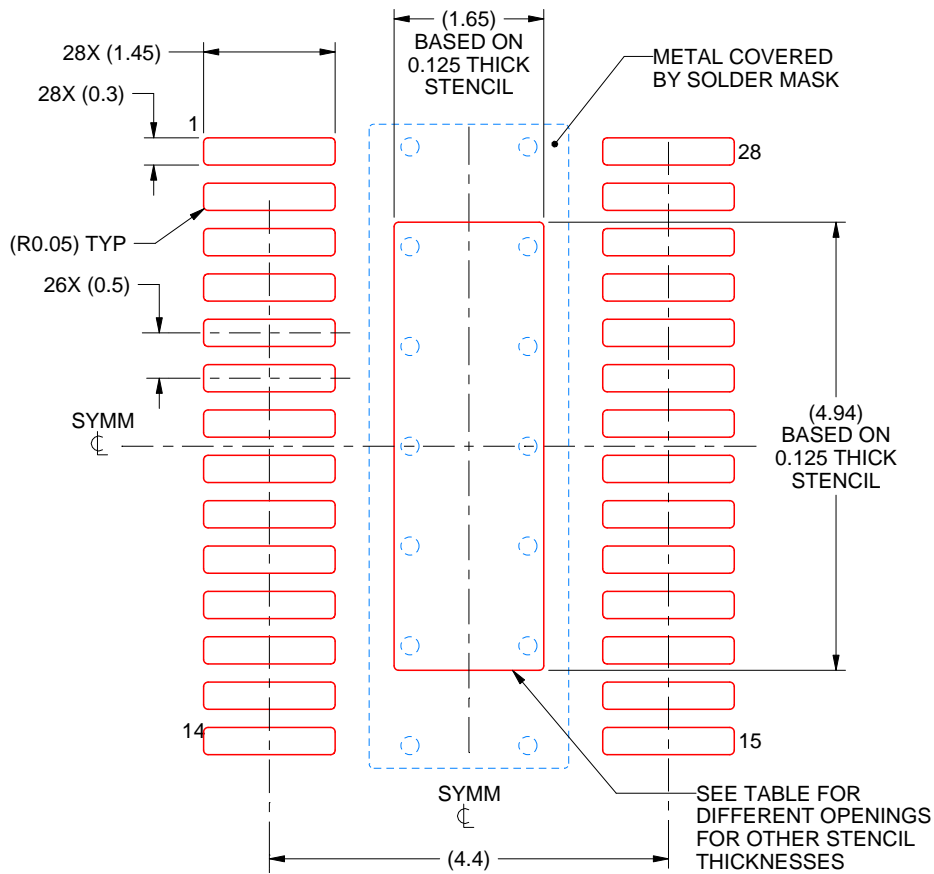
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



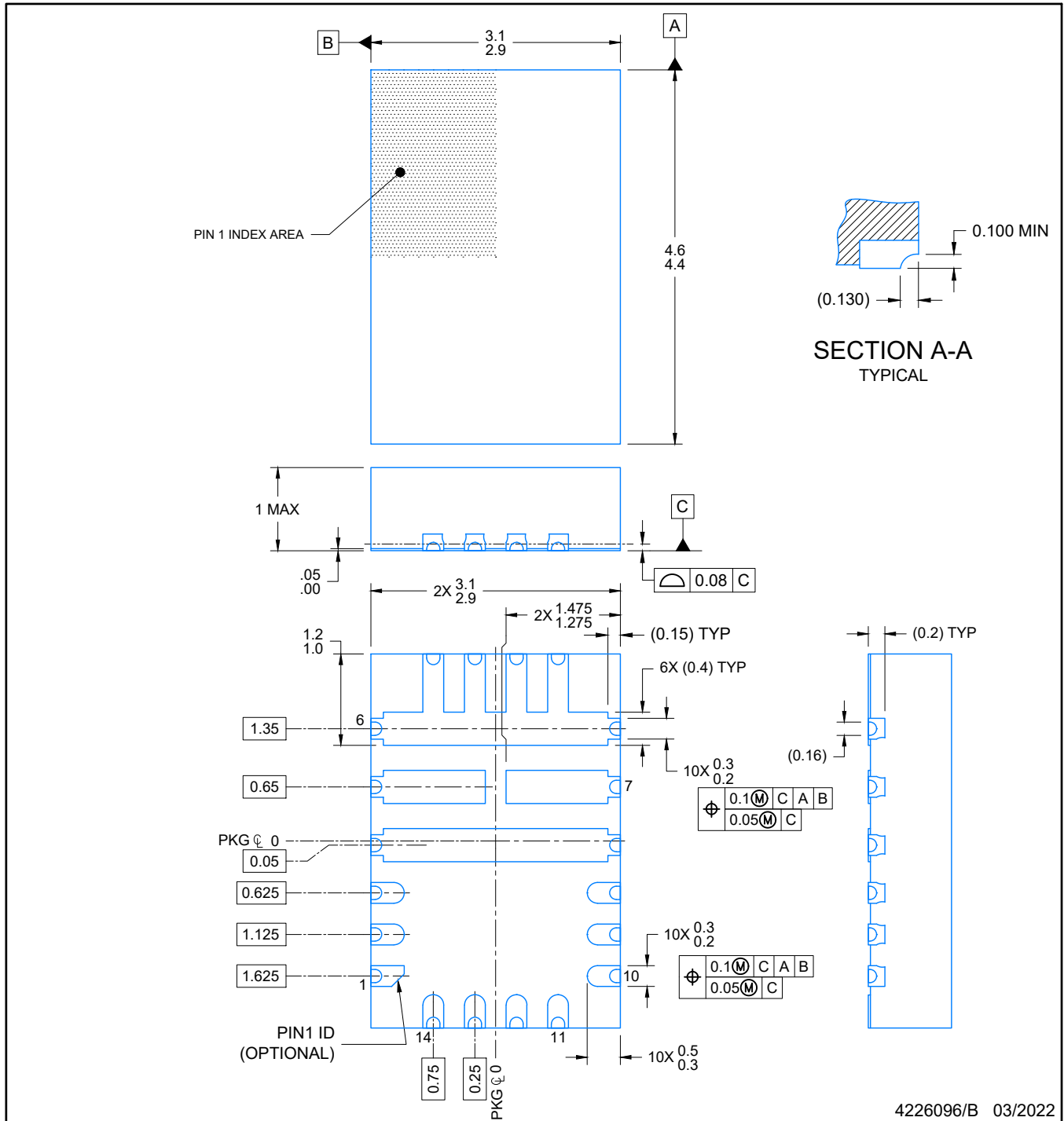
**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 12X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 1.84 X 5.52            |
| 0.125             | 1.65 X 4.94 (SHOWN)    |
| 0.15              | 1.51 X 4.51            |
| 0.175             | 1.39 X 4.18            |

4226237/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

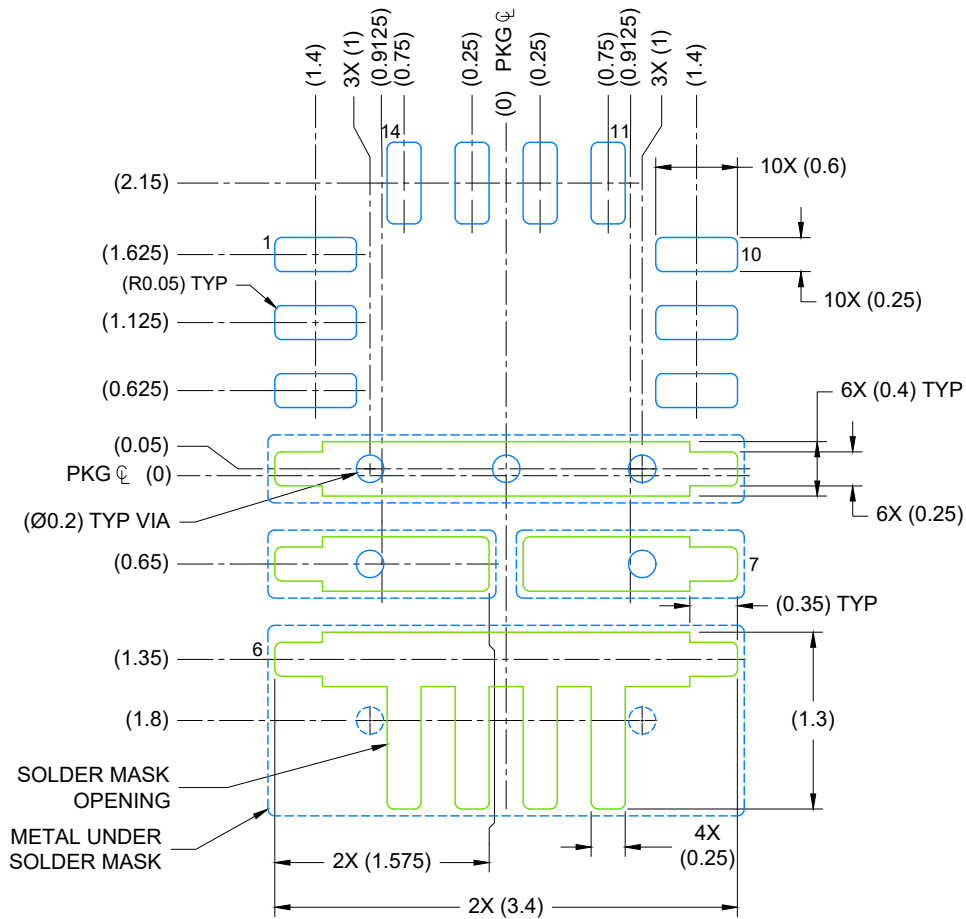


4226096/B 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

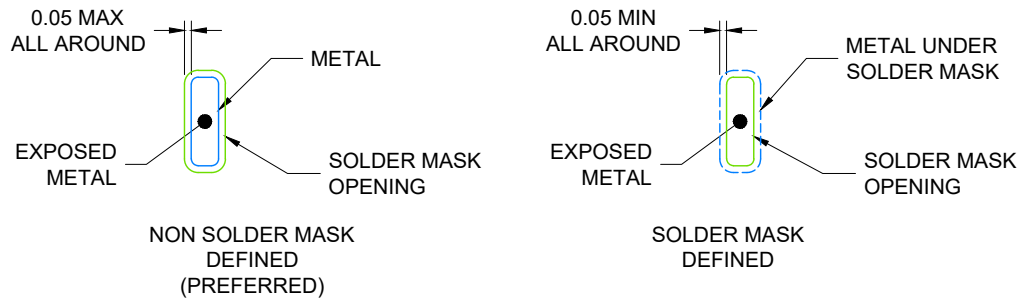




LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



SOLDER MASK DETAILS

4226096/B 03/2022

NOTES: (continued)

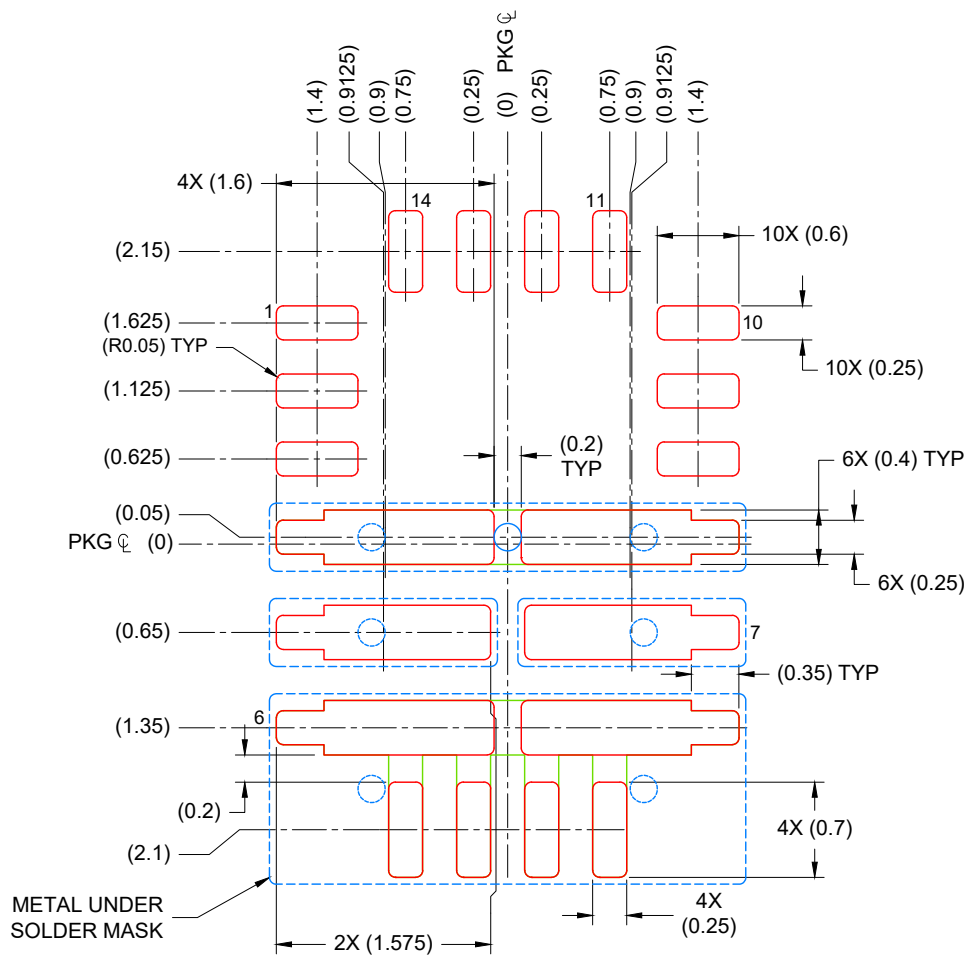
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN-HR - 1 mm max height

RXY0014A

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL  
 SCALE: 18X

4226096/B 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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