DS90UB949A-Q1 2K HDMI-to-FPD-Link III Bridge Serializer

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 2: –40°C to 105°C, T_A
- Supports TMDS clock frequencies up to 210 MHz for 3K (2880x1620) at 30Hz, QXGA (2048x1536), 2K (2880x1080), WUXGA (1920x1200), or 1080p60 with 24-bit color depth
- Single and dual FPD-Link III outputs, supports STP or STQ or coax cables
- High-definition multimedia (HDMI) v1.4b compatible inputs
- HDMI-Mode DisplayPort (DP++) inputs
- HDMI audio extraction for up to 8 channels
- High-speed back channel supporting GPIO up to 2 Mbps
- Tracks spread spectrum input clock to reduce EMI
- I2C (master/slave) with 1-Mbps fast-mode plus
- SPI pass-through interface
- Backward compatible with DS90UB926Q-Q1, DS90UB928Q-Q1, and DS90UB924-Q1 FPD-Link III deserializers

2 Applications

- Automotive Infotainment & cluster
  - Automotive head unit
  - Automotive rear seat entertainment display
  - Automotive center information display
  - Commercial vehicle instrument cluster
  - Automotive media hub
- Audio/video control system

3 Description

The DS90UB949A-Q1 is an HDMI-to-FPD-Link III bridge device which, when paired with the FPD-Link III DS90UB940-Q1/DS90UB948-Q1 deserializers, supplies 1-lane or 2-lane high-speed serial streams over cost-effective, 50-Ω single-ended coaxial, or 100-Ω differential shielded twisted-pair (STP) and shielded twisted quad (STQ) cables. The device can serialize an HDMI v1.4b input to support video resolutions up to 2880x1080 at 60 Hz with 24-bit color depth.

The FPD-Link III interface supports both video and audio data transmissions, and full duplex control—including I2C and SPI communication—over the same differential link. Video data consolidation and control over two differential pairs can help decrease the interconnect size, decrease the weight of the application, and simplify system design. EMI is minimized by the use of low-voltage differential signaling, data scrambling, and randomization. In backward-compatible mode, the DS90UB949A-Q1 supports up to 1920x720 resolution with 24-bit color depth over a single differential link when the device is paired with the DS90Ux92x-Q1 deserializers.

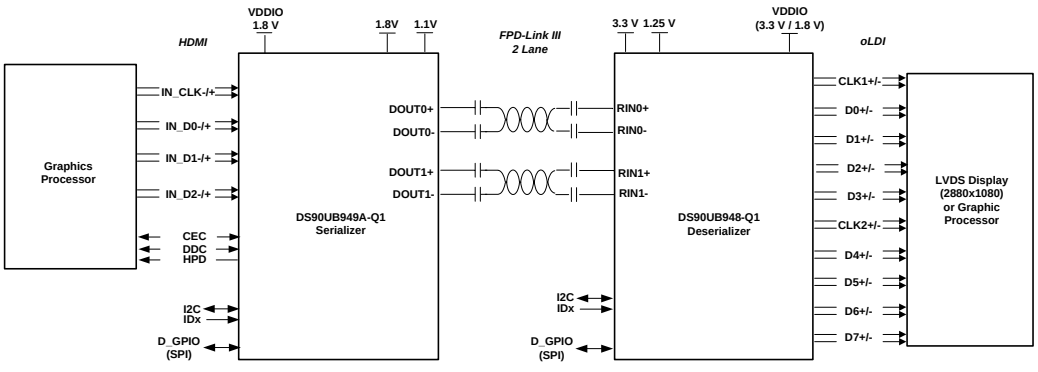
The DS90UB949A-Q1 supports multi-channel audio received through an external I2S interface. The device also has an optional auxiliary audio interface.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB949A-Q1	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Applications Diagram



HDMI – High Definition Multimedia Interface

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2019	*	Initial release

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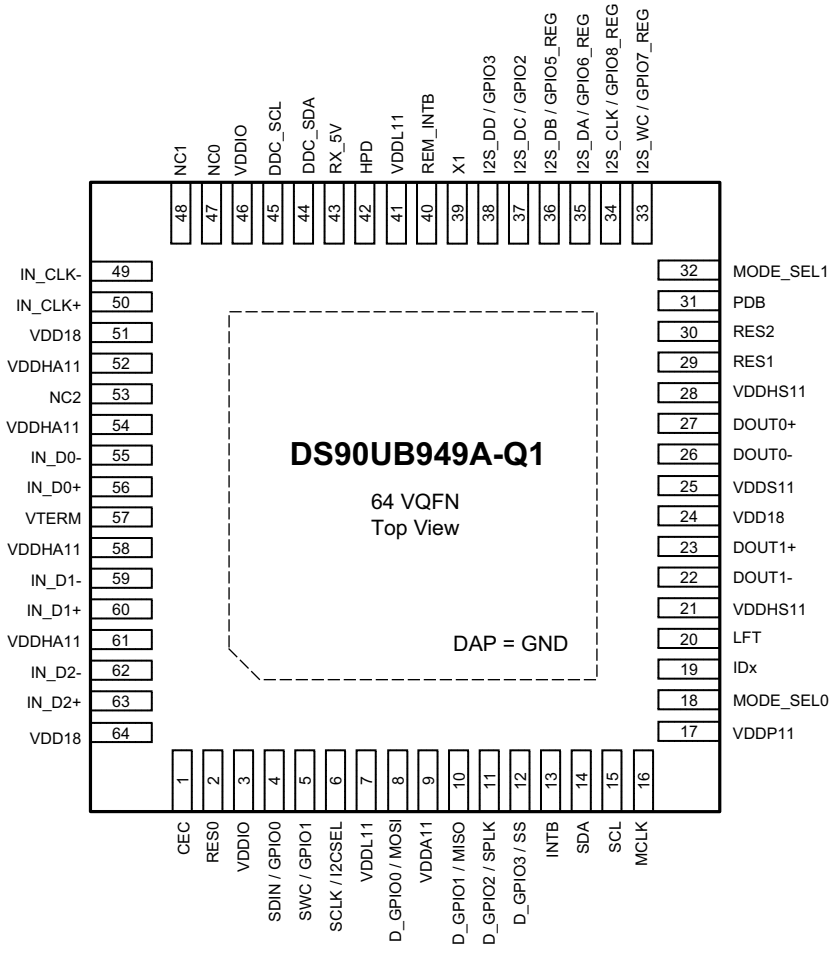
5 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
HDMI TMDS INPUT			
IN_CLK– IN_CLK+	49 50	I, TMDS	TMDS Clock Differential Input
IN_D0– IN_D0+	55 56	I, TMDS	TMDS Data Channel 0 Differential Input
IN_D1– IN_D1+	59 60	I, TMDS	TMDS Data Channel 1 Differential Input
IN_D2– IN_D2+	62 63	I, TMDS	TMDS Data Channel 2 Differential Input
OTHER HDMI			
CEC	1	IO, Open-Drain	Consumer Electronic Control Channel Input/Output Interface. Pullup with a 27-kΩ resistor to 3.3 V
DDC_SDA	44	IO, Open-Drain	DDC Slave Serial Data Pull up to RX_5V with a 47-kΩ resistor
DDC_SCL	45	I, Open-Drain	DDC Slave Serial Clock Pull up to RX_5V with a 47-kΩ resistor

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
HPD	42	O, Open-Drain	Hot Plug Detect Output. Pull up to RX_5V with a 1-kΩ resistor
RX_5V	43	I	HDMI 5-V Detect Input
X1	39	I, LVCMOS	Optional Oscillator Input: This pin is the optional reference clock for CEC. It must be connected to a 25 MHz 0.1% (1000ppm), 45-55% duty cycle clock source at CMOS-level 1.8 V. Leave it open if unused.
FPD-LINK III SERIAL			
DOUT0–	26	O	FPD-Link III Inverting Output 0 The output must be AC-coupled with a 0.1-µF capacitor for interfacing with DS90Ux92x-Q1 deserializers and 0.1-µF or 33-nF capacitor for 94x deserializers
DOUT0+	27	O	FPD-Link III True Output 0 The output must be AC-coupled with a 0.1-µF capacitor for interfacing with DS90Ux92x-Q1 deserializers and 0.1-µF or 33-nF capacitor for 94x deserializers
DOUT1–	22	O	FPD-Link III Inverting Output 1 The output must be AC-coupled with a 0.1-µF capacitor for interfacing with DS90Ux92x-Q1 deserializers and 0.1-µF or 33-nF capacitor for 94x deserializers
DOUT1+	23	O	FPD-Link III True Output 1 The output must be AC-coupled with a 0.1-µF capacitor for interfacing with DS90Ux92x-Q1 deserializers and 0.1-µF or 33-nF capacitor for 94x deserializers
LFT	20	Analog	FPD-Link III Loop Filter Connect with a 10-nF capacitor to GND.
CONTROL			
I2CSEL	6	I, LVCMOS	I2C Voltage Level Strap Option Tie to V_{DDIO} with a 10-kΩ resistor for 1.8-V I2C operation. Leave floating for 3.3-V I2C operation. This pin is read as an input at power up. Issuing either of the digital resets via register 0x01 will cause the I2C_VSEL value to be reset to 3.3-V operation.
IDx	19	Analog	I2C Serial Control Bus Device ID Address Select
INTB	13	O, Open-Drain	Open-Drain. Remote interrupt. Active LOW. Pull up to VDDIO with a 4.7-kΩ resistor.
MODE_SEL0	18	Analog	Mode Select 0. See Table 6.
MODE_SEL1	32	Analog	Mode Select 1. See Table 6.
PDB	31	I, LVCMOS	Power-Down Mode Input Pin
REM_INTB	40	O, Open-Drain	Remote interrupt. Mirrors status of INTB_IN from the deserializer. Note: External pullup to 1.8 V required. Recommended pullup: 4.7 kΩ. INTB = H, Normal Operation INTB = L, Interrupt Request
SCL	15	IO, Open-Drain	I2C Clock Input / Output Interface Open-drain. Must have an external pullup resistor to 1.8 V or 3.3 V. See I2CSEL pin. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
SDA	14	IO, Open-Drain	I2C Data Input / Output Interface Open-drain. Must have an external pullup to resistor to 1.8 V or 3.3 V. See I2CSEL pin. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
SPI PINS (DUAL LINK MODE ONLY)			
MOSI	8	IO, LVCMOS	SPI Master Out Slave In. Shared with D_GPIO0
MISO	10	IO, LVCMOS	SPI Master In Slave Out. Shared with D_GPIO1
SPLK	11	IO, LVCMOS	SPI Clock. Shared with D_GPIO2
SS	12	IO, LVCMOS	SPI Slave Select. Shared with D_GPIO3
HIGH-SPEED (HS) BIDIRECTIONAL CONTROL CHANNEL GPIO PINS (DUAL LINK MODE ONLY)			
D_GPIO0	8	IO, LVCMOS	HS GPIO0. Shared with MOSI
D_GPIO1	10	IO, LVCMOS	HS GPIO1. Shared with MISO
D_GPIO2	11	IO, LVCMOS	HS GPIO2. Shared with SPLK

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
D_GPIO3	12	IO, LVCMOS	HS GPIO3. Shared with SS
BIDIRECTIONAL CONTROL CHANNEL (BCC) GPIO PINS			
GPIO0	4	IO, LVCMOS	BCC GPIO0. Shared with SDIN
GPIO1	5	IO, LVCMOS	BCC GPIO1. Shared with SWC
GPIO2	37	IO, LVCMOS	BCC GPIO2. Shared with I2S_DC
GPIO3	38	IO, LVCMOS	BCC GPIO3. Shared with I2S_DD
REGISTER-ONLY GPIO			
GPIO5_REG	36	IO, LVCMOS	General-Purpose Input/Output 5 Local register control only. Shared with I2S_DB
GPIO6_REG	35	IO, LVCMOS	General-Purpose Input/Output 6 Local register control only. Shared with I2S_DA
GPIO7_REG	33	IO, LVCMOS	General-Purpose Input/Output 7 Local register control only. Shared with I2S_WC
GPIO8_REG	34	IO, LVCMOS	General-Purpose Input/Output 8 Local register control only. Shared with I2S_CLK
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_CLK	34	I, LVCMOS	Slave Mode I2S Clock Input. Shared with GPIO8_REG
I2S_DA	35	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO6_REG
I2S_DB	36	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO5_REG
I2S_DC	37	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO2
I2S_DD	38	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO3
I2S_WC	33	I, LVCMOS	Slave Mode I2S Word Clock Input. Shared with GPIO7_REG
AUXILIARY I2S CHANNEL PINS			
MCLK	16	IO, LVCMOS	Master Mode I2S System Clock Input/Output
SCLK	6	O, LVCMOS	Master Mode I2S Clock Ouput. Shared with I2CSEL. This pin is sampled following power-up as I2CSEL, then it will switch to SCLK operation as an output.
SDIN	4	I, LVCMOS	Master Mode I2S Data Input. Shared with GPIO0
SWC	5	O, LVCMOS	Master Mode I2S Word Clock Ouput. Shared with GPIO1
POWER AND GROUND			
GND	Thermal Pad	GND	Ground. Connect to Ground plane with at least 9 vias.
VDD18	24 51 64	Power	1.8-V (±5%) Analog supply. Refer to Figure 25 or Figure 26.
VDDA11	9	Power	1.1-V (±5%) Analog supply. Refer to Figure 25 or Figure 26.
VDDHA11	52 54 58 61	Power	1.1-V (±5%) TMDS supply. Refer to Figure 25 or Figure 26.
VDDHS11	21 28	Power	1.1-V (±5%) supply. Refer to Figure 25 or Figure 26.
VDDIO	3 46	Power	1.8-V (±5%) IO supply. Refer to Figure 25 or Figure 26.
VDDL11	7 41	Power	1.1-V (±5%) Digital supply. Refer to Figure 25 or Figure 26.
VDDP11	17	Power	1.1-V (±5%) PLL supply. Refer to Figure 25 or Figure 26.
VDDS11	25	Power	1.1-V (±5%) Serializer supply. Refer to Figure 25 or Figure 26.
VTERM	57	Power	3.3-V (±5%) Supply for DC-coupled internal termination OR 1.8-V (±5%) Supply for AC-coupled internal termination Refer to Figure 25 or Figure 26.
OTHER			

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
NC0 NC1 NC2	47 48 53	—	No connect. Leave floating. Do not connect to VDD or GND.
RES0 RES1	2 29	—	Reserved. Tie to GND.
RES2	30	—	Reserved. Connect with 50 Ω to GND.

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{DD11}	Supply voltage	–0.3	1.7	V
V_{DD18}	Supply voltage	–0.3	2.5	V
V_{DDIO}	Supply voltage	–0.3	2.5	V
	OpenLDI inputs	–0.3	2.75	V
	LVCMOS I/O voltage	–0.3	V_{DDIO} + 0.3	V
	1.8-V tolerant I/O	–0.3	2.5	V
	3.3-V tolerant I/O	–0.3	4	V
	5-V tolerant I/O	–0.3	5.3	V
	FPD-Link III output voltage	−0.3	1.7	V
	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5		±750	
		(IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pins 22, 23, 26, and 27)	±15000	
			Contact Discharge (Pins 22, 23, 26, and 27)	±8000	
		(ISO10605) R_D = 330 Ω, C_S = 150 pF R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air Discharge (Pins 22, 23, 26, and 27)	±15000	
			Contact Discharge (Pins 22, 23, 26, and 27)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD11}	Supply voltage	1.045	1.1	1.155	V
V_{DD18}	Supply voltage	1.71	1.8	1.89	V
V_{DDIO}	LVCMOS supply voltage	1.71	1.8	1.89	V
	V_{DDI2C}, 1.8-V operation	1.71	1.8	1.89	V
	V_{DDI2C}, 3.3-V operation	3.135	3.3	3.465	V
	HDMI termination (V_{TERM}), DC-coupled	3.135	3.3	3.465	V
	HDMI termination (V_{TERM}), AC-coupled	1.71	1.8	1.89	V
T_A	Operating free air temperature	–40	25	105	°C
T_{CLH1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under following condition: **-40C ≤ starting ambient temperature (Ts) < 0C**. (1)	Ts		80	°C
T_{CLH2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under following condition: **0C ≤ starting ambient temperature (Ts) ≤ 105C**. (1)	Ts		105	°C
T_{CHL1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is falling under following condition: **45C < starting ambient temperature (Ts) ≤ 105C**. (1)	25		Ts	°C

(1) The input and output PLLs are calibrated at the ambient start up temperature (Ts) when the device is powered on or when reset using the PDB pin. The PLLs will stay locked up to the specified ending temperature.

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_{CHL2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is falling under following condition: **-20C ≤ starting ambient temperature (Ts) ≤ 45C**.(1)	Ts-20		Ts	°C
	TMDS frequency	25		210	MHz
	Supply noise(2) (DC-50 MHz)			25	mV_{P-P}

(2) Supply noise testing was done without any capacitors or ferrite beads connected. A sinusoidal signal is AC-coupled to the V_{DD11} supply of the serializer until the deserializer loses lock.

6.4 Thermal Information

THERMAL METRIC(1)		DS90UB949A RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
1.8-V LVCMOS I/O							
V_{IH}	High level input voltage		SCLK/I2CSEL, PDB, D_GPIO0/MOSI, D_GPIO1/MISO, D_GPIO2/SPLK, D_GPIO3/SS, SDIN/GPIO0, SWC/GPIO1, MCLK I2S_DC/GPIO2, I2S_DD/GPIO3, I2S_DB/GPIO5_REG, I2S_DA/GPIO6_REG, I2S_CLK/GPIO8_REG, I2S_WC/GPIO7_REG	0.65 × V_{DDIO}			V
V_{IL}	Low level input voltage			0		0.35 × V_{DDIO}	V
I_{IN}	Input current	V_{IN} = 0 V or 1.89 V		−10		10	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA		0.7 × V_{DDIO}		V_{DDIO}	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		GND		0.26 × V_{DDIO}	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			–50		mA
I_{OZ}	TRI-STATE output current	V_{OUT} = 0 V or V_{DDIO}, PDB = L		–10		10	µA
TMDS INPUTS -- FROM HDMI v1.4b SECTION 4.2.5							
V_{ICM1}	Input common-mode voltage	IN_CLK ≤ 210 MHz	IN_D[2:0]+, IN_D[2:0]– IN_CLK+, IN_CLK– V_{TERM} = 1.8 V (±5%) or VTERM = 3.3 V (±5%)	V_{TERM} – 400		V_{TERM} – 37.5	mV
V_{ICM2}	Input common-mode voltage	IN_CLK ≤ 210 MHz		V_{TERM} – 10		V_{TERM} + 10	mV
V_{IDIFF}	Input differential voltage level	IN_CLK ≤ 210 MHz		150		1200	mV_{P-P}
R_{TMDS}	Termination resistance	Differential	IN_D[2:0]+, IN_D[2:0]– IN_CLK+, IN_CLK–	90	100	110	Ω
HDMI IO -- FROM HDMI v1.4b SECTION 4.2.7 to 4.2.9							
V_{RX_5V}	5-V power signal		RX_5V	4.8		5.3	V
I_{5V_Sink}	5-V input current				55		mA
$V_{OH,HPD}$	High level output voltage, HPD	I_{OH} = –4 mA	HPD, R_{PU} = 1 kΩ	2.4		5.3	V
$V_{OL,HPD}$	Low level output voltage, HPD	I_{OL} = 4 mA		GND		0.4	V
$I_{IZ,HPD}$	Power-down input current, HPD	PDB = L		–10		10	uA

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DC Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
$V_{IL,DDC}$	Low level input voltage, DDC		DDC_SCL, DDC_SDA			0.3 × $V_{DD,DDC}$	V
$V_{IH,DDC}$	High level input voltage, DDC			2.7			V
$I_{IZ,DDC}$	Power-down input current, DDC	PDB = L		–10		10	µA
$V_{IH,CEC}$	High level input voltage, CEC		CEC	2			V
$V_{IL,CEC}$	Low level input voltage, CEC					0.8	V
$V_{HY,CEC}$	Input hysteresis, CEC				0.4		V
$V_{OL,CEC}$	Low level output voltage, CEC			GND		0.6	V
$V_{OH,CEC}$	High level output voltage, CEC			2.5		3.63	V
I_{OFF_CEC}	Power-down input current, CEC	PDB = L		–1.8		1.8	µA
FPD-LINK III DIFFERENTIAL DRIVER							
V_{ODp-p}	Output differential voltage		DOUT[1:0]+, DOUT[1:0]–	900		1200	mV_{p-p}
ΔV_{OD}	Output voltage unbalance				1	50	mV
V_{OS}	Output differential offset voltage				550		mV
ΔV_{OS}	Offset voltage unbalance				1	50	mV
I_{OS}	Output short-circuit current	FPD-Link III outputs = 0 V			–50		mA
R_T	Termination resistance	Single-ended		40	50	60	Ω
SUPPLY CURRENT(1)							
I_{DD11}	Supply current, normal operation	Colorbar pattern			300	510	mA
I_{DD18}	Supply current, normal operation				25	50	
$I_{DD,VTERM}$	V_{TERM} current, normal operation				60		mA
I_{DDZ11}	Supply current, power-down mode	PDB = L			15		mA
I_{DDZ18}	Supply current, power-down mode				5		
$I_{DDZ,VTERM}$	V_{TERM} current, power-down mode				5		mA

(1) Specification is ensured by bench characterization.

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO FREQUENCY(1)							
$R_{b,FC}$	Forward channel GPIO frequency	Single-lane, IN_CLK = 25 MHz – 105 MHz	GPIO[3:0], D_GPIO[3:0]			0.25 × IN_CLK	MHz
		Dual-lane, IN_CLK/2 = 25 MHz – 105 MHz				0.125 × IN_CLK	
$t_{GPIO,FC}$	GPIO pulse width, forward channel	Single-lane, IN_CLK = 25 MHz – 105 MHz	GPIO[3:0], D_GPIO[3:0]	>2 / IN_CLK			s
		Dual-lane, IN_CLK/2 = 25 MHz – 105 MHz		>2 / (IN_CLK/2)			
TMDS INPUT							
Skew-Intra	Maximum intra-pair skew *(between ±)*		IN_CLK±, IN_D[2:0]±			0.4	UI_{TMDS}(2)
Skew-Inter	Maximum inter-pair skew *(between differential pairs)*					0.2 × T_{char}(3) + 1.78	ns

(1) Back channel rates are available on the companion deserializer datasheet.
(2) One bit period of the TMDS input.
(3) Ten bit periods of the TMDS input.

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AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
I_{TJIT}	Input total jitter tolerance	Per HDMI CTS ver 1.4b(4) Per Test ID 8-7: TMDS - Jitter Tolerance	IN_CLK±			0.3	UI_{TMDS}(2)
FPD-LINK III OUTPUT							
t_{LHT}	Low voltage differential low-to-high transition time				80		ps
t_{HLT}	Low voltage differential high-to-low transition time				80		ps
t_{XZD}	Output active to OFF delay	PDB = L			100		ns
t_{PLD}	Lock time (HDMI Rx)				12		ms
t_{SD}	Delay — latency		IN_CLK±		145 × T(2)		s
t_{DJIT}	Output total jitter (see Figure 5)	Random Pattern	Single-lane: measured with CDR loop BW = f/15 (7MHz)		0.3		UI_{FPD3}(5)
			Dual-lane: measured with CDR loop BW = f/30 (7MHz)				
λ_{STXBW}	Jitter transfer function (-3-dB bandwidth)				960		kHz
δ_{STX}	Jitter transfer function peaking				0.1		dB

(4) Per Test ID 8-7: TMDS - Jitter Tolerance:
1) D_JITTER = 500kHz, C_JITTER = 10MHz
Set C_JITTER component to 0.25*T_{BIT} at TP1
Set D_JITTER component to 0.3*TBIT at TP1
2) Set C_JITTER component to 0.25*T_{BIT} at TP1
Set D_JITTER component to 0.3TBIT at TP1D_JITTER = 1MHz, C_JITTER = 7MHz
Set C_JITTER component to 0.25*T_{BIT} at TP1
Set D_JITTER component to 0.3*TBIT at TP1
Note: TP1 is the edges of eye diagram shown in the HDMI specification
A CDR filter is applied at 4MHz with BER ≤1 E-10

(5) One bit period of the serializer output.

6.7 DC and AC Serial Control Bus Characteristics

Over V_{DDI2C} supply and temperature ranges unless otherwise specified. V_{DDI2C} can be 1.8 V (±5%) or 3.3 V (±5%) (refer to I2CSEL pin description for 1.8-V or 3.3-V operation).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH,I2C}$	Input high level, I2C	SDA and SCL, V_{DDI2C} = 1.8 V	0.7 × V_{DDI2C}			V
		SDA and SCL, V_{DDI2C} = 3.3 V	0.7 × V_{DDI2C}			V
$V_{IL,I2C}$	Input low level voltage, I2C	SDA and SCL, V_{DDI2C} = 1.8 V			0.3 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3 V			0.3 × V_{DDI2C}	V
V_{HY}	Input hysteresis, I2C	SDA and SCL, V_{DDI2C} = 1.8 V or 3.3 V		>50		mV
$V_{OL,I2C}$	Output low level, I2C	SDA and SCL, V_{DDI2C} = 1.8-V, fast-mode, 3-mA sink current	GND		0.2 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3-V, 3-mA sink current	GND		0.4	V
$I_{IN,I2C}$	Input current, I2C	SDA and SCL, V_{DDI2C} = 0 V	–800		–600	µA
		SDA and SCL, V_{DDI2C} = V_{DD18} or V_{DD33}	–10		10	µA
$C_{IN,I2C}$	Input capacitance, I2C	SDA and SCL		5		pF

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6.8 Recommended Timing for the Serial Control Bus

Over I2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard-mode	>0		100	kHz
		Fast-mode	>0		400	kHz
		Fast-mode plus	>0		1	MHz
t_{LOW}	SCL low period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode plus	0.5			µs
t_{HIGH}	SCL high period	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode plus	0.26			µs
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode plus	0			µs
$t_{SU;DAT}$	Data setup time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode plus	50			ns
$t_{SU;STO}$	Setup time for STOP condition	Standard-mode	4			µs
		Fast-mode	0.6			µs
		Fast-mode plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode plus	0.5			µs
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode plus			120	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode plus			120	ns
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode plus			50	ns

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6.9 Timing Diagrams

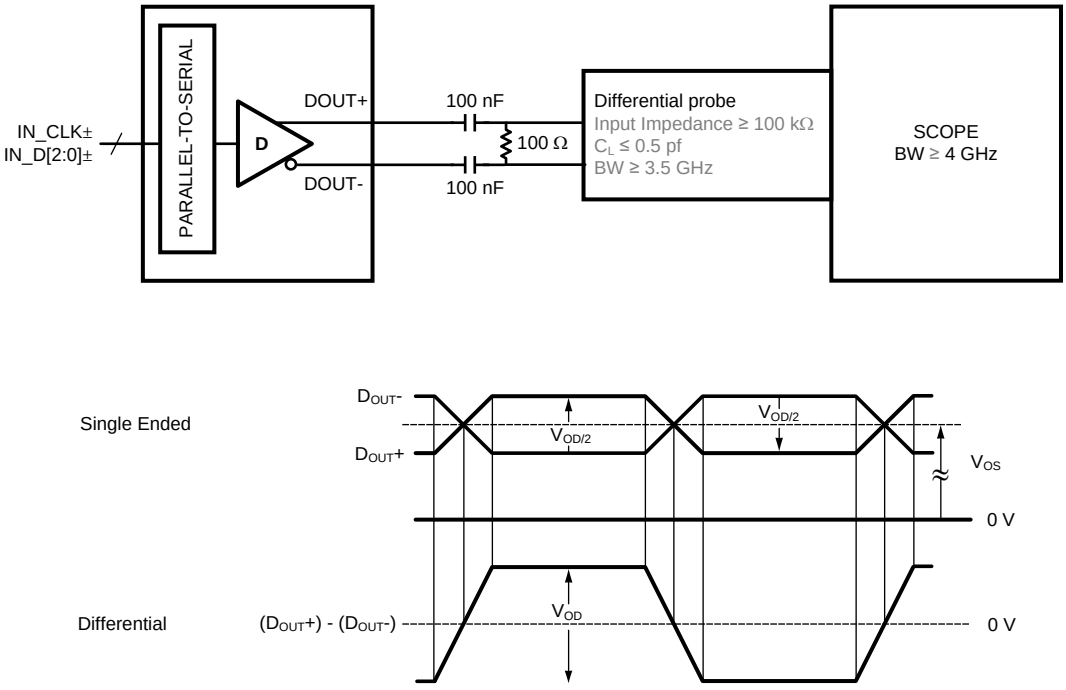

Figure 1. Serializer V_{OD} Output

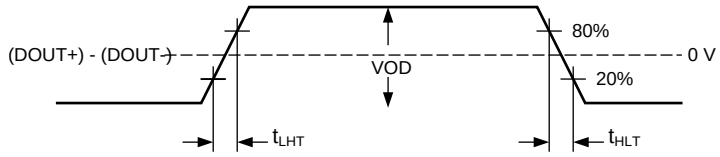

Figure 2. Output Transition Times

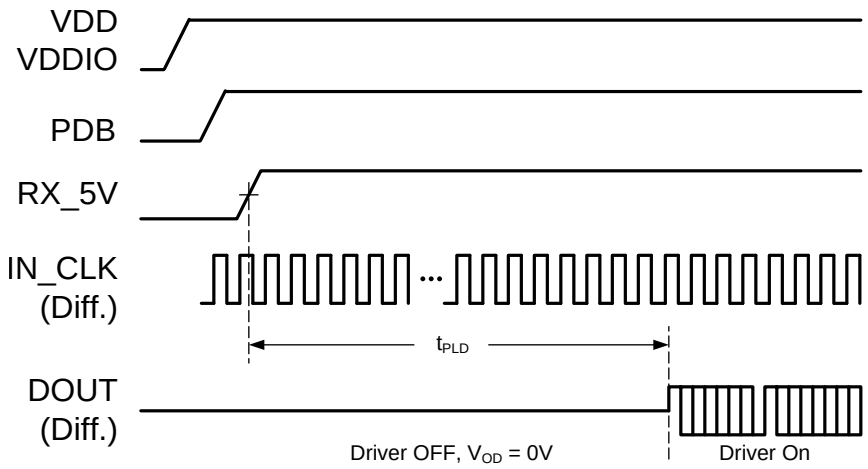

Figure 3. Serializer Lock Time

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Timing Diagrams (continued)

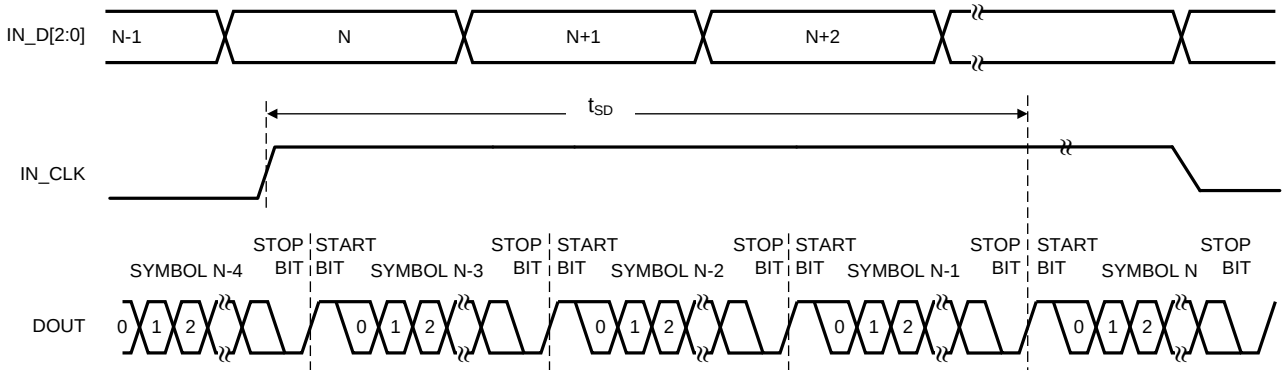

Figure 4. Latency Delay

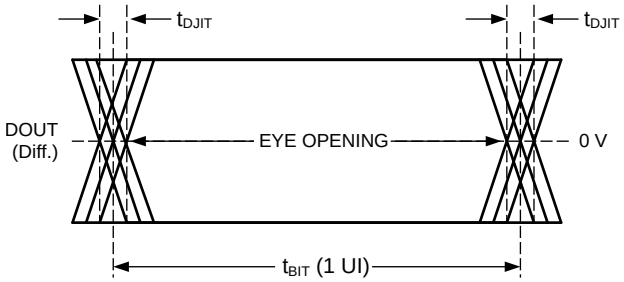

Figure 5. Serializer Output Jitter

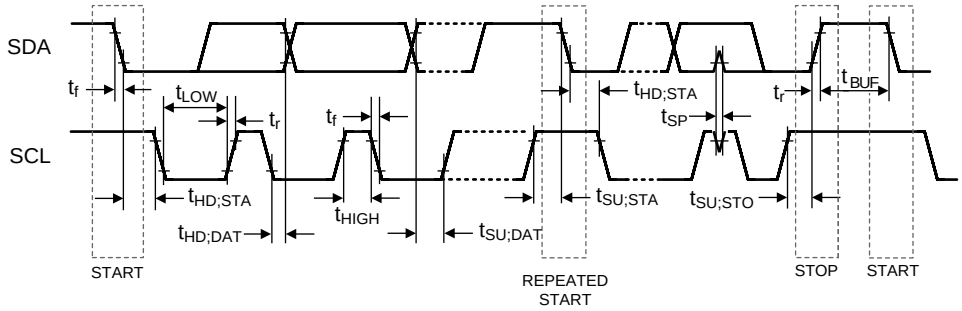

Figure 6. Serial Control Bus Timing Diagram

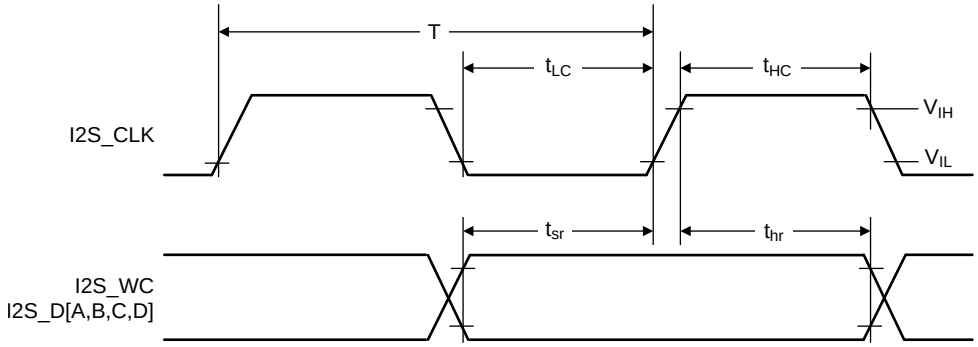

Figure 7. I2S Timing Diagram

6.10 Typical Characteristics

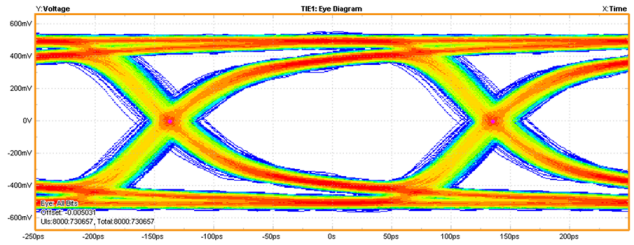

Figure 8. DOUT0 Eye at 3.675 Gbps

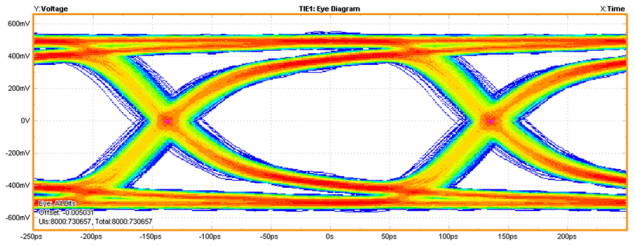

Figure 9. DOUT1 Eye at 3.675 Gbps

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7 Detailed Description

7.1 Overview

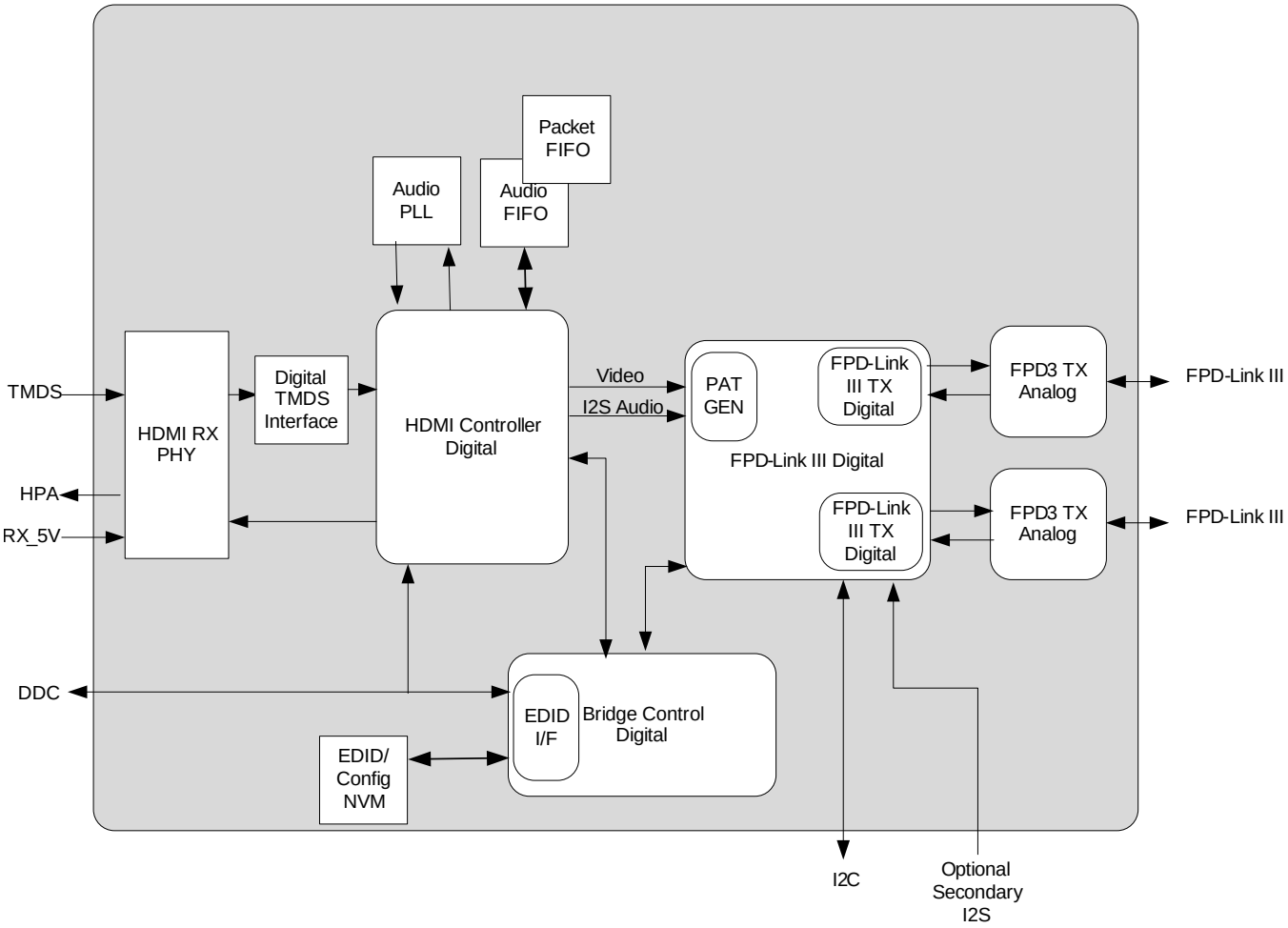
The DS90UB949A-Q1 converts an HDMI interface (3 TMDS data channels + 1 TMDS Clock) to an FPD-Link III interface. This device transmits a 35-bit symbol operating at up to a 3.675-Gbps line rate over a single serial pair or two serial pairs. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

The DS90UB949A-Q1 serializer can be used with the DS90UB926Q-Q1, DS90UB928Q-Q1, DS90UB924-Q1, DS90UB940-Q1, or DS90UB948-Q1 deserializer.

The DS90UB949A-Q1 serializer and companion deserializer can incorporate an I2C-compatible interface. The I2C-compatible interface allows the user to program the serializer or deserializer devices from a local host controller. The devices can also incorporate a bidirectional control channel (BCC) that allows communication between the serializer and deserializer as well as between remote I2C slave devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer), combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C-compatible masters at either side of the serial link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Definition Multimedia Interface (HDMI)

HDMI is a leading interface standard used to transmit digital video and audio from sources (such as a DVD player) to sinks (such as an LCD display). The interface is capable of transmitting high-definition video and audio. Other HDMI signals consist of various control and status data that travel bidirectionally.

7.3.1.1 HDMI Receive Controller

The HDMI receiver is an HDMI version 1.4b compliant receiver. The HDMI receiver can operate in up to 2880x1080 at 60 Hz resolution. The configuration used in the DS90UB949A-Q1 does not include version 1.4b features, such as the ethernet channel (HEC) or Audio Return Channel (ARC).

7.3.2 Transition Minimized Differential Signaling

HDMI uses Transition Minimized Differential Signaling (TMDS) over four differential pairs (three TMDS channels and one TMDS clock) to transmit video and audio data. TMDS is widely used to transmit high-speed serial data. The technology incorporates a form of 8b/10b encoding, and the differential signaling allows the device to reduce electromagnetic interference (EMI) and achieve high skew tolerance.

7.3.3 Enhanced Display Data Channel

The Display Data Channel (DDC) is a collection of digital communication protocols between a computer display and a graphics adapter that enables the display to send the supported display modes to the adapter. The DDC also allows the computer host to adjust monitor parameters, such as brightness and contrast.

7.3.4 Extended Display Identification Data (EDID)

EDID is a data structure provided by a digital display to describe the display capabilities to a video source. By providing this information, the video source can then send video data with the proper timing and resolution that the display supports. The DS90UB949A-Q1 supports several options for delivering display identification (EDID) information to the HDMI graphics source. The EDID information is accessible through the DDC interface and complies with the DDC and EDID requirements given in the HDMI v1.4b specification.

The EDID configurations supported are as follows:

- External local EDID (EEPROM)
- Internal EDID loaded into device memory
- Remote EDID connected to I2C bus at deserializer side
- Internal pre-programmed EDID

The EDID mode selected should be configurable from the MODE_SEL pins or from internal control registers. For all modes, the EDID information should be accessible at the default address of 0xA0.

7.3.4.1 External Local EDID (EEPROM)

The DS90UB949A-Q1 can be configured to allow a local EEPROM EDID device. The local EDID device may implement any EDID configuration allowable by the HDMI v1.4b and DVI 1.0 standards, including multiple extension blocks up to 32KB.

7.3.4.2 Internal EDID (SRAM)

The DS90UB949A-Q1 also allows the internal loading of an EDID profile up to 256 bytes. This SRAM storage is volatile and requires loading from an external I2C master (local or remote). The internal EDID is reloadable and readable (local/remote) from control registers during normal operation.

7.3.4.3 External Remote EDID

The serializer copies the remote EDID connected to the I2C bus of the remote deserializer into the internal SRAM. The remote EDID device can be a standalone I2C EEPROM, or integrated into the digital display panel. In this mode, the serializer automatically accesses the Bidirectional Control Channel to search for the EDID information at the default address 0xA0. When the EDID is found, the serializer copies the remote EDID into the local SRAM.

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Feature Description (continued)

7.3.4.4 Internal Pre-Programmed EDID

The serializer also has an internal eFuse that is loaded into the internal SRAM with pre-programmed 256-byte EDID data at start-up. This EDID profile supports several generic video (480p, 720p) and audio (2-channel audio) timing profiles within the single-link operating range of the device (25-MHz to 105-MHz pixel clock). In this mode, the internal EDID SRAM data is readable from the DDC interface. The EDID contents are below:

0x00	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0x00	0x53	0x0E	0x49	0x09	0x01	0x00	0x00	0x00
0x1C	0x18	0x01	0x03	0x80	0x34	0x20	0x78	0x0A	0xEC	0x18	0xA3	0x54	0x46	0x98	0x25
0x0F	0x48	0x4C	0x00	0x00	0x00	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x1D	0x00	0x72	0x51	0xD0	0x1E	0x20	0x6E	0x50
0x55	0x00	0x00	0x20	0x21	0x00	0x00	0x18	0x00	0x00	0x00	0xFD	0x00	0x3B	0x3D	0x62
0x64	0x08	0x00	0x0A	0x20	0x20	0x20	0x20	0x20	0x20	0x00	0x00	0x00	0xFC	0x00	0x54
0x49	0x2D	0x44	0x53	0x39	0x30	0x55	0x78	0x39	0x34	0x39	0x0A	0x00	0x00	0x00	0x10
0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x01	0x57
0x02	0x03	0x15	0x40	0x41	0x84	0x23	0x09	0x7F	0x05	0x83	0x01	0x00	0x00	0x66	0x03
0x0C	0x00	0x10	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x00	0x00	0x00

Feature Description (continued)

The device supports TMDS clocks in the range of 25 MHz to 105 MHz over one lane, or 50 MHz to 210 MHz over two lanes. The FPD-Link III serial stream rate is 3.675 Gbps maximum (875 Mbps minimum) when transmitting either over one lane or both lanes.

7.3.9 Back Channel Data Transfer

The backward channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding, and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, CRC, and 4 bits of standard GPIO information with a line rate of 5, 10, or 20 Mbps (configured by the compatible deserializer).

7.3.10 FPD-Link III Port Register Access

The DS90UB949A-Q1 contains two downstream ports, therefore some registers must be duplicated to allow control and monitoring of the two ports. To facilitate this, a TX_PORT_SEL register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) will be available independent of the settings in the TX_PORT_SEL register.

Setting the TX_PORT0_SEL or TX_PORT1_SEL bit will allow a read of the register for the selected port. If both bits are set, port1 registers will be returned. Writes will occur to ports for which the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

Setting the PORT1_I2C_EN bit will enable a second I2C slave address, allowing access to the second port registers through the second I2C address. If this bit is set, the TX_PORT0_SEL and TX_PORT1_SEL bits will be ignored.

7.3.11 Power Down (PDB)

The serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 1.71 V to 1.89 V. To save power, disable the link when the display is not required (PDB = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0 V for at least 3 ms before releasing or driving high. In the case where PDB is pulled up to V_{DDIO} directly, a 10-kΩ pullup resistor and a >10-µF capacitor to ground are required (see *Power-Up Requirements and PDB Pin*).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held LOW for at least 3 ms before going high again.

7.3.12 Serial Link Fault Detect

The DS90UB949A-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 10). The DS90UB949A-Q1 will detect any of the following conditions:

1. Cable open
2. “+” to “–” short
3. ”+” to GND short
4. ”–” to GND short
5. ”+” to battery short
6. ”–” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT– connections reversed)

NOTE

The device will detect any of the above conditions, but does not report specifically which one has occurred.

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Feature Description (continued)

7.3.13 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions (see registers 0xC6 and 0xC7 in the *Register Maps*). For the remote interrupt condition, the INTB pin works in conjunction with the INTB_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN pin is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW. To determine the interrupt source, read the ISR register.
5. A read to ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the deserializer INTB_IN. This would be when the downstream device releases the INTB_IN pin on the deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

7.3.14 Remote Interrupt Pin (REM_INTB)

REM_INTB will mirror the status of INTB_IN pin on the deserializer and does not need to be cleared. If the serializer is not linked to the deserializer, REM_INTB will be high.

7.3.15 General-Purpose I/O

7.3.15.1 GPIO[3:0] and D_GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose I/Os in either forward channel (outputs) or back channel (inputs) mode. GPIO and D_GPIO modes may be configured from the registers. The same registers configure either GPIO or D_GPIO, depending on the status of PORT1_SEL and PORT0_SEL bits (0x1E[1:0]). D_GPIO operation requires 2-lane FPD-Link III mode. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3 / D_GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2 / D_GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1 / D_GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0 / D_GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

7.3.15.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. These different modes are controlled by a compatible deserializer. Consult the appropriate deserializer datasheet for details on how to configure the back channel frequency. See Table 2 for details about D_GPIOs in various modes.

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Table 2. Back Channel D_GPIO Effective Frequency

HSCC_MODE (ON DES)	MODE	NUMBER OF D_GPIOs	SAMPLES PER FRAME	D_GPIO EFFECTIVE FREQUENCY(1) (kHz)			D_GPIOs ALLOWED
				5-Mbps BC(2)	10-Mbps BC(3)	20-Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst-case back channel frequency (–20%) and a 4X sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 and BC_HS_CTL = 0 on deserializer.
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 and BC_HS_CTL = 0 on deserializer.
(4) 20 Mbps corresponds to BC FREQ SELECT = X and BC_HS_CTL = 1 on deserializer.

7.3.15.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See Table 3 for GPIO enable and configuration.

NOTE

Local GPIO value may be configured and read either through local register access, or remote register access through the Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer, as is the case for GPIO[3:0].

Table 3. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x11[7:4] = 0x01	Output, L
	0x11[7:4] = 0x09	Output, H
	0x11[7:4] = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x11[3:0] = 0x1	Output, L
	0x11[3:0] = 0x9	Output, H
	0x11[3:0] = 0x3	Input, Read: 0x1C[7]
GPIO_REG6	0x10[7:4] = 0x1	Output, L
	0x10[7:4] = 0x9	Output, H
	0x10[7:4] = 0x3	Input, Read: 0x1C[6]
GPIO_REG5	0x10[3:0] = 0x1	Output, L
	0x10[3:0] = 0x9	Output, H
	0x10[3:0] = 0x3	Input, Read: 0x1C[5]
GPIO3	0x0F[3:0] = 0x1	Output, L
	0x0F[3:0] = 0x9	Output, H
	0x0F[3:0] = 0x3	Input, Read: 0x1C[3]
GPIO2	0x0E[7:4] = 0x1	Output, L
	0x0E[7:4] = 0x9	Output, H
	0x0E[7:4] = 0x3	Input, Read: 0x1C[2]
GPIO1	0x0E[3:0] = 0x1	Output, L
	0x0E[3:0] = 0x9	Output, H
	0x0E[3:0] = 0x3	Input, Read: 0x1C[1]
GPIO0	0x0D[3:0] = 0x1	Output, L
	0x0D[3:0] = 0x9	Output, H
	0x0D[3:0] = 0x3	Input, Read: 0x1C[0]

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7.3.16 SPI Communication

The SPI control channel uses the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available: forward channel and reverse channel modes. In forward channel mode, the SPI master is located at the serializer, such that the direction of sending SPI data is in the same direction as the video data. In reverse channel mode, the SPI master is located at the deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI control channel can operate in a high-speed mode when writing data, but the channel must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round-trip data latency. On the other hand, data for SPI writes can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

NOTE

SPI cannot be used to access the serializer and deserializer registers.

7.3.16.1 SPI Mode Configuration

SPI is configured over the I2C using the High-Speed Control Channel Configuration (HSCC_CONTROL) register 0x43 on the deserializer. HSCC_MODE (0x43[2:0]) must be configured for either high-speed, forward channel SPI mode (110) or high-speed, reverse channel SPI mode (111).

7.3.16.2 Forward-Channel SPI Operation

In forward-channel SPI operation, the SPI master located at the serializer generates the SPI Clock (SPLK), Master Out / Slave In data (MOSI), and active low Slave Select (SS). The serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the deserializer, the SPI signals are regenerated using the pixel clock. To preserve setup and hold time, the deserializer will hold MOSI data while the SPLK signal is high. The deserializer can also delay the SPLK by one pixel clock relative to the MOSI data, increasing the setup by one pixel clock.

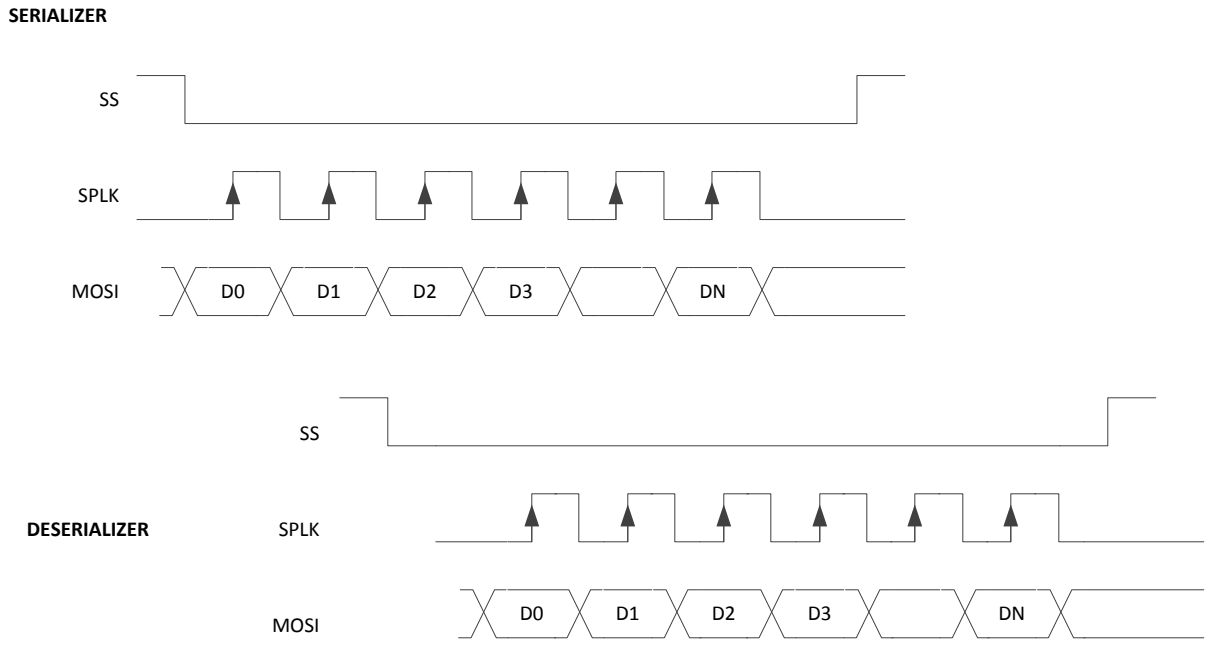

Figure 11. Forward Channel SPI Write

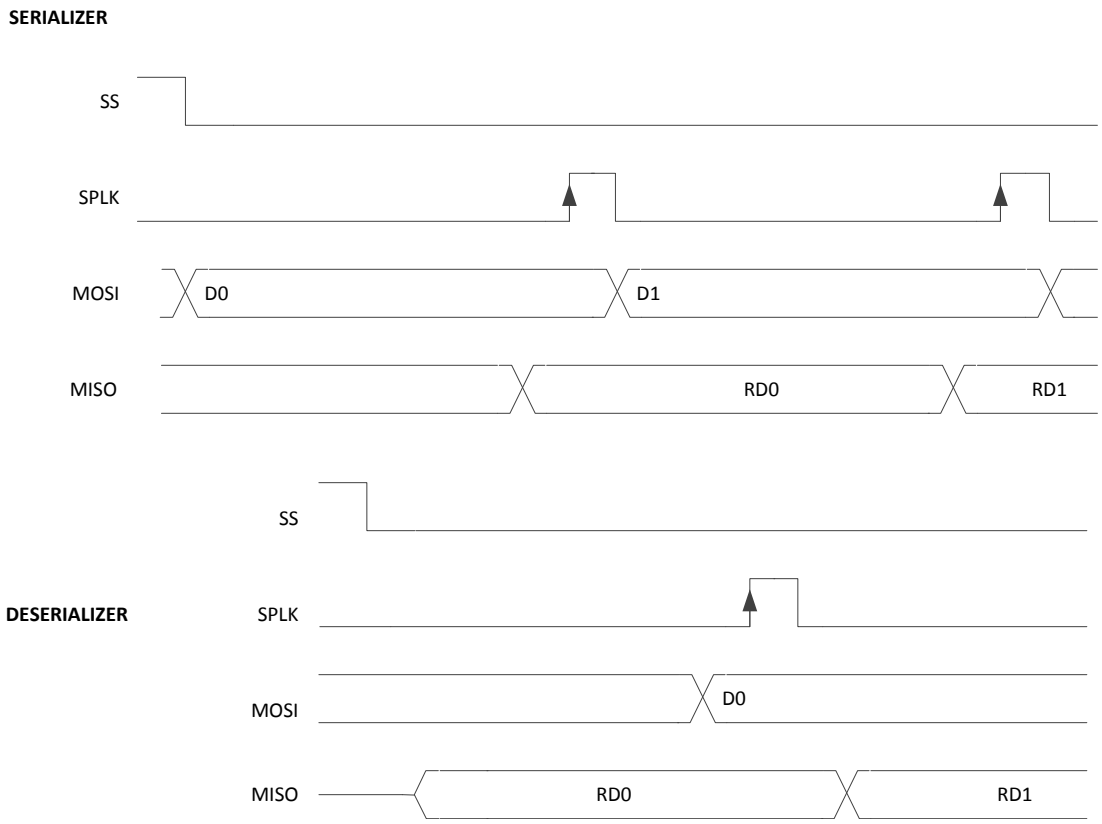

Figure 12. Forward Channel SPI Read

7.3.16.3 Reverse Channel SPI Operation

In reverse channel SPI operation, the deserializer samples the Slave Select (SS) and the SPI Clock (SCLK) in the internal oscillator clock domain. Upon detection of the active SPI clock edge, the deserializer can also sample the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the serializer over the back channel. The deserializer sends SPI information in a back channel frame to the serializer. In each back channel frame, the deserializer sends an indication of the Slave Select value. The Slave Select should be inactive (high) for at least one back-channel frame period to ensure propagation to the serializer.

Because data is delivered in separate back channel frames and then buffered, the data may be regenerated in bursts. Figure 13 shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivered the remaining data bits.

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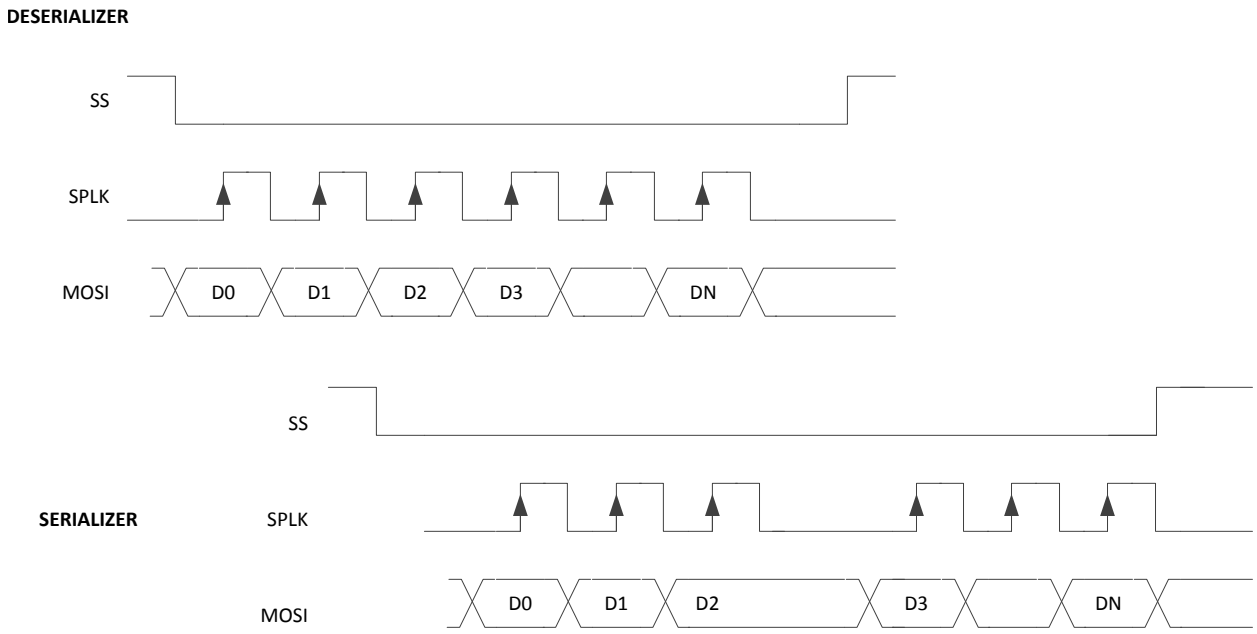

Figure 13. Reverse Channel SPI Write

For reverse-channel SPI reads, the SPI master must wait for a round-trip response before the master can generate the sampling edge of the SPI clock. This is similar to operation in forward channel mode. Note that each back channel frames sends out one data/clock sample.

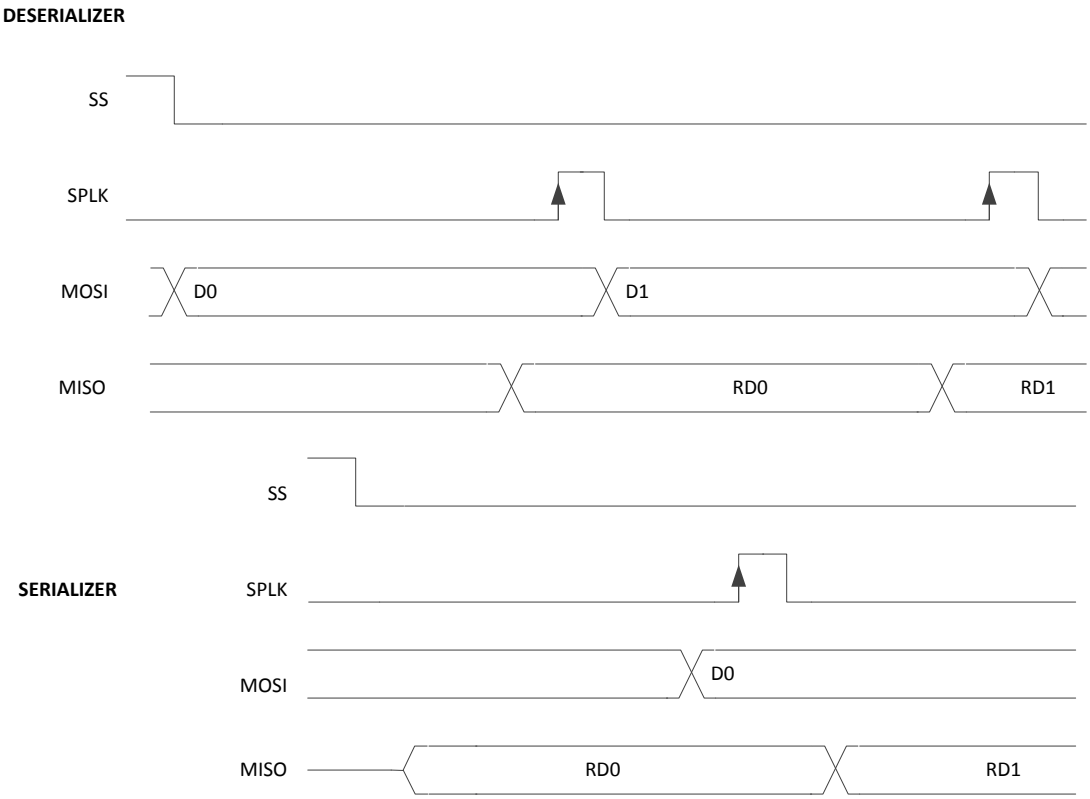

Figure 14. Reverse Channel SPI Read

For both reverse-channel SPI writes and reads, the SPI_SS signal should be deasserted for at least one back channel frame period.

Table 4. SPI SS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

7.3.17 Backward Compatibility

This FPD-Link III serializer is backward-compatible to the DS90UB926Q-Q1, DS90UB928Q-Q1 and DS90UB924-Q1 for TMDS clock frequencies ranging from 25 MHz to 96 MHz. Enabling backward compatibility is not required. When paired with a backward-compatible device, the serializer will auto-detect to 1-lane FPD-Link III on the primary channel (DOUT0±).

7.3.18 Audio Modes

The DS90UB949A-Q1 supports several audio modes and functions:

- HDMI Mode
- DVI Mode
- AUX Audio Channel

Because the default audio mode for DS90UB926Q-Q1 is I2S surround sound and the DS90UB926Q-Q1 cannot receive more than two channels of audio while in 24 bit mode, the DS90UB949A-Q1 will automatically transmit 18-bit video to a DS90UB926Q-Q1. To transmit 24-bit video to a DS90UB926Q-Q1, I2S Surround must be disabled by writing to register 0x1A[0]=0.

7.3.18.1 HDMI Audio

The DS90UB949A-Q1 allows embedded audio in the HDMI interface to be transported over the FPD-Link III serial link and output on the compatible deserializer. Depending on the number of channels, HDMI audio can be output on several I2S pins on the deserializer, or it can be converted to TDM to output on one audio output pin on the deserializer.

7.3.18.2 DVI I2S Audio Interface

The DS90UB949A-Q1 serializer features six I2S input pins that, when paired with a compatible deserializer, supports 7.1 high-definition (HD), surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the lesser of IN_CLK/2 or 13 MHz. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. Refer to Figure 15 and Figure 16 for I2S connection diagram and timing information.

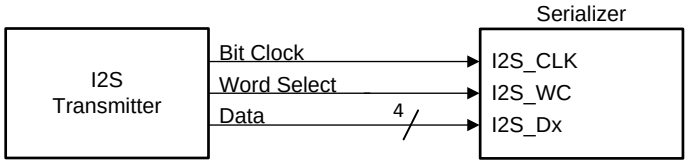

Figure 15. I2S Connection Diagram

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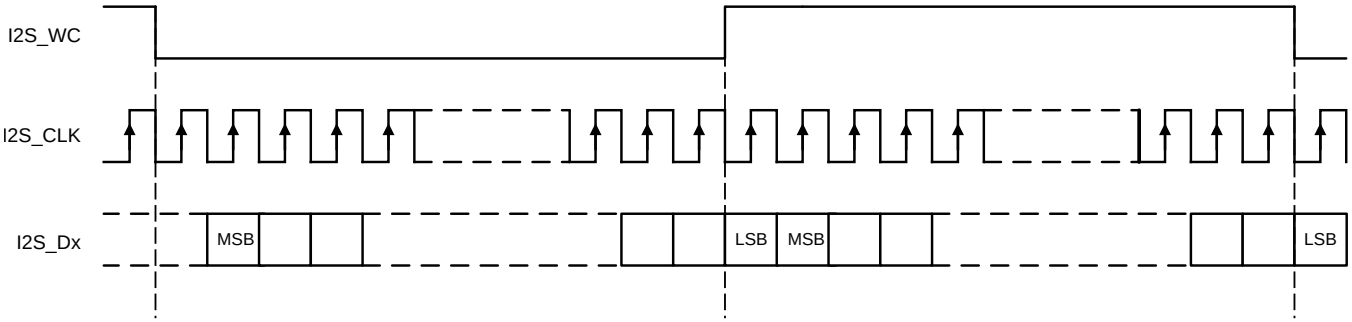

Figure 16. I2S Frame Timing Diagram

Table 5 covers several common I2S sample rates:

Table 5. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.18.2.1 I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated data island transport frames. Data island frames may be disabled from control registers if forward-channel frame transport of I2S data is desired. In this mode, only I2S_DA is transmitted to a DS90UB928Q-Q1, DS90UB940-Q1, or DS90UB948-Q1 deserializer. If connected to a DS90UB926Q-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround sound mode, which transmits all four I2S data inputs (I2S_D[A..D]), may only be operated in data-island transport mode. This mode is only available when connected to a DS90UB928Q-Q1, DS90UB940-Q1, or DS90UB948-Q1 deserializer.

7.3.18.2.2 I2S Repeater

I2S audio may be fanned out and propagated in the repeater application. By default, data is propagated through the data island transport during the video blanking periods. If frame transport is desired, then the I2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream serializers and deserializers for surround sound transport using the data island transport. If 4-channel operation using the I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (see Table 10).

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7.3.18.3 AUX Audio Channel

The AUX audio channel is a single separate I2S audio data channel that may be transported independently of the main audio stream received in either HDMI mode or DVI mode. This channel is shared with the GPIO[1:0] interface and is supported by the DS90UB940-Q1 and DS90UB948-Q1 deserializers.

7.3.18.4 TDM Audio Interface

In addition to the I2S audio interface, the DS90UB949A-Q1 serializer also supports TDM format. A number of specifications for TDM format are in common use, so the DS90UB949A-Q1 offers flexible support for word length, bit clock, number of channels to be multiplexed, and so forth. For example, assume that the word clock signal (I2S_WC) period = 256 × bit clock (I2S_CLK) time period. In this case, the DS90UB949A-Q1 can multiplex four channels with maximum word length of 64 bits each, or eight channels with a maximum word length of 32 bits each. Figure 17 shows the multiplexing of eight channels with 24-bit word length in a format similar to I2S.

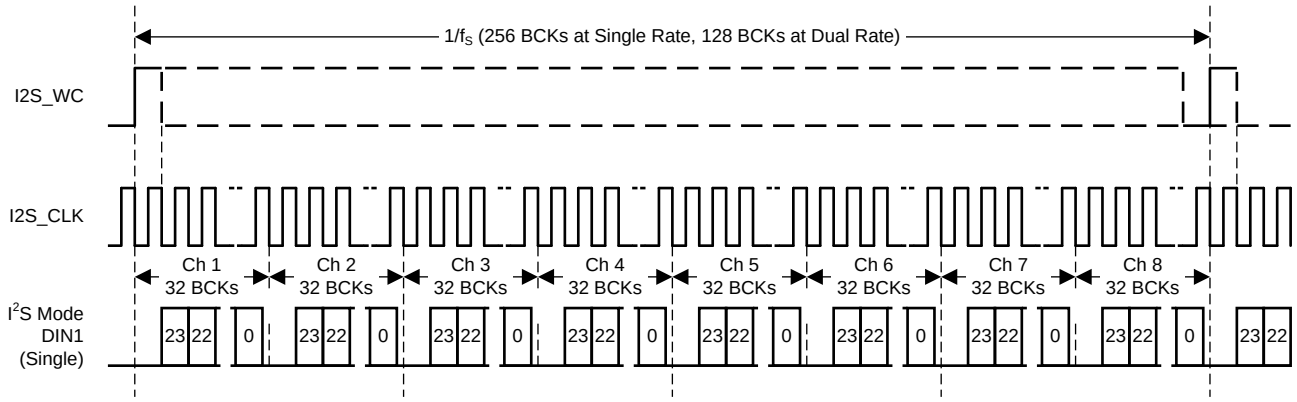

Figure 17. TDM Format

7.3.19 Built-In Self Test (BIST)

An optional at-speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.19.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by either the BISTEN pin or the BIST configuration register. The test may select either an external TMDS clock or the internal Oscillator Clock (OSC) frequency. In the absence of the TMDS clock, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received that contained one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until a reset (through either a new BIST test or during power down). A high on PASS indicates that no errors were detected. A Low on PASS indicates that one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See Figure 18 for the BIST mode flow diagram.

Step 1: The Serializer is paired with another FPD-Link III deserializer and BIST Mode is enabled through the BISTEN pin or through the register on the deserializer. Right after BIST is enabled, part of the BIST sequence requires that bit 0x04[5] is toggled locally on the serializer (set 0x04[5]=1, then set 0x04[5]=0). The desired clock source is selected either through the deserializer BISTC pin or through register on the deserializer.

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Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. When the serializer and the deserializer are in BIST mode and the deserializer acquires a lock state, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To stop the BIST mode, the deserializer BISTEN pin is set low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error-free, the PASS output will remain high. If one or more errors were detected, the PASS output will output a constant low. The PASS output state is held until a new BISTEN toggle, the device is RESET, or the device is powered down. The BIST duration is user-controlled by the duration of the BISTEN signal.

Step 4: The link returns to normal operation after the deserializer BISTEN pin is low. Figure 19 shows the waveform diagram of a typical BIST test for two cases: Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

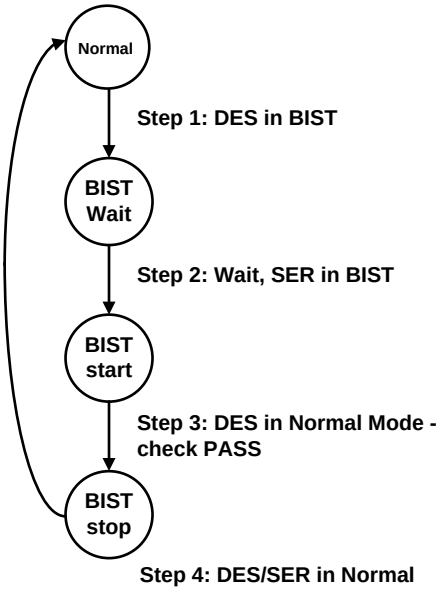

Figure 18. BIST Mode Flow Diagram

7.3.19.2 Forward-Channel and Back-Channel Error Checking

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal, all-zeroes pattern. The internal, all-zeroes pattern goes through the scrambler, DC balancing, and so forth, and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back channel data is checked for CRC errors once the serializer locks onto the back channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 10). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until the register is cleared or the serializer enters BIST mode again.

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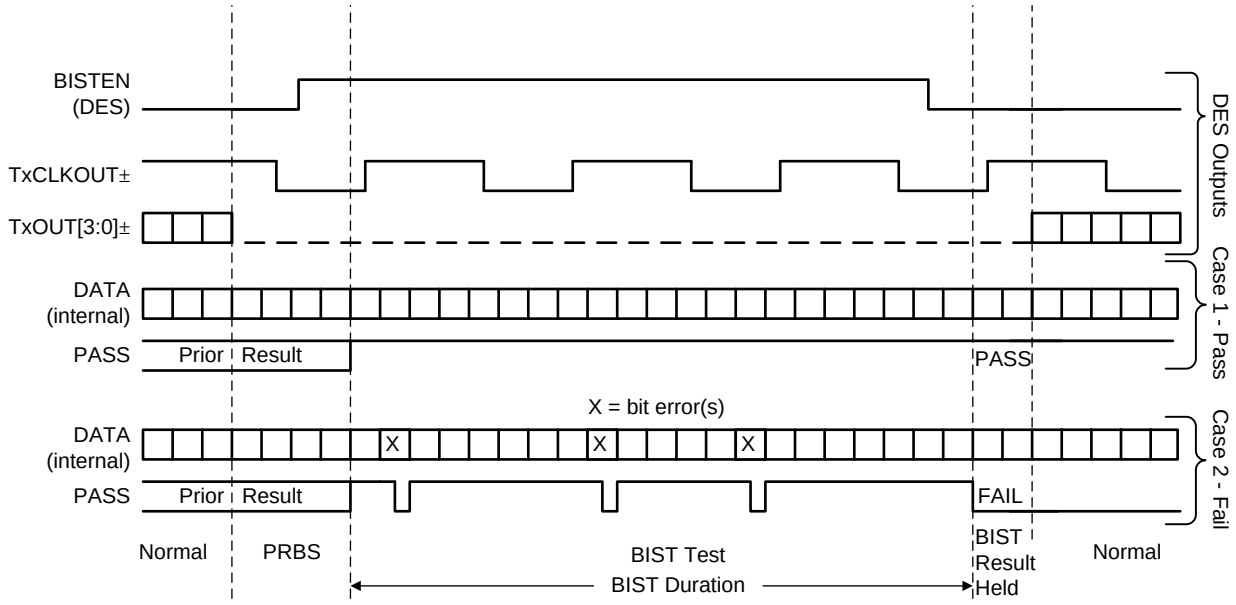

Figure 19. BIST Waveforms in Conjunction With Deserializer Signals

7.3.20 Internal Pattern Generation

The DS90UB949A-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power-down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to the *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices application note* (SNLA132).

7.3.20.1 Pattern Options

The DS90UB949A-Q1 serializer pattern generator can generate 17 default patterns to use in basic testing and debugging of panels. Each can be inverted using register bits (Table 10) shown below:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

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Additionally, the pattern generator incorporates one user-configurable, full-screen, 24-bit color controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when auto-scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when auto-scrolling is enabled.

7.3.20.2 Color Modes

By default, the pattern generator operates in 24-bit color mode where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 10). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled. The 2 least significant bits will be 0.

7.3.20.3 Video Timing Modes

The pattern generator has two video timing modes: external and internal. In external timing mode, the pattern generator detects the video frame timing present on the DE and VS inputs. If vertical sync signaling is not present on VS, the pattern generator determines the vertical blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the pattern generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (Table 10).

7.3.20.4 External Timing

In external timing mode, the pattern generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. The pattern generator extracts the active frame dimensions from the incoming signals to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the pattern generator determines the vertical blank time by detecting a long period of pixel clocks without deassertion.

7.3.20.5 Pattern Inversion

The pattern generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen Cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

7.3.20.6 Auto Scrolling

The pattern generator supports an auto-scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

7.3.20.7 Additional Features

Additional pattern generator features can be accessed through the *Pattern Generator Indirect Register Map*. It consists of the Pattern Generator Indirect Address (PGIA reg_0x66 — Table 10) and the Pattern Generator Indirect Data (PGID reg_0x67 — Table 10). See *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* application note (SNLA132).

7.3.21 Spread-Spectrum Clock Tolerance

The DS90UB949A-Q1 tolerates a spread-spectrum input clock to help reduce EMI. The following triangular SSC profile is supported:

- Frequency deviation ≤ 2.5%
- Modulation rate ≤ 100 kHz

Note: Maximum frequency deviation and maximum modulation rate are not supported simultaneously. Some typical examples:

- Frequency deviation: 2.5%, modulation rate: 50 kHz
- Frequency deviation: 1.25%, modulation rate: 100 kHz

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7.4 Device Functional Modes

7.4.1 Mode Select Configuration Settings (MODE_SEL[1:0])

Configuration of the device may be done through the MODE_SEL[1:0] input pins, or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs. See Table 7 and Table 8. These values will be latched into register location during power up:

Table 6. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
EDID_SEL: Display ID Select	0	Look for remote EDID, if none found, use internal SRAM EDID. Can be overridden from register. Remote EDID address may be overridden from default 0xA0.
	1	Use external local EDID.
AUX_I2S: AUX Audio Channel	0	HDMI audio.
	1	HDMI + AUX audio channel.
EXT_CTL: External Controller Override	0	Internal HDMI control.
	1	External HDMI control from I2C interface pins.
COAX: Cable Type	0	Enable FPD-Link III for twisted-pair cabling.
	1	Enable FPD-Link III for coaxial cabling.
REM_EDID_LOAD: Remote EDID Load	0	Use internal SRAM EDID.
	1	If available, remote EDID is copied into internal SRAM EDID.

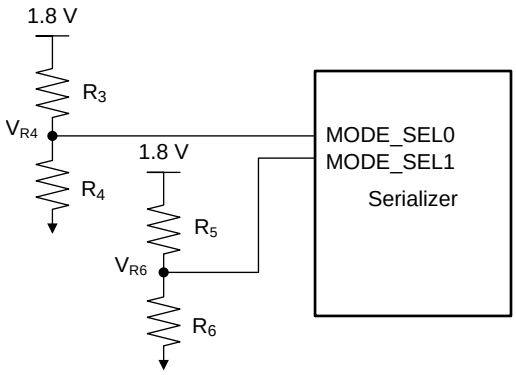

Figure 20. MODE_SEL[1:0] Connection Diagram

Table 7. Configuration Select (MODE_SEL0)

NO.	RATIO V_{R4}/V_{DD18}	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULLUP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULLDOWN R4 kΩ (1% tol)	EDID_SEL	AUX_I2S
1	0	0	OPEN	Any value less than 100 (1)	0	0
2	0.208	0.374	118	30.9	0	1
3	0.553	0.995	82.5	102	1	0
4	0.668	1.202	68.1	137	1	1

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

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Table 8. Configuration Select (MODE_SEL1)

NO.	RATIO V_{R6}/V_{DD18}	TARGET V_{R6} (V)	SUGGESTED RESISTOR PULLUP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULLDOWN R6 kΩ (1% tol)	EXT_CTL	COAX	REM_EDID_LOAD
1	0	0	OPEN	Any value less than 100(1)	0	0	0
2	0.208	0.374	118	30.9	0	0	1
3	0.323	0.582	107	51.1	0	1	0
4	0.440	0.792	113	88.7	0	1	1
5	0.553	0.995	82.5	102	1	0	0
6	0.668	1.202	68.1	137	1	0	1
7	0.789	1.420	56.2	210	1	1	0
8	1	1.8	Any value less than 100(1)	OPEN	1	1	1

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

The strapped values can be viewed and/or modified in the following locations:

- EDID_SEL : Latched into BRIDGE_CTL[0], EDID_DISABLE (0x4F[0]).
- AUX_I2S : Latched into BRIDGE_CFG[1], AUDIO_MODE[1] (0x54[1]).
- EXT_CTL: Latched into BRIDGE_CFG[7], EXT_CONTROL (0x54[7]).
- COAX : Latched into DUAL_CTL1[7], COAX_MODE (0x5B[7]).
- REM_EDID_LOAD : Latched into BRIDGE_CFG[5] (0x54[5]).

7.4.2 FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The following modes are supported:

7.4.2.1 Single-Link Operation

Single-link mode transmits the video over a single FPD-Link III to a single receiver. Single-link mode supports frequencies up to 96 MHz for 24-bit video when paired with the DS90UB924/DS90UB940-Q1/DS90UB948-Q1. This mode is compatible with the DS90UB926Q-Q1/DS90UB928Q-Q1 when operating below 85 MHz. If the downstream device is capable, the secondary FPD-Link III link could be used for high-speed control.

In forced single mode (set through DUAL_CTL1 register), the secondary TX Phy and back channel are disabled.

7.4.2.2 Dual-Link Operation

In dual-link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. The receiver must be a DS90UB940-Q1 or DS90UB948-Q1 that can receive the dual-stream video. Dual-link mode can support an HDMI clock frequency of up to 210 MHz, with each FPD-Link III TX port running at one-half the frequency. This allows support up to 2880x1080. The secondary FPD-Link III link could be used for high-speed control. Note that dual link can support 170MHz when paired with DS90UB940-Q1 and 192MHz when paired with DS90UB948-Q1.

Dual-link mode may be automatically configured when connected to a DS90UB940-Q1/DS90UB948-Q1, if the video meets minimum frequency requirements. Dual Link mode may also be forced using the DUAL_CTL1 register.

For dual lane operation, if the High-Speed Control Channel (HSCC) is desired, force the back channel capabilities for Port 1.

- Force the back channel capability for Port1:
  - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
  - Set Reg0x20=0x8F (Make Port1 Dual link capable in Deserializer Capabilities register)
  - Set Reg0x1E=0x01 (Select Port0 in Port Select register to restore the register default value)
- For forcing dual lane mode, use the following configuration:

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– Set Reg0x5B[2:0]=011b (disable auto-detect and force dual link mode in the DUAL_CTL1 register)

Any device configuration, including this one, should be written as a part of the Init A sequence as shown in Figure 33.

7.4.2.3 Replicate Mode

In this mode, the FPD-Link III TX operates as a 1:2 Repeater. The same video (up to 105 MHz, 24-bit color) is delivered to each receiver.

Replicate mode may be automatically configured when connected to two independent deserializers.

7.4.2.4 Auto-Detection of FPD-Link III Modes

The DS90UB949A-Q1 automatically detects the capabilities of downstream links and can resolve whether a single device, dual-capable device, or multiple single link devices are connected.

In addition to the downstream device capabilities, the DS90UB949A-Q1 will be able to detect the HDMI pixel clock frequency to select the proper operating mode.

If the DS90UB949A-Q1 detects two independent devices, it will operate in replicate mode, sending the single channel video on both connections. If the device detects a device on the secondary link, but not the first, it can send the video only on the second link.

Auto-detection can be disabled to allow forced modes of operation using the Dual Link Control Register (DUAL_CTL1).

The frequency detection circuit may change the single / dual mode during a temperature ramp. When the ambient temperature around the DS90UB949A-Q1 changes by more than 40°C, and when PCLK is between 60 MHz and 78 MHz, the auto-detect feature can switch the device configuration from single-lane to dual-lane mode (or vice-versa), even though the input PCLK has not changed. This causes a configuration change in deserializer, resulting in a momentary loss of lock that may result in display flicker. TI recommends to configure the device to force the single-lane or dual-lane mode of operation.

- For forcing single-lane mode, use the following configuration:
  - If the deserializer is set in HSCC mode prior to forcing single-lane mode, force the back channel capability for Port1:
    - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
    - Set Reg0x20=0x8F (Make Port1 dual-link capable in Deserializer Capabilities register)
    - Set Reg0x1E=0x01 (Select Port0 in Port Select register to restore the register default value)
  - Set Reg0x5B[2:0]=100b (Enable auto-detect and disable dual-link mode in DUAL_CTL1 register)
- For forcing dual-lane mode, use the following configuration:
  - If the deserializer is set in HSCC mode prior to forcing dual-lane mode, force the back channel capability for Port1:
    - Set Reg0x1E=0x02 (Select Port1 in Port Select register)
    - Set Reg0x20=0x8F (Make Port1 Dual link capable in Deserializer Capabilities register)
  - Set Reg0x5B[2:0]=011b (Disable auto-detect and force dual-link mode in DUAL_CTL1 register)

Any device configuration, including this one, should be written as a part of the Init A sequence as shown in Figure 33

7.4.2.5 Frequency Detection Circuit May Reset the FPD-Link III PLL During a Temperature Ramp

When ambient temperature around the DS90UB949A-Q1 changes by more than 40°C, the frequency detection logic in the device can RESET the FPD-Link III PLL even though the input PCLK has not changed. This behavior may result in a loss of lock in the deserializer, and flicker on the system display.

The following programming sequence is required for all systems. This should be written after the user register configuration of the DS90UB949A-Q1 and downstream deserializer configuration.

- Disable the *Reset FPD-Link III PLL on Frequency Change* feature after the DS90UB949A-Q1 power up.
  - Set Reg0x5B[5]=0b (Disable PLL reset feature through RST_PLL_FREQ field in DUAL_CTL1 register).

Any device configuration, including this one, should be written as a part of the Init A sequence as shown in Figure 33.

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7.5 Programming

7.5.1 Serial Control Bus

This serializer may also be configured through a I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set through a resistor divider (see R1 and R2 in Figure 21) connected to the IDx pin.

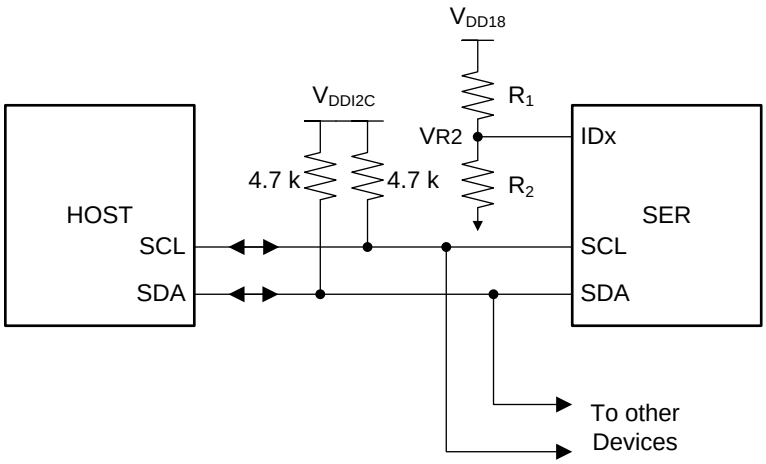

Figure 21. Serial Control Bus Connection

The serial control bus consists of two signals: SCL and SDA. SCL is a Serial Bus Clock Input and SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DD18} or V_{DD33}. For most applications, a 4.7-kΩ pullup resistor is recommended. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled high or driven low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage on the IDx input pin. See Table 10 for more information.

Table 9. Serial Control Bus Addresses for IDx

NO.	RATIO V_{R2} / V_{DD18}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	7-BIT ADDRESS	8-BIT ADDRESS
1	0	0	OPEN	Any value less than 100 (1)	0x0C	0x18
2	0.208	0.374	118	30.9	0x0E	0x1C
3	0.323	0.582	107	51.1	0x10	0x20
4	0.440	0.792	113	88.7	0x12	0x24
5	0.553	0.995	82.5	102	0x14	0x28
6	0.668	1.202	68.1	137	0x16	0x2C
7	0.789	1.420	56.2	210	0x18	0x30
8	1	1.8	Any value less than 100 (1)	OPEN	0x1A	0x34

(1) This resistor does not need to be 1% tolerance. 5% is acceptable.

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The serial bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions low while SDA is high. A STOP occurs when SDA transitions high while SCL is also high. See Figure 22.

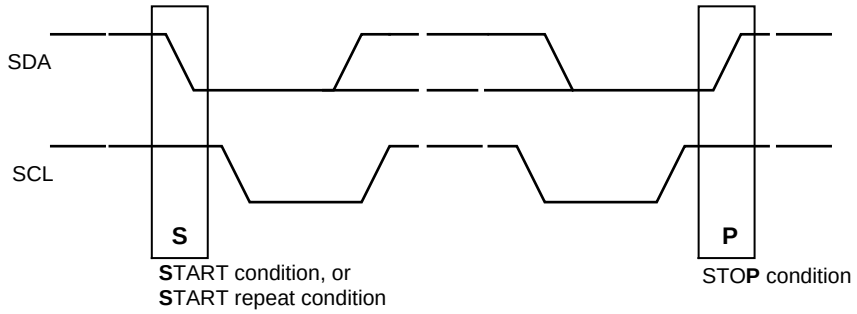

Figure 22. Start and Stop Conditions

To communicate with an I2C slave, the host controller (master) sends data to the slave address and waits for a response. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match a slave address of the device, it not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a Stop condition on the bus. All communication on the bus begins with either a Start condition or a Start-Repeated condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 23 and a WRITE is shown in Figure 24.

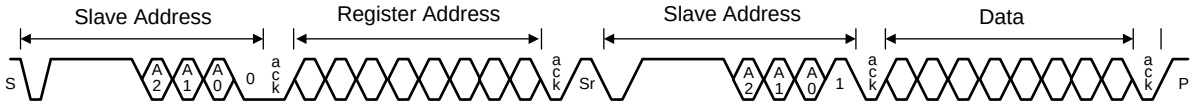

Figure 23. Serial Control Bus — Read

Figure 24. Serial Control Bus — Write

The I2C Master located at the serializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to the *I2C Communication Over FPD-Link III With Bidirectional Control Channel* application note (SNLA131).

7.5.2 Multi-Master Arbitration Support

The Bidirectional Control Channel in the FPD-Link III devices implements I2C-compatible bus arbitration in the proxy I2C master implementation. When sending a data bit, each I2C master senses the value on the SDA line. If the master is sending a logic 1 but senses a logic 0, the master has lost arbitration. It will stop driving SDA and retry the transaction when the bus becomes idle. Thus, multiple I2C masters may be implemented in the system.

Ensure that all I2C masters on the bus support multi-master arbitration.

Assign I2C addresses with more than a single bit set to 1 for all devices on the I2C bus. 0x6A, 0x7B, and 0x37 are some examples of good choices for an I2C address. 0x40 and 0x20 are some examples of bad choices for an I2C address.

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If the system does require master-slave operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available read/write registers in the deserializer to allow masters to communicate with each other to pass control between the two masters. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one master to another.

7.5.3 I2C Restrictions on Multi-Master Operation

The I2C specification does not provide for arbitration between masters under certain conditions. The system should make sure the following conditions cannot occur to prevent in undefined condition on the I2C bus:

- One master generates a Start-Repeated condition while another master is sending a data bit.
- One master generates a Stop condition while another master is sending a data bit.
- One master generates a Start-Repeated condition while another master sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C slave.

7.5.4 Multi-Master Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices, the DS90UB949A-Q1 or DS90UB940-Q1/DS90UB948-Q1 registers may be accessed simultaneously from both local and remote I2C masters. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I2C slaves would still be allowed in only one direction at a time.

7.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices, simultaneous access to serializer or deserializer registers from both local and remote I2C masters may cause incorrect operation, thus restrictions should be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in an read or write error.

Two basic options are recommended. The first is to allow device register access only from one controller. This would allow only the host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer would not be allowed to access the deserializer or serializer registers.

The second basic option is to allow local register access only, with no access to remote serializer or deserializer registers. The host controller would be allowed to access the serializer registers, while a controller at the deserializer could access the deserializer registers only. Access to remote I2C slaves would still be allowed in one direction.

In a very limited case, remote and local access to the deserializer registers could be allowed at the same time. Register access is ensured to work correctly if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the Bidirectional Control Channel from one master to another.

7.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only one direction should be active at any time across the Bidirectional Control Channel. If both directions are required, some method of transferring control between I2C masters should be implemented.

7.5.7 Prevention of I2C Faults During Abrupt System Faults

In rare instances, FPD-Link III back-channel data errors caused by system fault conditions (from example, abrupt power downs of the remote deserializer or cable disconnects) may result in the DS90UB949A-Q1 sending inadvertent I2C transactions on the local I2C bus prior to determining loss of valid back channel signal. To minimize the impact of these types of events:

- Set DS90UB949A-Q1 register 0x16 = 0x02 to minimize the duration of inadvertent I2C events. Any device configuration, including this one, should be written as a part of the Init A sequence as shown in Figure 33
- Ensure all I2C masters on the bus support multi-master arbitration.
- Ensure all I2C masters on the bus support multi-master arbitration:
  - 0x6A, 0x7B, and 0x37 are examples of good choices for an I2C address.
  - 0x40 and 0x20 are examples of bad choices for an I2C address.

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7.6 Register Maps

Table 10. Serial Control Bus Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
0	0x00	I2C Device ID	7:1	RW	Strap	DEVICE_ID	7-bit address of Serializer. Defaults to address configured by the IDx strap pin.
			0	RW	0x00	ID Setting	I2C ID setting. 0: Device I2C address is from IDx strap pin (default). 1: Device I2C address is from 0x00[7:1].
1	0x01	Reset A software I2C reset command issued by writing to register 0x01 is supported only when operating I2C in the 3.3V mode.	7:5		0x00		Reserved.
			4	RW		HDMI Reset	HDMI Digital Reset. Resets the HDMI digital block. This bit is self-clearing. 0: Normal operation. 1: Reset.
			3:2				Reserved.
			1	RW		Digital RESET1	Reset the entire digital block including registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset. Following setting of this bit, software should also set bit 0x4F[1] (BRIDGE_CTL register). This will restore register values that are initially loaded from Non- Volatile Memory to their default state.
			0	RW		Digital RESET0	Reset the entire digital block except registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table. Registers 0x015, 0x18, 0x19, 0x1A, 0x48-0x55, 0xC0, 0xC2, 0xC3, 0xC6, 0xC8, and 0xCE are also restored to their default value when this bit is set.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
3	0x03	General Configuration	7	RW	0xD2	Back channel CRC Checker Enable	Enable/disable back channel CRC Checker. 0: Disable. 1: Enable (default).
			6				***Reserved***.
			5	RW		I2C Remote Write Auto Acknowledge Port0/Port1	Automatically acknowledge I2C remote writes. When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Note: this mode will prevent any NACK from a remote device from reaching the I2C master. 0: Disable (default). 1: Enable. If PORT1_SEL is set, this register controls Port1 operation.
			4	RW		Filter Enable	HS, VS, DE two-clock filter. When enabled, pulses less than two full TMDS clock cycles on the DE, HS, and VS inputs will be rejected. 0: Filtering disable. 1: Filtering enable (default).
			3	RW		I2C Pass-through Port0/Port1	I2C pass-through mode. Read/Write transactions matching any entry in the Slave Alias registers will be passed through to the remote Deserializer. 0: Pass-through disabled (default). 1: Pass-through enabled. If PORT1_SEL is set, this register controls Port1 operation.
			2				***Reserved.***
			1	RW		TMDS Clock Auto	Switch over to internal oscillator in the absence of TMDS Clock. 0: Disable auto-switch. 1: Enable auto-switch (default).
			0				***Reserved.***
4	0x04	Mode Select	7	RW	0x80	Failsafe State	Input failsafe state. 0: Failsafe to High. 1: Failsafe to Low (default).
			6				***Reserved.***
			5	RW		CRC Error Reset	Clear back channel CRC Error counters. This bit is NOT self-clearing. 0: Normal operation (default). 1: Clear counters.
			4	RW		Video gate	This prevents video from being set during the blanking interval. In the DS90UB949, RGB data is not gated with DE by default. However, to enable packetized audio in DS90UB949, this bit must be set. 1: Gate RGB data with DE in DS90UB949 0: Pass RGB data independent of DE in DS90UB949
			3:0				Reserved.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
5	0x05	I2C Control	7:5		0x00		***Reserved.***
			4:3	RW		SDA Output Delay	Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns (default). 01: 280ns. 10: 320ns. 11: 360ns.
			2	RW		Local Write Disable	Disable remote writes to local registers. Setting this bit to 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer. 0: Enable (default). 1: Disable.
			1	RW		I2C Bus Timer Speedup	Speed up I2C bus Watchdog Timer. 0: Watchdog Timer expires after approximately 1s (default). 1: Watchdog Timer expires after approximately 50µs.
			0	RW		I2C Bus Timer Disable	Disable I2C bus Watchdog Timer. The I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1s, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 0: Enable (default). 1: Disable.
6	0x06	DES ID	7:1	RW	0x00	DES Device ID Port0/Port1	7-bit I2C address of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates the Deserializer Device ID for the Deserializer attached to Port1.
			0	RW		Freeze Device ID Port0/Port1	Freeze Deserializer Device ID. 1: Prevents auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. 0: Allows auto-loading of the Deserializer Device ID from the Bidirectional Control Channel. If PORT1_SEL is set, this register is with reference to Port1.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
7	0x07	Slave ID[0]	7:1	RW	0x00	Slave ID 0 Port0/Port1	7-bit I2C address of the remote Slave 0 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 0. If PORT1_SEL is set, this register is with reference to Port1.
			0				***Reserved.***
8	0x08	Slave Alias[0]	7:1	RW	0x00	Slave Alias ID 0 Port0/Port1	7-bit Slave Alias ID of the remote Slave 0 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 0 register. A value of 0 in this field disables access to the remote Slave 0. If PORT1_SEL is set, this register is with reference to Port1.
			0				***Reserved.***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB Port0/Port1	Number of back channel CRC errors – 8 least significant bits. Cleared by 0x04[5]. If PORT1_SEL is set, this register is with reference to Port1.
11	0x0B		7:0	R	0x00	CRC Error MSB Port0/Port1	Number of back channel CRC errors – 8 most significant bits. Cleared by 0x04[5]. If PORT1_SEL is set, this register is with reference to Port1.
12	0x0C	General Status	7:5				***Reserved.***
			4		0x00	Link Lost Port0/Port1	Link lost flag for selected port: This bit indicates that loss of link has been detected. This register bit will stay high until cleared using the CRC Error Reset in register 0x04. If PORT1_SEL is set, this register is with reference to Port1.
			3	R		BIST CRC Error Port0/Port1	Back channel CRC error(s) during BIST communication with Deserializer. This bit is cleared upon loss of link, restart of BIST, or assertion of CRC Error Reset bit in 0x04[5]. 0: No CRC errors detected during BIST. 1: CRC error(s) detected during BIST. If PORT1_SEL is set, this register is with reference to Port1.
			2	R		TMDS Clock Detect	Pixel clock status: 0: Valid clock not detected at HDMI input. 1: Valid clock detected at HDMI input.
			1	R		DES Error Port0/Port1	CRC error(s) during normal communication with Deserializer. This bit is cleared upon loss of link or assertion of 0x04[5]. 0: No CRC errors detected. 1: CRC error(s) detected. If PORT1_SEL is set, this register is with reference to Port1.
			0	R		Link Detect Port0/Port1	Link detect status: 0: Cable link not detected. 1: Cable link detected. If PORT1_SEL is set, this register is with reference to Port1.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
13	0x0D	GPIO0 Configuration	7:4	R		Revision ID	Revision ID.
			3	RW	0x00	GPIO0 Output Value D_GPIO0 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH. If PORT1_SEL is set, this register controls the D_GPIO0 pin.
			2:0	RW		GPIO0 Mode D_GPIO0 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss. If PORT1_SEL is set, this register controls the D_GPIO0 pin.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
14	0x0E	GPIO1 and GPIO2 ConfigurationD_ GPIO1 and D_GPIO2 Configuration	7	RW	0x00	GPIO2 Output Value D_GPIO2 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH. If PORT1_SEL is set, this register controls the D_GPIO2 pin.
			6:4	RW		GPIO2 Mode D_GPIO2 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss. If PORT1_SEL is set, this register controls the D_GPIO2 pin.
			3	RW		GPIO1 Output Value D_GPIO1 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH. If PORT1_SEL is set, this register controls the D_GPIO1 pin.
			2:0	RW		GPIO1 Mode D_GPIO1 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss. If PORT1_SEL is set, this register controls the D_GPIO1 pin.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
15	0x0F	GPIO3 Configuration D_GPIO3 Configuration	7:4		0x00		***Reserved.***
			3	RW		GPIO3 Output Value D_GPIO3 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH. If PORT1_SEL is set, this register controls the D_GPIO3 pin.
			2:0	RW		GPIO3 Mode D_GPIO3 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE™. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss. If PORT1_SEL is set, this register controls the D_GPIO3 pin.
16	0x10	GPIO5_REG and GPIO6_REG Configuration	7	RW	0x00	GPIO6_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO6_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE™. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO5_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO5_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE™. 01: GPIO mode, output. 11: GPIO mode; input.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
17	0x11	GPIO7_REG and GPIO8_REG Configuration	7	RW	0x00	GPIO8_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO8_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO7_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO7_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
18	0x12	Data Path Control	7		0x00		***Reserved.***
			6	RW		Pass RGB	Setting this bit causes RGB data to be sent independent of DE. 0: Normal operation. 1: Pass RGB independent of DE.
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low). 1: DE is inverted (active low, idle high).
			4	RW		I2S Repeater Regen	Regenerate I2S data from Repeater I2S pins. 0: Repeater pass through I2S from video pins (default). 1: Repeater regenerate I2S from I2S pins.
			3	RW		I2S Channel B Enable Override	I2S Channel B Enable Override. 0: Disable I2S Channel B override. 1: Set I2S Channel B Enable from 0x12[0].
			2	RW		18-Bit Video Select	0: Select 24-bit video mode. 1: Select 18-bit video mode.
			1	RW		I2S Transport Select	Select I2S transport mode: 0: Enable I2S Data Island transport (default). 1: Enable I2S Data Forward Channel Frame transport.
			0	RW		I2S Channel B Enable	I2S Channel B Enable. 0: I2S Channel B disabled. 1: Enable I2S Channel B on B1 input. Note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
19	0x13	General Purpose Control	7	R	0x88	MODE_SEL1 Done	Indicates MODE_SEL1 value has stabilized and has been latched.
			6:4	R		MODE_SEL1 Decode	Returns the 3-bit decode of the MODE_SEL1 pin. 000: mode1 001: mode2 010: mode3 011: mode4 100: mode5 101: mode6 110: mode7 111: mode8 See Table 8
			3	R		MODE_SEL0 Done	Indicates MODE_SEL0 value has stabilized and has been latched.
			2:0	R		MODE_SEL0 Decode	Returns the 3-bit decode of the MODE_SEL0 pin. 000: mode1 001: mode2 010: mode3 011: mode4 See Table 7
20	0x14	BIST Control	7:3		0x00		***Reserved.***
			2:1	RW		OSC Clock Source	Allows choosing different OSC clock frequencies for forward channel frame. OSC clock frequency in functional mode when TMDS clock is not present and 0x03[2]=1: 00: 50 MHz oscillator. 01: 50 MHz oscillator. 10: 100 MHz oscillator. 11: 25 MHz oscillator.
							Clock source in BIST mode i.e. when 0x14[0]=1: 00: External pixel clock. 01: 33 MHz oscillator. 1x: 100 MHz oscillator.
			0	RW		BIST Enable	BIST control: 0: Disabled (default). 1: Enabled.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
21	0x15	I2C Voltage Select	7:0	RW	0x01	I2C Voltage Select	Selects 1.8 or 3.3 V for the I2C_SDA and I2C_SCL pins. This register is loaded from the I2C_VSEL strap option from the SCLK pin at power-up. At power-up, a logic LOW will select 3.3 V operation, while a logic HIGH (pull-up resistor attached) will select 1.8 V signaling. Issuing either of the digital resets via register 0x01 will cause the I2C_VSEL value to be reset to 3.3V operation. Reads of this register return the status of the I2C_VSEL control: 0: Select 1.8 V signaling. 1: Select 3.3 V signaling. This bit may be overwritten via register access or via eFuse program by writing an 8-bit value to this register: Write 0xb5 to set I2C_VSEL. Write 0xb6 to clear I2C_VSEL.
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0. Set to at least 1 or greater.
			0	RW		Timer Control	Disable Bidirectional Control Channel (BCC) Watchdog Timer: 0: Enable BCC Watchdog Timer operation (default). 1: Disable BCC Watchdog Timer operation.
23	0x17	I2C Control	7	RW	0x1E	I2C Pass All Port0/Port1	0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID (default). 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID. If PORT1_SEL is set, this bit controls Port1 operation.
			6:4	RW		SDA Hold Time	Internal SDA hold time: Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.
24	0x18	SCL High Time	7:0	RW	0x7F	TX_SCL_HIGH	I2C Master SCL high time: This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25 MHz rather than the nominal 25 MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952ns * (TX_SCL_HIGH + 5).

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
25	0x19	SCL Low Time	7:0	RW	0x7F	TX_SCL_LOW	I2C Master SCL low time: This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25 MHz rather than the nominal 25 MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952ns * (TX_SCL_LOW + 5).
26	0x1A	Data Path Control 2	7:4				***Reserved.***
			3	R	Strap	SECONDARY _AUDIO	Enable Secondary Audio. This register indicates that the AUX audio channel is enabled. The control for this function is via the AUX_AUDIO bit in the BRIDGE_CFG register offset 0x54). The AUX_AUDIO control is strapped from the MODE_SEL0 pin at power-up.
			2		0x01		Reserved.
			1	RW		MODE_28B	Enable 28-bit Serializer Mode. 0: 24-bit high-speed data + 3 low-speed control (DE, HS, VS). 1: 28-bit high-speed data mode.
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport: 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0. 1: 5.1- or 7.1-channel audio is enabled. Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection (default).
27	0x1B	BIST BC Error Count	7:0	R	0x00	BIST BC Error Port0/Port1	BIST back channel CRC error counter. This register stores the back channel CRC error count during BIST Mode (saturates at 255 errors). Clears when a new BIST is initiated or by 0x04[5]. If PORT1_SEL is set, this register indicates Port1 status.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
28	0x1C	GPIO Pin Status 1	7	R	0x00	GPIO7_REG Pin Status	GPIO7_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			6	R		GPIO6_REG Pin Status	GPIO6_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			5	R		GPIO5_REG Pin Status	GPIO5_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			4				***Reserved.***
			3	R		GPIO3 Pin Status D_GPIO3 Pin Status	GPIO3 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO3 input pin status.
			2	R		GPIO2 Pin Status D_GPIO2 Pin Status	GPIO2 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO2 input pin status.
			1	R		GPIO1 Pin Status D_GPIO1 Pin Status	GPIO1 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO1 input pin status.
			0	R		GPIO0 Pin Status D_GPIO0 Pin Status	GPIO0 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO0 input pin status.
29	0x1D	GPIO Pin Status 2	7:1		0x00		***Reserved***
			0	R		GPIO8_REG Pin Status	GPIO8_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
30	0x1E	Transmitter Port Select	7:3				Reserved.
			2	RW	0x01	PORT1_I2C_EN	Port1 I2C Enable. Enables secondary I2C address. The second I2C address provides access to Port1 registers as well as registers that are shared between Port0 and Port1. The second I2C address value will be set to DeviceID + 1 (7-bit format). The PORT1_I2C_EN bit must also be set to allow accessing remote devices over the second link when the device is in Replicate mode.
			1	RW		PORT1_SEL	Selects Port1 for register access from primary I2C address. For writes, Port1 registers and shared registers will both be written. For reads, Port1 registers and shared registers will be read. This bit must be cleared to read Port0 registers. This bit is ignored if PORT1_I2C_EN is set.
			0	RW		PORT0_SEL	Selects Port0 for register access from primary I2C address. For writes, Port0 registers and shared registers will both be written. For reads, Port0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then Port1 registers will be read. This bit is ignored if PORT1_I2C_EN is set.
31	0x1F	Frequency Counter	7:0	RW	0x00	Frequency Count	Frequency counter control. A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 40ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
32	0x20	Deserializer Capabilities 1	7	RW	0x00	FREEZE_DES_CAP Port0/Port1	Freeze Deserializer Capabilities. Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21. If PORT1_SEL is set, this register indicates Port1 capabilities.
			6	RW	0x00	HSCC_MODE[0] Port0/Port1	High-Speed Control Channel bit 0. Lowest bit of the 3-bit HSCC indication. The other 2 bits are contained in Deserializer Capabilities 2. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
			5			SEND_FREQ Port0/Port1	Send Frequency Training Pattern. Indicates the should send the Frequency Training Pattern. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
			4	RW	0x00	SEND_EQ Port0/Port1	Send Equalization Training Pattern. Indicates the should send the Equalization Training Pattern. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
			3	RW		DUAL_LINK_CAP Port0/Port1	Dual link Capabilities. Indicates if the Deserializer is capable of dual link operation. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
			2	RW		DUAL_CHANNEL Port0/Port1	Dual Channel 0/1 Indication. In a dual-link capable device, indicates if this is the primary or secondary channel. 0: Primary channel (channel 0). 1: Secondary channel (channel 1). This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
32	0x20	Deserializer Capabilities 1	1	RW	0x00	VID_24B_HD_AUD Port0/Port1	Deserializer supports 24-bit video concurrently with HD audio. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
			0	RW		DES_CAP_FC_GPIO Port0/Port1	Deserializer supports GPIO in the Forward Channel Frame. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this register indicates Port1 capabilities.
33	0x21	Deserializer Capabilities 2	7:2				Reserved.
			1:0	RW	0x00	HSCC_MODE[2:1] Port0/Port1	High-Speed Control Channel bits [2:1]. Upper bits of the 3-bit HSCC indication. The lowest bit is contained in Deserializer Capabilities 1. 000: Normal back channel frame, GPIO mode. 001: High Speed GPIO mode, 1 GPIO. 010: High Speed GPIO mode, 2 GPIOs. 011: High Speed GPIO mode: 4 GPIOs. 100: Reserved. 101: Reserved. 110: High Speed, Forward Channel SPI mode. 111: High Speed, Reverse Channel SPI mode. In Single Link devices, only Normal back channel frame modes are supported. If PORT1_SEL is set, this register indicates Port1 capabilities.
38	0x26	Link Detect Control	7:3				Reserved.
			2:0	RW	0x00	LINK DETECT TIMER	Bidirectional Control Channel Link Detect Timer. This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 000: 162 microseconds. 001: 325 microseconds. 010: 650 microseconds. 011: 1.3 milliseconds. 100: 10.25 microseconds. 101: 20.5 microseconds. 110: 41 microseconds. 111: 82 microseconds.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
48	0x30	SCLK_CTRL	7	RW	0x00	SCLK/WS	SCLK to Word Select Ratio. 0 : 64. 1 : 32.
			6:5	RW		MCLK/SCLK	MCLK to SCLK Select Ratio. 00 : 4. 01 : 2. 10 : 1. 11 : 8.
			4:3	RW		CLEAN CLOCK_DIV	Clock Cleaner divider. 00 : FPD_VCO_CLOCK/8. 01 : FPD_VCO_CLOCK/4. 10 : FPD_VCO_CLOCK/2. 11 : AON_OSC.
			2:1	RW		CLEAN Mode	If non-zero, the SCLK Input or HDMI N generated Audio Clock is cleaned digitally before being used. 00 : Off. 01 : ratio of 1. 10 : ratio of 2. 11 : ratio of 4.
			0	RW		MASTER	If set, the SCLK I/O and the WS_IO are used as an output and the Clock Generation Circuits are enabled, otherwise they are inputs.
49	0x31	AUDIO_CTS0	7:0	RW	0x00	CTS[7:0]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
50	0x32	AUDIO_CTS1	7:0	RW	0x00	CTS[15:8]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
51	0x33	AUDIO_CTS2	7:0	RW	0x00	CTS[23:16]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
52	0x34	AUDIO_N0	7:0	RW	0x00	N[7:0]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
53	0x35	AUDIO_N1	7:0	RW	0x00	N[15:8]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
54	0x36	AUDIO_N2_COEFF	7:4	RW	0x00	COEFF[3:0]	Selects the LPF_COEFF in the Clock Cleaner (Feedback is divided by 2^COEFF).
			3:0	RW	0x00	N[19:16]	If non-zero, the CTS value is used to generate a new clock from the PFD PLLs VCO.
55	0x37	CLK_CLEAN_STS	7:6				Reserved.
			5:3	R	0x00	IN_FIFO_LVL	Clock Cleaner Input FIFO Level.
			2:0	R	0x00	OUT_FIFO_LVL	Clock Cleaner Output FIFO Level.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
64	0x40	ANA_IA_CTL	7:5	RW			Reserved
			4:2	RW	0x00	ANA_IA_SEL (Analog Indirect Select)	Analog Register Select: Selects target for register access 000 : Disabled 001 : HDMI Channel 0 Registers 010 : HDMI Channel 1 Registers 011 : HDMI Channel 2 Registers 100 : HDMI Share Registers 101 : FPD3 TX Registers 110 : Simultaneous access to HDMI Channel 0-2 registers
			1	RW		ANA_AUTO_INC (Analog Indirect Increment)	Analog Register Auto Increment: Enables auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1
			0	RW		ANA_IA_READ (Analog Indirect Read)	Start Analog Register Read: Setting this allows generation of a read strobe to the analog block upon setting of the ANA_IA_ADDR register. In auto-increment mode, read strobes will also be asserted following a read of the ANA_IA_DATA register. This function is only required for analog blocks that need to pre-fetch register data.
65	0x41	ANA_IA_ADDR	7:0	RW	0x00	ANA_IA_ADDR Analog Indirect Address)	Analog Register Offset: This register contains the 8-bit register offset for the indirect access.
66	0x42	ANA_IA_DATA	7:0	RW	0x00	ANA_IA_DATA (Analog Indirect Data)	Analog Register Data: Writing this register will cause an indirect write of the ANA_IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register
72	0x48	APB_CTL	7:5				Reserved.
			4:3	RW	0x00	APB_SELECT	APB Select: Selects target for register access. 00 : HDMI APB interface. 01 : EDID SRAM. 10 : Configuration Data (read only). 11 : Die ID (read only).
			2	RW		APB_AUTO_INC	APB Auto Increment: Enables auto-increment mode. Upon completion of an APB read or write, the APB address will automatically be incremented by 0x4 for HDMI registers or by 0x1 for others.
			1	RW		APB_READ	Start APB Read: Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATAx registers. The APB_ADRx registers should be programmed prior to setting this bit. This bit will be cleared when the read is complete.
			0	RW		APB_ENABLE	APB Interface Enable: Set to a 1 to enable the APB interface. The APB_SELECT bits indicate what device is selected.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
73	0x49	APB_ADR0	7:0	RW	0x00	APB_ADR0	APB Address byte 0 (LSB).
74	0x4A	APB_ADR1	7:0	RW	0x00	APB_ADR1	APB Address byte 1 (MSB).
75	0x4B	APB_DATA0	7:0	RW	0x00	APB_DATA0	Byte 0 (LSB) of the APB Interface Data.
76	0x4C	APB_DATA1	7:0	RW	0x00	APB_DATA1	Byte 1 of the APB Interface Data.
77	0x4D	APB_DATA2	7:0	RW	0x00	APB_DATA2	Byte 2 of the APB Interface Data.
78	0x4E	APB_DATA3	7:0	RW	0x00	APB_DATA3	Byte 3 (MSB) of the APB Interface Data.
79	0x4F	BRIDGE_CTL	7:5				Reserved.
			4	RW	0x00	CEC_CLK_SRC	CEC Clock Source Select: Selects clock source for generating the 32.768 KHz clock for CEC operations in the HDMI Receive Controller. 0 : Selects internal generated clock. 1 : Selects external 25 MHz oscillator clock.
			3	RW		CEC_CLK_EN	CEC Clock Enable: Enable CEC clock generation. Enables generation of the 32.768 KHz clock for the HDMI Receive controller. This bit should be set prior to enabling CEC operation via the HDMI controller registers.
			2	RW		EDID_CLEAR	Clear EDID SRAM: Set to 1 to enable clearing the EDID SRAM. The EDID_INIT bit must be set at the same time for the clear to occur. This bit will be cleared when the initialization is complete.
			1	RW		EDID_INIT	Initialize EDID SRAM from EEPROM: Causes a reload of the EDID SRAM from the non-volatile EDID EEPROM. This bit will be cleared when the initialization is complete.
			0	R	Strap	EDID_DISABLE	Disable EDID access via DDC/I2C: Disables access to the EDID SRAM via the HDMI DDC interface. This value is loaded from the MODE_SEL0 pin at power-up.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
80	0x50	BRIDGE_STS	7	R	0x03	RX5V_DETECT	RX +5V detect: Indicates status of the RX_5V pin. When asserted, indicates the HDMI interface has detected valid voltage on the RX_5V input.
			6	R		HDMI_INT	HDMI Interrupt Status: Indicates an HDMI Interrupt is pending. HDMI interrupts are serviced through the HDMI Registers via the APB Interface.
			5				Reserved.
			4	R		INIT_DONE	Initialization Done: Initialization sequence has completed. This step will complete after configuration complete (CFG_DONE).
			3	R		REM_EDID_LOAD	Remote EDID Loaded: Indicates EDID SRAM has been loaded from a remote EDID EEPROM device over the Bidirectional Control Channel. The EDID_CKSUM value indicates if the EDID load was successful.
			2	R		CFG_DONE	Configuration Complete: Indicates automatic configuration has completed. This step will complete prior to initialization complete (INIT_DONE).
			1	R		CFG_CKSUM	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2's complement checksum in the last 128 bytes of the EEPROM. A value of 1 indicates the checksum passed.
			0	R		EDID_CKSUM	EDID checksum Status: Indicates result of EDID checksum during EDID initialization. The device verifies the 2's complement checksum in the first 256 bytes of the EEPROM. A value of 1 indicates the checksum passed.
81	0x51	EDID_ID	7:1	RW	0x50	EDID_ID	EDID I2C Slave Address: I2C address used for accessing the EDID information. These are the upper 7 bits in 8-bit format addressing, where the lowest bit is the Read/Write control.
			0	RW	0	EDID_RDONLY	EDID Read Only: Set to a 1 puts the EDID SRAM memory in read-only mode for access via the HDMI DDC interface. Setting to a 0 allows writes to the EDID SRAM memory.
82	0x52	EDID_CFG0	7				Reserved.
			6:4	RW	0x01	EDID_SDA_HOLD	Internal SDA Hold Time: This field configures the amount of internal hold time provided for the DDC_SDA input relative to the DDC_SCL input. Units are 40 nanoseconds. The hold time is used to qualify the start detection to avoid false detection of Start or Stop conditions.
			3:0	RW	0x0E	EDID_FLTR_DPTH	I2C Glitch Filter Depth: This field configures the maximum width of glitch pulses on the DDC_SCL and DDC_SDA inputs that will be rejected. Units are 5 nanoseconds.
83	0x53	EDID_CFG1	7:2				Reserved.
			1:0	RW	0x00	EDID_SDA_DLY	SDA Output Delay: This field configures output delay on the DDC_SDA output when the EDID memory is accessed. Setting this value will increase output delay in units of 40ns. Nominal output delay values for DDC_SCL to DDC_SDA are: 00 : 240ns. 01 : 280ns. 10 : 320ns. 11 : 360ns.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
84	0x54	BRIDGE_CFG	7	RW	Strap	EXT_CTL	External Control: When this bit Is set, the internal bridge control function is disabled. This disables initialization of the HDMI Receiver. These operations must be controlled by an external controller attached to the I2C interface. This value is loaded from the MODE_SEL1 pin at power-up.
			6	RW	0x00	HDMI_INT_EN	HDMI Interrupt Enable: When this bit is set, Interrupts from the HDMI Receive controller will be reported on the INTB pin. Software may check the BRIDGE_STS register to determine if the interrupt is from the HDMI Receiver.
			5	RW	Strap	DIS_REM_EDID	Disable Remote EDID load: Disables automatic load of EDID SRAM from a remote EDID EEPROM. By default, the device will check the remote I2C bus for an EEPROM with a valid EDID, and load the EDID data to local EDID SRAM. If this bit is set to a 1, the remote EDID load will be bypassed. This value is loaded from the MODE_SEL1 pin at power-up.
			4	RW	0x00	AUTO_INIT_DIS	Disable Automatic initialization: The Bridge control will automatically initialize the HDMI Receiver for operation. Setting this bit to a 1 will disable automatic initialization of the HDMI Receiver. In this mode, initialization of the HDMI Receiver must be done through EEPROM configuration or via external control.
			3				Reserved.
			2	RW	0x00	AUDIO_TDM	Enable TDM Audio: Setting this bit to a 1 will enable TDM audio for the HDMI audio.
			1	RW		AUDIO_MODE	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0 : HDMI audio. 1 : Local/DVI audio. Local audio is sourced from the device I2S pins rather than from HDMI, and is useful in modes such as DVI that do not include audio.
			0	RW	Strap	AUX_AUDIO_EN	AUX Audio Channel Enable: Setting this bit to a 1 will enable the AUX audio channel. This allows sending additional 2-channel audio in addition to the HDMI or DVI audio. This bit is loaded from the MODE_SEL0 pin at power-up.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
85	0x55	AUDIO_CFG	7	RW	0x00	TDM_2_PARALLEL	Enable I2S TDM to parallel audio conversion: When this bit is set, the I2S TDM to parallel conversion module is enabled. The clock output from the I2S TDM to parallel conversion module is them used to send data to the deserializer.
			6	RW		HDMI_I2S_OUT	HDMI Audio Output Enable: When this bit is set, the HDMI I2S audio data will be output on the I2S audio interface pins. This control is ignored if the BRIDGE_CFG:AUDIO_MODE is not set to 00 (HDMI audio only).
			5:4				Reserved.
			3	RW	0x0C	RST_ON_TYPE	Reset Audio FIFO on Type Change: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio type.
			2	RW		RST_ON_AIF	Reset Audio FIFO on Audio Infoframe: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Infoframe checksum.
			1	RW		RST_ON_AVI	Reset Audio FIFO on Audio Video Information Infoframe: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Video Information Infoframe checksum.
			0	RW		RST_ON_ACR	Reset Audio FIFO on Audio Control Frame: When this bit is set, the internal bridge control function will reset the HDMI Audio FIFO on a change in the Audio Control Frame N or CTS fields.
90	0x5A	DUAL_STS	7	R	0x00	FPD3_LINK_RDY	This bit indicates that the FPD-Link III has detected a valid downstream connection and determined capabilities for the downstream link.
			6	R		FPD3_TX_STS	FPD-Link III transmit status: This bit indicates that the FPD-Link III transmitter is active and the receiver is LOCKED to the transmit clock. It is only asserted once a valid input has been detected, and the FPD-Link III transmit connection has entered the correct mode (Single vs. Dual mode).
			5:4	R		FPD3_PORT_STS	FPD3 Port Status: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 00: Dual FPD-Link III Transmitter mode. 01: Single FPD-Link III Transmit on port 0. 10: Single FPD-Link III Transmit on port 1. 11: Replicate FPD-Link III Transmit on both ports.
			3	R		TMDS_VALID	HDMI TMDS Valid: This bit indicates the TMDS interface is recovering valid TMDS data from HDMI.
			2	R		HDMI_PLL_LOCK	HDMI PLL lock status: Indicates the HDMI PLL has locked to the incoming HDMI clock.
			1	R		NO_HDMI_CLK	No HDMI Clock Detected: This bit indicates the Frequency Detect circuit did not detect an HDMI clock greater than the value specified in the FREQ_LOW register.
			0	R		FREQ_STABLE	HDMI Frequency is Stable: Indicates the Frequency Detection circuit has detected a stable HDMI clock frequency.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
91	0x5B	DUAL_CTL1	7	RW	Strap	FPD3_COAX_MODE	FPD3 Coax Mode: Enables configuration for the FPD3 Interface cabling type. 0 : Twisted Pair. 1 : Coax This bit is loaded from the MODE_SEL1 pin at power-up.
			6	RW	0	DUAL_SWAP	Dual Swap Control: Indicates current status of the Dual Swap control. If automatic correction of Dual Swap is disabled via the DISABLE_DUAL_SWAP control, this bit may be modified by software.
			5	RW	1	RST_PLL_FREQ	Reset FPD3 PLL on Frequency Change: When set to a 1, frequency changes detected by the Frequency Detect circuit will result in a reset of the FPD3 PLL. Set to 0.
			4	RW	0	FREQ_DET_PLL	Frequency Detect Select PLL Clock: Determines the clock source for the Frequency detection circuit: 0 : HDMI clock (prior to PLL). 1: HDMI PLL clock.
			3	RW	0	DUAL_ALIGN_DE	Dual align on DE (valid in dual-link mode): 0: Data will be sent on alternating links without regard to odd/even pixel position. 1: Odd/Even data will be sent on the primary/secondary links, respectively, based on the assertion of DE.
			2	RW	0	DISABLE_DUAL	Disable Dual Mode: During Auto-detect operation, setting this bit to a 1 will disable Dual FPD-Link III operation. 0: Normal Auto-detect operation. 1: Only Single or Replicate operation supported. This bit will have no effect if FORCE_LINK is set.
			1	RW	0	FORCE_DUAL	Force dual mode: When FORCE_LINK bit is set, the value on this bit controls single versus dual operation: 0: Single FPD-Link III Transmitter mode. 1: Dual FPD-Link III Transmitter mode.
			0	RW	0	FORCE_LINK	Force Link Mode: Forces link to dual or single mode, based on the FORCE_DUAL control setting. If this bit is 0, mode setting will be automatically set based on downstream device capabilities as well as the incoming data frequency. 0 : Auto-Detect FPD-Link III mode. 1 : Forced Single or Dual FPD-Link III mode.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
92	0x5C	DUAL_CTL2	7	RW	0	DISABLE_DUAL_SWAP	Disable Dual Swap: Prevents automatic correction of swapped Dual link connection. Setting this bit allows writes to the DUAL_SWAP control in the DUAL_CTL1 register.
			6	RW	0x00	FORCE_LINK_RDY	Force Link Ready: Forces link ready indication, bypassing back channel link detection.
			5	RW		FORCE_CLK_DET	Force Clock Detect: Forces the HDMI/OpenLDI clock detect circuit to indicate presence of a valid input clock. This bypasses the clock detect circuit, allowing operation with an input clock that does not meet frequency or stability requirements.
			4:3	RW		FREQ_STBL_THR	Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 40us. 01 : 80us. 10 : 320us. 11 : 1.28ms.
			2:0	RW	0x02	FREQ_HYST	Frequency Detect Hysteresis: The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
93	0x5D	FREQ_LOW	7				Reserved.
			6	RW	0	HDMI_RST_MODE	HDMI Phy Reset Mode: 0 : Reset HDMI Phy on change in mode or frequency. 1 : Don't reset HDMI Phy on change in mode or frequency if +5V is asserted.
			5:0	RW	6	FREQ_LO_THR	Frequency Low Threshold: Sets the low threshold for the HDMI Clock frequency detect circuit in MHz. This value is used to determine if the HDMI clock frequency is too low for proper operation.
94	0x5E	FREQ_HIGH	7				Reserved.
			6:0	RW	44	FREQ_HI_THR	Frequency High Threshold: Sets the high threshold for the HDMI Clock frequency detect circuit in MHz.
95	0x5F	HDMI Frequency	7:0	R	0x00	HDMI_FREQ	HDMI frequency: Returns the value of the HDMI frequency in MHz. A value of 0 indicates the HDMI receiver is not detecting a valid signal.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
96	0x60	SPI_TIMING1	7:4	RW	0x02	SPI_HOLD	SPI Data Hold from SPI clock: These bits set the minimum hold time for SPI data following the SPI clock sampling edge. In addition, this also sets the minimum active pulse width for the SPI output clock. 0: Do not use. 0x1-0xF: Hold = (SPI_HOLD + 1) * 40ns. For example, default setting of 2 will result in 120ns data hold time.
			3:0	RW	0x02	SPI_SETUP	SPI Data Setup to SPI Clock: These bits set the minimum setup time for SPI data to the SPI clock active edge. In addition, this also sets the minimum inactive width for the SPI output clock. 0: Do not use. 0x1-0xF: Hold = (SPI_SETUP + 1) * 40ns. For example, default setting of 2 will result in 120ns data setup time.
97	0x61	SPI_TIMING2	7:4				Reserved.
			3:0	RW	0x00	SPI_SS_SETUP	SPI Slave Select Setup: This field controls the delay from assertion of the Slave Select low to initial data timing. Delays are in units of 40ns. Delay = (SPI_SS_SETUP + 1) * 40ns.
98	0x62	SPI_CONFIG	7:2				Reserved.
			1	R	0x00	SPI_CPHA	SPI Clock Phase setting: Determines which phase of the SPI clock is used for sampling data. 0: Data sampled on leading (first) clock edge. 1: Data sampled on trailing (second) clock edge. This bit is read-only, with a value of 0. There is no support for CPHA of 1.
			0	RW		SPI_CPOL	SPI Clock Polarity setting: Determines the base (inactive) value of the SPI clock. 0: base value of the clock is 0. 1: base value of the clock is 1. This bit affects both capture and propagation of SPI signals.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted. 0000: Checkerboard. 0001: White/Black (default). 0010: Black/White. 0011: Red/Cyan. 0100: Green/Magenta. 0101: Blue/Yellow. 0110: Horizontal Black-White/White-Black. 0111: Horizontal Black-Red/White-Cyan. 1000: Horizontal Black-Green/White-Magenta. 1001: Horizontal Black-Blue/White-Yellow. 1010: Vertical Black-White/White-Black. 1011: Vertical Black-Red/White-Cyan. 1100: Vertical Black-Green/White-Magenta. 1101: Vertical Black-Blue/White-Yellow. 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers. 1111: VCOM. See TI App Note AN-2198.
			3				***Reserved.***
			2	RW		Color Bars Pattern	Enable color bars: 0: Color Bars disabled (default). 1: Color Bars enabled. Overrides the selection from reg_0x64[7:4].
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern: 0: Color sequence from top left is (YCBR) (default). 1: Color sequence from top left is (RBCY).
			0	RW		Pattern Generator Enable	Pattern Generator enable: 0: Disable Pattern Generator (default). 1: Enable Pattern Generator.

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
101	0x65	Pattern Generator Configuration	7		0x00		***Reserved.***
			6	RW		Checkerboard Scale	Scale Checkered Patterns: 0: Normal operation (each square is 1x1 pixel) (default). 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels). Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color: 0: Use white and black in the Checkerboard pattern (default). 1: Use the Custom Color and black in the Checkerboard pattern.
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness (default). 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default). 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: The Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals (default). 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. See TI App Note AN-2198.
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output (default). 1: Invert the color output. See TI App Note AN-2198.
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern (default). 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note AN-2198.
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note AN-2198

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
112	0x70	Slave ID[1]	7:1	RW	0x00	Slave ID 1 Port0/Port1	7-bit I2C address of the remote Slave 1 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 1. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
113	0x71	Slave ID[2]	7:1	RW	0x00	Slave ID 2 Port0/Port1	7-bit I2C address of the remote Slave 2 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 2. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
114	0x72	Slave ID[3]	7:1	RW	0x00	Slave ID 3 Port0/Port1	7-bit I2C address of the remote Slave 3 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 3. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
115	0x73	Slave ID[4]	7:1	RW	0x00	Slave ID 4 Port0/Port1	7-bit I2C address of the remote Slave 4 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 4. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
116	0x74	Slave ID[5]	7:1	RW	0x00	Slave ID 5 Port0/Port1	7-bit I2C address of the remote Slave 5 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 5. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
117	0x75	Slave ID[6]	7:1	RW	0x00	Slave ID 6 Port0/Port1	7-bit I2C address of the remote Slave 6 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 6. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
118	0x76	Slave ID[7]	7:1	RW	0x00	Slave ID 7 Port0/Port1	7-bit I2C address of the remote Slave 7 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 7. If PORT1_SEL is set, this register controls Port 1 Slave ID.
			0				***Reserved.***
119	0x77	Slave Alias[1]	7:1	RW	0x00	Slave Alias ID 1 Port0/Port1	7-bit Slave Alias ID of the remote Slave 1 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 1 register. A value of 0 in this field disables access to the remote Slave 1. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
120	0x78	Slave Alias[2]	7:1	RW	0x00	Slave Alias ID 2 Port0/Port1	7-bit Slave Alias ID of the remote Slave 2 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 2 register. A value of 0 in this field disables access to the remote Slave 2. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
121	0x79	Slave Alias[3]	7:1	RW	0x00	Slave Alias ID 3 Port0/Port1	7-bit Slave Alias ID of the remote Slave 3 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 3 register. A value of 0 in this field disables access to the remote Slave 3. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
122	0x7A	Slave Alias[4]	7:1	RW	0x00	Slave Alias ID 4 Port0/Port1	7-bit Slave Alias ID of the remote Slave 4 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 4 register. A value of 0 in this field disables access to the remote Slave 4. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
123	0x7B	Slave Alias[5]	7:1	RW	0x00	Slave Alias ID 5 Port0/Port1	7-bit Slave Alias ID of the remote Slave 5 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 5 register. A value of 0 in this field disables access to the remote Slave 5. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
124	0x7C	Slave Alias[6]	7:1	RW	0x00	Slave Alias ID 6 Port0/Port1	7-bit Slave Alias ID of the remote Slave 6 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 6 register. A value of 0 in this field disables access to the remote Slave 6. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***

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Register Maps (continued)

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
125	0x7D	Slave Alias[7]	7:1	RW	0x00	Slave Alias ID 7 Port0/Port1	7-bit Slave Alias ID of the remote Slave 7 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 7 register. A value of 0 in this field disables access to the remote Slave 7. If PORT1_SEL is set, this register controls Port 1 Slave Alias.
			0				***Reserved.***
198	0xC6	ICR	7	RW	0x00	IE_IND_ACC	Interrupt on Indirect Access Complete: Enables interrupt on completion of Indirect Register Access.
			6	RW		IE_RXDET_INT	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	RW		IE_RX_INT	Interrupt on Receiver interrupt: Enables interrupt on indication from the Receiver. Allows propagation of interrupts from downstream devices.
			4	RW			Reserved.
			3	RW			Reserved.
			2	RW			Reserved.
			1	RW			Reserved.
			0	RW		INT_EN	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
199	0xC7	ISR	7	R	0x00	IS_IND_ACC	Interrupt on Indirect Access Complete: Indirect Register Access has completed.
			6	R		IS_RXDET_INT	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	R		IS_RX_INT	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from down-stream device.
			4	R			Reserved.
			3	R			Reserved.
			2	R			Reserved.
			1	R			Reserved.
			0	R		INT	Global Interrupt: Set if any enabled interrupt is indicated.
240	0xF0	TX ID	7:0	R	0x5F	ID0	First byte ID code: "_".
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code: "U".
242	0xF2		7:0	R	0x42	ID2	Third byte of ID code: "B".
243	0xF3		7:0	R	0x39	ID3	Fourth byte of ID code: "9".
244	0xF4		7:0	R	0x34	ID4	Fifth byte of ID code: "4".
245	0xF5		7:0	R	0x39	ID5	Sixth byte of ID code: “9”.

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Register Maps (continued)

NOTE

Registers 0x40, 0x41, and 0x42 of the Serial Control Bus Registers are used to access the Page 0x10 and 0x14 registers.

Table 11. Page 0x10 Register

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
73	0x49	OLDI_PLL_STATE_MC_CNTL	7:5		0x00		Reserved
			4	RW		OLDI_STATE_MC_RESET	Enable HDMI PLL reset state 0: Disable state machine reset (normal operation). 1: Enable state machine reset.
			3:0				Reserved, when writing to this register always write '0000b to these bits.

Table 12. Page 0x14 Register

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
73	0x49	FPD_PLL_STATE_MC_CNTL	7:5		0x00		Reserved
			4	RW		FPD_STATE_MC_RESET	Enable FPD PLL reset state 0: Disable state machine reset (normal operation). 1: Enable state machine reset.
			3:0				Reserved, when writing to this register always write '0000b to these bits.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Applications Information

The DS90UB949A-Q1 can interface between a host (graphics processor) and a display, supporting 24-bit color depth (RGB888) and a high-definition (2880x1080) digital video format. The DS90UB949A-Q1 can receive an 8-bit RGB stream with a pixel clock rate of up to 210 MHz, together with four I2S audio streams.

8.2 Typical Applications

Bypass capacitors should be placed near the power supply pins. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until the power is stable. See and typical STP and coax connection diagrams.

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Typical Applications (continued)

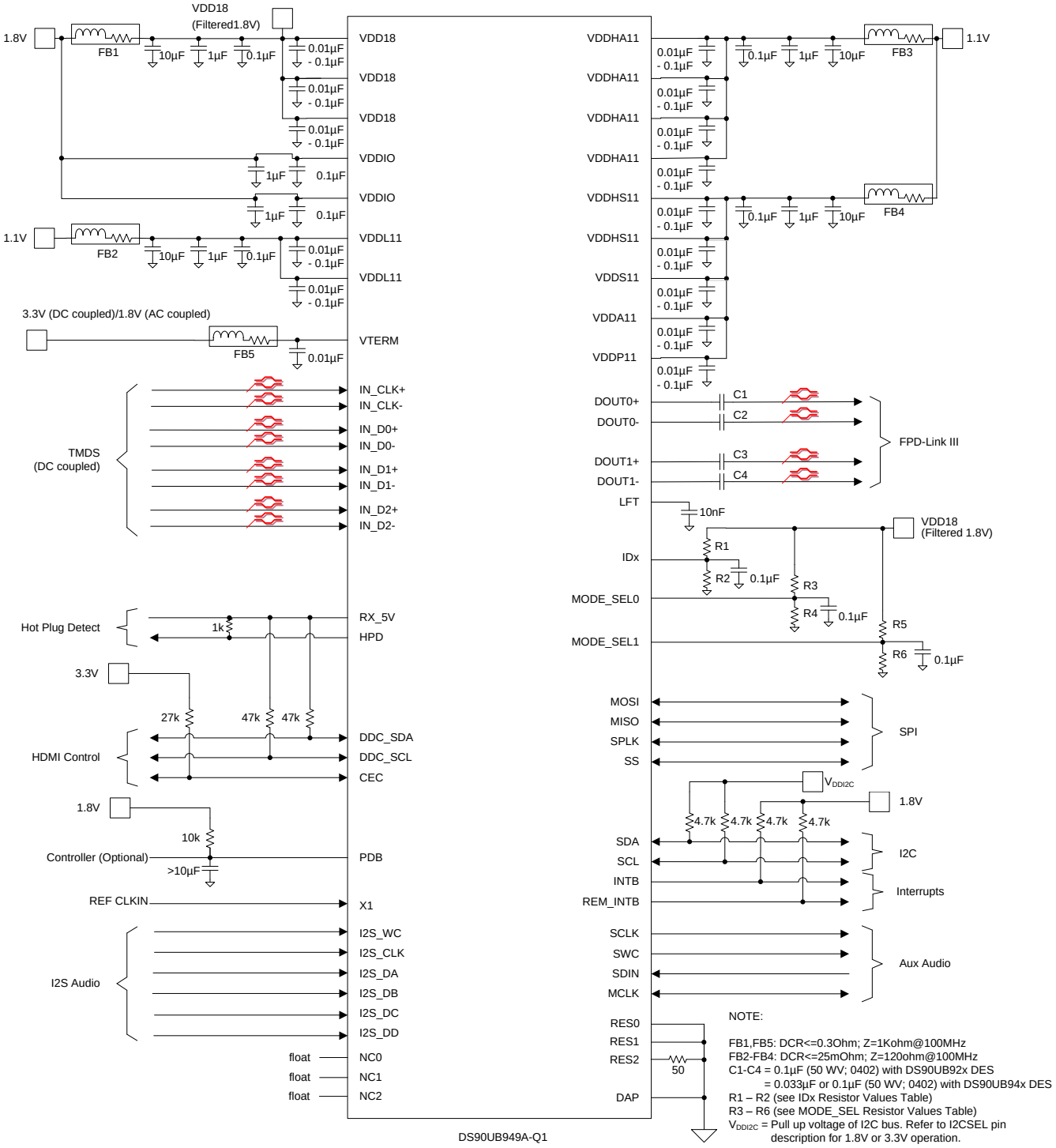

Figure 25. Typical Application Connection -- STP

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Typical Applications (continued)

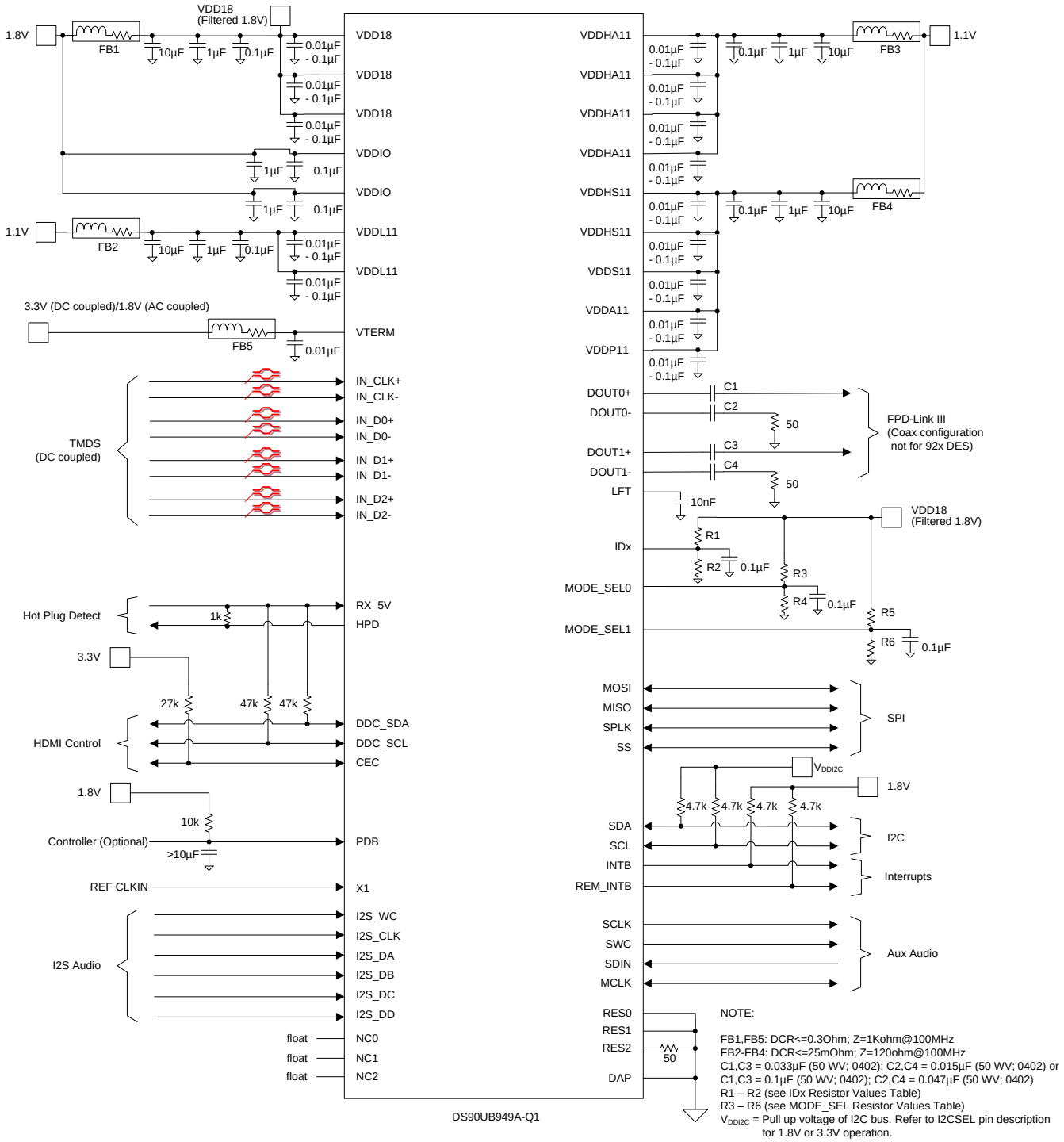
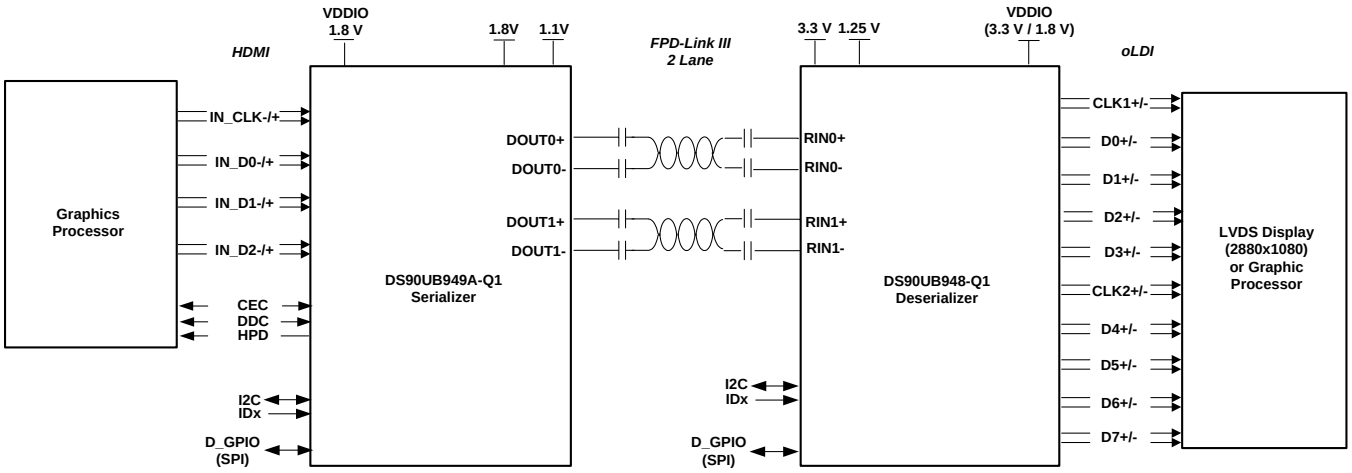


Figure 26. Typical Application Connection -- Coax

Typical Applications (continued)



HDMI – High Definition Multimedia Interface

Figure 27. Typical System Diagram

8.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in Figure 28.

Table 13. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V
STP configuration, AC-coupling capacitor for DOUT0± and DOUT1± with DS90Ux92x-Q1 deserializers. Note the 92x does not support single-ended coax unless specifically specified.	100 nF
STP/STQ configuration, AC-coupling capacitor for DOUT0± and DOUT1± with DS90Ux94x-Q1 deserializers	33 nF or 100 nF
Coax configuration, AC-coupling capacitor for DOUT0± and DOUT1± with DS90Ux94x-Q1 deserializers	100 nF on DOUT0/1+; 47nF on DOUT0/1– or 33 nF on DOUT0/1+; 15nF on DOUT0/1–

For applications that use a single-ended, 50-Ω coaxial cable, the unused data pins (DOUT0–, DOUT1–) should use a 15-nF capacitor and should be terminated with a 50-Ω resistor.

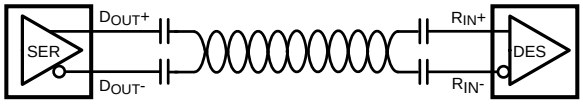


Figure 28. AC-Coupled Connection (STP)

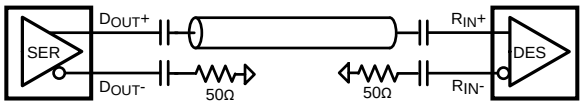


Figure 29. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC-coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

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8.2.2 Detailed Design Procedure

8.2.2.1 High-Speed Interconnect Guidelines

See *Channel-Link PCB and Interconnect Design-In Guidelines,* (SNLA008) and *Transmission Line RAPIDESIGNER Operation and Application Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs.
- Use the S/2S/3S rule in spacings:
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias.
- Use differential connectors when operating above 500-Mbps line speed.
- Maintain balance of the traces.
- Minimize skew within the pair.
- Terminate as close to the TX outputs and RX inputs as possible.

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187) available on www.ti.com.

8.2.3 Application Curves

Figure 30 corresponds to 1080p60 video application with a 2-lane FPD-Link III output. Figure 31 corresponds to a 3.36-Gbps single-lane output from a 96-MHz input.

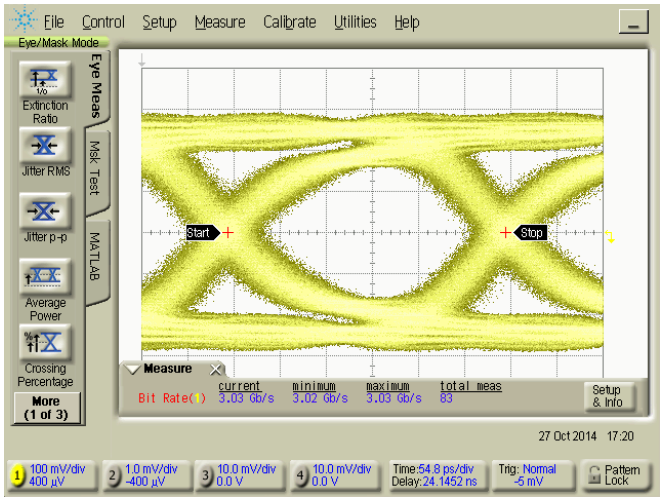

Figure 30. Serializer Output at 2.975 Gbps (85-MHz Clock)

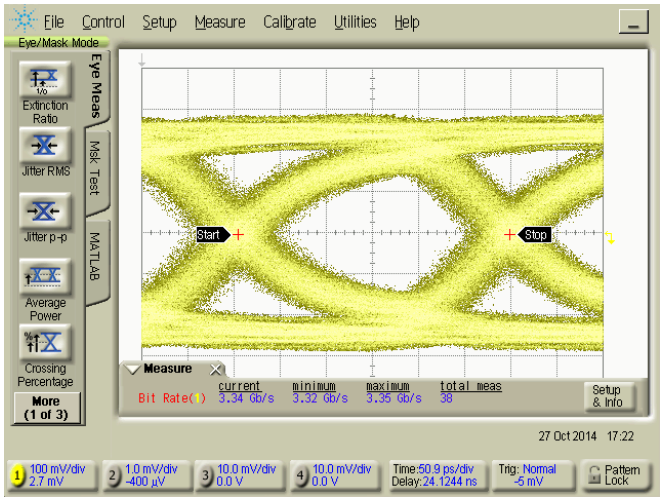

Figure 31. Serializer Output at 3.36 Gbps (96-MHz Clock)

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9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The *Pin Functions* table in the *Pin Configuration and Functions* section provides guidance on which circuit blocks are connected to which power pins. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 Power-Up Requirements and PDB Pin

The power supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin may be used to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DDIO}, a 10-kΩ pullup and a >10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until all power supplies have reached steady state.

The recommended power up sequence is as follows: V_{DD18}, V_{TERM}, V_{DD11}, wait until all supplies have settled, activate PDB, then apply HDMI input. There will be no functional impact to using a different sequence than shown below, but the current draw on V_{TERM} during power up may be higher in other cases.

The initialization sequence A shown in Figure 33 consists of any user defined device configurations and the following:

1. Set Register 0x5B bit 5 to 0. This disables the FPD3 PLL from resetting when a frequency change is detected.
2. Set Register 0x16 to 0x02. This minimizes the duration of inadvertent I2C events.

The initialization sequence B shown in Figure 33 should be performed after the HDMI clock has stabilized. Sequence B consists of the following:

1. Reset the HDMI PLL by writing the following registers:
   - Register 0x40 = 0x10
   - Register 0x41 = 0x49
   - Register 0x42 = 0x10
   - Register 0x42 = 0x00
2. Reset the FPD PLL by writing the following registers:
   - Register 0x40 = 0x14
   - Register 0x41 = 0x49
   - Register 0x42 = 0x10
   - Register 0x42 = 0x00

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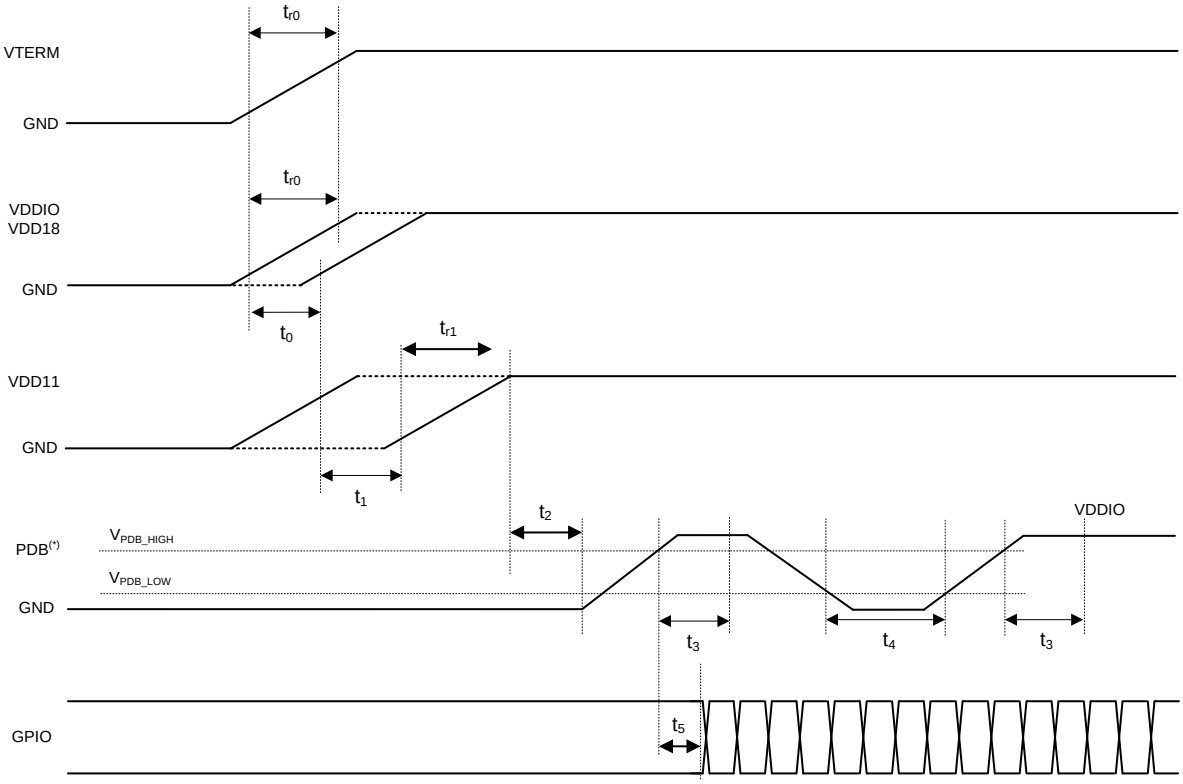
Power-Up Requirements and PDB Pin (continued)



(*) TI recommends that the designer assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

Figure 32. Recommended Power Sequencing

VTERM must come before VDD18 when VTERM = 1.8 V. This requirement is not applicable when VTERM = 3.3 V.

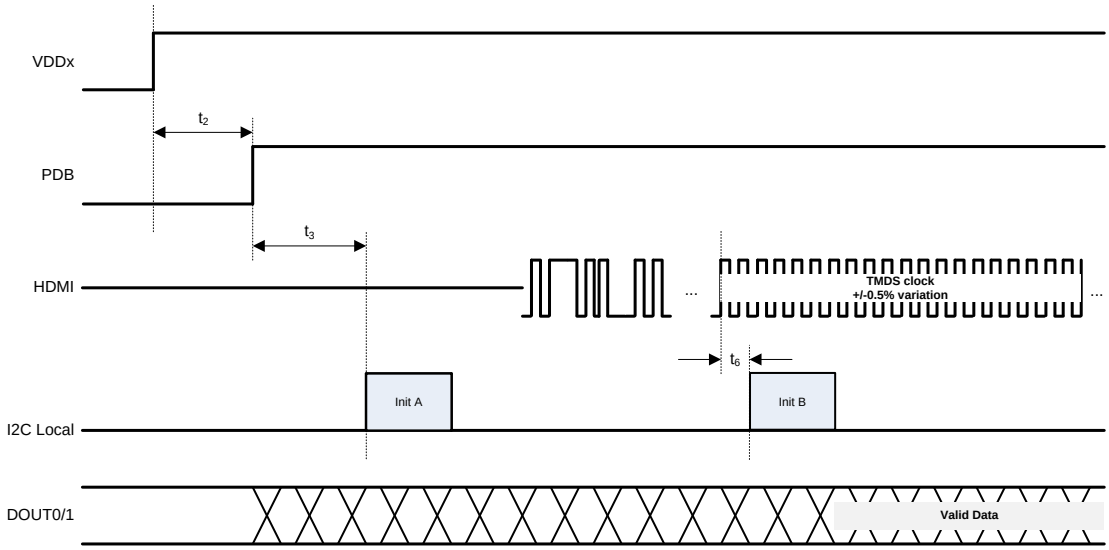


Figure 33. Initialization Sequencing

Power-Up Requirements and PDB Pin (continued)

The Init A and Init B sequence should consist of any user-defined device configurations.

Table 14. Power-Up Sequencing Constraints

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD18, VDDIO	VDD18 / VDDIO voltage range		1.71		1.89	V
VTERM	VTERM voltage range	DC-coupled HDMI termination	3.135		3.465	V
		AC-coupled HDMI termination	1.71		1.89	V
VDD11	VDD11 voltage range		1.045		1.155	V
V_{PDB_LOW}	PDB LOW threshold Note: V_{PDB} should not exceed limit for respective I/O voltage before 90% voltage of VDD12	VDDIO = 1.8V ± 5%	0.35 × VDDIO			V
V_{PDB_HIGH}	PDB HIGH threshold	VDDIO = 1.8V ± 5%			0.65 × VDDIO	V
t_{r0}	VTERM / VDDIO / VDD18 rise time	These time constants are specified for rise time of power supply voltage ramp (10% -90%).			1.5	ms
t_{r1}	VDD11 rise time	These time constants are specified for rise time of power supply voltage ramp (10% -90%).			1.5	ms
t_0	VDDIO / VDD18 delay time	VTERM needs to ramp-up before VDD18 and VDDIO.	0			ms
t_1	VDD11 delay time	VDDIO and VDD18 need to ramp-up before VDD11.	0			ms
t_2	PDB delay time	PDB should be released after all supplies are stable.	0			ms
t_3	I2C ready time	Starting from PDB high, the local I2C access is available after this time.	2			ms
t_4	Hard reset time	PDB negative pulse width required for the device reset.	2			ms
t_5	PDB to HDMI delay time	Keep GPIOs low or high until after PDB release.	0			ms
t_6	HDMI Clock Stable to PLL Reset (Init B)	HDMI Clock must be within 0.5% of the target frequency and stable.	1			µs

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10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement uses the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness—especially at high frequencies—and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 10 μF. The voltage rating of the capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, place the smaller value closest to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50-μF to 100-μF range and will smooth low frequency switching noise. TI recommends connecting the power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For the DS90UB949A-Q1, only one common ground plane is required to connect all device-related ground pins.

Use at least a four-layer board with a power and ground plane. Place LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the LLP style package, including PCB design and manufacturing requirements, is provided in TI *Leadless Leadframe Package (LLP) application report* (SNOA401).

10.2 Layout Example

Figure 34 is derived from a layout design of the DS90UB949A-Q1. This graphic is used to demonstrate proper high-speed routing when designing in the serializer.

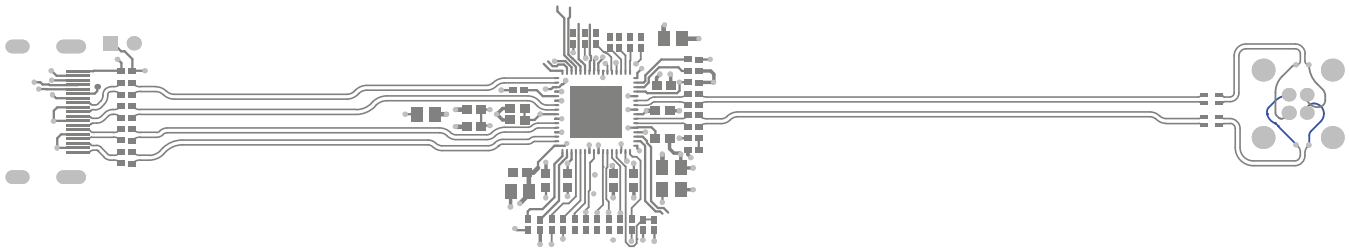

Figure 34. DS90UB949A-Q1 Serializer Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Soldering Specifications application report* (SNOA549)
- Texas Instruments, *IC Package Thermal Metrics application report* (SPRA953)
- Texas Instruments, *Channel-Link PCB and Interconnect Design-In Guidelines application report* (SNLA008)
- Texas Instruments, *Transmission Line RAPIDESIGNER Operation and Applications Guide application note* (SNLA035)
- Texas Instruments, *Leadless Leadframe Package (LLP) application report* (SNOA401)
- Texas Instruments, *LVDS Owner's Manual* (SNLA187)
- Texas Instruments, *I2C Communication Over FPD-Link III With Bidirectional Control Channel application report* (SNLA131)
- Texas Instruments, *Using the I2S Audio Interface of DS90Ux92x FPD-Link III Devices application report* (SNLA221)
- Texas Instruments, *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices application report* (SNLA132)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UB949ATRGCRQ1	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ
DS90UB949ATRGCRQ1.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ
DS90UB949ATRGCRQ1.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ
DS90UB949ATRGCTQ1	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ
DS90UB949ATRGCTQ1.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ
DS90UB949ATRGCTQ1.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UB949AQ

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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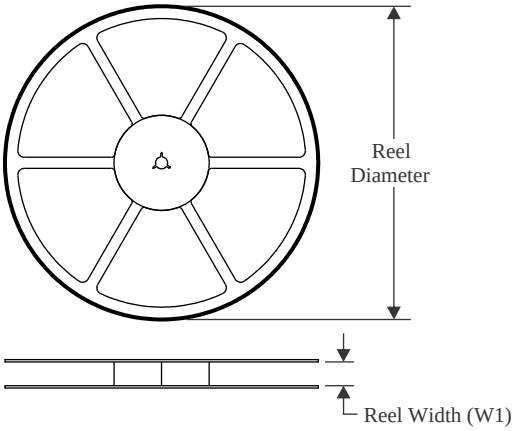
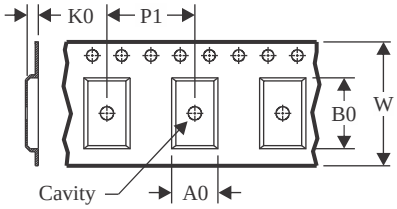
TAPE AND REEL INFORMATION

REEL DIMENSIONS

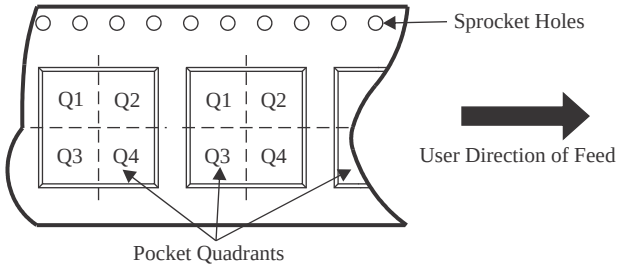


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

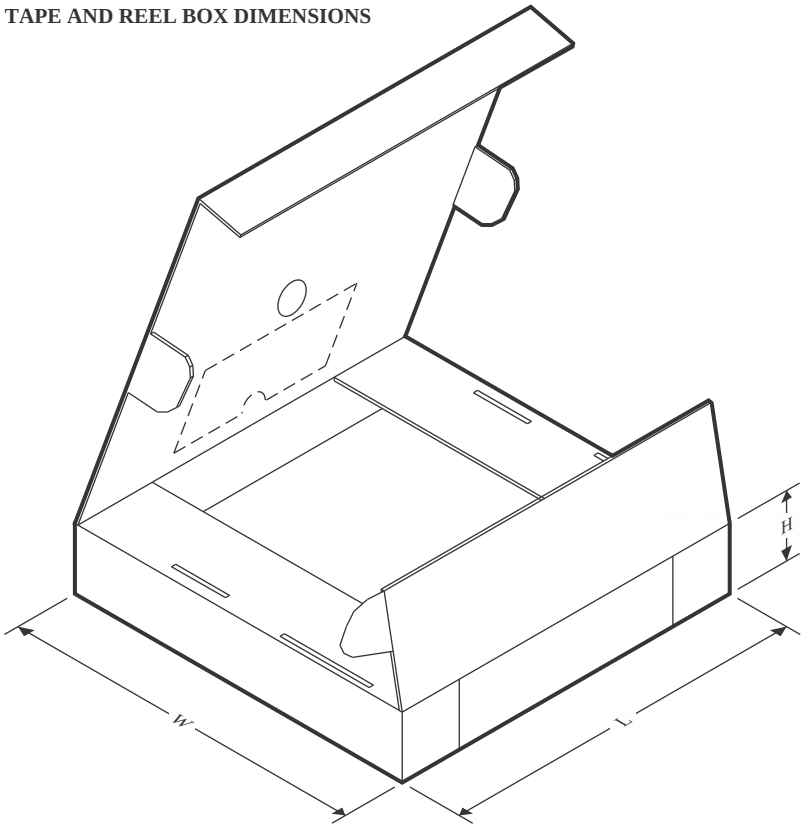
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB949ATRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UB949ATRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UB949ATRGCTQ1	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
DS90UB949ATRGCTQ1	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB949ATRGCRQ1	VQFN	RGC	64	2000	367.0	367.0	38.0
DS90UB949ATRGCRQ1	VQFN	RGC	64	2000	367.0	367.0	35.0
DS90UB949ATRGCTQ1	VQFN	RGC	64	250	210.0	185.0	35.0
DS90UB949ATRGCTQ1	VQFN	RGC	64	250	210.0	185.0	35.0

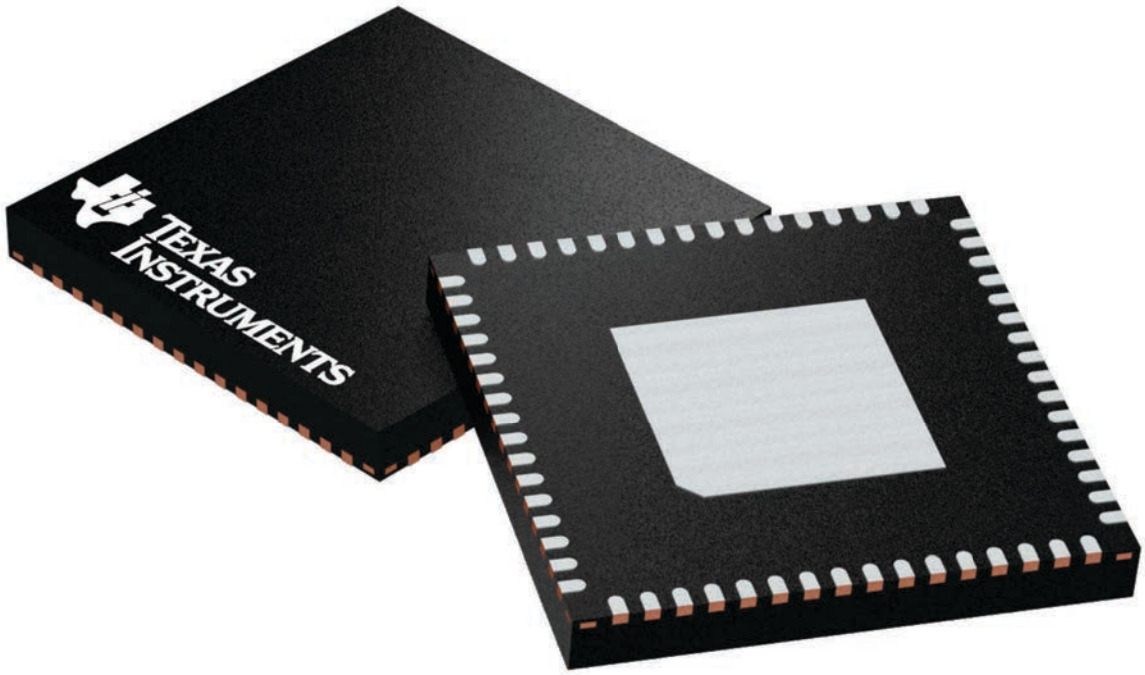
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

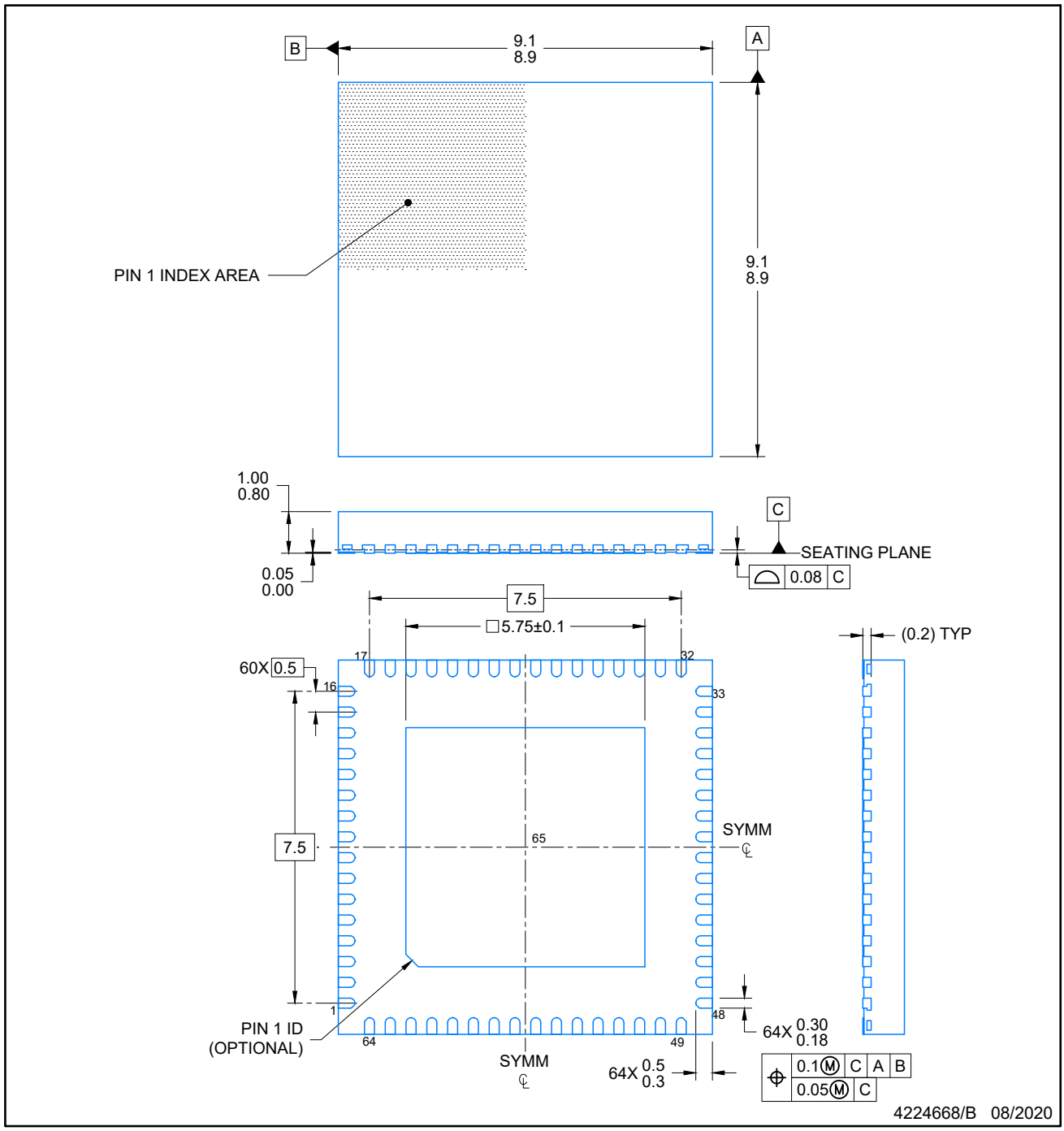
4224597/A

PACKAGE OUTLINE

RGC0064K

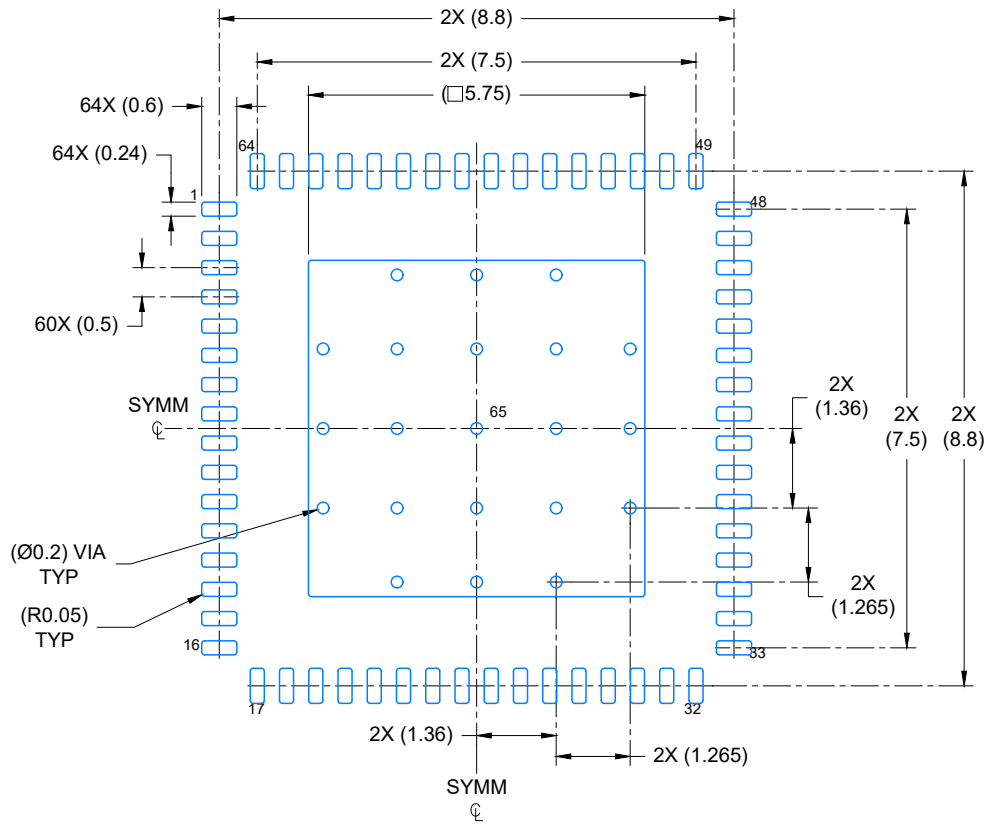
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

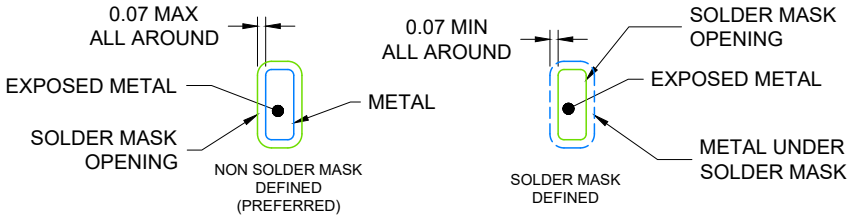


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

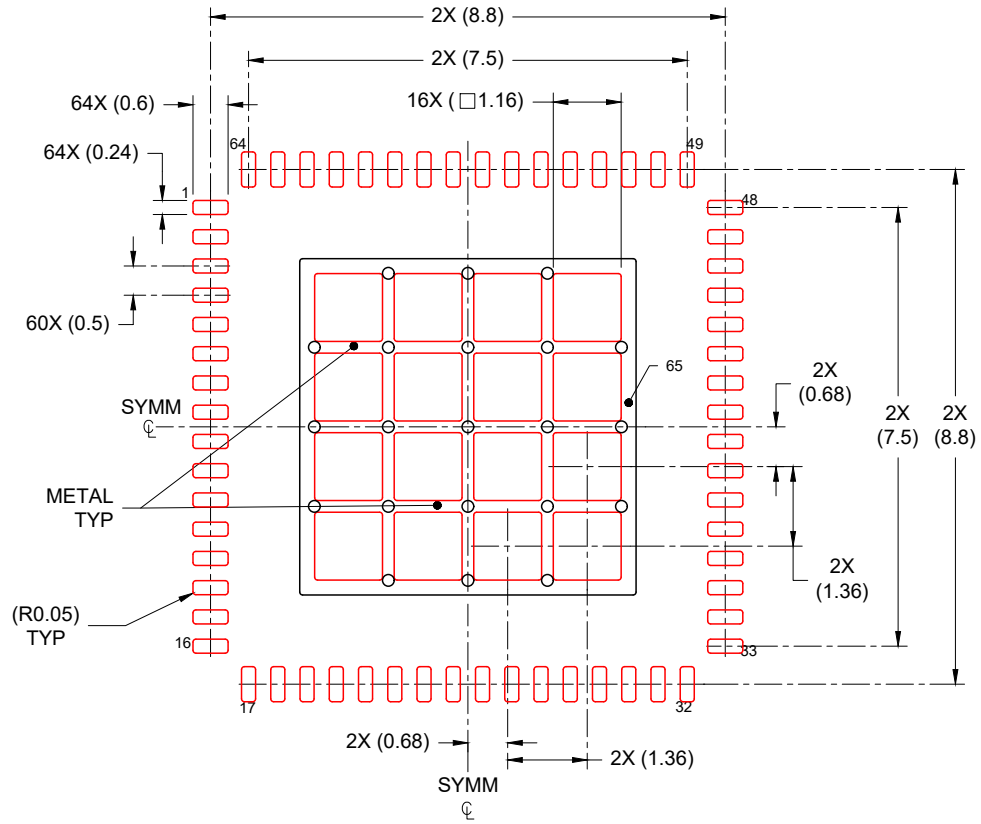


SOLDER MASK DETAILS

4224668/B 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED COVERAGE BY AREA
SCALE: 8X

4224668/B 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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