

DS92LV040A 4 Channel Bus LVDS Transceiver

1 Features

- Bus LVDS Signaling
- Propagation Delay: Driver 2.3 ns Max, Receiver 3.2 ns Max
- Low power CMOS Design
- 100% Transition Time 1 ns Driver Typical, 1.3 ns Receiver Typical
- High Signaling Rate Capability (above 155 Mbps)
- 0.1 V to 2.3 V Common Mode Range for $V_{ID} = 200$ mV
- 70 mV Receiver Sensitivity
- Supports Open and Terminated Failsafe on Port Pins
- 3.3-V Operation
- Glitch Free Power up/down (Driver & Receiver Disabled)
- Light Bus Loading (5 pF Typical) per Bus LVDS Load
- Balanced Output Impedance
- Product Offered in 44 Pin WQFN Package
- High Impedance Bus Pins on Power Off ($V_{CC} = 0$ V)

2 Applications

Designed for Double Termination Applications

3 Description

The DS92LV040A is one in a series of Bus LVDS transceivers designed specifically for high speed, low power backplane or cable interfaces. The device operates from a single 3.3-V power supply and includes four differential line drivers and four receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3-V LVTTTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation while consuming minimal power and reducing EMI. In addition, the differential signaling provides common mode noise rejection greater than ± 1 V.

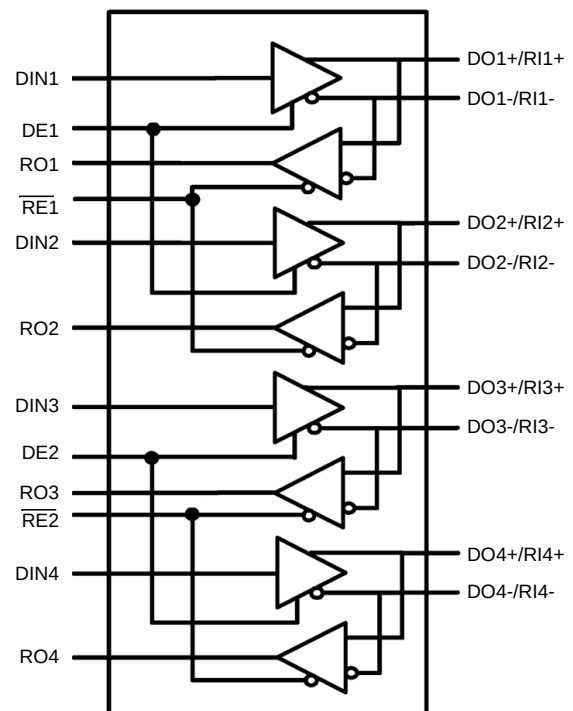
The receiver threshold is less than $+0/-70$ mV. The receiver translates the differential Bus LVDS to standard (LVTTTL/LVCMOS) levels. (See the [Application Information](#) Section for more details.)

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS92LV040A	WQFN (44)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Functional Diagram



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4 Revision History

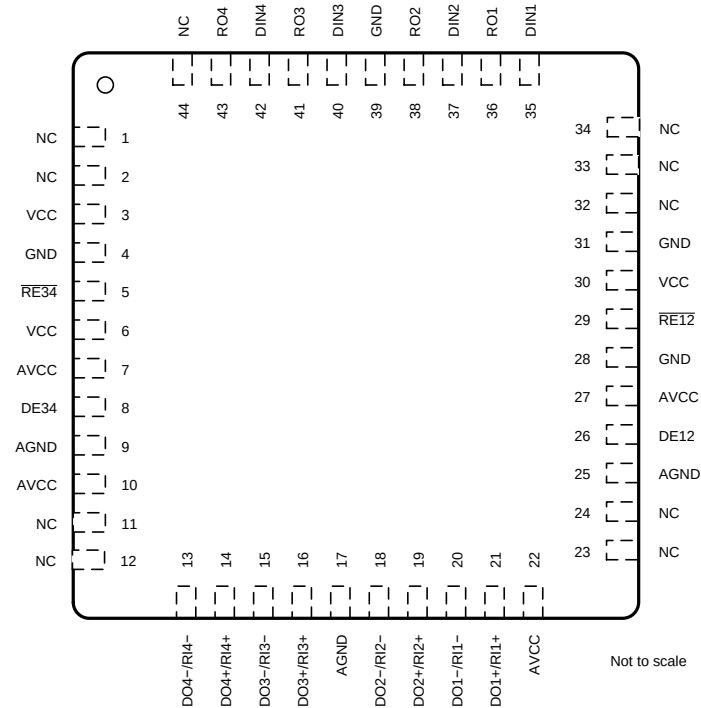
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E	Page
• Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Added "Driver Short Circuit Current Duration" to the <i>Absolute Maximum Ratings</i>	4
• Deleted Note 4: "Only one output at a time should be shorted..." from the <i>DC Electrical Characteristics</i> table.....	5

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	3

5 Pin Configuration and Functions

**NJN Package
WQFN (44 Pin)
Top View**



Pin Functions

PIN NAME	PIN #	INPUT/ OUTPUT	DESCRIPTIONS
DO+/RI+	14, 16, 19, 21	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO-/RI-	13, 15, 18, 20	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D _{IN}	35, 37, 40, 42	I	LVTTTL Driver Input. No pull up or pull down is attached to this pin
RO	36, 38, 41, 43	O	LVTTTL Receiver Output.
$\overline{\text{RE12}}$	29	I	Receiver Enable LVTTTL Input (Active Low). This pin, when low, configures receiver outputs, RO1 and RO2 active. When this pin is high, RO1 and RO2 are TRI-STATE. If this pin is floating, a weak current source to V _{CC} causes RO1 and RO2 to be TRI-STATE
$\overline{\text{RE34}}$	5	I	Receiver Enable LVTTTL Input (Active Low). This pin, when low, configures receiver outputs, RO3 and RO4 active. When this pin is high, RO3 and RO4 are TRI-STATE. If this pin is floating, a weak current source to V _{CC} causes RO3 and RO4 to be TRI-STATE
DE12	26	I	Driver Enable LVTTTL Input (Active High). This pin, when high, configures driver outputs, DO1+/RIN1+, DO1-/RIN1- and DO2+/RIN2+, DO2-/RIN2- active. When this pin is low, driver outputs 1 and 2 are TRI-STATE. If this pin is floating, a weak current source to V _{CC} causes driver outputs 1 and 2 to be active
DE34	8	I	Driver Enable LVTTTL Input (Active High). This pin, when high, configures driver outputs, DO3+/RIN3+, DO3-/RIN3- and DO4+/RIN4+, DO4-/RIN4- active. When this pin is low, driver outputs 3 and 4 are TRI-STATE. If this pin is floating, a weak current source to V _{CC} causes driver outputs 3 and 4 to be active
GND	4, 28, 31, 39	Ground	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V _{CC}	3, 6, 30	Power	V _{CC} for digital circuitry (must connect to V _{CC} on PC board). These pins connected internally.
AGND	9, 17, 25	Ground	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV _{CC}	7, 10, 22, 27	Power	Analog V _{CC} (must connect to V _{CC} on PC board). These pins connected internally.
NC	1, 2, 11, 12, 23, 24, 32, 33, 34, 44	N/A	Reserved for future use, leave open circuit.
DAP		GND	Must connect to GND plane through vias to achieve the theta ja specified under Absolute Maximum Ratings. The DAP (die attach pad) is the heat transfer material that is centered on the bottom of the WQFN package. Refer to application note AN-1187 () for attachment details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾ccr ⁽³⁾

	MIN	MAX	UNIT
Supply Voltage, V_{CC}		4	V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3	$V_{CC} + 0.3$ V	V
Driver Input Voltage (D_{IN})	−0.3	$V_{CC} + 0.3$ V	V
Driver Short Circuit Current Duration	Continuous		
Receiver Output Voltage (R_{OUT})	−0.3	$V_{CC} + 0.3$ V	V
Bus Pin Voltage ($DO\pm/RI\pm$)	−0.3	3.9	V
Storage temperature, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD} , ΔV_{OD} and V_{ID} .

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge ⁽¹⁾⁽²⁾	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽³⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽⁴⁾	±1000	

- (1) All typicals are given for $V_{CC} = +3.3$ V and $T_A = +25^\circ\text{C}$, unless otherwise stated.
- (2) ESD Rating: HBM (1.5 k Ω , 100 pF) > 4 kV EIAJ (0 Ω , 200 pF) > 250.
- (3) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{CC} Supply Voltage	3		3.6	V
Receiver Input Voltage	0		2.4	V
T_A Ambient Free Air Temperature	−40		85	°C
Slowest Input Edge Rate, $\Delta t/\Delta V$ (20% to 80%) ⁽¹⁾	Data		1	ns/V
	Control		3	ns/V

- (1) Generator waveforms for all tests unless otherwise specified: $f = 25$ MHz, $Z_O = 50$ Ω , t_r , $t_f = <1$ ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1 ns/V; control signals equal to or faster than 3 ns/V. In general, the faster the input edge rate, the better the AC performance.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DS92LV040A	UNIT
		NJN (WQFN)	
		44 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Package must be mounted to pc board in accordance with AN-1187 ([SNOA401](#)) to achieve thermals.

6.5 DC Electrical Characteristics⁽¹⁾

Over recommended operating supply voltage and temperature ranges unless otherwise specified.⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS		PIN	MIN	TYP	MAX	UNIT
V _{OD}	Output Differential Voltage	R _L = 27Ω, Figure 1		DO+/ DO-	200	300	460	mV
ΔV _{OD}	V _{OD} Magnitude Change					5	27	mV
V _{OS}	Offset Voltage				1.1	1.3	1.5	V
ΔV _{OS}	Offset Magnitude Change					5	10	mV
V _{OHD}	Driver Output High Voltage	R _L = 27Ω				1.4	1.65	V
V _{OLD}	Driver Output Low Voltage	R _L = 27Ω			0.95	1.1		V
I _{OSD}	Driver Output Short Circuit Current	V _{OD} = 0V, DE = V _{CC} . Driver outputs shorted together					30	45
V _{OHR}	Receiver Voltage Output High ⁽⁴⁾	V _{ID} = +300 mV	I _{OH} = -4 mA	R _{OUT}	V _{CC} -0.2			V
		Inputs Open			V _{CC} -0.2		V	
		Inputs Terminated, R _L = 27Ω			V _{CC} -0.2		V	
V _{OLR}	Receiver Voltage Output Low	I _{OL} = 4.0 mA, V _{ID} = -300 mV				0.05	0.100	V
I _{OD}	Receiver Output Dynamic Current	V _{ID} = 300mV, V _{OUT} = V _{CC} -1.0V			-50	33		mA
		V _{ID} = -300mV, V _{OUT} = 1.0V				36	60	mA
V _{TH}	Input Threshold High ⁽⁵⁾	DE = 0V, Over common mode range		DO+/ DO-		-40	0	mV
V _{TL}	Input Threshold Low ⁽⁵⁾				-70	-40		mV
V _{CMR}	Receiver Common Mode Range				V _{ID} /2		2.4 - V _{ID} /2	V
I _{IN}	Input Current	DE = 0V, $\overline{RE}$ = 2.4V, V _{IN} = +2.4V or 0V			-20	±1	+20	μA
		V _{CC} = 0V, V _{IN} = +2.4V or 0V			-20	±1	+20	μA
V _{IH}	Minimum Input High Voltage				D _{IN} , DE, $\overline{RE}$	2.0		V _{CC}
V _{IL}	Maximum Input Low Voltage			GND			0.8	V
I _{IH}	Input High Current	V _{IN} = V _{CC} or 2.4V		-20		±2.5	+20	μA
I _{IL}	Input Low Current	V _{IN} = GND or 0.4V		-20		±2.5	+20	μA
V _{CL}	Input Diode Clamp Voltage	I _{CLAMP} = -18 mA		-1.5		-0.8		V
I _{CCD}	Power Supply Current Drivers Enabled, Receivers Disabled	No Load, DE = $\overline{RE}$ = V _{CC} , DIN = V _{CC} or GND		V _{CC}			20	40
I _{CCR}	Power Supply Current Drivers Disabled, Receivers Enabled	DE = $\overline{RE}$ = 0V, V _{ID} = ±300mV				27	40	mA
I _{CCZ}	Power Supply Current, Drivers and Receivers TRI-STATE	DE = 0V; $\overline{RE}$ = V _{CC} , DIN = V _{CC} or GND				28	40	mA
I _{CC}	Power Supply Current, Drivers and Receivers Enabled	DE = V _{CC} ; $\overline{RE}$ = 0V, DIN = V _{CC} or GND, R _L = 27Ω				70	100	mA
I _{OFF}	Power Off Leakage Current	V _{CC} = 0V or OPEN, D _{IN} , DE, $\overline{RE}$ = 0V or OPEN, V _{APPLIED} = 3.6V (Port Pins)		DO+/ DO-	-20		+20	μA
C _{OUTPUT}	Capacitance at Bus Pins			DO+/ DO-		5		pF
C _{OUTPUT}	Capacitance at R _{OUT}			R _{OUT}		5		pF

- (1) The DS92LV040A functions within datasheet specification when a resistive load is applied to the driver outputs.
- (2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.
- (3) All typicals are given for V_{CC} = +3.3 V and T_A = +25°C, unless otherwise stated.
- (4) V_{OH} fail-safe terminated test performed with 27 Ω connected between RI+ and RI- inputs. No external voltage is applied.
- (5) Propagation delays, transition times, and receiver threshold are ensured by design and characterization.

6.6 AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified.⁽¹⁾

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP	MAX	UNIT
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low ⁽³⁾	$R_L = 27\Omega$, Figure 2, Figure 3, $C_L = 10\text{ pF}$	1	1.5	2.3	ns
t_{PLHD}	Differential Prop. Delay Low to High ⁽³⁾		1	1.5	2.3	ns
t_{SKD1}	Differential Skew $ t_{PHLD} - t_{PLHD} $ (duty cycle) ^{(4) (3)}			80	160	ps
t_{CCSK}	Channel to Channel Skew (all 4 channels) ⁽³⁾⁽⁵⁾			220	400	ps
t_{TLH}	Transition Time Low to High (20% to 80%)		0.4	0.75	1.3	ns
t_{THL}	Transition Time High to Low (80% to 20%)	$R_L = 27\Omega$, Figure 4, Figure 5, $C_L = 10\text{ pF}$	0.4	0.75	1.3	ns
t_{PHZ}	Disable Time High to Z			5	10	ns
t_{PLZ}	Disable Time Low to Z			5	10	ns
t_{PZH}	Enable Time Z to High			5	10	ns
t_{PZL}	Enable Time Z to Low			5	10	ns
f_{MAXD}	Ensured operation per data sheet up to the Min. Duty Cycle 45/55%, Transition time $\leq 25\%$ of period ⁽³⁾		85	125		MHz
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLDR}	Differential Prop. Delay High to Low ⁽³⁾	Figure 6, Figure 7, $C_L = 15\text{ pF}$	1.6	2.4	3.2	ns
t_{PLHDR}	Differential Prop Delay Low to High ⁽³⁾		1.6	2.4	3.2	ns
t_{SDK1R}	Differential Skew $ t_{PHLD} - t_{PLHD} $ (duty cycle) ⁽⁴⁾⁽³⁾			85	160	ps
t_{CCSKR}	Channel to Channel Skew (all 4 channels) ⁽³⁾⁽⁵⁾			140	300	ps
t_{TLHR}	Transition Time Low to High (10% to 90%) ⁽³⁾		0.85	1.25	2	ns
t_{THLR}	Transition Time High to Low (90% to 10%) ⁽³⁾	$R_L = 500\Omega$, Figure 8, Figure 9, $C_L = 15\text{ pF}$	0.85	1.03	2	ns
t_{PHZ}	Disable Time High to Z			3	10	ns
t_{PLZ}	Disable Time Low to Z			3	10	ns
t_{PZH}	Enable Time Z to High			3	10	ns
t_{PZL}	Enable Time Z to Low			3	10	ns
f_{MAXR}	Ensured operation per data sheet up to the Min. Duty Cycle 45/55%, Transition time $\leq 25\%$ of period ⁽³⁾		85	125		MHz

- (1) Generator waveforms for all tests unless otherwise specified: $f = 25\text{ MHz}$, $Z_O = 50\ \Omega$, t_r , $t_f = <1\text{ ns}$ (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1 ns/V ; control signals equal to or faster than 3 ns/V . In general, the faster the input edge rate, the better the AC performance.
- (2) C_L includes probe and fixture capacitance.
- (3) Propagation delays, transition times, and receiver threshold are ensured by design and characterization.
- (4) $t_{SKD1} |t_{PHLD} - t_{PLHD}|$ is the worst case pulse skew (measure of duty cycle) over recommended operation conditions.
- (5) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

7 Parameter Measurement Information

7.1 Test Circuits and Timing Waveforms

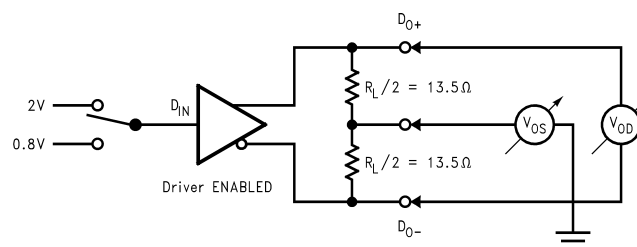


Figure 1. Differential Driver DC Test Circuit

Test Circuits and Timing Waveforms (continued)

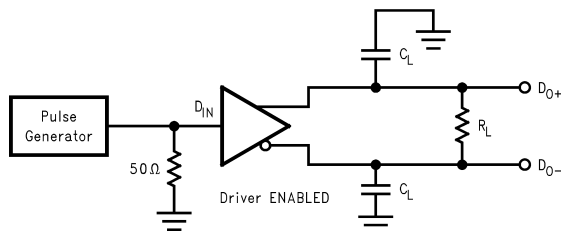


Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

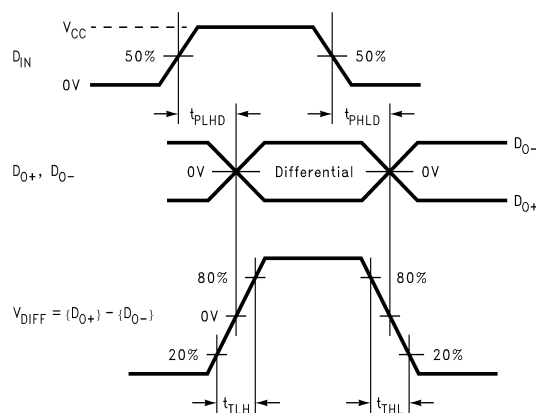


Figure 3. Differential Driver Propagation Delay and Transition Time Waveforms

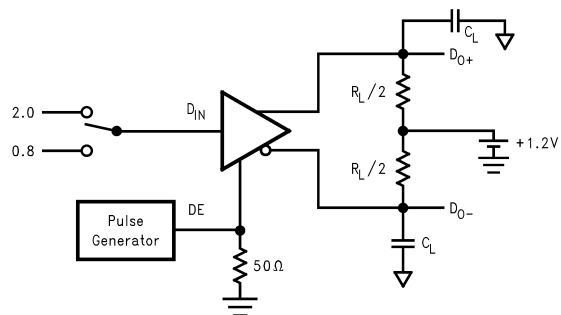


Figure 4. Driver TRI-STATE Delay Test Circuit

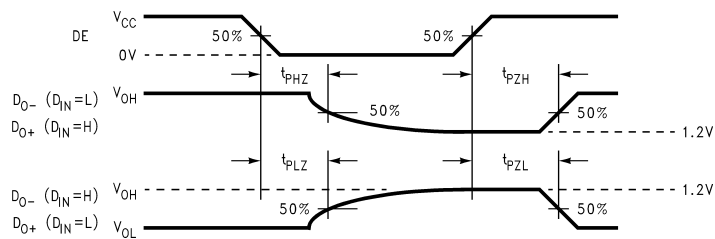
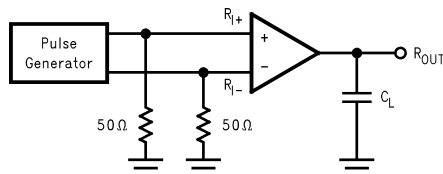
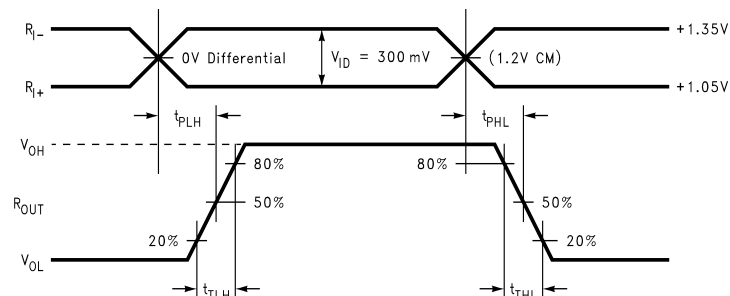
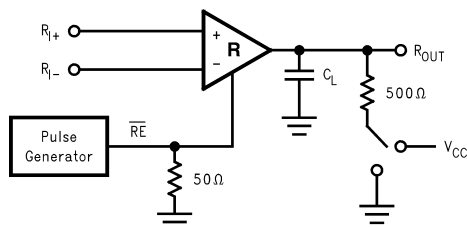
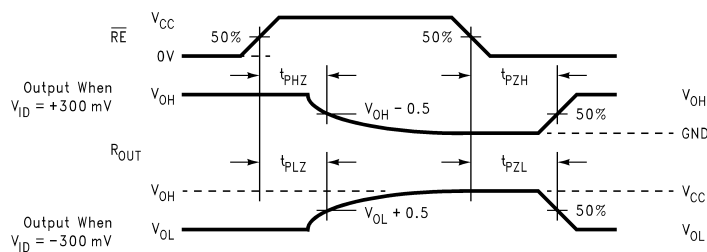


Figure 5. Driver TRI-STATE Delay Waveforms

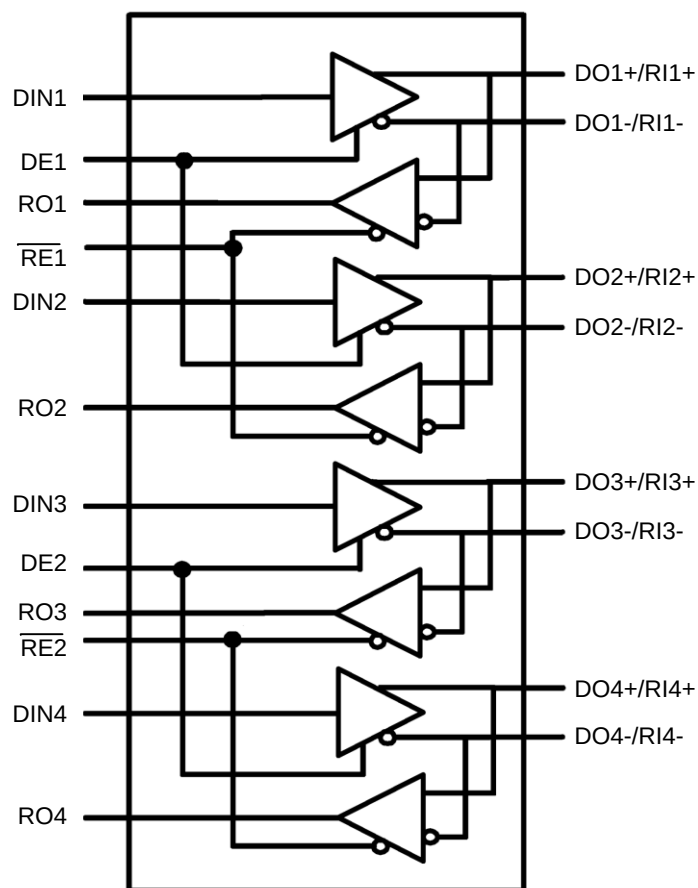
Test Circuits and Timing Waveforms (continued)

Figure 6. Receiver Propagation Delay and Transition Time Test Circuit

Figure 7. Receiver Propagation Delay and Transition Time Waveforms

Figure 8. Receiver TRI-STATE Delay Test Circuit

Figure 9. Receiver TRI-STATE Delay Waveforms

8 Detailed Description

8.1 Overview

BLVDS drivers and receivers are intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Z_0) is in the range of 50 Ω to 100 Ω . Two termination resistors of Z_0 Ω each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

8.2 Functional Block Diagram



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8.3 Feature Description

The DS92LV040A differential line driver is a balanced current mode design. A current mode driver, generally speaking has a high output impedance (100 Ω) and supplies a reasonably constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). The current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state.

Feature Description (continued)

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL designs. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers. The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

8.4 Device Functional Modes

Table 1. Functional Table

MODE SELECTED	DE	$\overline{\text{RE}}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

Table 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	D _{IN}	DO+	DO–
H	L	L	H
H	H	H	L
H	0.8V < D _{IN} < 2.0V	X	X
L	X	Z	Z

Table 3. Receiver Mode

INPUTS		OUTPUT
$\overline{\text{RE}}$	(RI+) – (RI–)	L
L	L (< –70 mV)	
L	H (> 0 mV)	H
L	–70 mV < V _{ID} < 0 mV	X
H	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS92LV040A is a Bus LVDS transceiver intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Z_O) is in the range of 50 Ω to 100 Ω . Two termination resistors of Z_O Ω each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

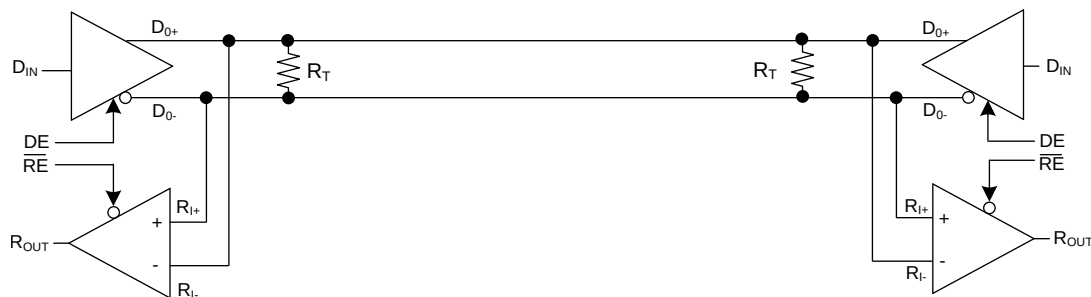
The output current is typically 12 mA. The current mode requires that a resistive termination be employed to terminate the signal and to complete the loop. Unterminated configurations are not allowed. The 12 mA loop current will develop a differential voltage of about 300 mV across a 27 Ω (double terminated 54 Ω differential transmission backplane) effective resistance, which the receiver detects with a 230 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (300 mV – 70 mV = 230 mV)). The signal is centered around +1.2 V (Driver Offset, V_{OS}) with respect to ground. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 600 mV.

9.2 Typical Application

9.2.1 Multipoint Communications

In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference compared to multi-drop is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

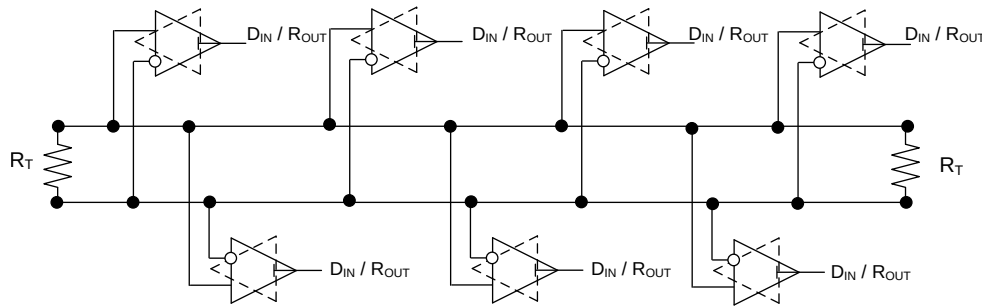
The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.



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Figure 10. Bidirectional Half-Duplex Point-to-Point Applications

Typical Application (continued)



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Figure 11. Multi-Point Bus Applications

9.2.2 Design Requirements

For this design example, use the parameters listed in [Table 4](#).

Table 4. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 to 3.6 V
Driver input voltage	0.8 to 3.3 V
Driver signaling rate	DC to 200 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance (differential)	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 to 3.6 V
Receiver input voltage	0 to ($V_{CC} - 0.8$) V
Receiver signaling rate	DC to 200 Mbps
Ground shift between driver and receiver	± 1 V

9.2.3 Detailed Design Procedure

9.2.3.1 Supply Voltage

The DS92LV040A is operated from a single supply. The device can support operations with a supply as low as 3 V and as high as 3.6 V.

9.2.3.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μ F to 1000 μ F) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to μ F range) must be installed locally next to the integrated circuit.

9.2.3.3 Termination Resistors

Multipoint LVDS communication channel employs a current source driving a transmission line which is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100- Ω impedance, the termination resistors should be between 90 Ω and 110 Ω . The line termination resistors are typically placed at the ends of the transmission line.

9.2.3.4 Interconnecting Media

The backplane and connectors should have a matched differential impedance. Use controlled impedance traces which match the differential impedance of your transmission medium (ie. backplane or cable) and termination resistor(s). Run the differential pair trace lines as close together as possible as soon as they leave the IC. This helps eliminate reflections and ensure noise is coupled as common-mode. In fact, it has been determined that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver. Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result.

Stub lengths should be kept to a minimum. The typical transition time of the DS92LV040A Bus LVDS output is 0.75 ns (20% to 80%). The extrapolated 100 percent time is 0.75/0.6 or 1.25 ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 1.25 ns/5 is 250 picoseconds. Let velocity equal 160 ps per inch for a typical loaded backplane. Then maximum stub length is 250 ps/160 ps/in or 1.56 inches. To determine the maximum stub for the backplane, determine the propagation velocity for the actual conditions (refer to application notes AN 905 and AN 808)

10 Power Supply Recommendations

The driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ± 1 V. Board level and local device level bypass capacitance should be used and are covered Supply Bypass Capacitance.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per [SLLD009](#), printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in [Figure 12](#).

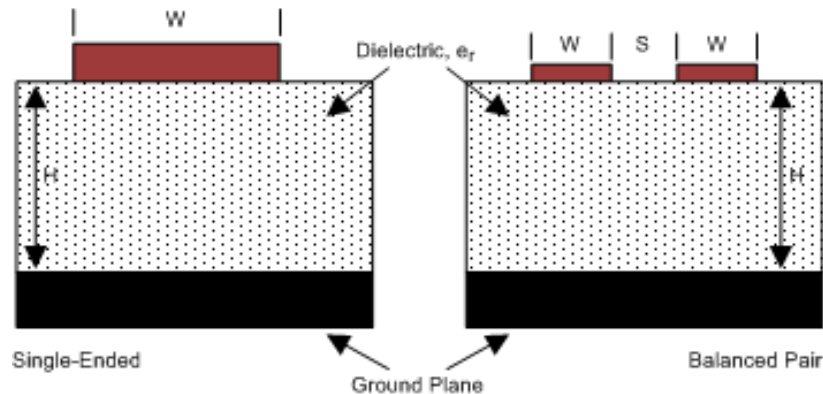


Figure 12. Microstrip Topology

Striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing the signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_0 based on the overall noise budget and reflection allowances. Footnotes 1⁽¹⁾, 2⁽²⁾, and 3⁽³⁾ provide formulas for Z_0 and t_{PD} for differential and single-ended traces. ⁽¹⁾ ⁽²⁾ ⁽³⁾

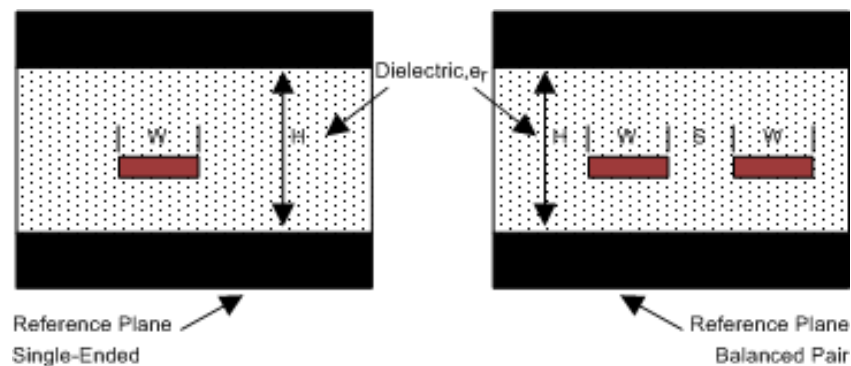


Figure 13. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with multipoint LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving multipoint LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.

(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (continued)

- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to multipoint LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in [Figure 14](#).

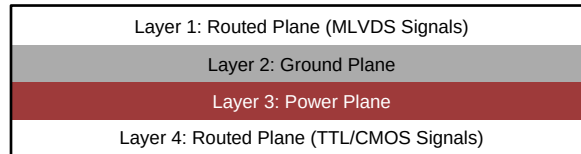


Figure 14. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in [Figure 15](#).

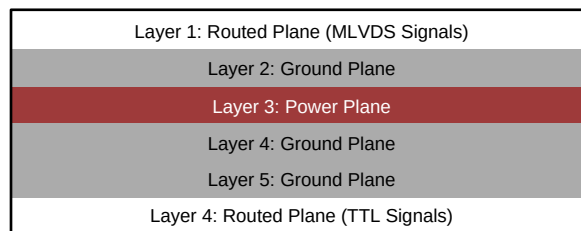


Figure 15. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an multipoint LVDS link to benefit from the electromagnetic field cancellation. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

If there are two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent multipoint LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

Layout Guidelines (continued)

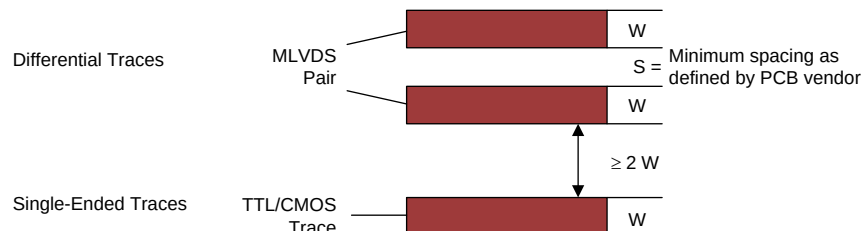


Figure 16. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

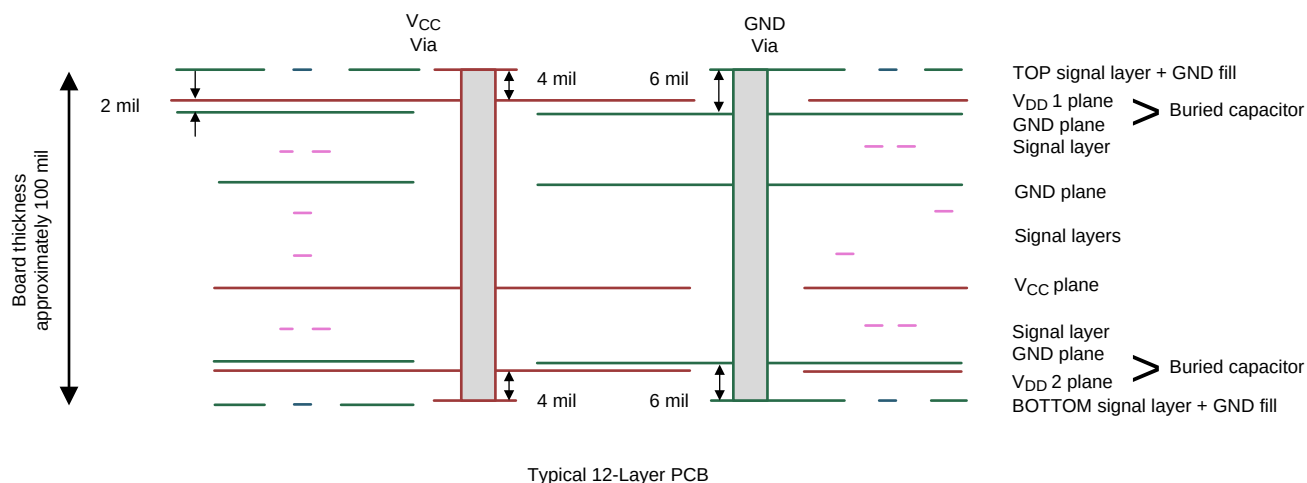


Figure 17. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 18(a).

Layout Guidelines (continued)

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μ F, and 0.1 μ F are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in Figure 18(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This results in a poor solder connection.



Figure 18. Typical Decoupling Capacitor Layouts

11.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 19.

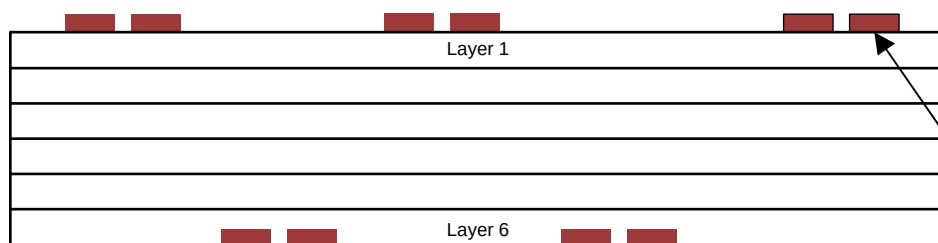


Figure 19. Staggered Trace Layout

Layout Example (continued)

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in [Figure 20](#). Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

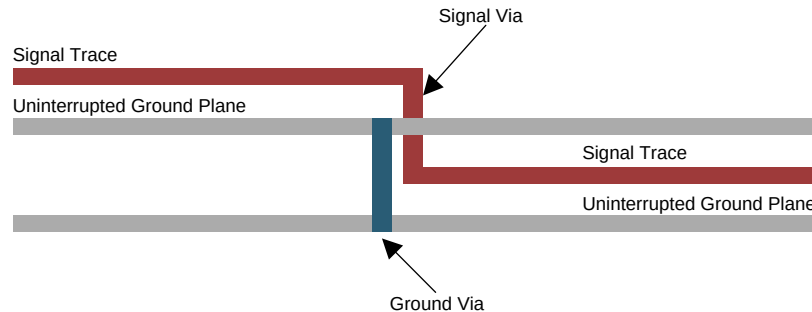


Figure 20. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

General application guidelines and hints may be found in the following application notes:), A).

For related documentation see the following:

- AN-808 ([SNLA028](#))
- AN-977 ([SNLA166](#))
- AN-971 ([SNLA165](#))
- AN-903 ([SNLA034](#))

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS92LV040ATLQA/NO.A	Active	Production	WQFN (NPN) 44	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQA/NOPB	Active	Production	WQFN (NPN) 44	250 SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQAX/NO.A	Active	Production	WQFN (NPN) 44	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQAX/NO.B	Active	Production	WQFN (NPN) 44	2500 LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS92LV040ATLQAX/NOPB	Active	Production	WQFN (NPN) 44	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

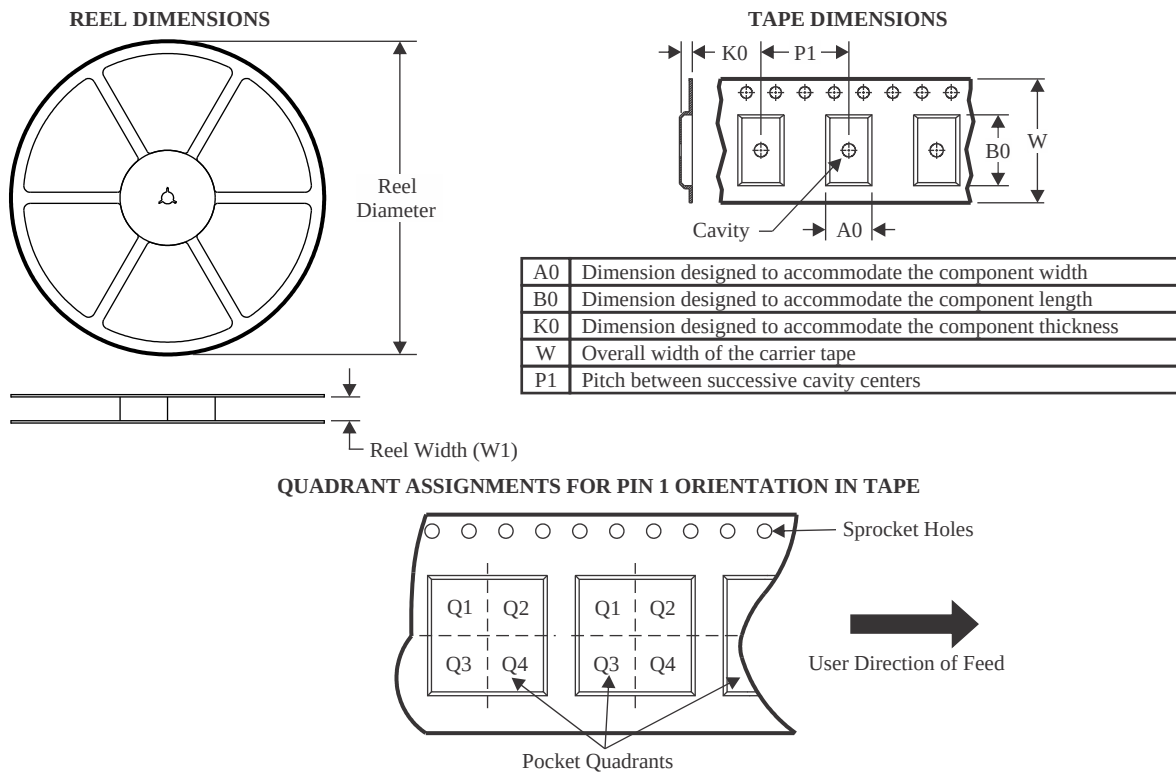
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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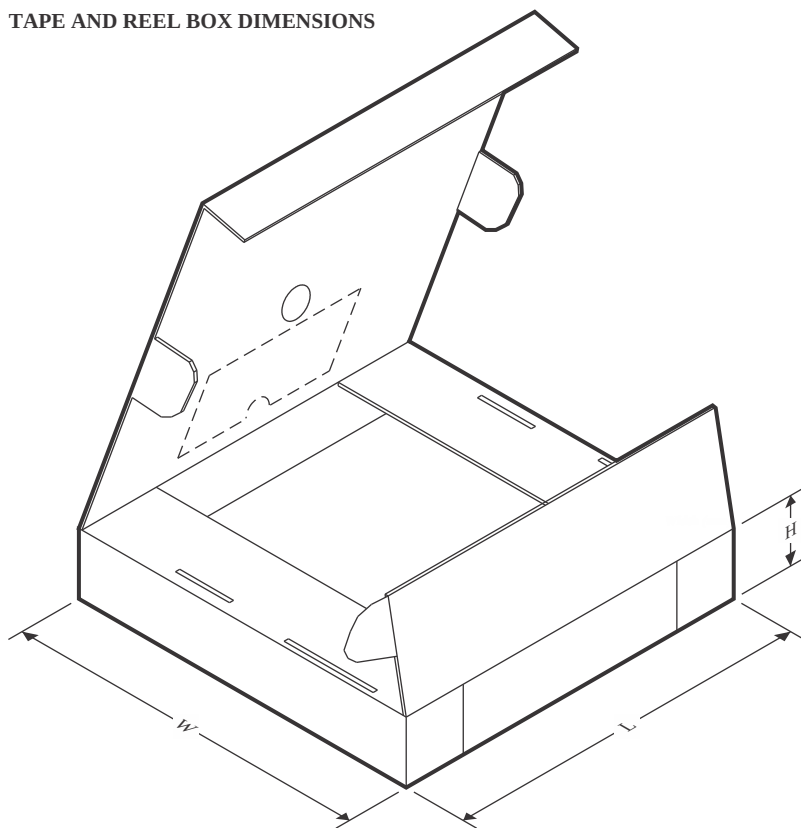
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV040ATLQA/NOPB	WQFN	NJN	44	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV040ATLQAX/NOPB	WQFN	NJN	44	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

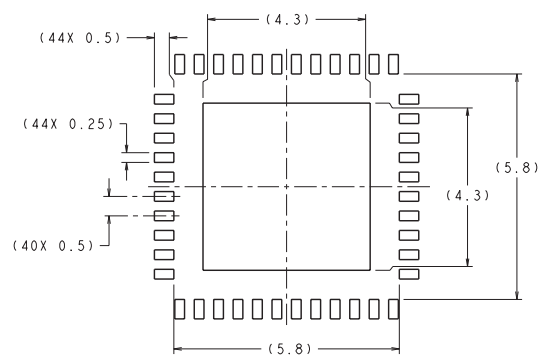
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

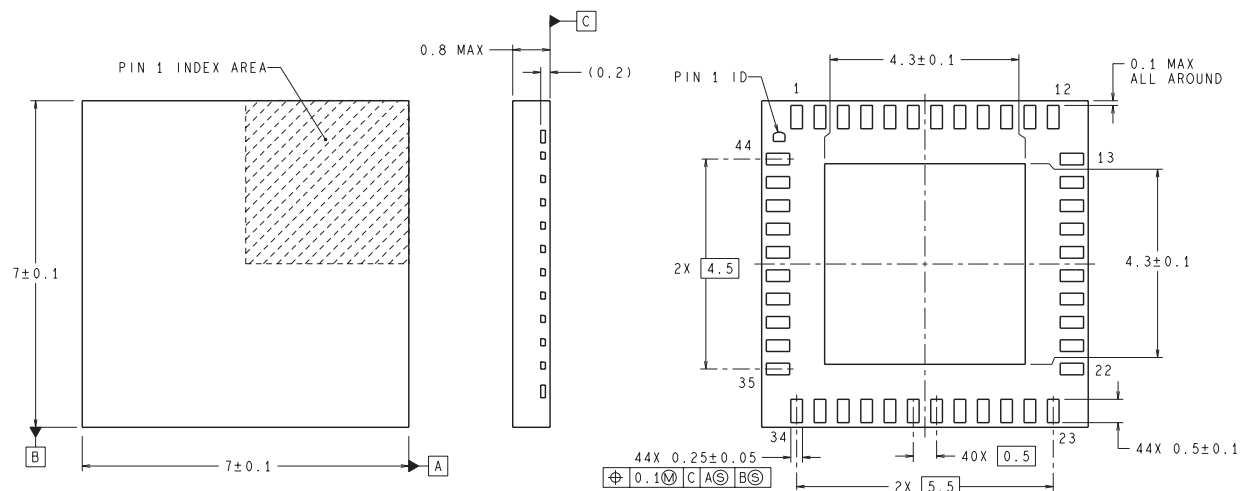
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV040ATLQA/NOPB	WQFN	NJN	44	250	208.0	191.0	35.0
DS92LV040ATLQAX/ NOPB	WQFN	NJN	44	2500	356.0	356.0	36.0

NJN0044A



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1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LQA44A (REV B)

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