1 Features

- **IEC 61000-4-2 level 4 ESD protection:**
  - ±30 kV contact discharge
  - ±30 kV air gap discharge
- **IEC 61000-4-5 surge protection:**
  - 6.2 A (8/20 µs)
- **IO capacitance:**
  - 0.5 pF (typical)
- **DC breakdown voltage:** ±8 V (typical)
- **Ultra low leakage current:** 50 nA (maximum)
- **Extremely low ESD clamping voltage**
  - 10.4 V at 16 A TLP
  - \( R_{\text{DYN}} \): 0.19 Ω
- **Low insertion loss:** 3.5 GHz (-3 dB bandwidth)
- **Supports high speed interfaces up to 7 Gbps**
- **Industrial temperature range:** –55°C to +150°C
- **Space-saving industry standard 0201 footprint** (0.6 mm × 0.3 mm × 0.3 mm)

2 Applications

- **End equipment:**
  - Vacuum robots
  - Wearables
  - Smart speakers
  - Portable electronics
  - Small appliances
  - Retail automation and payment
  - Laptops and desktops
  - TV and monitors
  - Docking stations
- ** Interfaces:**
  - USB 3.0
  - HDMI™ 1.4 and 2.0
  - DisplayPort™
  - SIM card

3 Description

The ESD451 is a bidirectional ESD protection diode for protecting data line and other I/O ports. The ESD451 is rated to dissipate ESD strikes up to ±30 kV per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 0.5 pF (typical) IO capacitance enabling high-speed interface protection for protocols such as USB 3.0. The extremely low dynamic resistance (0.19 Ω) and clamping voltage (10.4 V at 16 A TLP) is specified for system-level protection against transient events.

The ±30 kV ESD rating and 6.2 A surge provides robust transient protection in a tiny package for protecting 5.5 V power rails and data lines in portable electronics and other space constrained applications such as wearables.

The ESD451 is offered in the industry standard 0201 (DPL) package.

### Package Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>PACKAGE SIZE(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD451</td>
<td>DPL (X2SON, 2)</td>
<td>0.6 mm × 0.3 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

---

<table>
<thead>
<tr>
<th>IO</th>
<th>GND</th>
</tr>
</thead>
</table>

**Functional Block Diagram**
## Table of Contents

1 Features ................................................................. 1  
2 Applications ......................................................... 1  
3 Description ............................................................. 1  
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   6.2 ESD Ratings—JEDEC Specification ......................... 4  
   6.3 ESD Ratings—IEC Specification ............................. 4  
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   6.5 Thermal Information ........................................... 4  
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision * (April 2023) to Revision A (June 2023)

- Changed the status of the data sheet from: Advanced Information to: Production Data .......... 1
5 Pin Configuration and Functions

![Figure 5-1. DPL Package, 2-Pin X2SON (Top View)](image)

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO 1</td>
<td>I/O</td>
<td>ESD Protected Channel. If used as ESD IO, connect pin 2 to ground</td>
</tr>
<tr>
<td>IO 2</td>
<td>I/O</td>
<td>ESD Protected Channel. If used as ESD IO, connect pin 1 to ground</td>
</tr>
</tbody>
</table>

(1) I = input, O = output
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Pulse (2) (3)</td>
<td>57</td>
<td>6</td>
<td>W, A</td>
</tr>
<tr>
<td>IEC 61000-4-5 power (t&lt;sub&gt;p&lt;/sub&gt; - 8/20 µs)</td>
<td>IEC 61000-4-5 Current (t&lt;sub&gt;p&lt;/sub&gt; - 8/20 µs)</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65</td>
<td>155</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Voltages are with respect to GND unless otherwise noted.

(3) Measured at 25°C

6.2 ESD Ratings—JEDEC Specification

<table>
<thead>
<tr>
<th>Description</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt;</td>
<td>Electrostatic discharge</td>
<td>±2500</td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JS-002 (2)</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

<table>
<thead>
<tr>
<th>Description</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt;</td>
<td>Electrostatic discharge</td>
<td>±30000</td>
</tr>
<tr>
<td>IEC 61000-4-2 contact discharge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IEC 61000-4-2 air-gap discharge</td>
<td>±30000</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Description</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IO&lt;/sub&gt;</td>
<td>Input pin voltage</td>
<td>IO to GND</td>
<td>-5.5</td>
<td>5.5</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Operating free-air temperature</td>
<td></td>
<td>-55</td>
<td>150</td>
</tr>
</tbody>
</table>

6.5 Thermal Information

<table>
<thead>
<tr>
<th>Description</th>
<th>THERMAL METRIC (1)</th>
<th>ESD451</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DPL (X2SON)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 PINS</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>Junction-to-ambient thermal resistance</td>
<td>356.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JC(top)&lt;/sub&gt;</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>201.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>Junction-to-board thermal resistance</td>
<td>136.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>Junction-to-top characterization parameter</td>
<td>2.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>Junction-to-board characterization parameter</td>
<td>135.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JC(bot)&lt;/sub&gt;</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>NA</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
### 6.6 Electrical Characteristics
At TA=25°C (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>Reverse stand-off voltage $I_{IO} &lt; 100$ nA, across operating temperature range</td>
<td>-5.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Reverse leakage current $V_{IO} = 5.5$ V, $I_{IO}$ to GND or GND to $I_{IO}$</td>
<td>5</td>
<td>50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$V_{BRR}$</td>
<td>Break-down voltage $I_{IO} = 1$ mA, $I_{IO}$ to GND</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BRF}$</td>
<td>Break-down voltage $I_{IO} = 1$ mA, GND to $I_{IO}$</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HOLD}$</td>
<td>Holding voltage $TLP$, $I_{IO}$ to GND or GND to GND</td>
<td>7.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CLAMP}$</td>
<td>Clamping voltage with $TLP$ $I_{pp} = 1$ A, $TLP$, $I_{IO}$ to GND</td>
<td>7.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 5$ A, $TLP$, $I_{IO}$ to GND</td>
<td>8.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 16$ A, $TLP$, $I_{IO}$ to GND</td>
<td>10.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 1$ A, $TLP$, GND to $I_{IO}$</td>
<td>7.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 5$ A, $TLP$, GND to $I_{IO}$</td>
<td>8.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 16$ A, $TLP$, GND to $I_{IO}$</td>
<td>10.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clamping voltage with surge strike $I_{pp} = 6$ A, $t_p = 8/20$ µs, $I_{IO}$ to GND</td>
<td>9.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{pp} = 6$ A, $t_p = 8/20$ µs, GND to $I_{IO}$</td>
<td>9.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DYN}$</td>
<td>Dynamic resistance (3) $I_{IO}$ to GND</td>
<td>0.19</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>Line capacitance $V_{IO} = 0$ V, $f = 1$ MHz, $V_{pp} = 30$ mV, $I_{IO}$ to GND or $I_{IO}$ to GND</td>
<td>0.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Typical parameters are measured at 25°C
(2) Transition line pulse with 100 ns width and 10 ns rise and fall time
(3) Extraction of $R_{DYN}$ using least squares fit of TLP characteristics between $I = 10$ A and $I = 20$ A
(4) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
6.7 Typical Characteristics

Figure 6-1. Positive TLP Curve

Voltage at 30 ns = 10.3 V

Figure 6-2. Negative TLP Curve

Voltage at 30 ns = -8.4 V

Figure 6-3. +8-kV Clamped IEC Waveform

Figure 6-4. -8-kV Clamped IEC Waveform

Figure 6-5. Bias Voltage vs. Capacitance

Figure 6-6. Temperature vs. Capacitance
6.7 Typical Characteristics (continued)

Figure 6-7. Temperature vs. Leakage Current

Figure 6-8. Insertion Loss
7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESD451 is a diode type TVS which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. The device should be connected in parallel to the downstream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{\text{DYN}}$ of the triggered TVS holds this voltage ($V_{\text{CLAMP}}$) to a safe level for the protected IC. For more information on how to properly use this device, please refer to the ESD Packaging and Layout Guide for details.
8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

HDMI™ is a trademark of HDMI Licensing LLC.
DisplayPort™ is a trademark of Video Electronics Standards Association.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD451DPLR</td>
<td>ACTIVE</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>15000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>G</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer**: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

TAPE DIMENSIONS

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Pocket Quadrants

Sprocket Holes

User Direction of Feed

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD451DPLR</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>15000</td>
<td>178.0</td>
<td>8.4</td>
<td>0.36</td>
<td>0.66</td>
<td>0.33</td>
<td>2.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD451DPLR</td>
<td>X2SON</td>
<td>DPL</td>
<td>2</td>
<td>15000</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
</tbody>
</table>
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.  
B. This drawing is subject to change without notice.  
C. Small Outline No–Lead (SON) package configuration.  
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
Example Board Layout

Example Stencil Design (Note E)

Non Solder Mask Defined Pad

Contact your PCB vendor for allowable solder mask clearance

NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.  
E. Maximum stencil thickness 0.127 mm (5 mils). All linear dimensions are in millimeters.  
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.