ESD451W-Q1 Automotive 1-Channel ±30kV Bidirectional ESD Diode in a Wettable Flank 0402 Package

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- ISO 10605 (150pF, 330Ω & 330pF, 330Ω) ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 6A (8/20µs)
- IO capacitance:
  - 0.5pF (typical)
- DC breakdown voltage: ±8V (typical)
- Ultra low leakage current: 50nA (maximum)
- Extremely low ESD clamping voltage
  - 10.4V at 16A TLP
  - R_{DYN}: 0.19Ω
- Low insertion loss: 3.5GHz (-3dB bandwidth)
- Supports high speed interfaces up to 6Gbps
- Industrial temperature range: -55°C to +150°C
- Space saving industry standard 0402 footprint (1.0mm × 0.6mm)
- AEC-Q101 Qualified

2 Applications

- End equipment:
  - Vacuum robots
  - Wearables
  - Smart speakers
  - Portable electronics
  - Small appliances
  - Retail automation and payment
  - Laptops and desktops
  - TV and monitors
  - Docking stations
- Interfaces:
  - USB 2.0 and 3.0
  - HDMI™ 1.4 and 2.0
  - DisplayPort™
  - SIM card

3 Description

The ESD451W-Q1 is a bidirectional ESD protection diode for protecting data line and other I/O ports. ESD451W-Q1 is rated to dissipate ESD strikes up to ±30kV per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 0.5pF (typical) IO capacitance enabling high-speed interface protection for protocols such as USB 3.0. The extremely low dynamic resistance (0.19Ω) and clamping voltage (10.4V at 16A TLP) is specified for system-level protection against transient events.

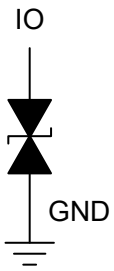
The ±30kV ESD rating and 6A surge provides robust transient protection in a tiny package for protecting 5.5V power rails and data lines in portable electronics and other space constrained applications such as wearables.

The ESD451W-Q1 is offered in a wettable flank 0402 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ESD451W-Q1	DPY (DFN1006, 2)	1.0mm × 0.6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

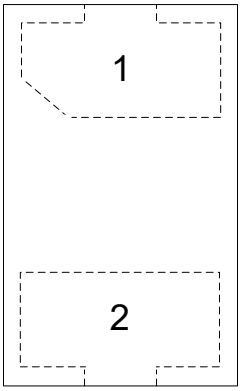


Figure 4-1. DPY Package, 2-Pin DFN1006 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
IO	2	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Peak Pulse (2) (3)	IEC 61000-4-5 power (t_p - 8/20 µs)		57	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		6	A
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

5.2 ESD Ratings - AEC Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 (1)	±2500	V
		Charged device model (CDM), per AEC Q101-005 (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 ESD Ratings - ISO Specifications

PARAMETER		TEST CONDITIONS		VALUE	UNIT
$V_{(ESD)}$	ISO 10605 Electrostatic Discharge	C = 150pF; R = 330Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330pF; R = 330Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	IO to GND	-5.5		5.5	V
T_A	Operating free-air temperature		-55		150	°C

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5.6 Thermal Information

THERMAL METRIC (1)		ESD451W-Q1 DPY (DFN1006) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	305.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	179.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	121.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	120.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <100nA, across operating temperature range	-5.5		5.5	V
I_{LEAK}	Reverse leakage current	V_{IO} = 5.5V, IO to GND or GND to IO		5	50	nA
V_{BR}	Breakdown voltage	I_{IO} = ±1mA, IO to GND	7	8	9	V
V_{CLAMP}	Clamping voltage with TLP	I_{PP} = 1A, TLP, IO to GND		8.2		V
		I_{PP} = 5A, TLP, IO to GND		9.2		V
		I_{PP} = 16A, TLP, IO to GND		11.5		V
		I_{PP} =1A, TLP, GND to IO		8.2		V
		I_{PP} =5A, TLP, GND to IO		9.2		V
		I_{PP} =16A, TLP, GND to IO		11.5		V
	Clamping voltage with surge strike (3)	I_{PP} = 6A, t_p = 8/20µs , IO to GND		10		V
		I_{PP} = 6A, t_p = 8/20µs , GND to IO		10		V
R_{DYN}	Dynamic resistance (2)	IO to GND		.24		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0V; f = 1MHz, V_{pp} = 30mV, IO to GND or IO to GND		0.5		pF

(1) Typical parameters are measured at 25℃
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10A and I = 20A
(3) Nonrepetitive current pulse 8 to 20µs exponentially decaying waveform according to IEC 61000-4-5

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5.8 Typical Characteristics

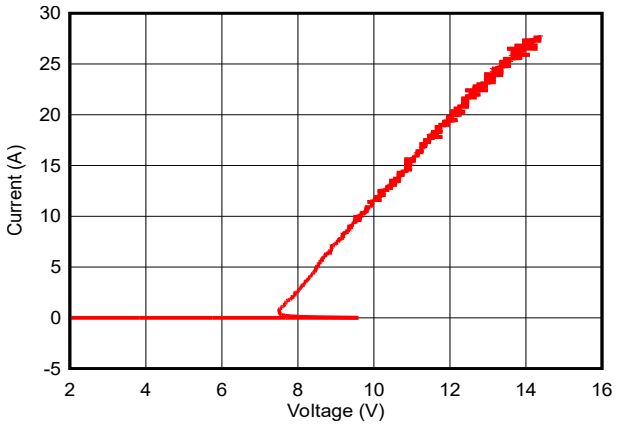


Figure 5-1. Positive TLP Curve

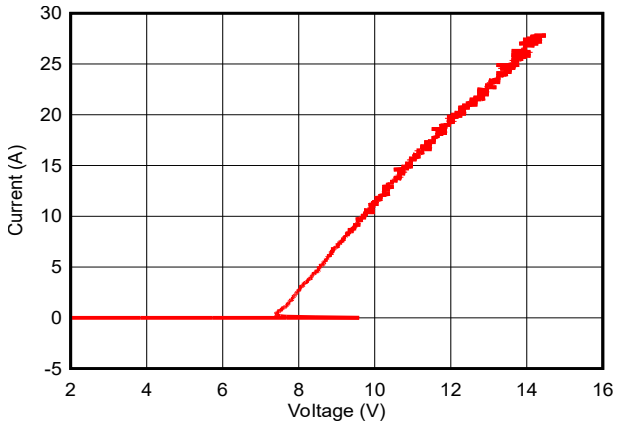


Figure 5-2. Negative TLP Curve

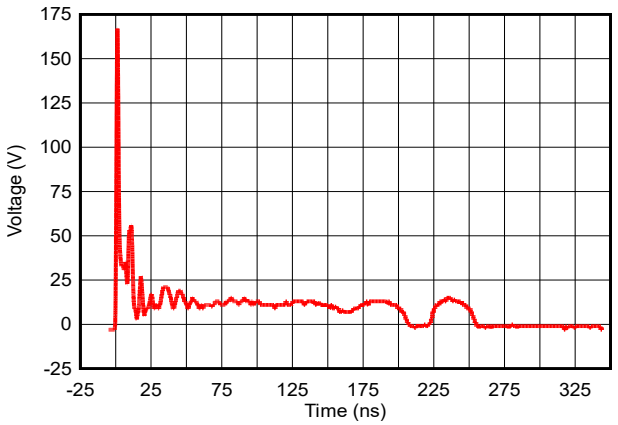


Figure 5-3. +8kV Clamped IEC Waveform

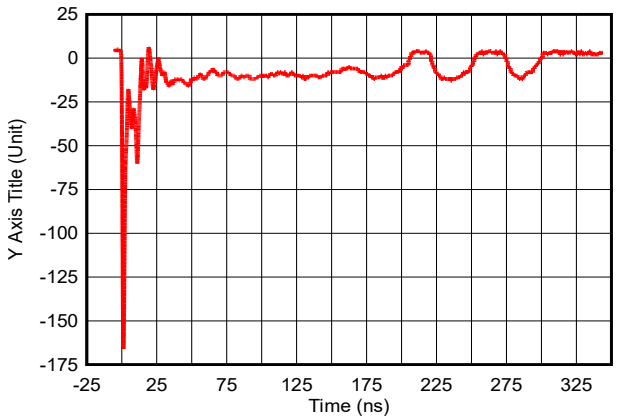


Figure 5-4. -8kV Clamped IEC Waveform

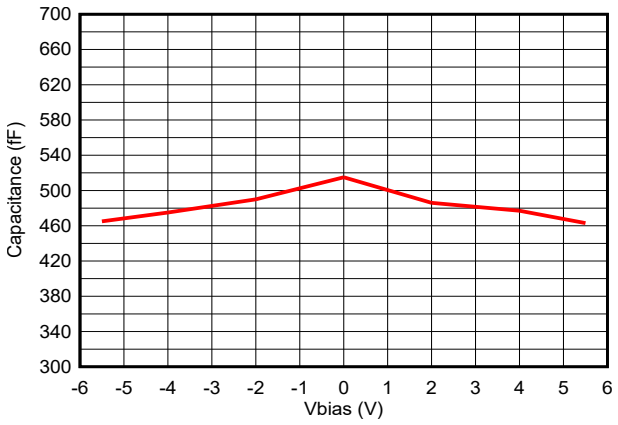


Figure 5-5. Capacitance vs Bias Voltage

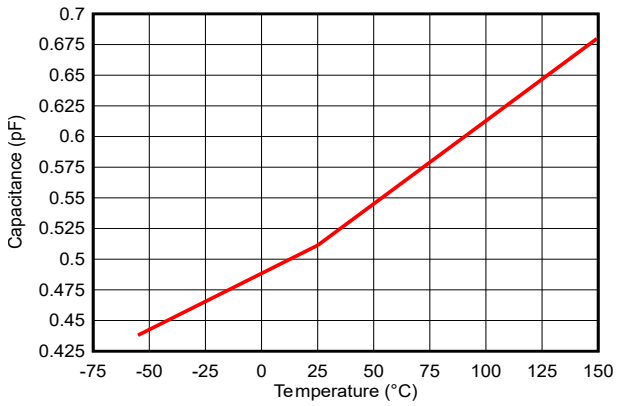


Figure 5-6. Capacitance vs Temperature

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5.8 Typical Characteristics (continued)

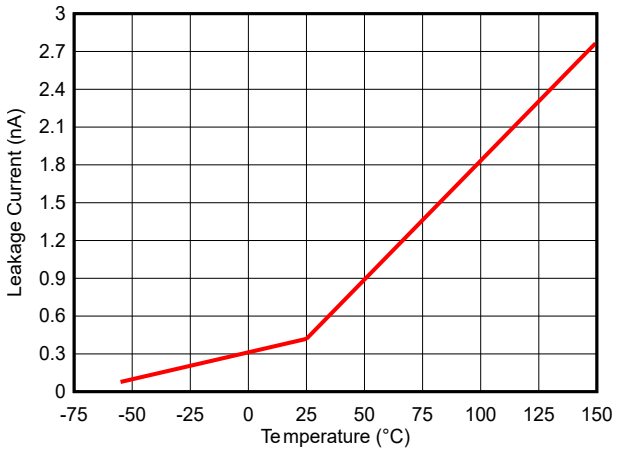


Figure 5-7. Leakage Current vs Temperature

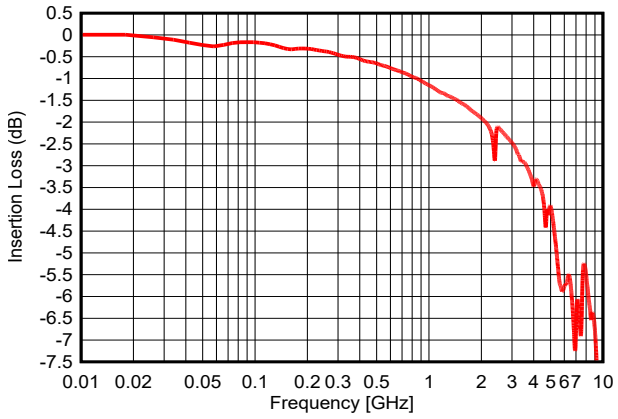


Figure 5-8. Insertion Loss

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6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD451WDPYRQ1	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	S6

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

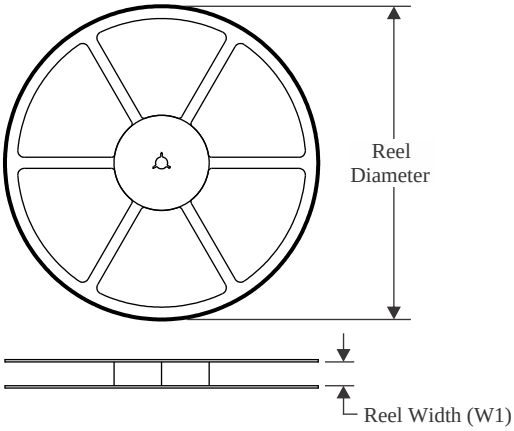
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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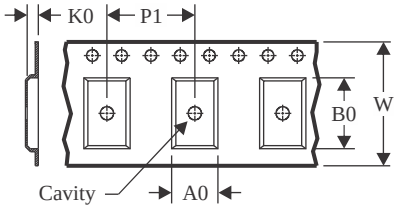
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

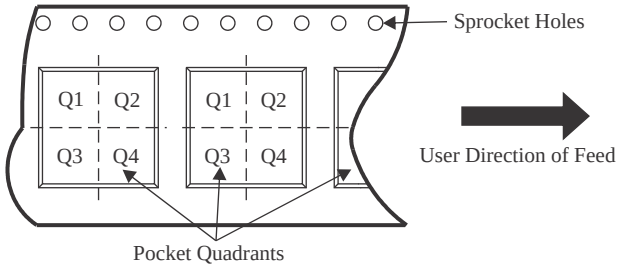


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

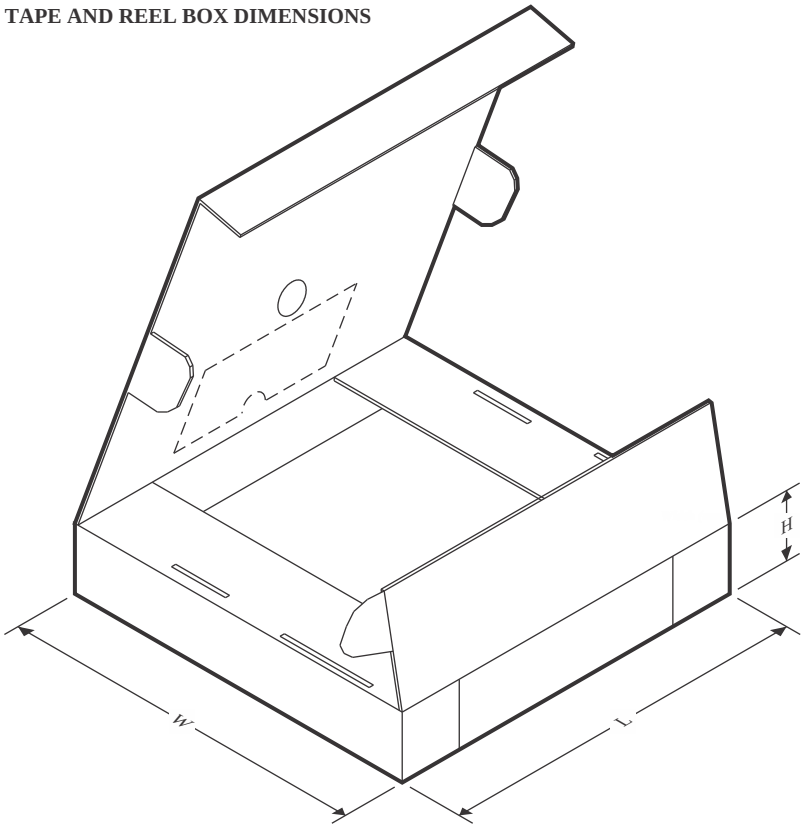
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD451WDPYRQ1	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD451WDPYRQ1	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231484/A

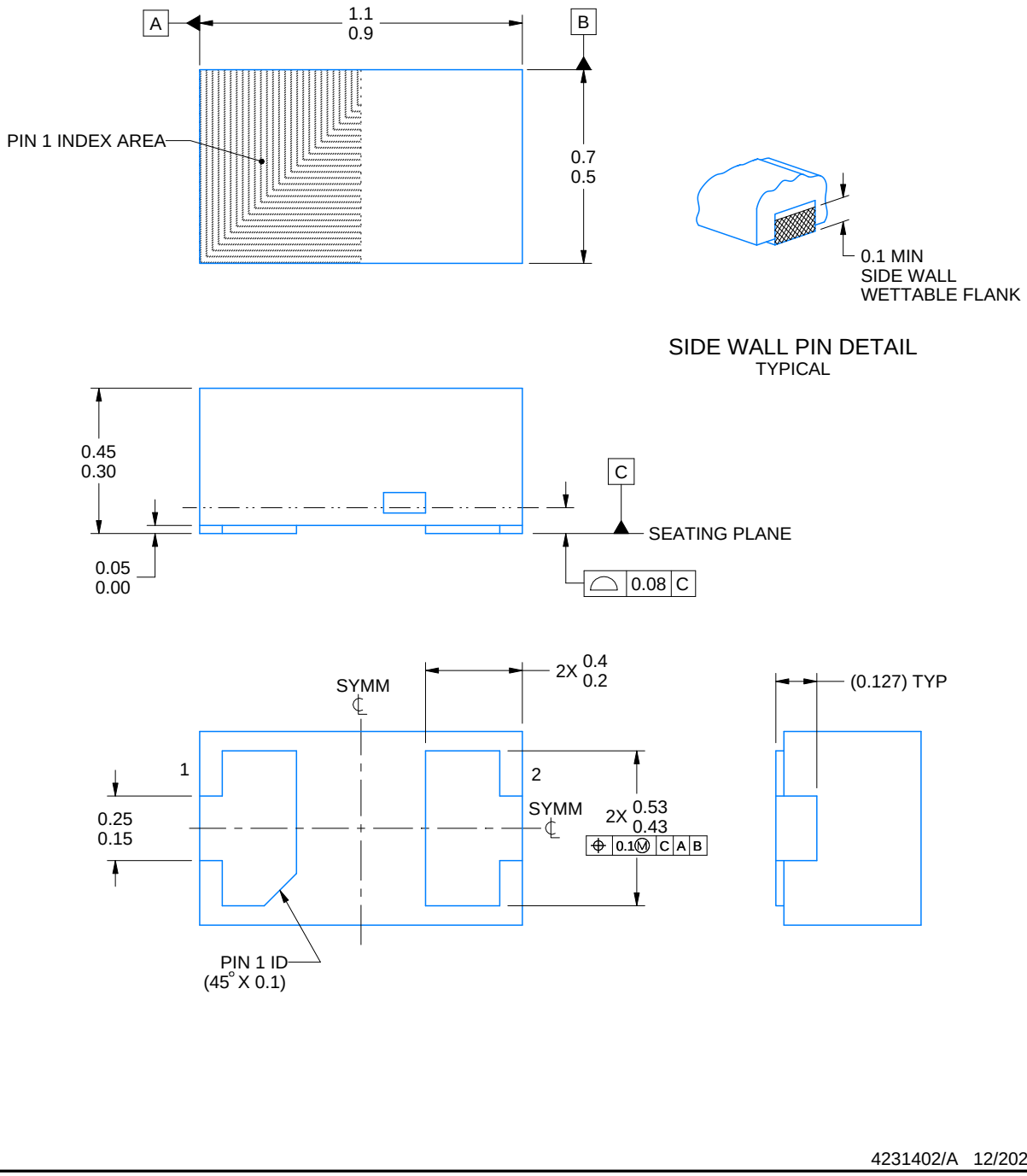
DPY0002B



PACKAGE OUTLINE

X1SON - 0.45 mm max height

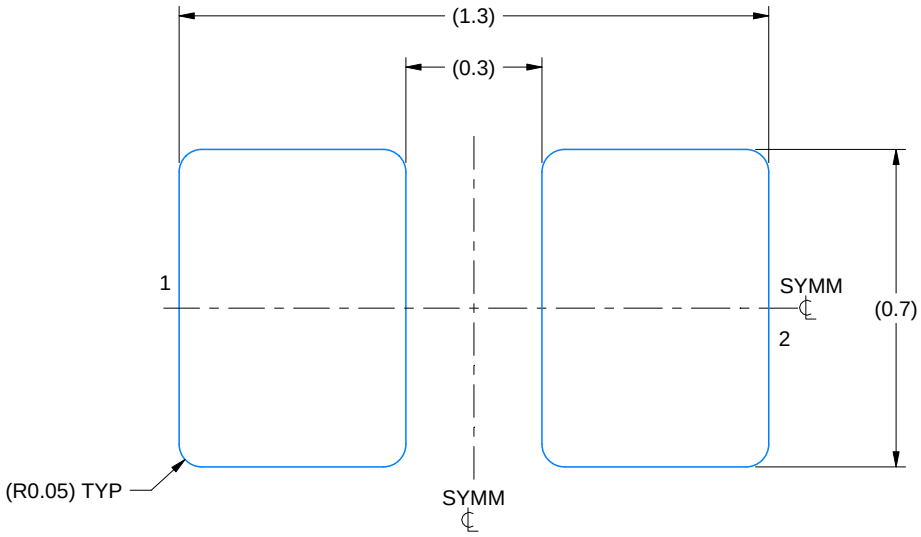
PLASTIC SMALL OUTLINE - NO LEAD



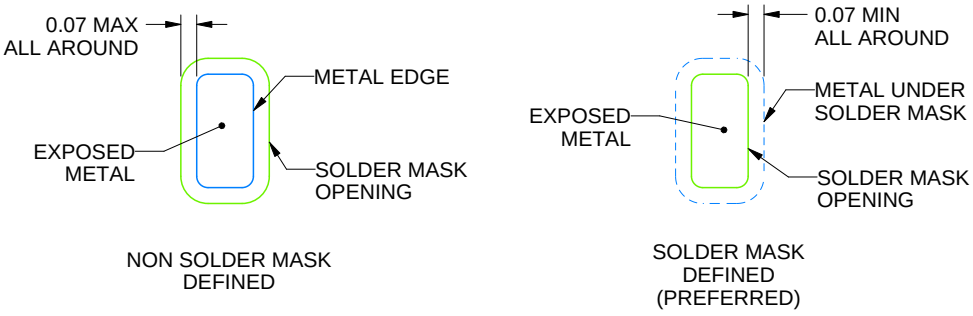
4231402/A 12/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

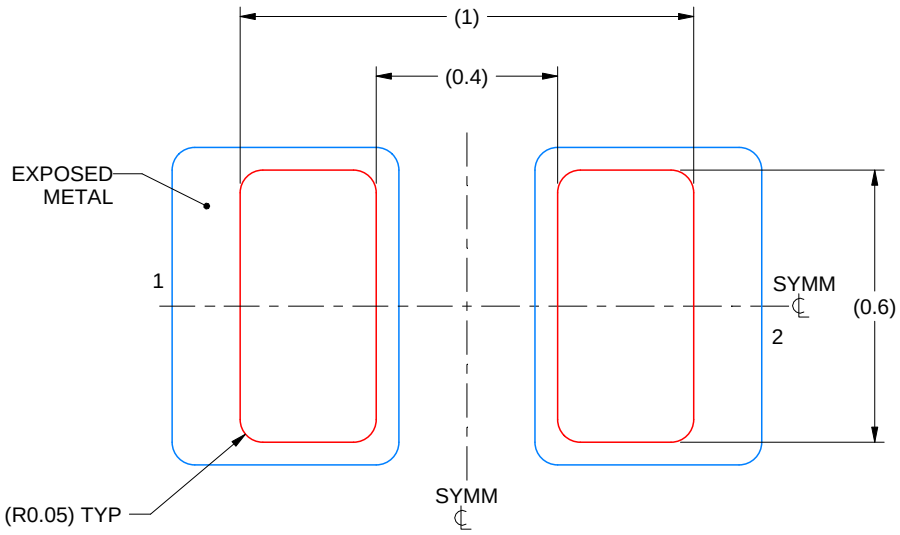


SOLDER MASK DETAILS

4231402/A 12/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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