ESD8x2 2-Channel, 36 V ESD Protection Diode

1 Features

- Working voltage 36 V
- Low leakage current 50 nA (maximum)
- IEC 61000-4-2 ESD protection:
  - ±25-kV contact and ±25-kV air (ESD852)
  - ±18-kV contact and ±18-kV air (ESD862)
- Robust surge protection:
  - IEC 61000-4-5 (8/20 µs): 4.3 A (ESD852)
  - IEC 61000-4-5 (8/20 µs): 3.1 A (ESD862)
- Bidirectional ESD protection
- I/O capacitance = 2.8 pF typical (ESD852)
- I/O capacitance = 2.6 pF typical (ESD862)
- SOT-23 (DBZ) small, standard, common footprint
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- Factory automation
- Communication equipments
- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial communications:
  - CAN / CAN-FD

3 Description

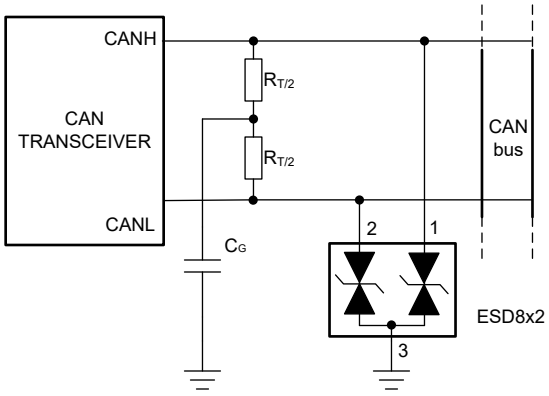
The ESD8x2 devices are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The devices are rated to dissipate ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 standard (±25-kV contact and airgap, or ±18-kV contact and airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The I_{PP} = 4.3A (8/20 µs surge waveform) capability of the ESD852 makes it an excellent choice for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 2.8 pF or 2.6 pF line capacitance of the ESD8x2 are an excellent choice for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
ESD852	2 Channels	DBZ (SOT-23, 3)
ESD862		

(1) For more information, see Section 9.



ESD8x2 Typical Application

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4 Pin Configuration and Functions

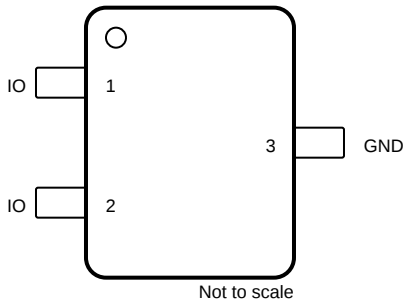

Figure 4-1. DBZ Package, SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		DEVICE	MIN	MAX	UNIT
Ppp	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD852		233	W
	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD862		175	W
I_{pp}	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C	ESD852		4.3	A
	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C	ESD862		3.1	A
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	°C
T_{stg}	Storage temperature		-65	155	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD852	±25000	V
			ESD862	±18000	V
		IEC 61000-4-2 Air Discharge, all pins	ESD852	±25000	V
			ESD862	±18000	V

5.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-36		36	V
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC[1]		ESD852	ESD862	UNIT
		DBZ (SOT-23)	DBZ (SOT-23)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.4	313.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.9	162.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.0	151.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.9	43.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	132.0	150.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–36		36	V
V_{BRF}	Forward breakdown voltage[1] [2]	I_{IO} = 10 mA, IO to GND		37.8	40	44.2	V
V_{BRR}	Reverse breakdown voltage [1] [2]	I_{IO} = –10 mA, IO to GND		–44.2	-40	–37.8	V
V_{CLAMP}	Clamping voltage[3]	I_{PP} = 1 A, t_p = 8/20 µs, IO to GND	ESD852		43		V
		I_{PP} = 4.3 A, t_p = 8/20 µs, from IO to GND	ESD852		61		V
		I_{PP} = 1 A, t_p = 8/20 µs, from IO to GND	ESD862		47		V
		I_{PP} = 3.1 A, t_p = 8/20 µs, from IO to GND	ESD862		61		V
V_{CLAMP}	Clamping voltage[3]	IPP = 16 A, TLP, IO to GND or GND to IO	ESD852		63		V
			ESD862		64		V
I_{LEAK}	Leakage current	V_{IO} = ±36 V, IO to GND			5	50	nA
R_{DYN}	Dynamic resistance[4]	IO to GND and GND to IO	ESD852		0.49		Ω
			ESD862		0.49		Ω
C_L	Line capacitance[1]	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV	ESD852		2.8	3.5	pF
			ESD862		2.6	2.9	pF

(1) Measured from IO to GND on each channel.
(2) V_{BRF} and V_{BRR} are defined as the voltage when ± 10 mA is applied in the positive or negative direction respectively.
(3) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5.7 Typical Characteristics – ESD852

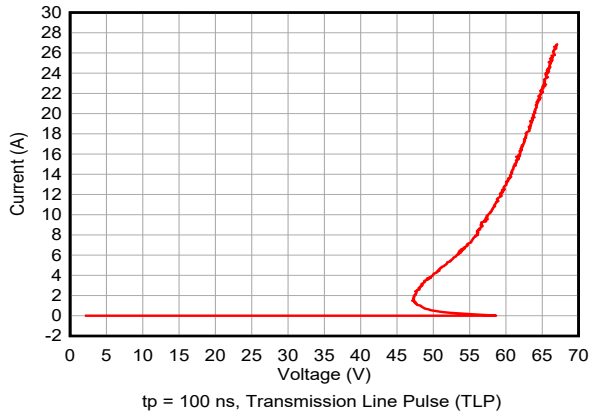

Figure 5-1. Positive TLP Curve

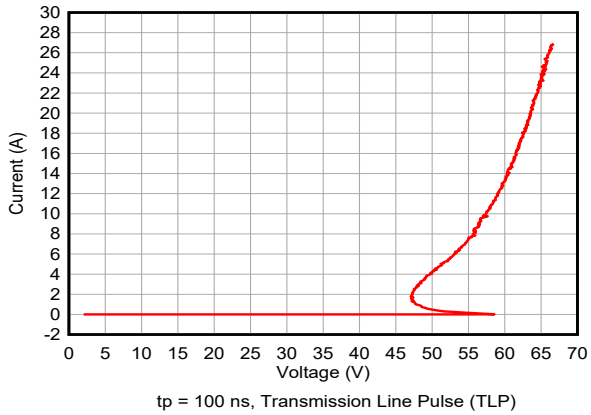

Figure 5-2. Negative TLP Curve

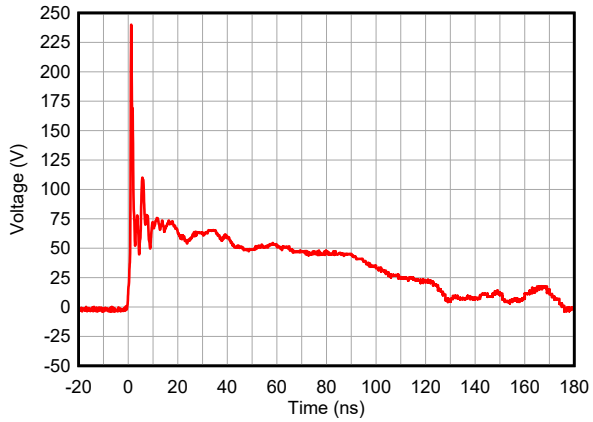

Figure 5-3. +8-kV Clamped IEC Waveform

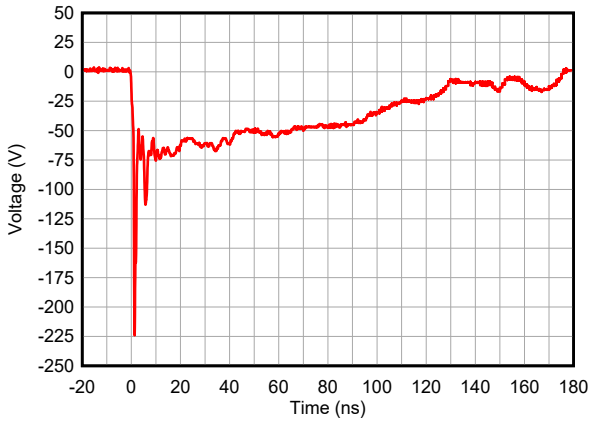

Figure 5-4. −8-kV Clamped IEC Waveform

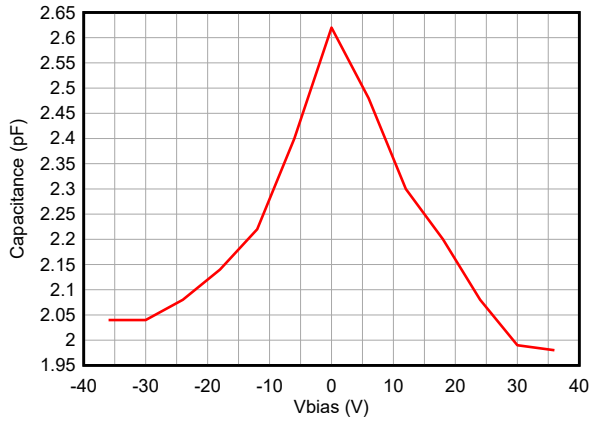

Figure 5-5. Capacitance vs. Bias Voltage

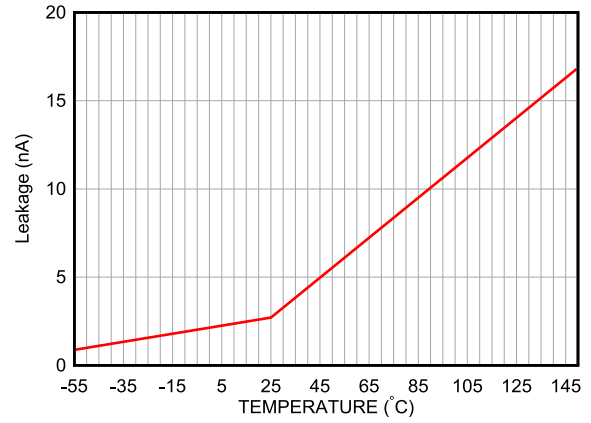

Figure 5-6. Leakage vs. Temperature

5.8 Typical Characteristics – ESD862

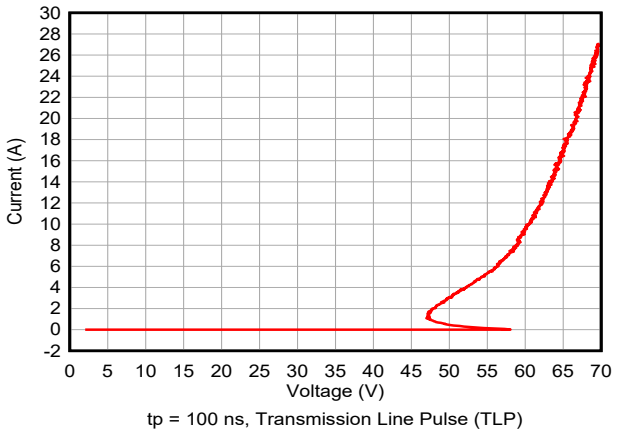

Figure 5-7. Positive TLP Curve

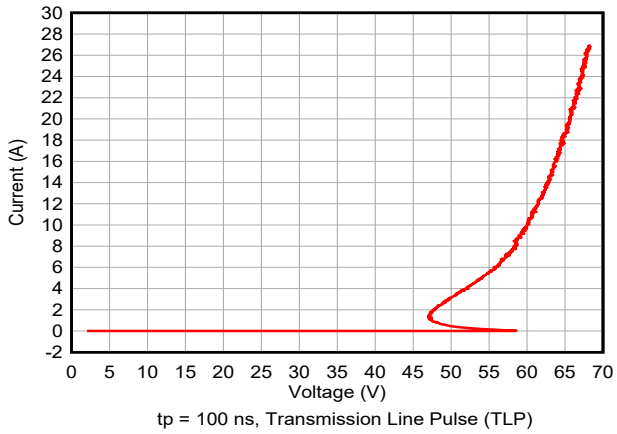

Figure 5-8. Negative TLP Curve

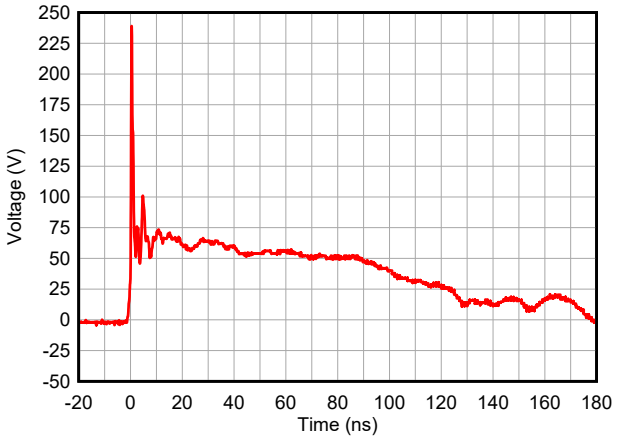

Figure 5-9. +8-kV Clamped IEC Waveform

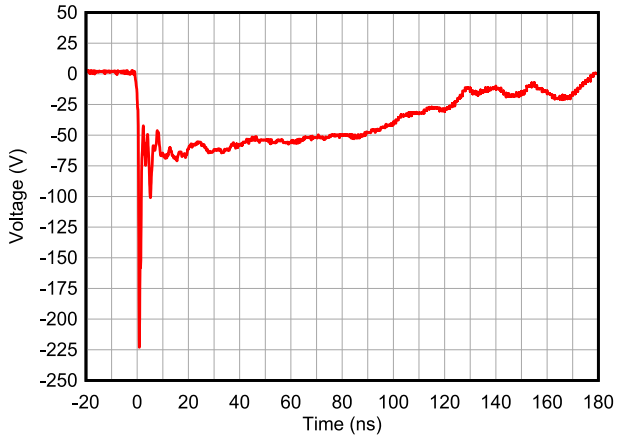

Figure 5-10. -8-kV Clamped IEC Waveform

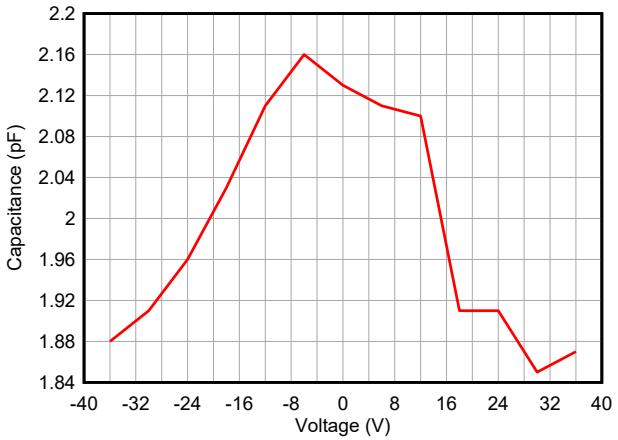

Figure 5-11. Capacitance vs. Bias Voltage

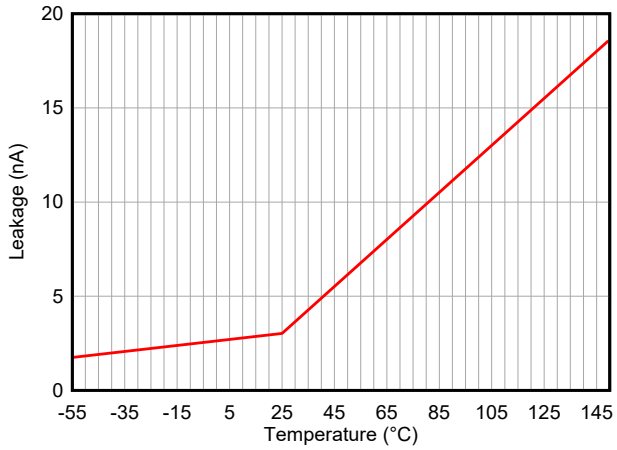

Figure 5-12. Leakage vs. Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD8x2 devices are ESD diodes which provide a path to ground for dissipating transient voltage spikes, such as ESD or surge on signal lines and power lines. Connect the devices in parallel to the down stream circuitry they are protecting. As the current from the transient passes through the ESD device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered ESD device holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

DATE	REVISION	NOTES
November 2023	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD852DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z38	Samples
ESD862DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z78	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

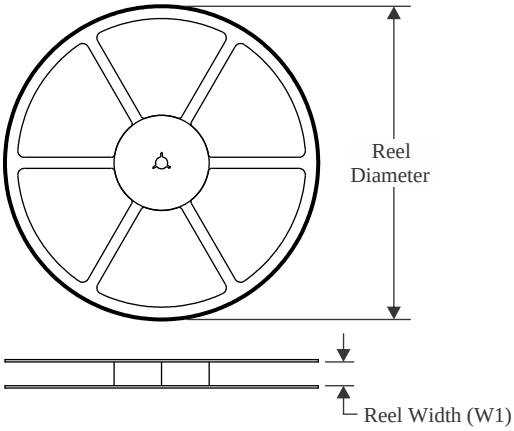
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

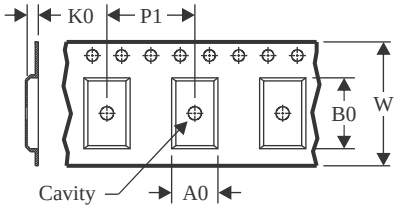
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

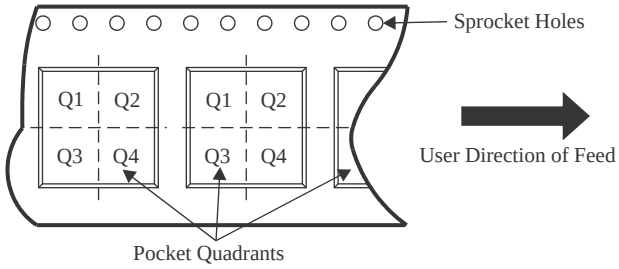


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

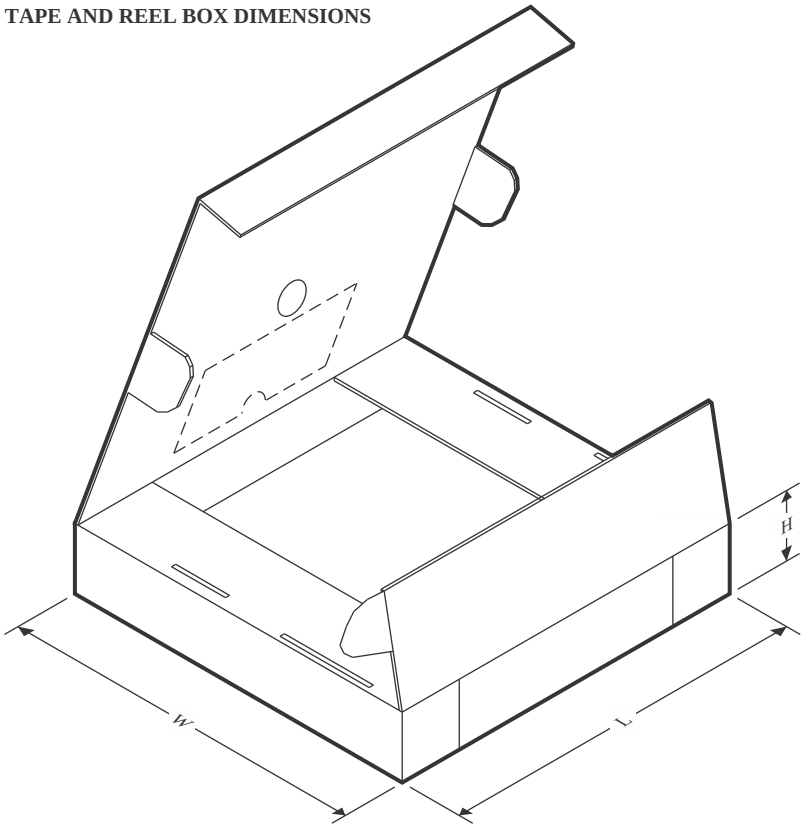
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD852DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD862DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

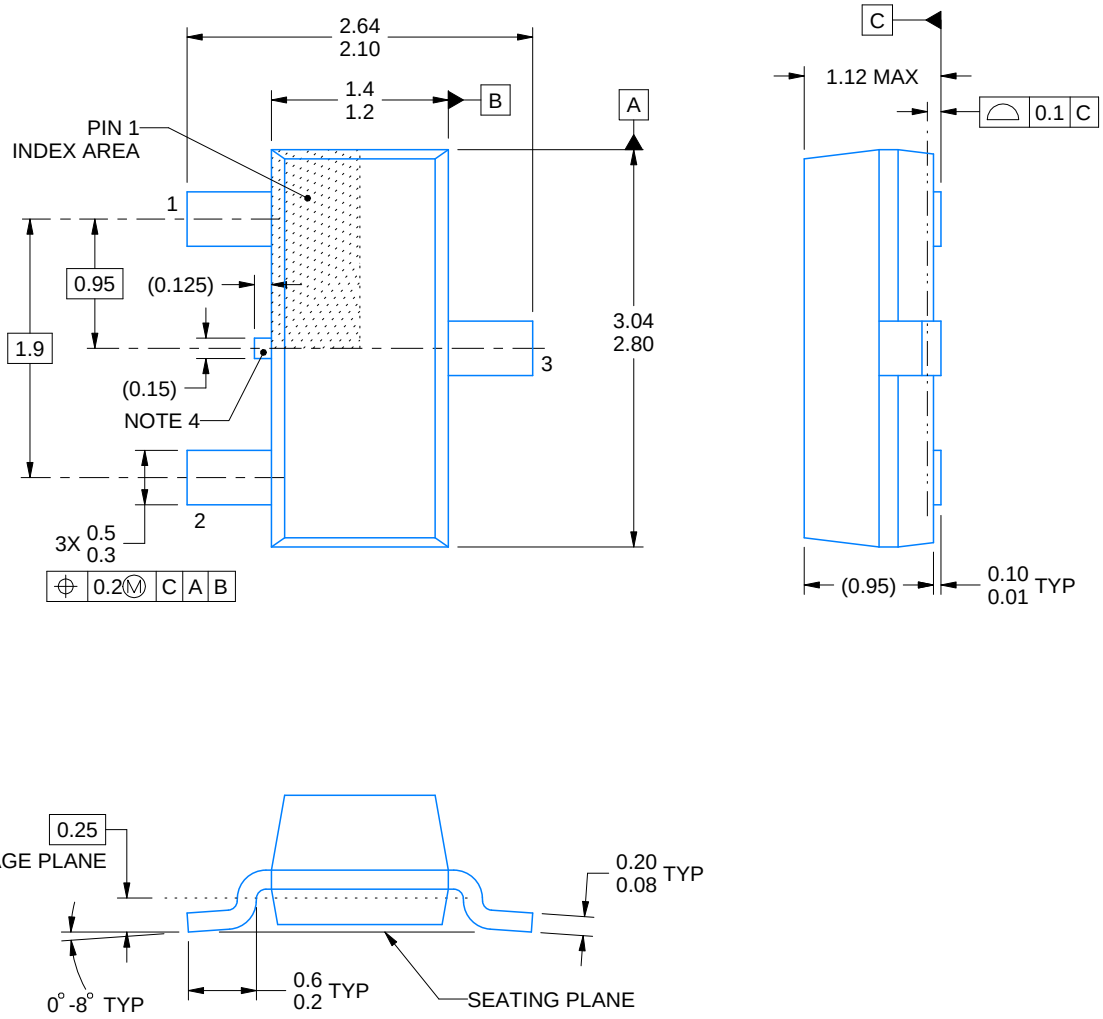
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD852DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD862DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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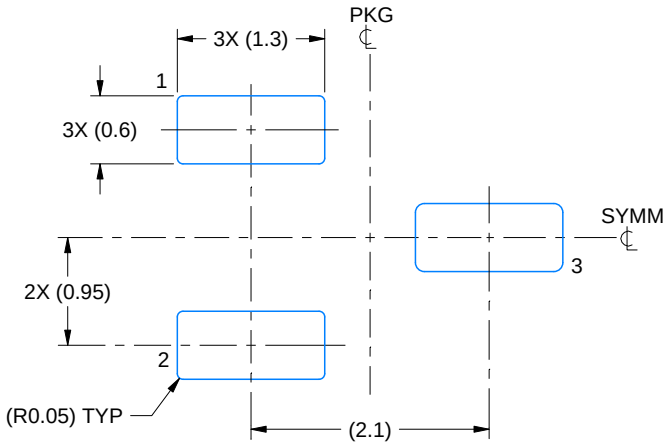
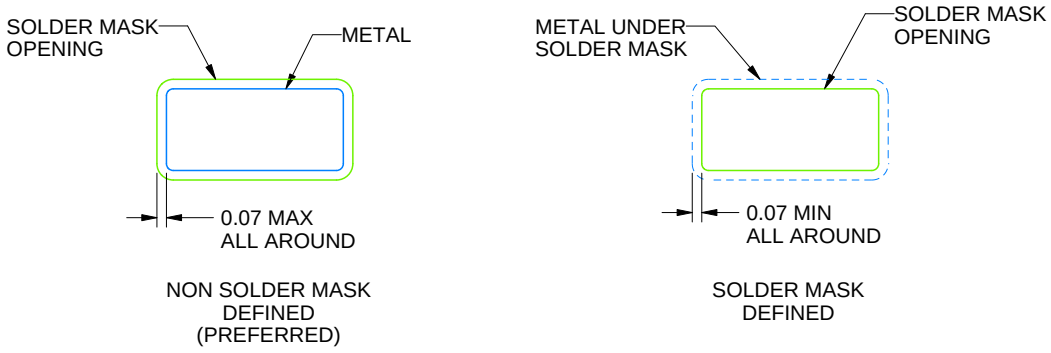
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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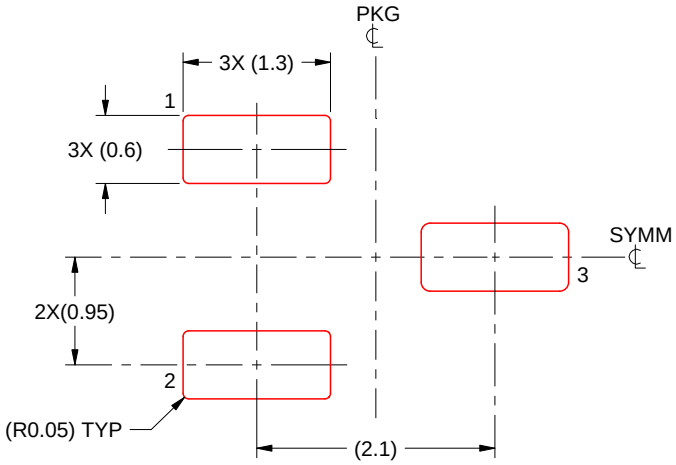
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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