10.3Gbps Thunderbolt™ Port and DisplayPort™ Switch

Check for Samples: HD3SS0001

FEATURES

- **Compatible with Thunderbolt™ Technology Electrical Standards and DisplayPort ™1.2a**
- **Wide –3dB Differential Bandwidth of Over 10GHz on 10G Path**
- **Supports DP and DP++ Configurations**
- **Handles HPD (5V tolerant) and Cable Detect**
- **Supports AUX and DDC MUX**
- **Excellent Dynamic Characteristics (on 10G path, typical values at 5GHz):**
  - **Crosstalk = –35dB**
  - **Off-Isolation = –24dB**
  - **Insertion Loss = –1.5dB**
  - **Return Loss = –20dB**
  - **Intra-pair Skew Added < 4ps**
- **Single 3.3V Power Supply**
- **Small 3x3mm 24-Pin QFN Package**
- **Low Power Consumption**
  - **3.3mW Typical Active Power**
  - **80 µW Typical Detect Mode**

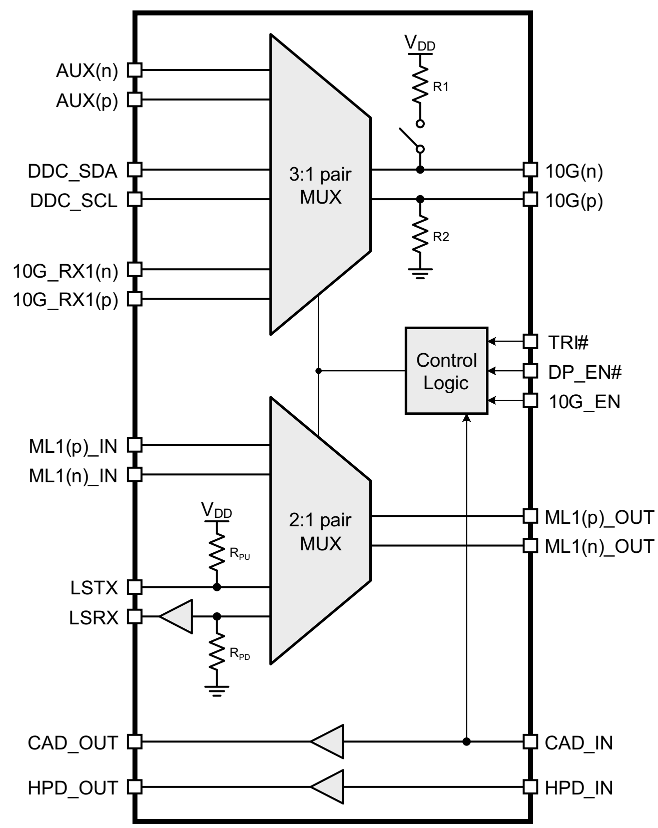
DESCRIPTION

The HD3SS0001 is a high-speed passive-switch device with integrated buffers and resistors, designed to support Thunderbolt™ technology, DisplayPort, and Dual Mode DisplayPort. The 10G path supports a high 10GHz bandwidth and excellent loss characteristics, while the DisplayPort path supports 5.4Gbps.

The integrated 3-pairs to 1-pair multiplexer (3:1 MUX) switches between DDC, AUX, and 10.3Gbps signals. The integrated 2-pairs to 1-pair multiplexer (2:1 MUX) switches between the Thunderbolt™ technology Low Speed UART transmit/receive pair and DisplayPort Main Link 1.

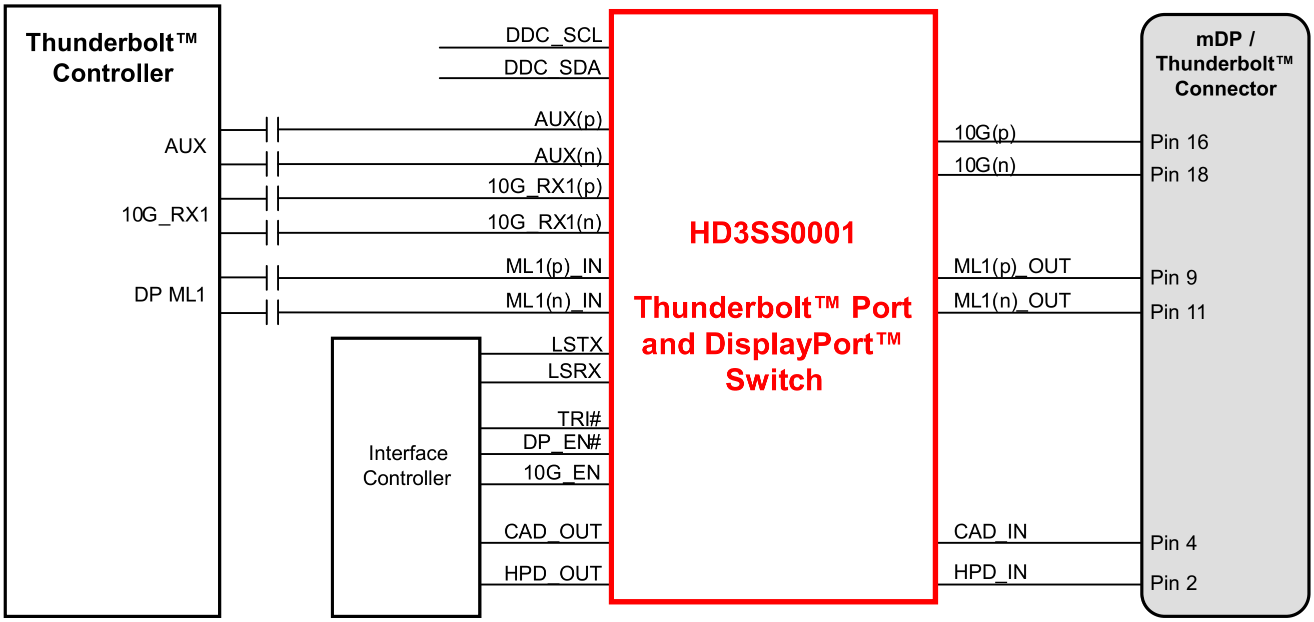
The MUXs are controlled by 4 input pins: TRI#, DP_EN#, 10G_EN, and CAD_IN (cable detect from the connector). The HD3SS0001 is packaged in a small 3x3mm 24-pin QFN, operates from a single 3.3V supply, and supports an ambient temperature range of –40°C to 85°C.

FUNCTIONAL DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION

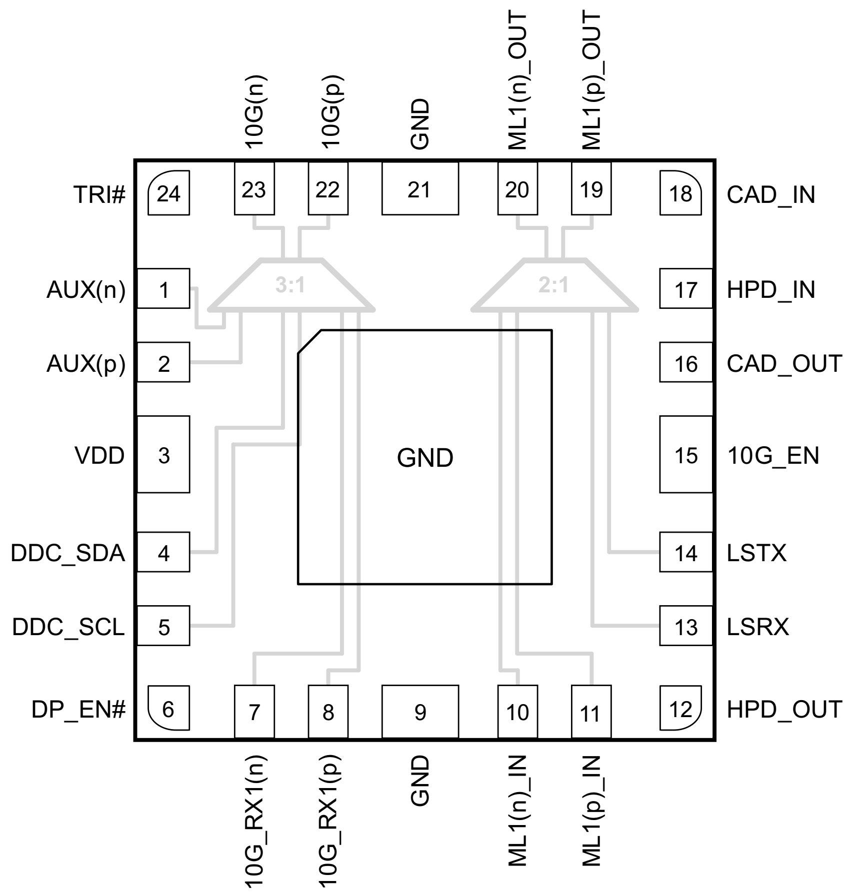


TRUTH TABLE

MODE	LOGICAL INPUT TO SET (1)				EFFECT		
	TRI#	DP_EN#	10G_EN	CAD_IN	2:1 MUX SELECTION (2)	3:1 MUX SELECTION (2)	PULL-UP RESISTOR on 10G(n)
Thunderbolt™ Protocol	1	1	1	X	LS	10G	Disconnected
	0	1	1	X	LS	Tri-stated	Disconnected
DisplayPort	1	0	0	0	ML	AUX	Connected
	0	0	0	0	Tri-Stated	Tri-stated	Connected
TMDS	1	0	0	1	ML	DDC	Connected
	0	0	0	1	Tri-Stated	Tri-stated	Connected
Detect Mode	X	1	0	X	LS	Tri-Stated	Connected
[Invalid]	X	0	1	X	Tri-Stated	Tri-Stated	Disconnected

(1) "X" = Don't Care.
(2) MUX Selection names are abbreviated.

PACKAGE PINOUT
(TOP VIEW)



MUX PIN MAPPING(1)

CONTROLLER-SIDE PIN	Connector-Side Pin
AUX(n)	10G(n)
DDC_SDA	
10G_RX1(n)	
AUX(p)	10G(p)
DDC_SCL	
10G_RX1(p)	
ML1(p)_IN	ML1(p)_OUT
LSTX	
ML1(n)_IN	ML1(n)_OUT
LSRX	

(1) NOTE: The HD3SS0001 can tolerate polarity inversions for the differential signals denoted by the (p) and (n) terminology, to ease potential board routing issues. LSTX/LSRX cannot be swapped, since LSRX is buffered and therefore unidirectional. Also, note that the integrated pullup on 10G(n) and the integrated pulldown on 10G(p) cannot be swapped.

PIN FUNCTIONS

PIN NO.	PIN NAME	I/O	SYSTEM SIDE	DESCRIPTION
11	ML1(p)_IN	I	Controller	DisplayPort MainLink1(p) input
10	ML1(n)_IN	I	Controller	DisplayPort MainLink1(n) input
24	TRI#	I	Controller	Tri-State control (see TRUTH TABLE)
6	DP_EN#	I	Controller	DisplayPort Enable, active-low (see TRUTH TABLE)
15	10G_EN	I	Controller	10.3Gbps Mode Enable (see TRUTH TABLE)
18	CAD_IN	I	Connector	Cable Detect
17	HPD_IN	I	Connector	Hot Plug Detect
2	AUX(p)	I/O	Controller	AUX Positive Signal
1	AUX(n)	I/O	Controller	AUX Negative Signal
5	DDC_SCL	I/O	Controller	DDC Clock
4	DDC_SDA	I/O	Controller	DDC Data
14	LSTX	I/O	Controller	UART TX Signal
13	LSRX	I/O	Controller	UART RX Signal
22	10G(p)	I/O	Connector	10G_RX1(p) or AUX(p) or DDC_SCL, with pull-down
23	10G(n)	I/O	Connector	10G_RX1(n) or AUX(n) or DDC_SDA, with pull-up
19	ML1(p)_OUT	I/O	Connector	DisplayPort MainLink1(p) output or LSTX
20	ML1(n)_OUT	I/O	Connector	DisplayPort MainLink1(n) output or LSRX
8	10G_RX1(p)	O	Controller	10.3Gbps Positive Signal
7	10G_RX1(n)	O	Controller	10.3Gbps Negative Signal
16	CAD_OUT	O	Controller	Cable Detect
12	HPD_OUT	O	Controller	Hot Plug Detect
3	V_{DD}	Power Supply	Controller	Power supply
9, 21, Center Pad	GND	Power Supply	Controller	Reference ground

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Supply voltage range(2)	V_{DD}	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin/buffers	–0.5	V_{DD}+0.5	
Electrostatic discharge	Human body model(3)		±1,500	V
	Charged-device model(4)		±500	
Continuous power dissipation		See Power Characteristics		

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC/ESDA JS-001-2011
(4) Tested in accordance with JEDEC JESD22 C101-E

THERMAL INFORMATION

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		HD3SS0001	UNITS
		24-PIN VQFN (RLL)	
θ_{JA}	Junction-to-ambient thermal resistance	41.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	43.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.3	
θ_{JB}	Junction-to-board thermal resistance	11.2	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	11.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

POWER CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
I_{DD}	Supply Current in Active Mode	Outputs Floating		1.0	1.3	mA
I_{DETECT}	Supply Current in Detect Mode	DP_EN# = 1, 10G_EN = 0		26	50	µA
P_D	Power Dissipation in Active Mode			3.3	4.7	mW
P_{Detect}	Power Dissipation in Detect Mode			80	150	µW

(1) The maximum ratings are simulated for V_{DD} = 3.6V.

RECOMMENDED OPERATING CONDITIONS

Typical values for all parameters are at V_{DD} = 3.3V and T_A = 25°C. (Temperature limits are specified by design)

PARAMETER		NOTES/CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6 (1)	V
T_A	Operating free-air temperature		–40		85	°C
V_{IH}	Input high voltage	CAD_IN, HPD_IN (2), TRI#, DP_EN#, and 10G_EN	2.0		V_{DD}	V
		ML1(n)_OUT (when 2:1 MUX selects LS)	2.0		V_{DD}	
V_{IL}	Input low voltage	CAD_IN, HPD_IN (2), TRI#, DP_EN#, and 10G_EN	–0.1		0.8	V
		ML1(n)_OUT (when 2:1 MUX selects LS)	–0.1		0.8	
V_{OH}	Output high voltage	CAD_OUT, HPD_OUT	2.7		V_{DD}	V
		LSRX (when 2:1 MUX selects LS)	2.7		V_{DD} (1)	
V_{OL}	Output low voltage	CAD_OUT, HPD_OUT	0.0		0.1	V
		LSRX (when 2:1 MUX selects LS)	0.0		0.1	
I_{IH}	High-level input current	TRI#, DP_EN#, 10G_EN, CAD_IN, and HPD_IN; V_{DD} = 3.6V, V_{IN} = V_{DD}			5	µA
		ML1(n)_OUT; V_{DD} = 3.6V; V_{IN} = V_{DD} (when 2:1 MUX selects LS)			3.75	
I_{IL}	Low-level input current	TRI#, DP_EN#, 10G_EN, CAD_IN, and HPD_IN; V_{DD} = 3.6V, V_{IN} = GND			100	nA
		ML1(n)_OUT; V_{DD} = 3.6V, V_{IN} = GND (when 2:1 MUX selects LS)			100	
V_{I/O_Diff}	Differential I/O voltage	AUX(p)/AUX(n), 10G_RX1(p)/ 10G_RX1(n), ML1(p)_IN/ML1(n)_IN, 10G(p)/10G(n), and ML1(p)_OUT/ML1(n)_OUT when MUX's are connected to Differential Signals.	0		1.8	Vpp
V_{I/O_CM}	Common mode I/O voltage	AUX(p)/AUX(n), 10G_RX1(p)/10G_RX1(n), ML1(p)_IN/ML1(n)_IN, 10G(p)/ 10G(n), and ML1(p)_OUT/ML1(n)_OUT when MUX's are connected to Differential Signals.	0		2.0	V

(1) V_{DD} range supports 3.0V to 3.6V, but for Thunderbolt products it is anticipated that the V_{DD} must be maintained at less than or equal to 3.4V to ensure that the V_{OH} on the LSRx do not exceed 3.4V.
(2) HPD_IN is 5V tolerant.

ELECTRICAL CHARACTERISTICS

(under recommended operation conditions)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Thunderbolt™ Technology 10.3Gbps Link: 10G_RX1(p), 10G_RX1(n) (1)						
R_L	Differential Return Loss	f = 5.0 GHz		–20		dB
I_L	Differential Insertion Loss	f = 5.0 GHz		–1.5		dB
O_{IRR}	Differential Off Isolation	f = 5.0GHz (see Figure 3)		–24		dB
X_{TALK}	Differential Crosstalk	f = 5.0 GHz		–35		dB
BW	Bandwidth	–3 dB		10		GHz
t_{PD}	Propagation Delay(from input to output)	R_{sc} and R_L = 50 Ω (see Figure 2)			200	ps
T_{SKEW}	Intra-Pair Skew Added	R_{sc} and R_L = 50 Ω (see Figure 2)			4	ps
C_{ON}	Outputs ON Capacitance	V_I = 0 V, Outputs Open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	$_{VI}$ = 0 V, Outputs Open Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V, I_O = –15 µA		7.5		Ω
ΔR_{ON}	On resistance match between pairs of the same channel	V_{DD} = 3.3V; I_O = –15 µA			1	Ω
T_{ON}	Control Line Change to MUX Output Switched	See Figure 1			400	µs
T_{OFF}					10	

(1) These values apply for CAD_IN tri-stated, unless otherwise noted.

ELECTRICAL CHARACTERISTICS (continued)

(under recommended operation conditions)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DisplayPort Link: ML1(p)_IN, ML1(n)_IN						
R_L	Differential Return Loss	f = 2.7 GHz		–16		dB
I_L	Differential Insertion Loss	f = 2.7 GHz; V_{CM} = 0 V		–0.8		dB
O_{IRR}	Differential Off-Isolation	f = 2.7 GHz (see Figure 3)		–20		dB
X_{TALK}	Differential Crosstalk	f = 2.7 GHz		–35		dB
BW	Differential Bandwidth	–3 dB		7		GHz
t_{PD}	Propagation Delay(from input to output)	R_{SC} and R_L = 50 Ω (see Figure 2)			200	ps
T_{SKEW}	Intra-pair Skew Added	R_{SC} and R_L = 50 Ω (see Figure 2)			4	ps
C_{ON}	Outputs ON Capacitance	$_{VI}$ = 0 V; Outputs Open; Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_I = 0 V; Outputs Open; Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V; I_O = –15 mA; V_{CM} = 0.5 V to 1.5 V; CAD_IN = 0 V		6	8	Ω
$ΔR_{ON}$	On resistance match between pairs of the same channel	V_{DD} = 3.3 V; I_O = -15 mA; V_{CM} = 0.5 V to 1.5 V			1	Ω
T_{ON}	Control Line Change to MUX Output Switched	See Figure 1			400	µs
T_{OFF}					10	
Thunderbolt™ Technology Low Speed UART : LSTX						
C_{ON}	Outputs ON capacitance	V_I = 0 V , Outputs Open, Switch ON		8		pF
C_{OFF}	Outputs OFF capacitance	V_I = 0 V, Outputs Open, Switch OFF		3		pF
R_{ON}	Output ON resistance	V_{DD} = 3 V, V_{CM} = 0 V to 3 V, I_O = –1 mA CAD_IN = 0 V		12	19	Ω
t_{PD}	Propagation Delay	LSTX to ML1(p)_OUT		200		ps
DisplayPort: AUX(p), AUX(n)						
C_{ON}	Outputs ON Capacitance	V_I = 0 V; Outputs Open; Switch ON		6		pF
C_{OFF}	Outputs OFF Capacitance	V_I = 0 V; Outputs Open; Switch OFF		3		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3V; I_O = –10 mA; AUX(p) = 0.3 V; AUX(n) = 3.0 V; CAD_IN = 0 V		12		Ω
$ΔR_{ON}$	On resistance match between pairs of the same channel	V_{DD} = 3.3 V; I_O = –10 mA; V_{CM} = 0.5 V to 1.5 V			1	Ω
T_{ON}	Control line change to Mux output switched	See Figure 2			40	ms
T_{OFF}					10	µs
Thunderbolt Technology Low Speed UART : LSRX						
C_{ON}	Outputs capacitance			3		pF
Z_O	Output impedance	V_{DD} = 3.3 V		60		Ω
t_{PD}	Propagation delay	ML1(n)_OUT to LSRX		3.2		ns
t_r	Rise Time	V_{DD} = 3 V	3			ns
t_f	Fall Time	V_{DD} = 3 V	3			ns
T_{ON}	Control line change to MUX Output Switched	See Figure 1			400	µs
T_{OFF}					10	µs

ELECTRICAL CHARACTERISTICS (continued)

(under recommended operation conditions)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DisplayPort : DDC_SCL, DDC_SDA						
C_{ON}	Outputs ON capacitance	V_I = 0 V, Outputs Open, Switch ON		9		pF
C_{OFF}	Outputs OFF capacitance	V_I = 0 V, Outputs Open, Switch OFF		3		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V, I_O = –10 mA, V_{CM} = 0.4 V, CAD_IN = 3.3 V		80	150	Ω
T_{ON}	Control line change to MUX output switched	See Figure 1			400	µs
T_{OFF}					10	
UART and 10G MUX Outputs : LSTX/LSRX/10G(p)/10G(n)						
R1	Integrated Pullup Resistance	10G(n) pin when in DP, TMDS, or Detect Mode		87	105	kΩ
R2	Integrated Pulldown Resistance	10G(p) pin when in DP, TMDS, or Detect Mode, or VDD = 0V		87	105	kΩ
R_{PU}	Integrated pullup resistance	LSTX		8.7		kΩ
R_{PD}	Integrated pulldown resistance	LSRX		1.2		MΩ

TEST DIAGRAMS

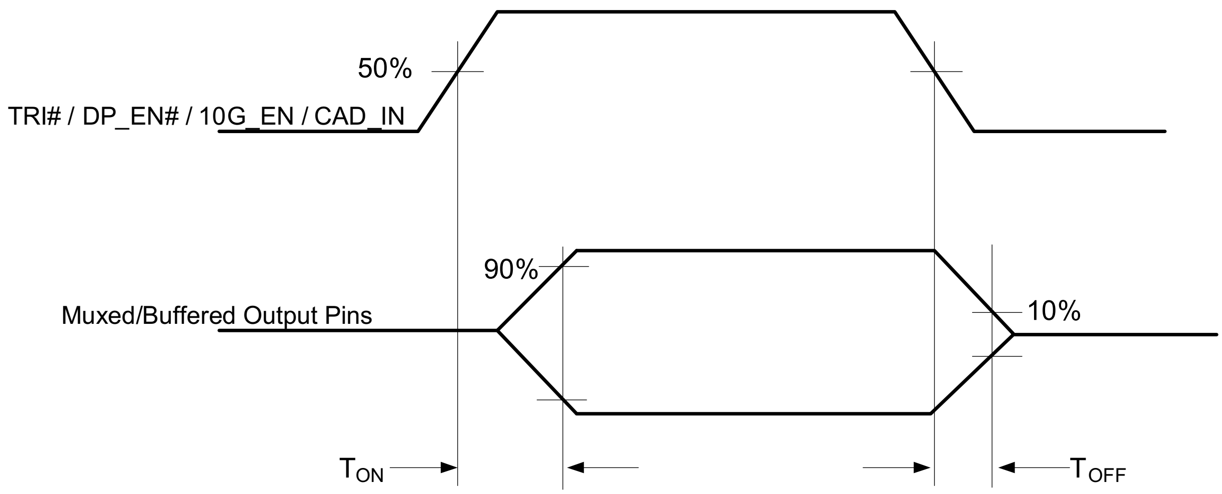
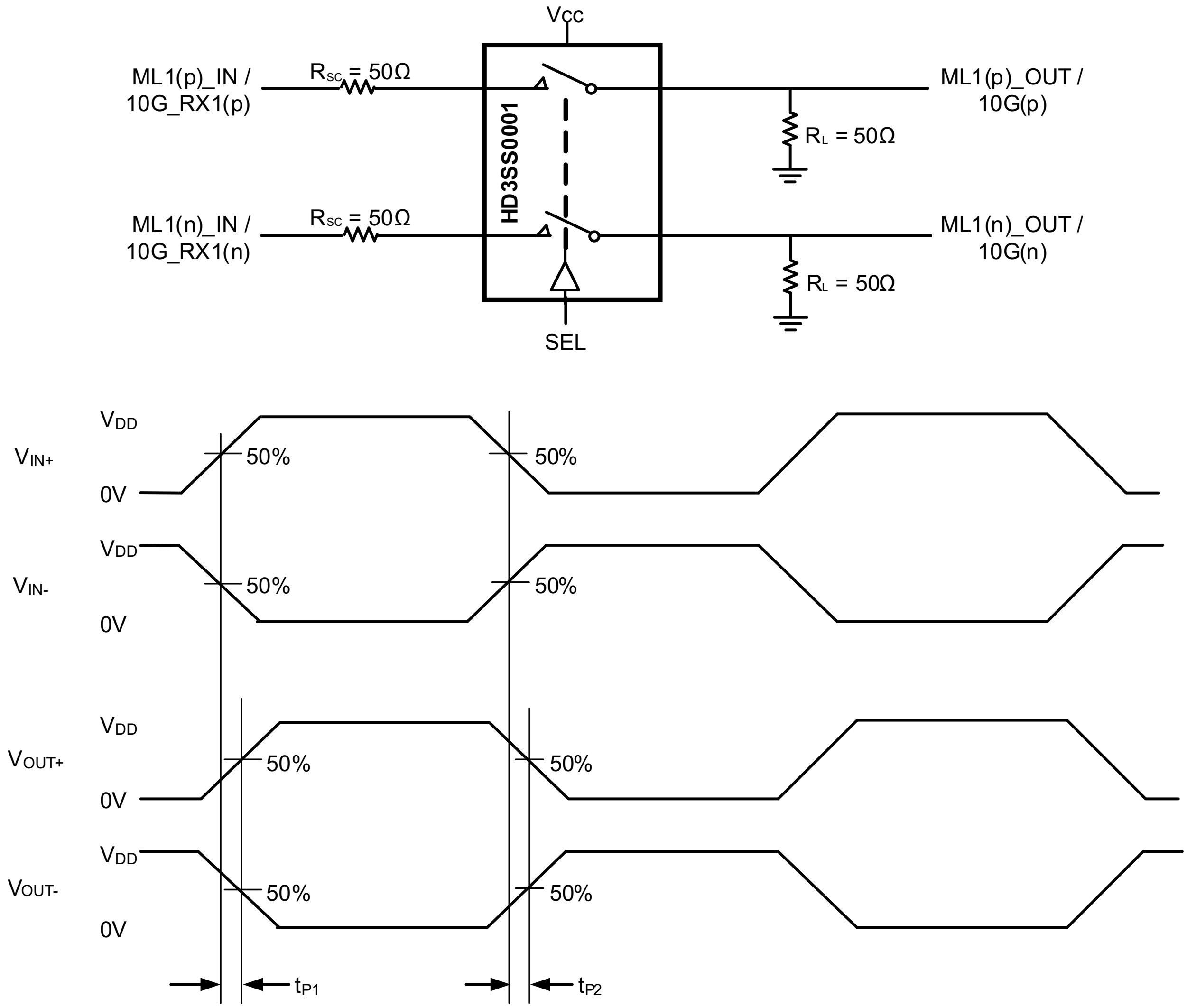


Figure 1. Control Line Change to Switched Signals



$t_{PD} = \text{Max}(t_{p1}, t_{p2})$

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b-b)}$ = Difference between t_{P1} and t_{P2} of same pair

Figure 2. Propagation Delay and Skew

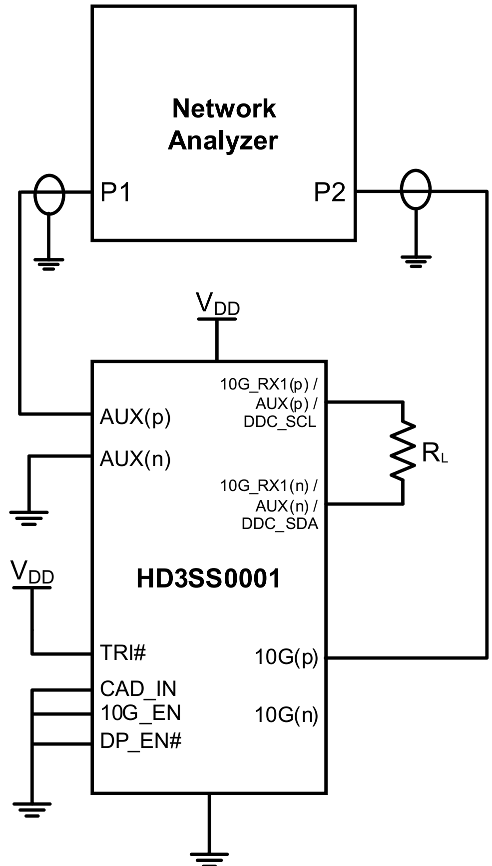


Figure 3. Off-Isolation Measurement Setup

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS0001RLLR	Active	Production	VQFN (RLL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3SS001
HD3SS0001RLLR.B	Active	Production	VQFN (RLL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3SS001

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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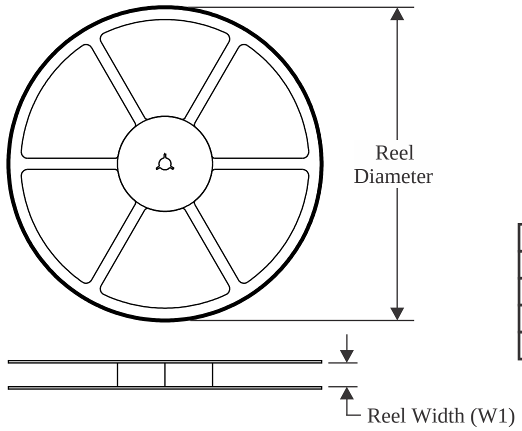
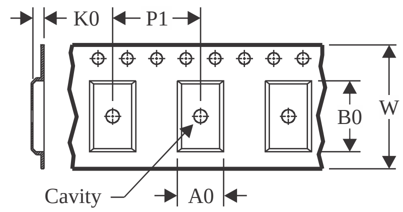
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

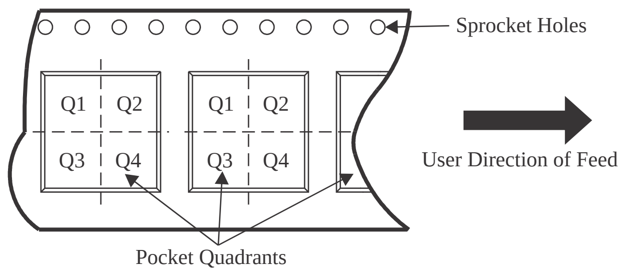


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

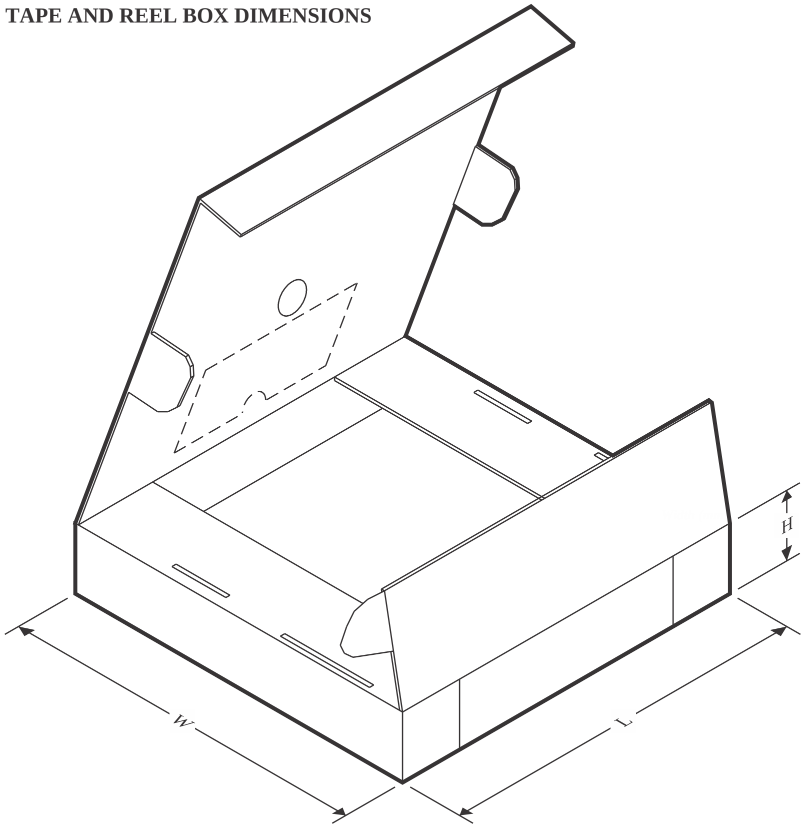
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS0001RLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

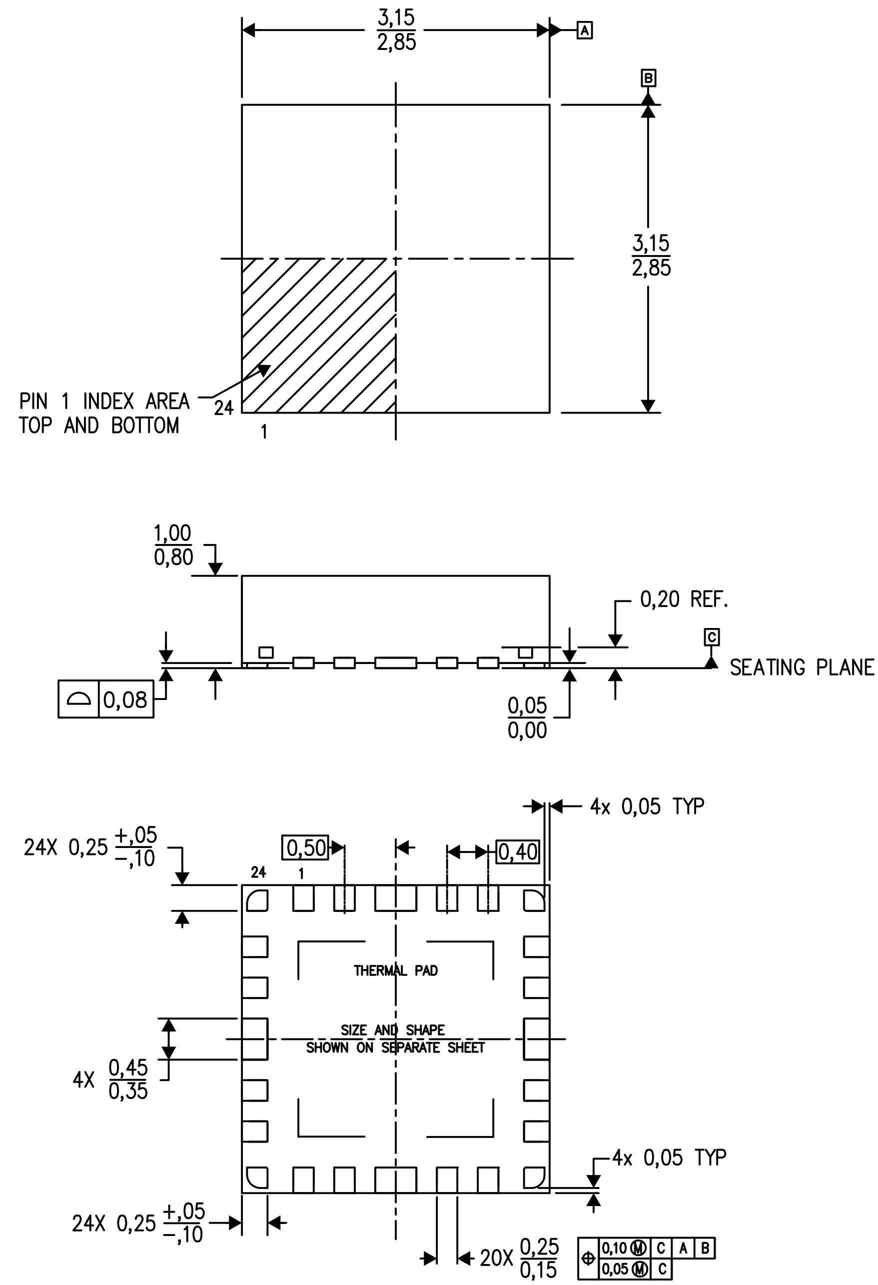
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

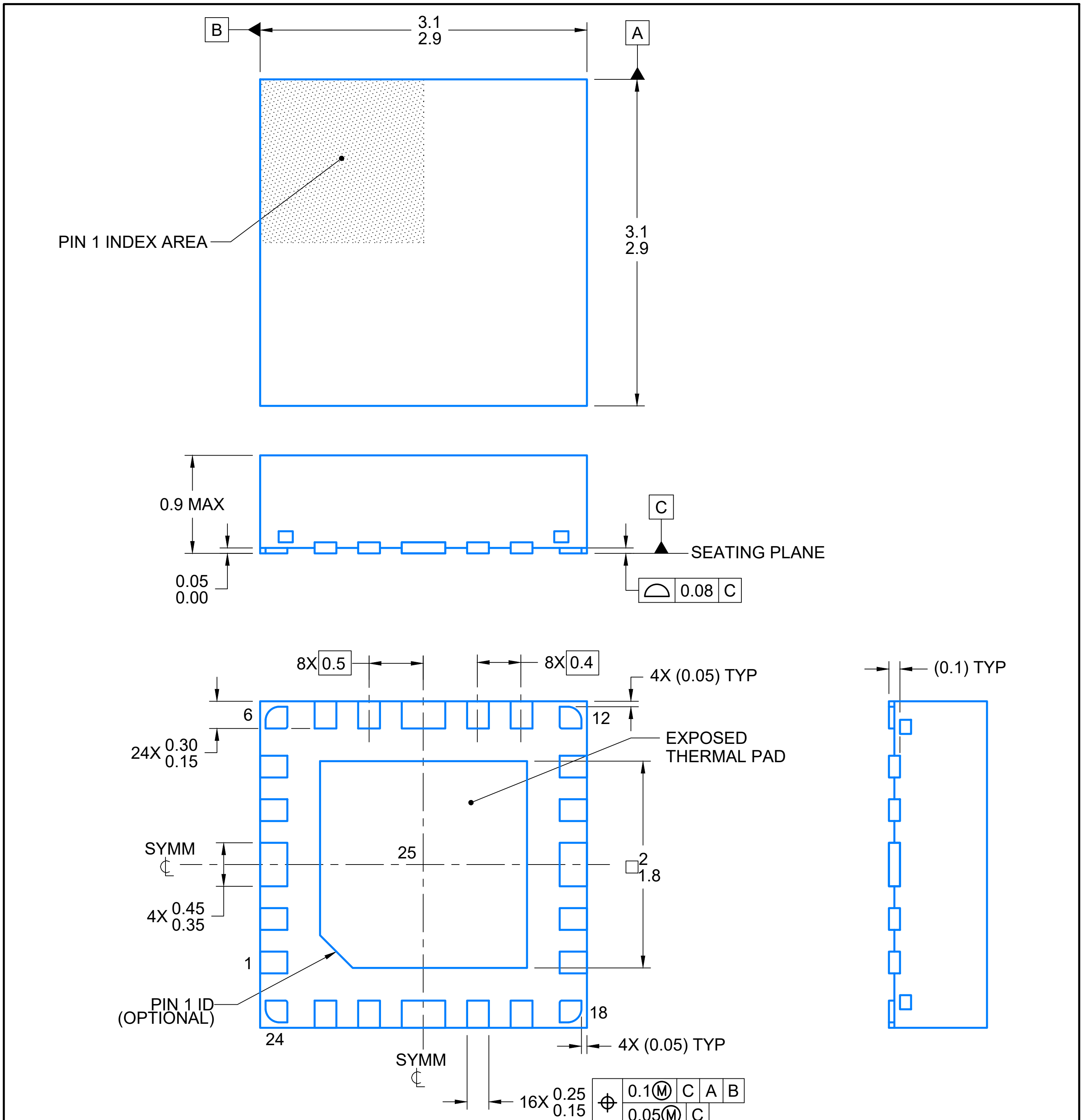
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS0001RLLR	VQFN	RLL	24	3000	346.0	346.0	33.0

RLL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4214704/C 08/13

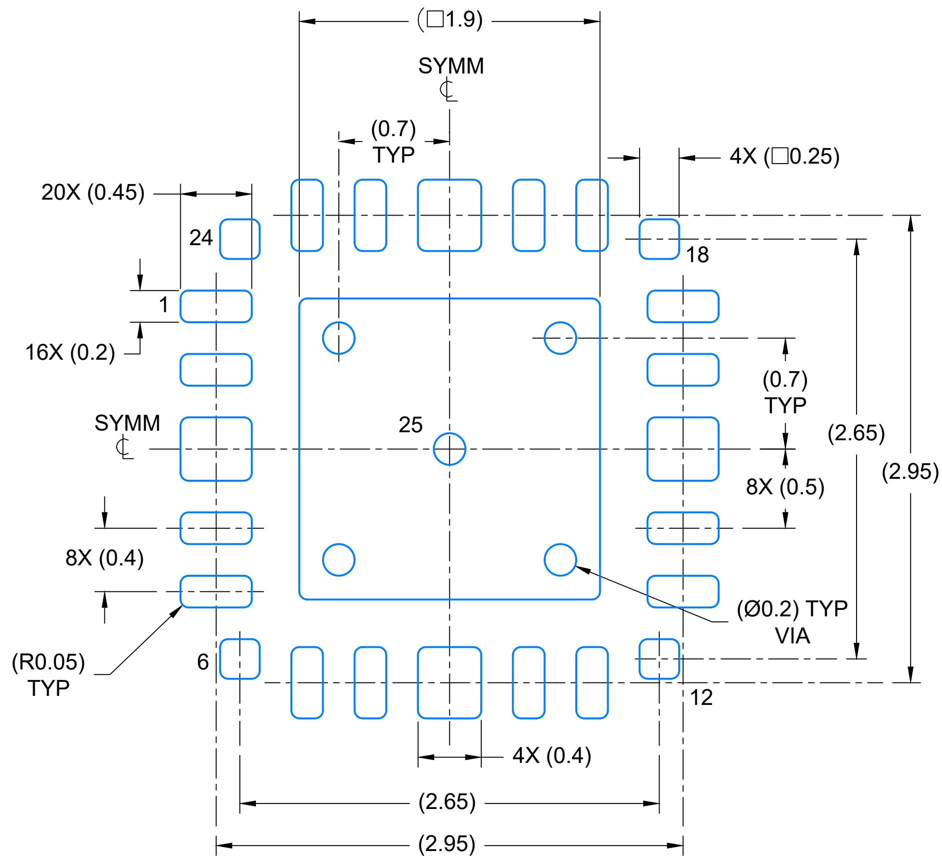
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



4217760 / C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

NON SOLDER MASK
DEFINED
(PREFERRED)

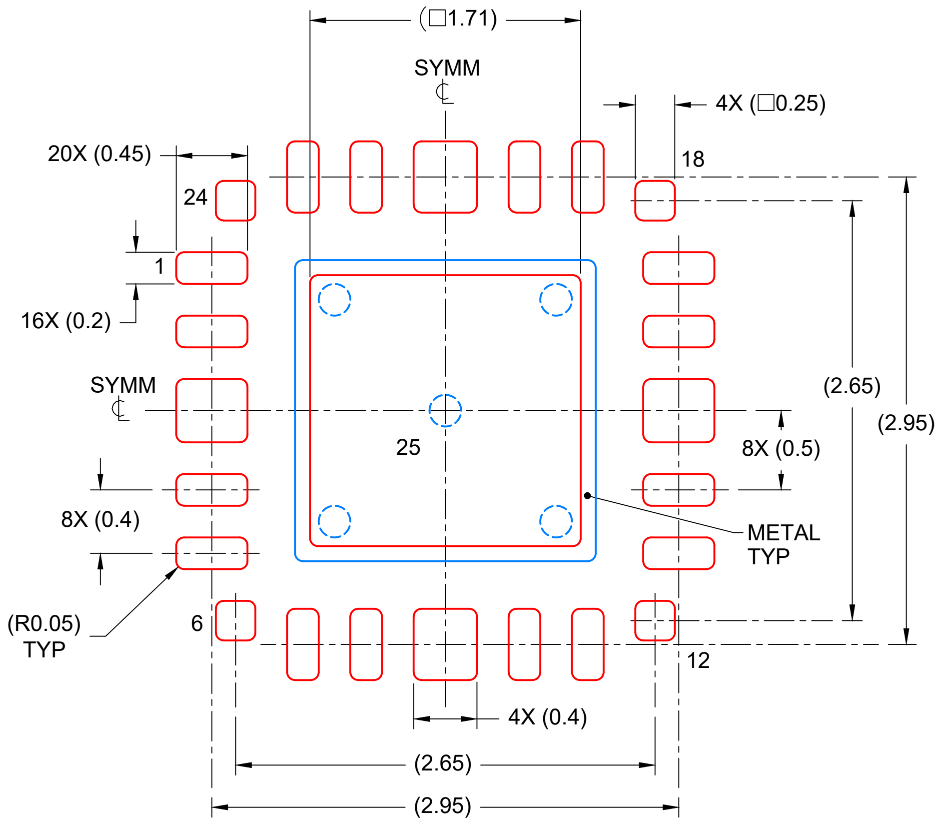
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4217760 / C 10/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..