

INA114

# Precision INSTRUMENTATION AMPLIFIER

## FEATURES

- **LOW OFFSET VOLTAGE:** 50µV max
- **LOW DRIFT:** 0.25µV/°C max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 115dB min
- **INPUT OVER-VOLTAGE PROTECTION:** ±40V
- **WIDE SUPPLY RANGE:** ±2.25 to ±18V
- **LOW QUIESCENT CURRENT:** 3mA max
- **8-PIN PLASTIC AND SOL-16**

## DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

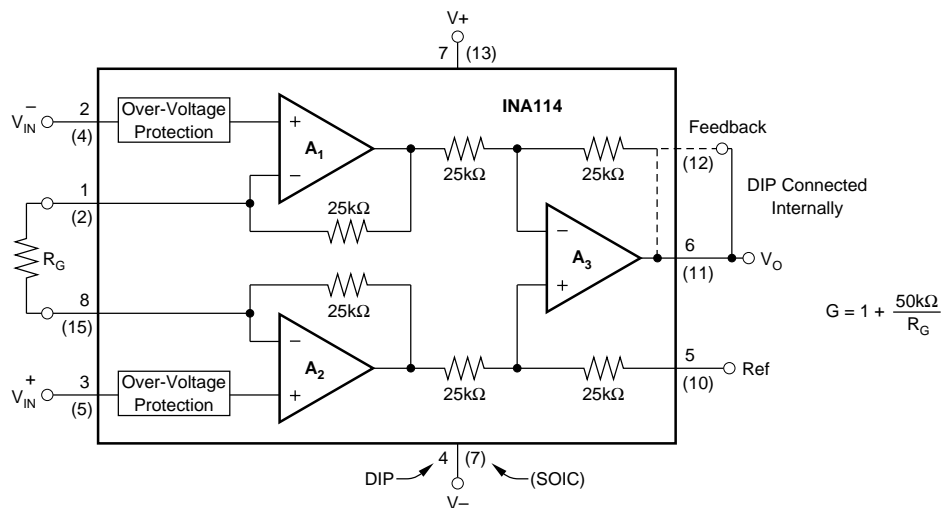
A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the -40°C to +85°C temperature range.

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111  
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 2\text{k}\Omega$ , unless otherwise noted.

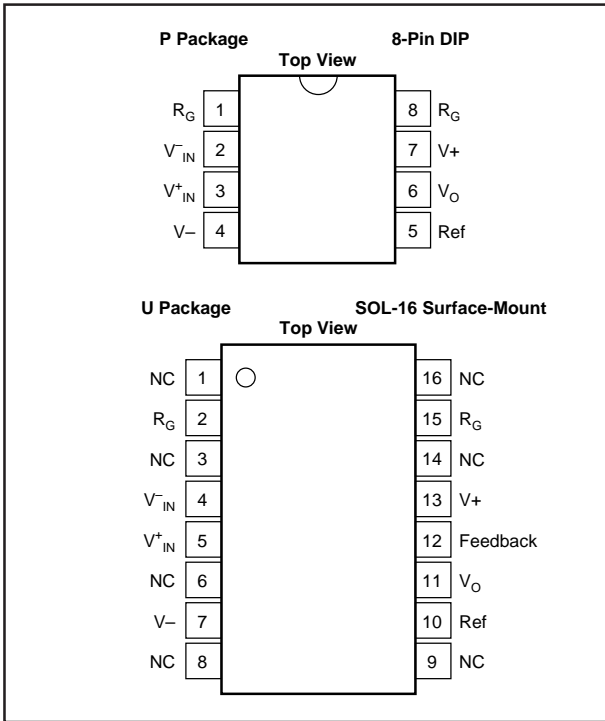
PARAMETER	CONDITIONS	INA114BP, BU			INA114AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b> Offset Voltage, RTI Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$ $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$  $V_{\text{CM}} = \pm 10\text{V}$ , $\Delta R_S = 1\text{k}\Omega$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$		$\pm 10 + 20/G$ $\pm 0.1 + 0.5/G$ $0.5 + 2/G$ $\pm 0.2 + 0.5/G$ $10^{10} \parallel 6$ $10^{10} \parallel 6$ $\pm 13.5$	$\pm 50 + 100/G$ $\pm 0.25 + 5/G$ $3 + 10/G$		$\pm 25 + 30/G$ $\pm 0.25 + 5/G$ * * * * *	$\pm 125 + 500/G$ $\pm 1 + 10/G$ * * * * *	$\mu\text{V}$ $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{mo}$ $\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$ $\text{V}$ $\text{V}$
<b>BIAS CURRENT</b> vs Temperature			$\pm 0.5$ $\pm 8$	$\pm 2$		* *	$\pm 5$	nA $\text{pA}/^\circ\text{C}$
<b>OFFSET CURRENT</b> vs Temperature			$\pm 0.5$ $\pm 8$	$\pm 2$		* *	$\pm 5$	nA $\text{pA}/^\circ\text{C}$
<b>NOISE VOLTAGE, RTI</b> $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f_B = 0.1\text{Hz}$ to $10\text{Hz}$ Noise Current $f = 10\text{Hz}$ $f = 1\text{kHz}$ $f_B = 0.1\text{Hz}$ to $10\text{Hz}$	$G = 1000$ , $R_S = 0\Omega$		15 11 11 0.4			* * * *		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$
<b>GAIN</b> Gain Equation Range of Gain Gain Error  Gain vs Temperature 50k $\Omega$ Resistance <sup>(1)</sup> Nonlinearity	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$  $G = 1$ $G = 10$ $G = 100$ $G = 1000$	1	$1 + (50\text{k}\Omega/R_G)$  $\pm 0.01$ $\pm 0.02$ $\pm 0.05$ $\pm 0.5$ $\pm 2$ $\pm 25$ $\pm 0.0001$ $\pm 0.0005$ $\pm 0.0005$ $\pm 0.002$	10000  $\pm 0.05$ $\pm 0.4$ $\pm 0.5$ $\pm 1$ $\pm 10$ $\pm 100$ $\pm 0.001$ $\pm 0.002$ $\pm 0.002$ $\pm 0.01$	*	* * * * * * * * * * * *	* * $\pm 0.5$ $\pm 0.7$ $\pm 2$ $\pm 10$ * $\pm 0.002$ $\pm 0.004$ $\pm 0.004$ $\pm 0.02$	V/V V/V % % % % ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$ % of FSR % of FSR % of FSR % of FSR
<b>OUTPUT</b> Voltage  Load Capacitance Stability Short Circuit Current	$I_O = 5\text{mA}$ , $T_{\text{MIN}}$ to $T_{\text{MAX}}$ $V_S = \pm 11.4\text{V}$ , $R_L = 2\text{k}\Omega$ $V_S = \pm 2.25\text{V}$ , $R_L = 2\text{k}\Omega$	$\pm 13.5$ $\pm 10$ $\pm 1$	$\pm 13.7$ $\pm 10.5$ $\pm 1.5$ 1000 $+20/-15$		* * *	* * *		V V V pF mA
<b>FREQUENCY RESPONSE</b> Bandwidth, -3dB  Slew Rate Settling Time, 0.01%  Overload Recovery	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $V_O = \pm 10\text{V}$ , $G = 10$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$ 50% Overdrive		1 100 10 1 0.6 18 20 120 1100 20			* * * * * * * * * *		MHz kHz kHz kHz V/ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
<b>POWER SUPPLY</b> Voltage Range Current	$V_{\text{IN}} = 0\text{V}$	$\pm 2.25$	$\pm 15$ $\pm 2.2$	$\pm 18$ $\pm 3$	* *	* *	* *	V mA
<b>TEMPERATURE RANGE</b> Specification Operating $\theta_{\text{JA}}$		-40 -40	80 80	85 125	* *		* *	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

\* Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50k $\Omega$ " term in the gain equation.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATIONS



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
INA114AP	8-Pin Plastic DIP	006	-40°C to +85°C
INA114BP	8-Pin Plastic DIP	006	-40°C to +85°C
INA114AU	SOL-16 Surface-Mount	211	-40°C to +85°C
INA114BU	SOL-16 Surface-Mount	211	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

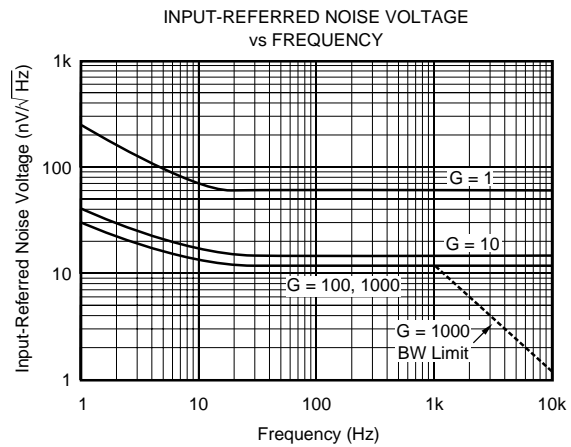
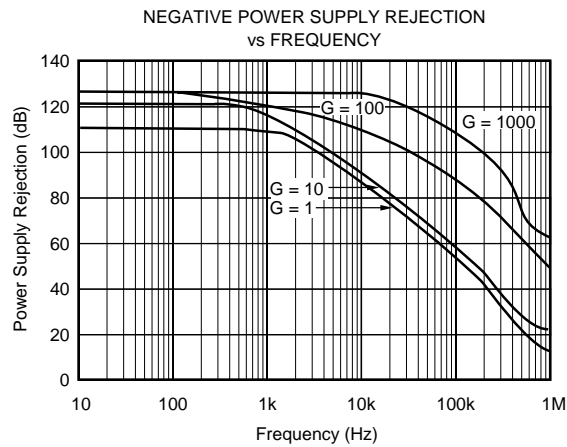
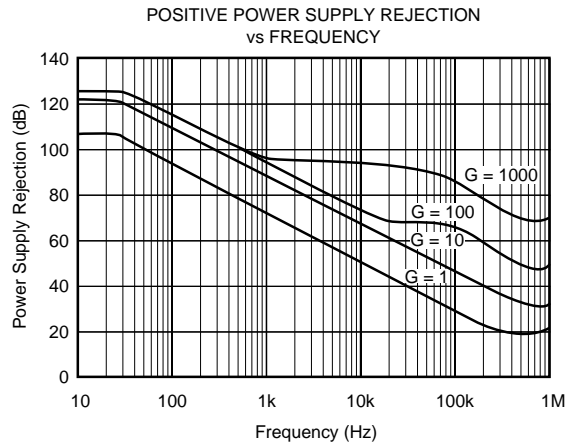
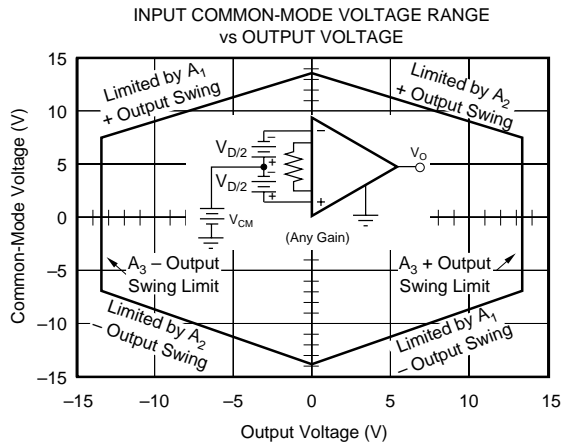
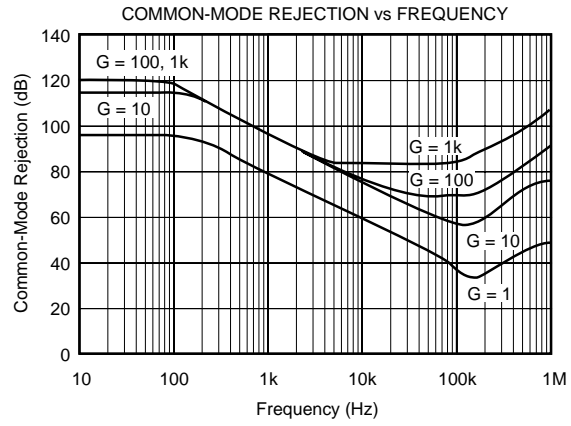
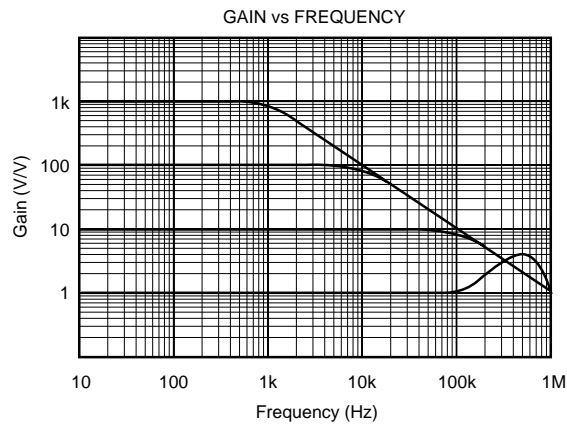
### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage .....	±18V
Input Voltage Range .....	±40V
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-40°C to +125°C
Junction Temperature .....	+150°C
Lead Temperature (soldering, 10s) .....	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

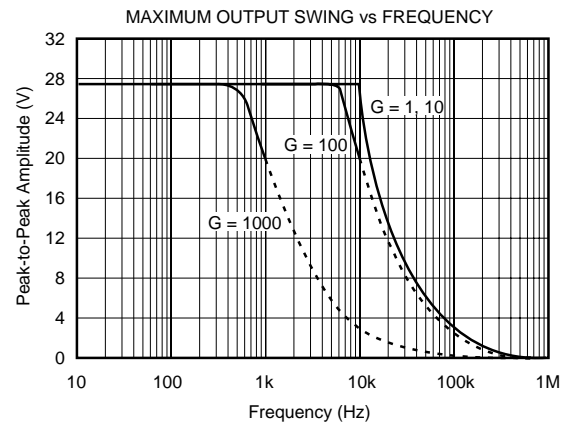
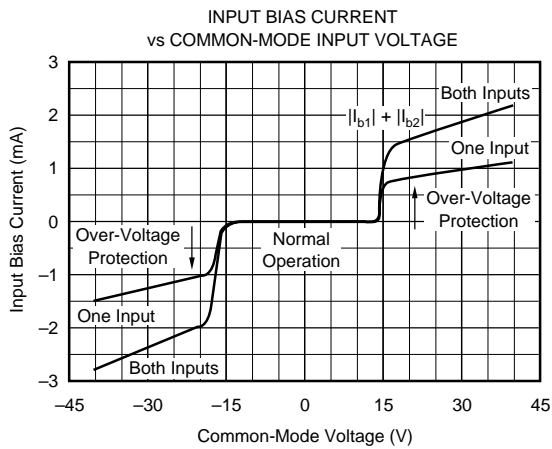
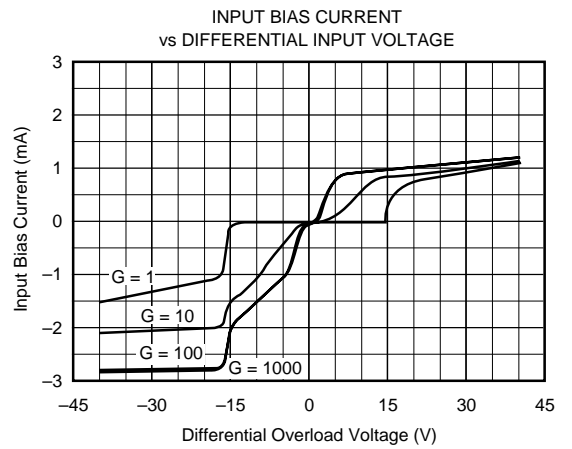
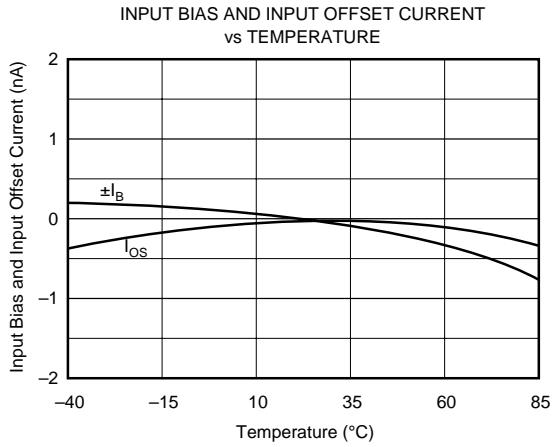
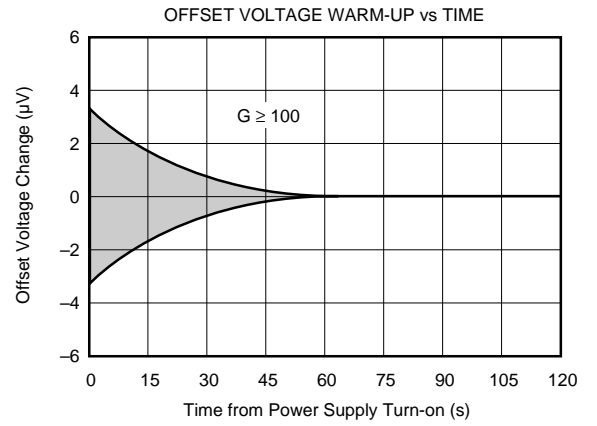
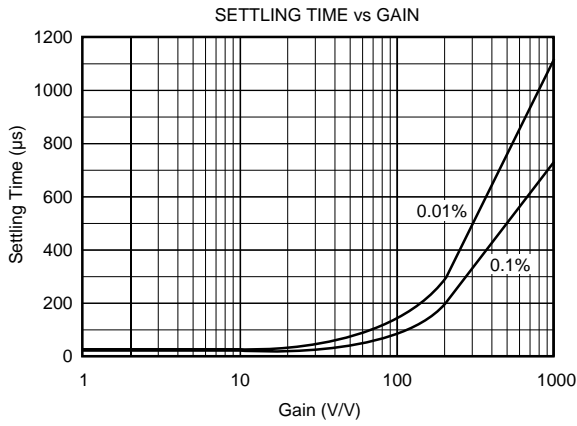
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



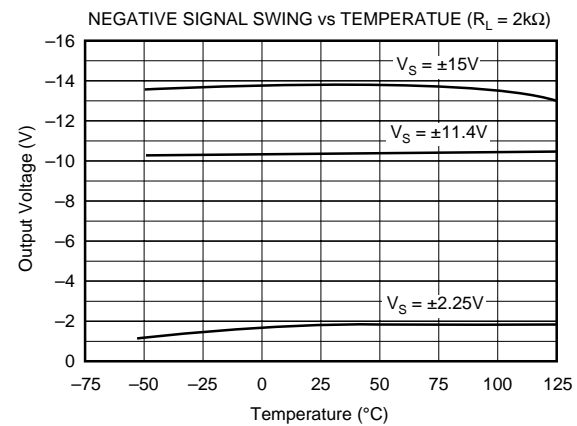
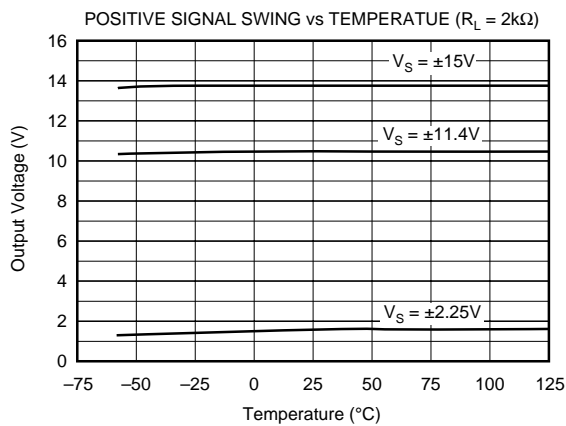
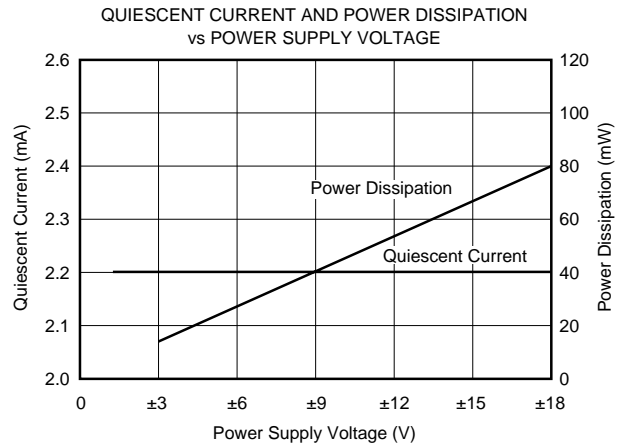
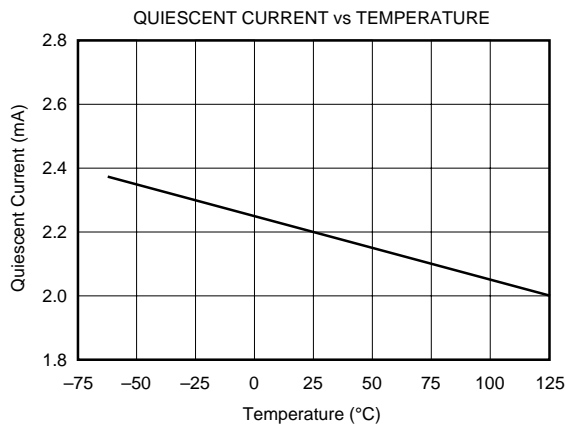
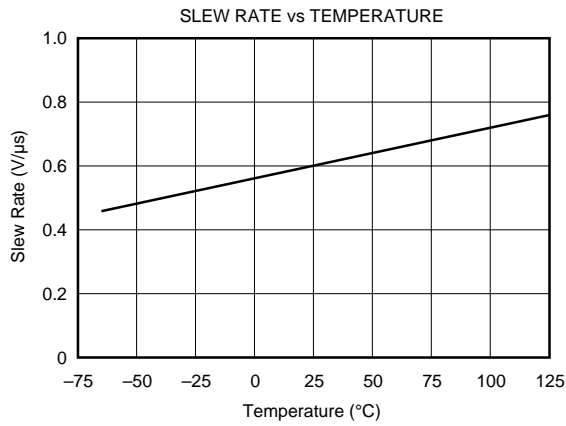
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.



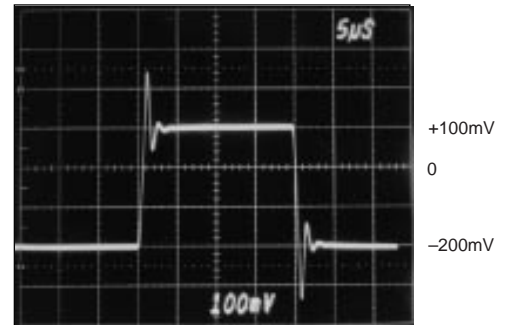
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

LARGE SIGNAL RESPONSE,  $G = 1$



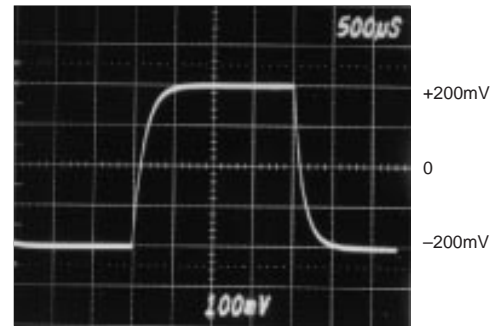
SMALL SIGNAL RESPONSE,  $G = 1$



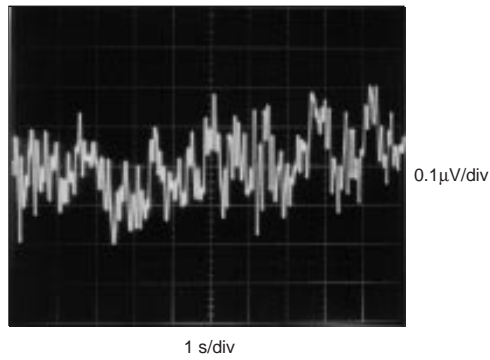
LARGE SIGNAL RESPONSE,  $G = 1000$



SMALL SIGNAL RESPONSE,  $G = 1000$



INPUT-REFERRED NOISE, 0.1 to 10Hz



# APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G = 1$ ).

## SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor,  $R_G$ :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute val-

ues. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

## NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA114 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

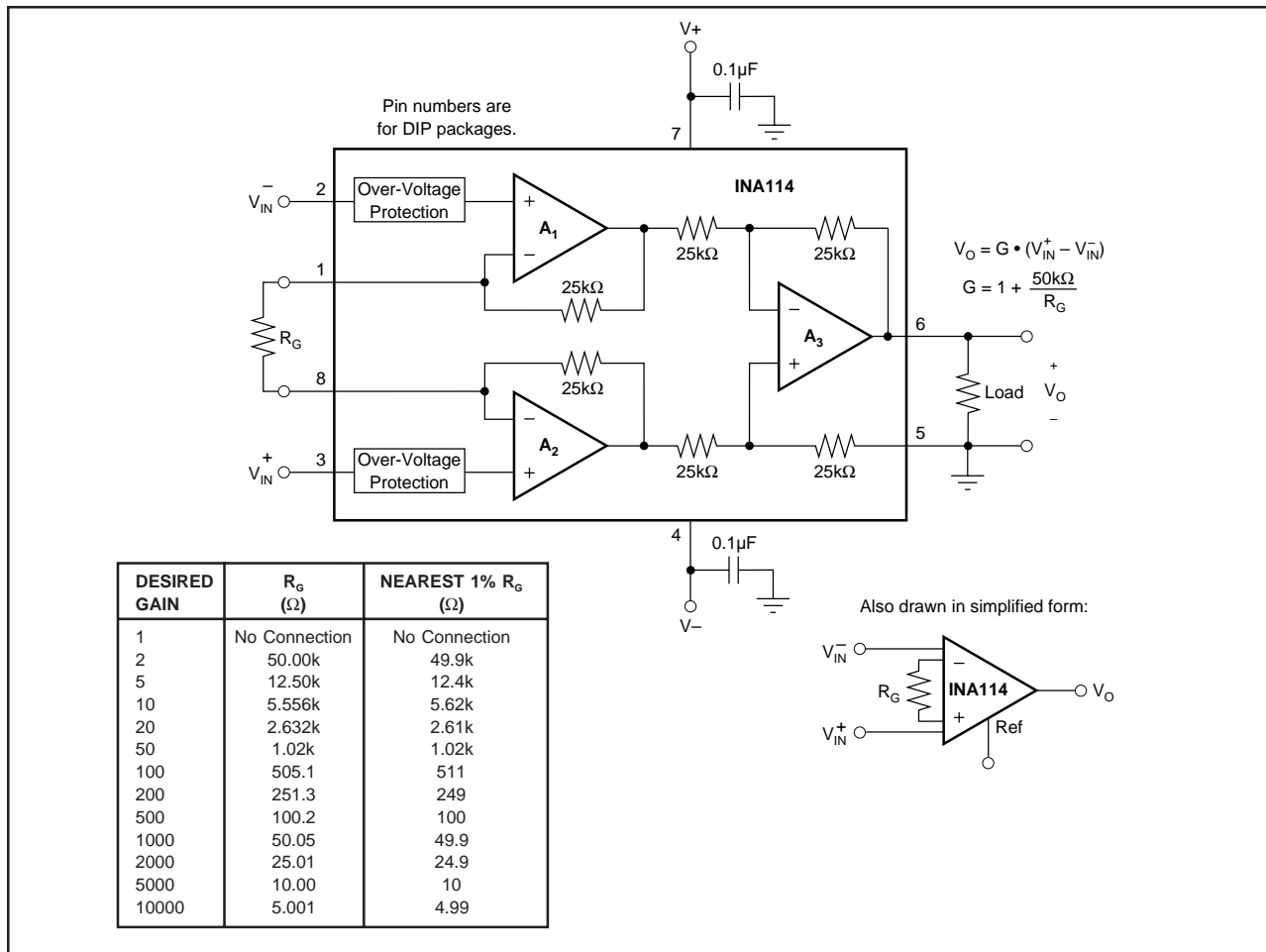


FIGURE 1. Basic Connections.



## OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

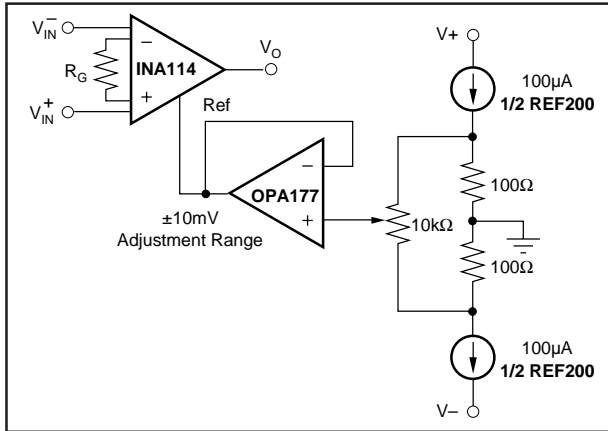


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than  $\pm 1\text{nA}$  (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

## INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately  $\pm 13.75\text{V}$  (or  $1.25\text{V}$  from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers,  $A_1$  and  $A_2$ . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage.”

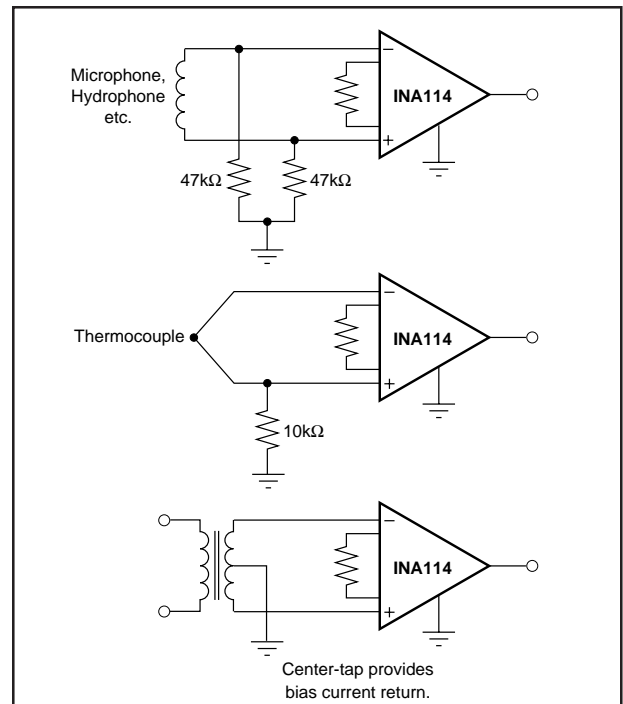


FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of  $A_1$  or  $A_2$  to saturate. Figure 4 shows the output voltage swing of  $A_1$  and  $A_2$  expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier,  $A_3$ . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of  $+20\text{V}$  on one input and  $+40\text{V}$  on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near  $0\text{V}$  even though both inputs are overloaded.

## INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to  $\pm 40\text{V}$ . For example, a condition of  $-40\text{V}$  on one input and  $+40\text{V}$  on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately  $1.5\text{mA}$ ). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input

current limit behavior. The inputs are protected even if no power supply voltage is present.

### OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through  $C_1$ . Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).



FIGURE 4. Voltage Swing of  $A_1$  and  $A_2$ .



FIGURE 5. Remote Load and Ground Sensing.



FIGURE 6. Buffered Output for Heavy Loads.



FIGURE 7. Shield Driver Circuit.



FIGURE 8. RTD Temperature Measurement Circuit.

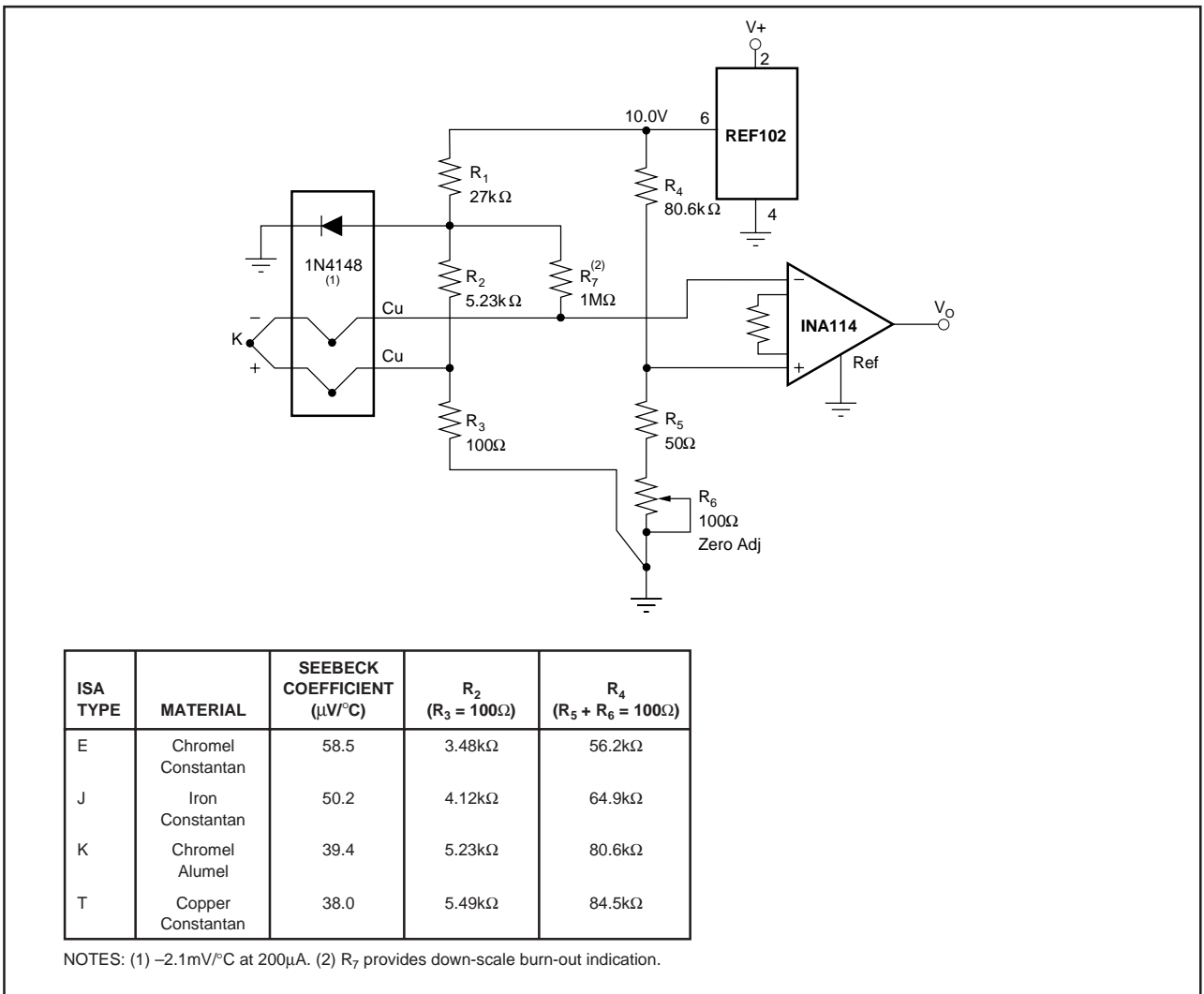


FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

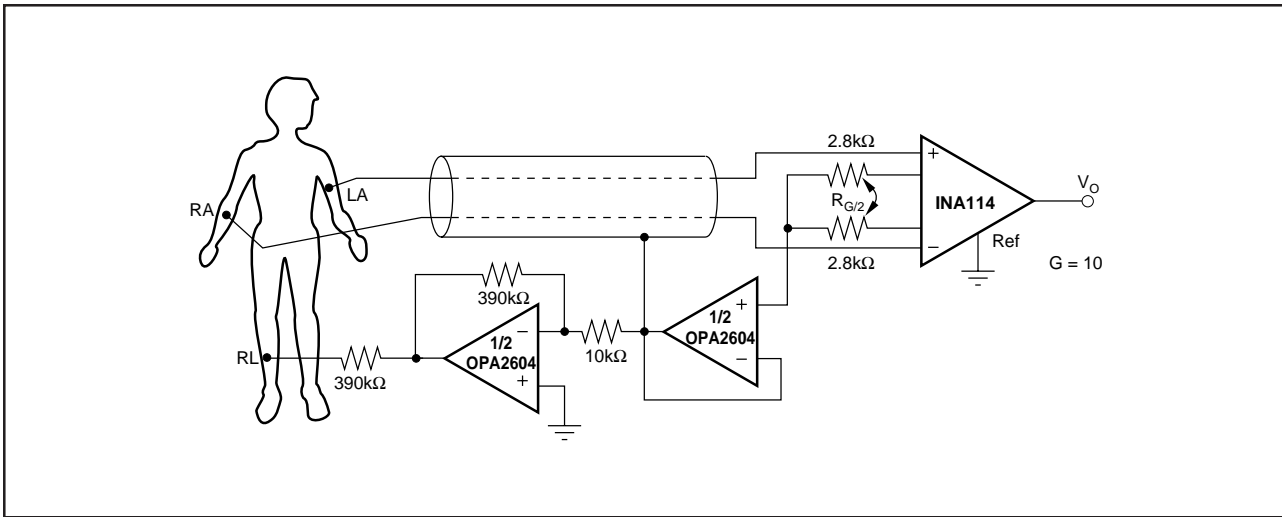


FIGURE 10. ECG Amplifier With Right-Leg Drive.

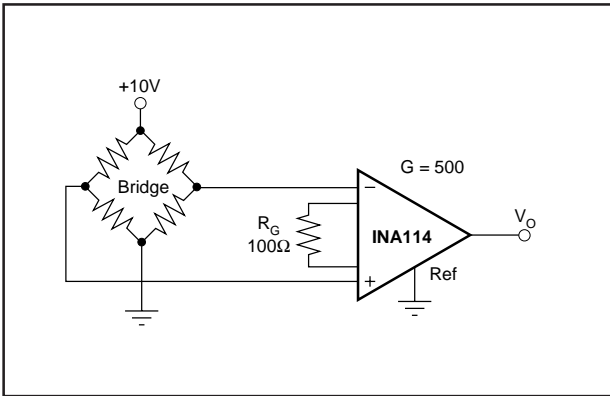


FIGURE 11. Bridge Transducer Amplifier.

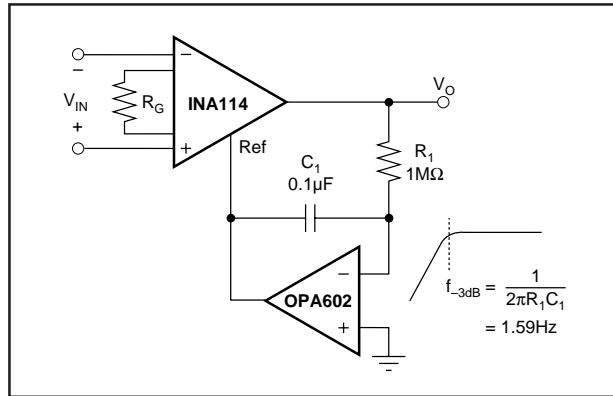


FIGURE 12. AC-Coupled Instrumentation Amplifier.

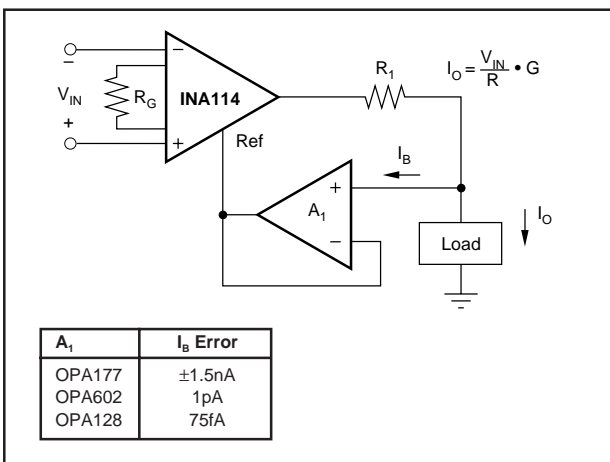


FIGURE 13. Differential Voltage-to-Current Converter.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA114AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114AP	<a href="#">Samples</a>
INA114APG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114AP	<a href="#">Samples</a>
INA114AU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU	<a href="#">Samples</a>
INA114AU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA114AU	<a href="#">Samples</a>
INA114AU/1KE4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	INA114AU	<a href="#">Samples</a>
INA114AUE4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU	<a href="#">Samples</a>
INA114BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114BP	<a href="#">Samples</a>
INA114BPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114BP	<a href="#">Samples</a>
INA114BU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA114BU	<a href="#">Samples</a>
INA114BU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI	Level-3-260C-168 HR		INA114BU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA114BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA114AU/1K	SOIC	DW	16	1000	356.0	356.0	35.0
INA114BU/1K	SOIC	DW	16	1000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA114AP	P	PDIP	8	50	506	13.97	11230	4.32
INA114APG4	P	PDIP	8	50	506	13.97	11230	4.32
INA114AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114AUE4	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BP	P	PDIP	8	50	506	13.97	11230	4.32
INA114BPG4	P	PDIP	8	50	506	13.97	11230	4.32
INA114BU	DW	SOIC	16	40	507	12.83	5080	6.6

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated