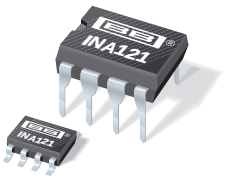
BURR - BROWN®



INA121

FET-Input, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: ±4pA
- LOW QUIESCENT CURRENT: ±450µA
- LOW INPUT OFFSET VOLTAGE: ±200µV
- LOW INPUT OFFSET DRIFT: ±2µV/°C
- LOW INPUT NOISE: 20nV/√Hz at f = 1kHz (G =100)
- HIGH CMR: 106dB
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW NONLINEARITY ERROR: 0.001% max
- INPUT PROTECTION TO ±40V
- 8-PIN DIP AND SO-8 SURFACE MOUNT

APPLICATIONS

- LOW-LEVEL TRANSDUCER AMPLIFIERS Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIERS ECG, EEG, EMG, Respiratory
- HIGH IMPEDANCE TRANSDUCERS
- CAPACITIVE SENSORS
- MULTI-CHANNEL DATA ACQUISITION
- PORTABLE, BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION

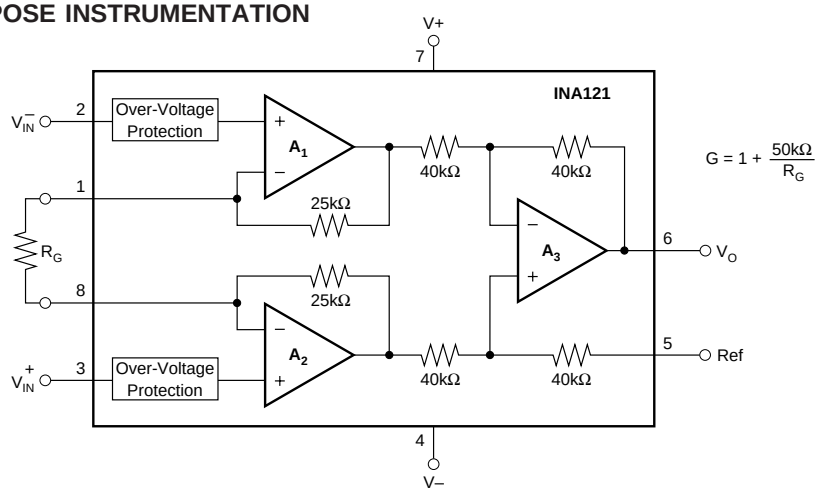
DESCRIPTION

The INA121 is a FET-input, low power instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and very small size make it ideal for a variety of general purpose applications. Low bias current (±4pA) allows use with high impedance sources.

Gain can be set from 1V to 10,000V/V with a single external resistor. Internal input protection can withstand up to ±40V without damage.

The INA121 is laser-trimmed for very low offset voltage (±200µV), low offset drift (±2µV/°C), and high common-mode rejection (106dB at G = 100). It operates on power supplies as low as ±2.25V (+4.5V), allowing use in battery operated and single 5V systems. Quiescent current is only 450µA.

Package options include 8-pin plastic DIP and SO-8 surface mount. All are specified for the –40°C to +85°C industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1412A
Printed in U.S.A. May, 1998

SBOS078

SPECIFICATIONS: V_S = ±15V

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, and IA reference = 0V, unless otherwise noted.

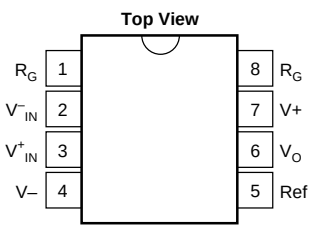
PARAMETER	CONDITIONS	INA121P, U			INA121PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI			±200±200/G	±500±500/G		±300±200/G	±1000±1000/G	µV
vs Temperature			±2±2/G	±5±20/G		*	±15±20/G	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±5±20/G	±50±150/G		*	*	µV/V
Long-Term Stability			±0.5			*		µV/mo
Impedance, Differential			10^{12} || 1			*		Ω || pF
Common-Mode	V_O = 0V		10^{12} || 12			*		Ω || pF
Input Voltage Range			See Text and Typical Curves			*		
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = –12.5V to 13.5V							
	G = 1	78	86		72	*		dB
	G = 10	91	100		85	*		dB
	G = 100	96	106		90	*		dB
	G = 1000		106			*		dB
BIAS CURRENT	V_{CM} = 0V		±4	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Offset Current			±0.5			*		pA
vs Temperature			See Typical Curve			*		
NOISE, RTI	R_S = 0Ω							
Voltage Noise: f = 10Hz	G = 100		30			*		nV/√Hz
f = 100Hz	G = 100		21			*		nV/√Hz
f = 1kHz	G = 100		20			*		nV/√Hz
f = 0.1Hz to 10Hz	G = 100		1			*		µVp-p
Current Noise: f = 1kHz			1			*		fA/√Hz
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10,000	*		*	V/V
Gain Error	V_O = –14V to 13.5V							
	G = 1		±0.01	±0.05		*	±0.1	%
	G = 10		±0.03	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5			*		%
Gain vs Temperature[1]	G = 1		±1	±10		*	*	ppm/°C
	G > 1		±25	±100		*	*	ppm/°C
Nonlinearity	V_O = –14V to 13.5V							
	G = 1		±0.0002	±0.001		*	±0.002	% of FSR
	G = 10		±0.0015	±0.005		*	±0.008	% of FSR
	G = 100		±0.0015	±0.005		*	±0.008	% of FSR
	G = 1000		±0.002			*		% of FSR
OUTPUT								
Voltage: Positive	R_L = 100kΩ		(V+)–0.9			*		V
Negative	R_L = 100kΩ		(V–)+0.15			*		V
Positive	R_L = 10kΩ	(V+)–1.5	(V+)–0.9		*	*		V
Negative	R_L = 10kΩ	(V–)+1	(V–)+0.25		*	*		V
Capacitance Load Drive			1000			*		pF
Short-Circuit Current			±14			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		600			*		kHz
	G = 10		300			*		kHz
	G = 100		50			*		kHz
	G = 1000		5			*		kHz
Slew Rate	V_O = ±10V, G ≤ 10		0.7			*		V/µs
Settling Time, 0.01%	G = 1 to 10		20			*		µs
	G = 100		35			*		µs
	G = 1000		260			*		µs
Overload Recovery	50% Input Overload		5			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Quiescent Current	I_O = 0V		±450	±525		*	*	µA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–55		125	*		*	°C
Storage		–55		125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Lead DIP			100			*		°C/W
SO-8 Surface Mount			150			*		°C/W

* Specification same as INA121P, U.

NOTE: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor, R_G.

PIN CONFIGURATION

Top View **8-Pin DIP and SO-8**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

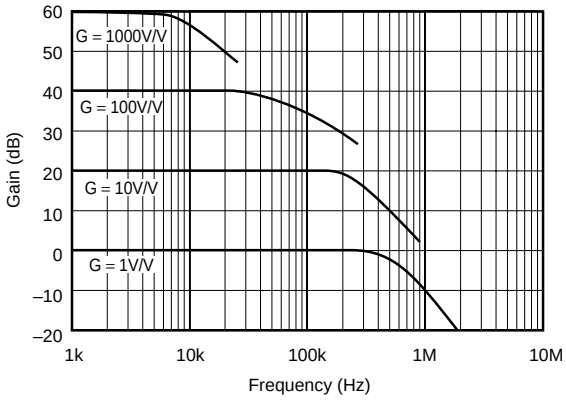
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
Single						
INA121P	8-Pin DIP	006	–40°C to +85°C	INA121P	INA121P	Rails
INA121PA	8-Pin DIP	006	–40°C to +85°C	INA121PA	INA121PA	Rails
INA121U	SO-8 Surface-Mount	182	–40°C to +85°C	INA121U	INA121U	Rails
"	"	"	"	"	INA121U/2K5	Tape and Reel
INA121UA	SO-8 Surface-Mount	182	–40°C to +85°C	INA121UA	INA121UA	Rails
"	"	"	"	"	INA121UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA121U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

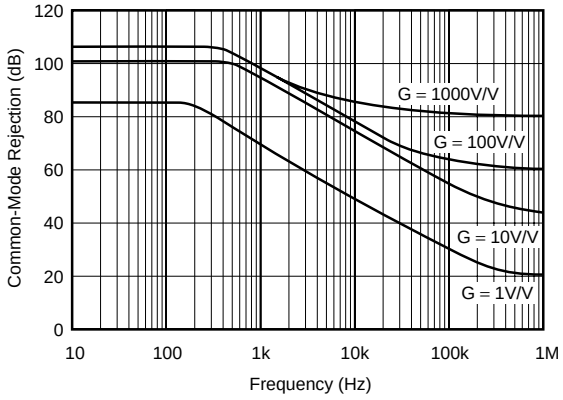
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

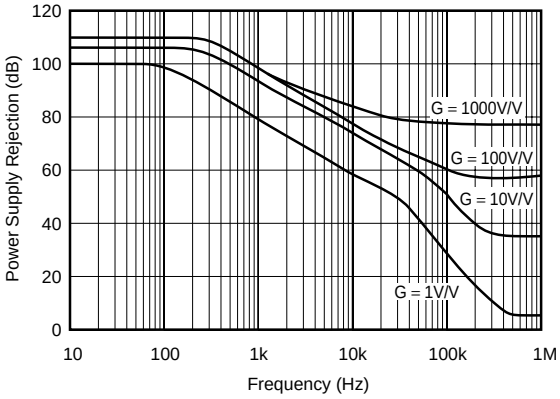
GAIN vs FREQUENCY



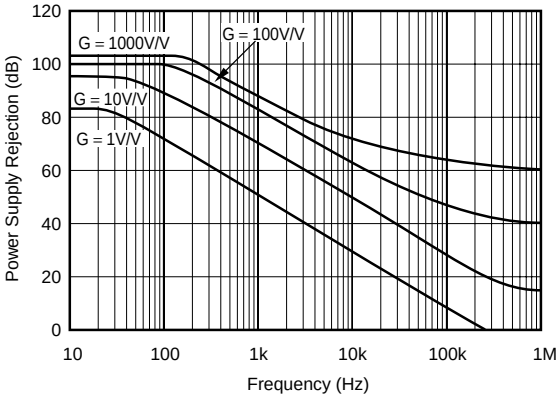
COMMON-MODE REJECTION vs FREQUENCY



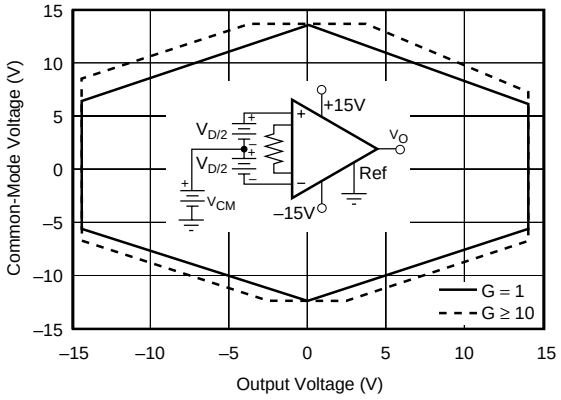
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



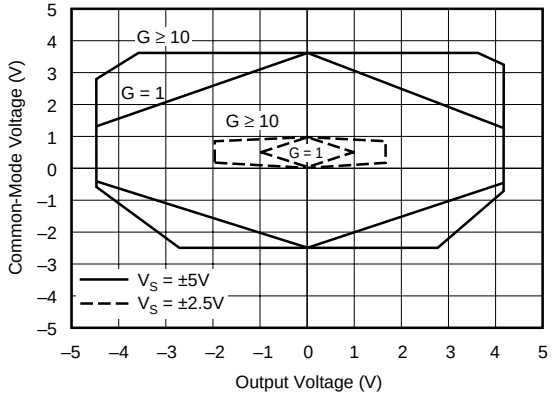
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±15V



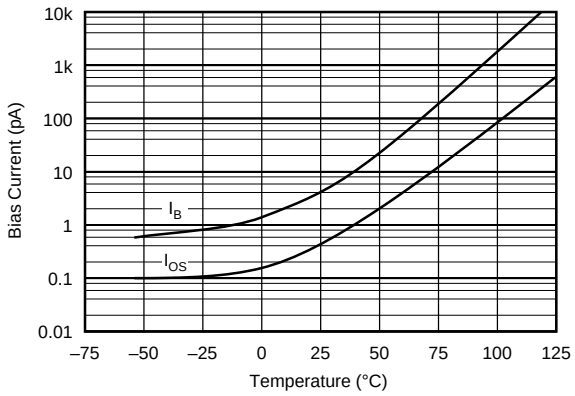
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±5V, ±2.5V



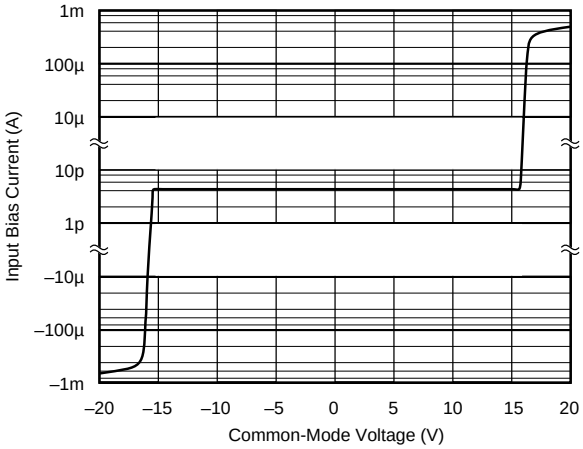
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

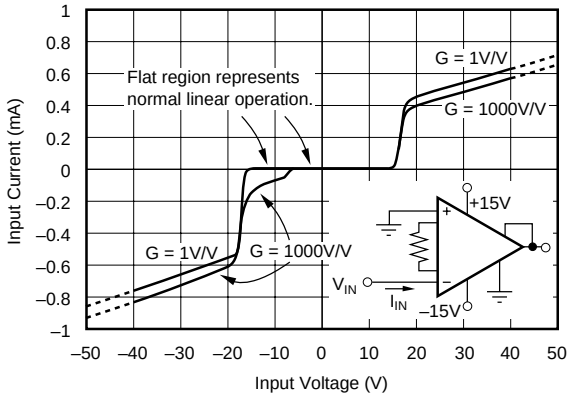
INPUT BIAS CURRENT vs TEMPERATURE



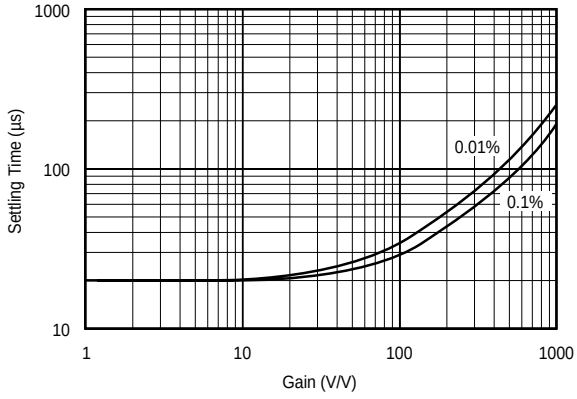
INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE



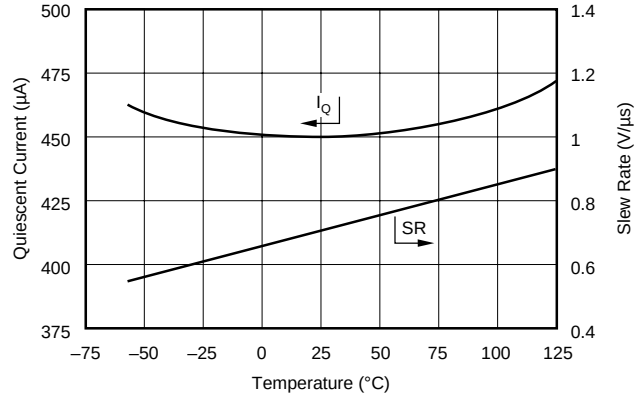
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



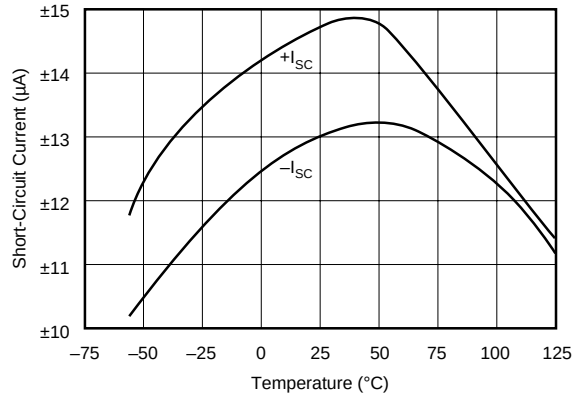
SETTLING TIME vs GAIN



QUIESCENT CURRENT AND SLEW RATE vs TEMPERATURE



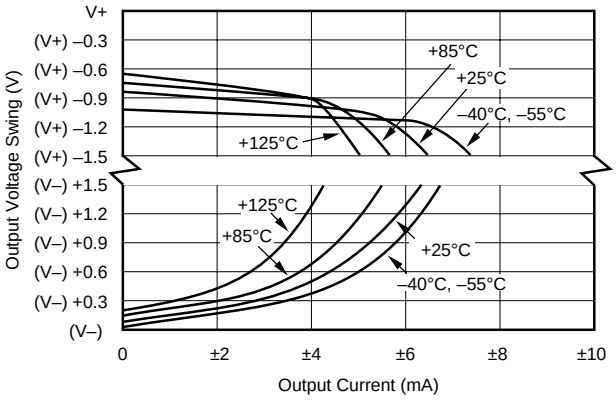
SHORT-CIRCUIT CURRENT vs TEMPERATURE



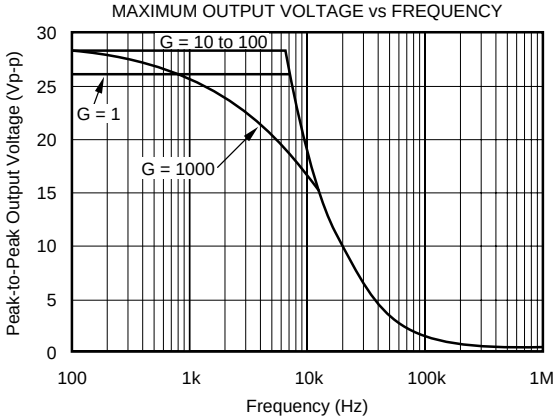
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

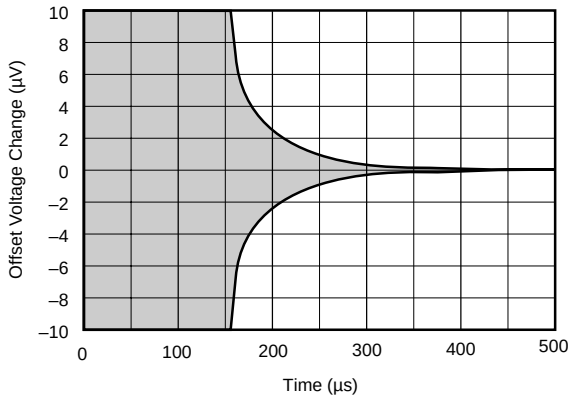
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



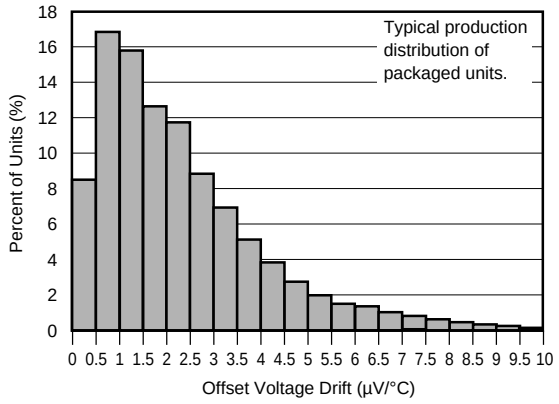
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



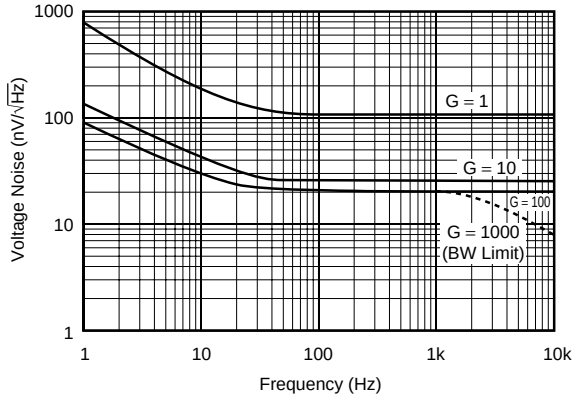
INPUT OFFSET VOLTAGE WARM-UP



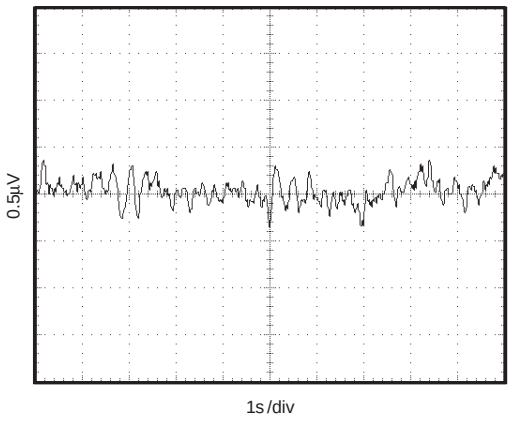
INPUT OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



INPUT-REFERRED NOISE VOLTAGE
vs FREQUENCY



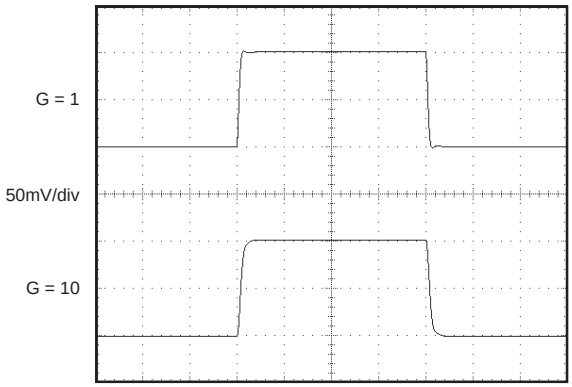
VOLTAGE NOISE 0.1 TO 10Hz
INPUT-REFERRED, G ≥ 100



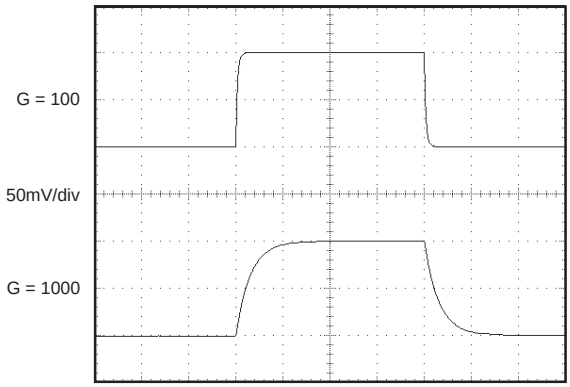
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

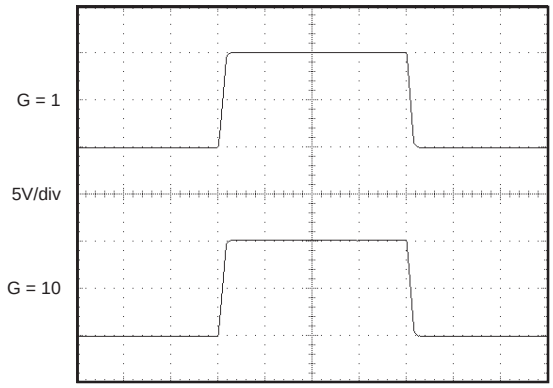
SMALL-SIGNAL STEP RESPONSE
(G = 1, 10)



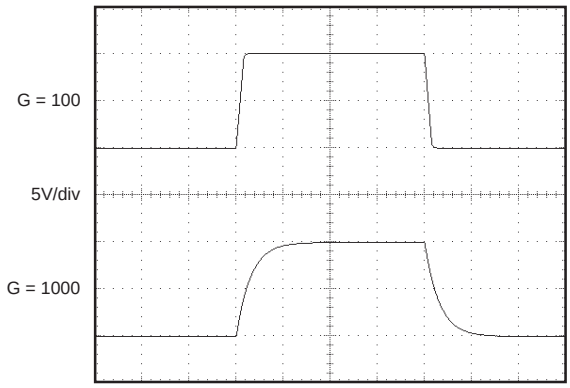
SMALL-SIGNAL STEP RESPONSE
(G = 100, 1000)



LARGE-SIGNAL STEP RESPONSE
(G = 1, 10)



LARGE-SIGNAL STEP RESPONSE
(G = 100, 1000)



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA121. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA121 is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

$$G = 1 + \frac{50\,k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA121.

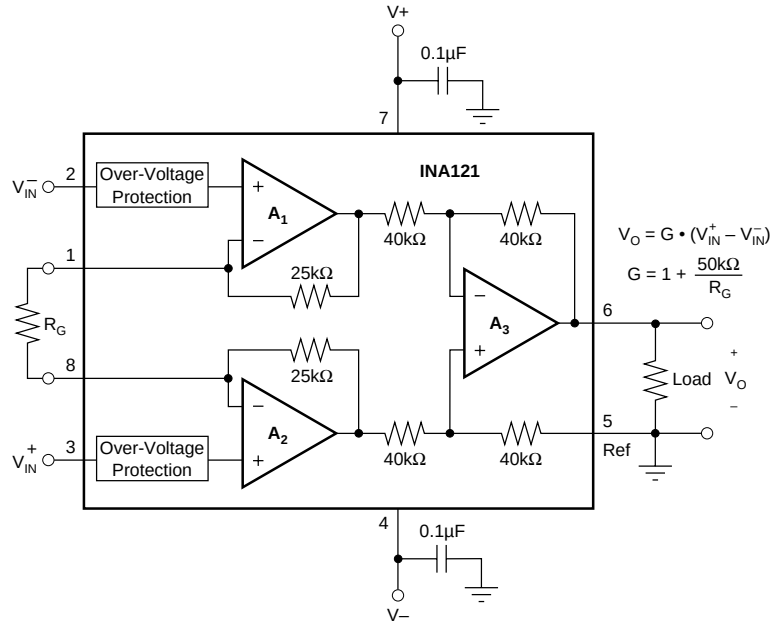
The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA121 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA121. Settling time also remains excellent at high gain.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:

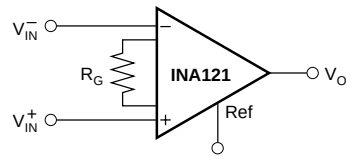


FIGURE 1. Basic Connections.

The INA121 provides excellent rejection of high frequency common-mode signals. The typical performance curve, "Common-Mode Rejection vs Frequency" shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^+ and V_{IN}^- connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA121's FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2kΩ to 50kΩ the INA114, INA128, or INA129 may provide lower offset voltage and drift. For very low source impedance (≤1kΩ), the INA103 may provide improved accuracy and lower noise. At very high source impedances (> 1MΩ) the INA116 is recommended.

OFFSET TRIMMING

The INA121 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

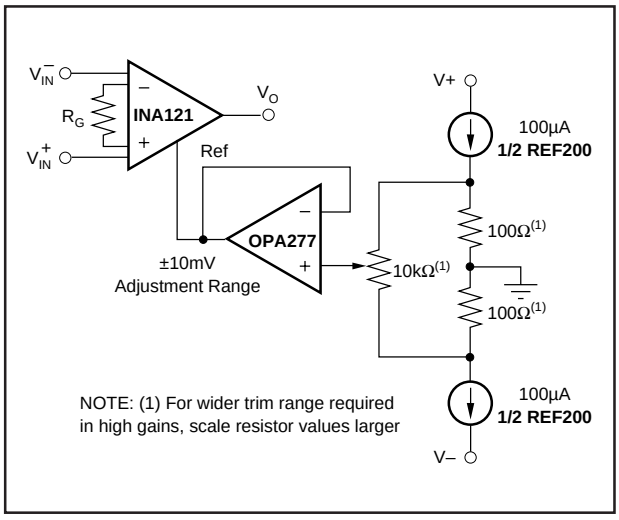


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA121 is extremely high—approximately $10^{12}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 4pA. High input impedance means that this input bias current changes very little with varying input voltage. Input circuitry must provide a path for this input bias current if the INA121 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA121 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

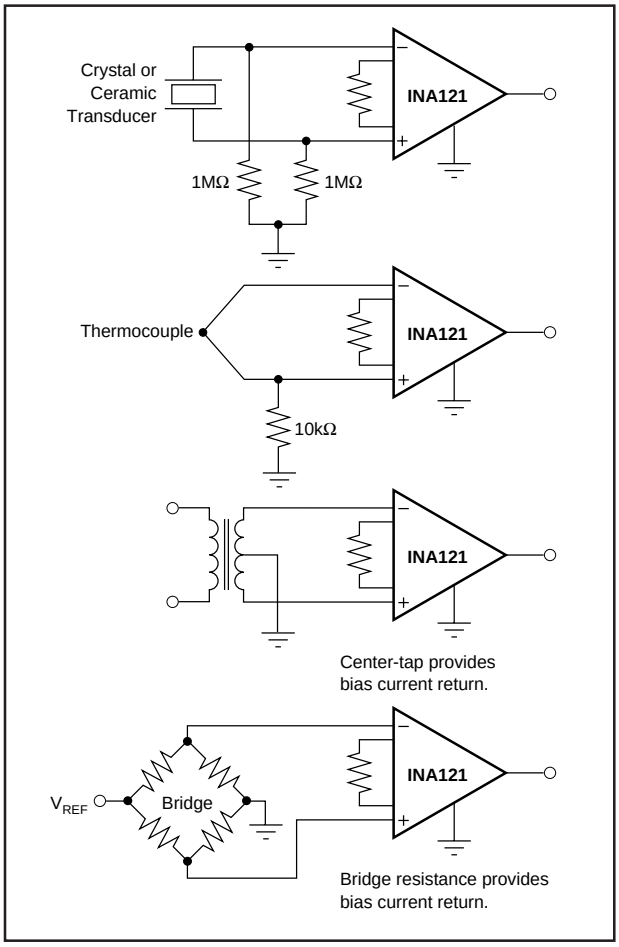


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA121 is from approximately 1.2V below the positive supply voltage to 2.1V above the negative supply. A differential input voltage causes the output voltage to increase. The linear input range, however, will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see typical performance curve "Input Common-Mode Range vs Output Voltage".

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA121 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA121 to increase the voltage swing.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A_3 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA121 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

INPUT FILTERING

The INA121's FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 5 shows proper implementation of this input filter to preserve the INA121's excellent high frequency common-mode rejection. Mismatch of the common-mode input time constant (R_1C_1 and R_2C_2), either from stray capacitance or mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor, C_3, reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2. Make C_3 much larger than C_1 and C_2. If properly matched, C_1 and C_2 also improve ac CMR.

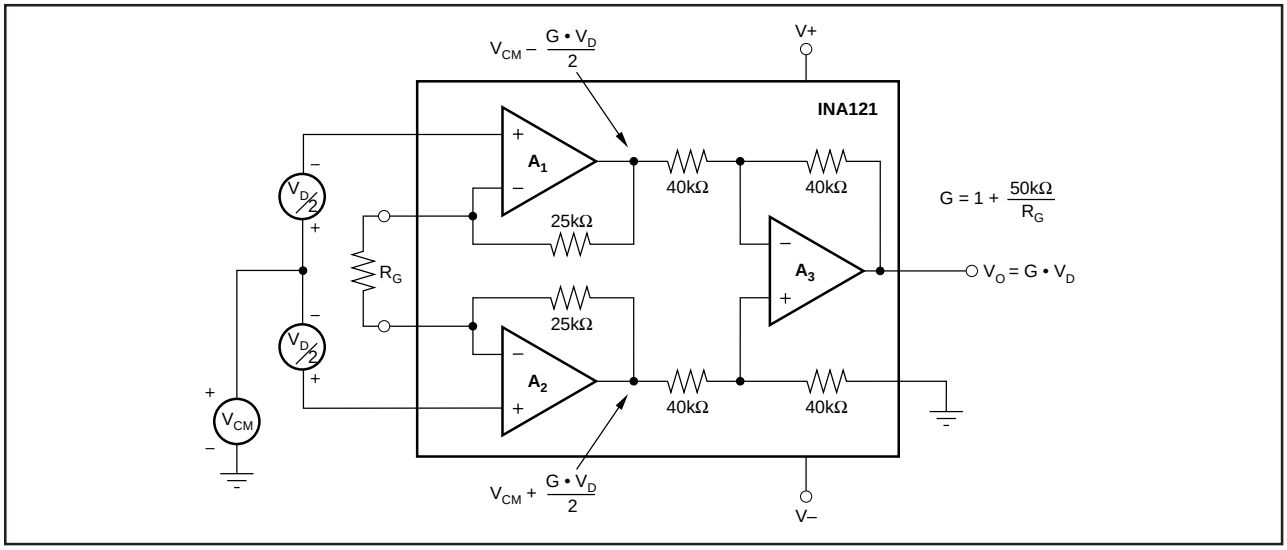


FIGURE 4. Voltage Swing of A_1 and A_2.

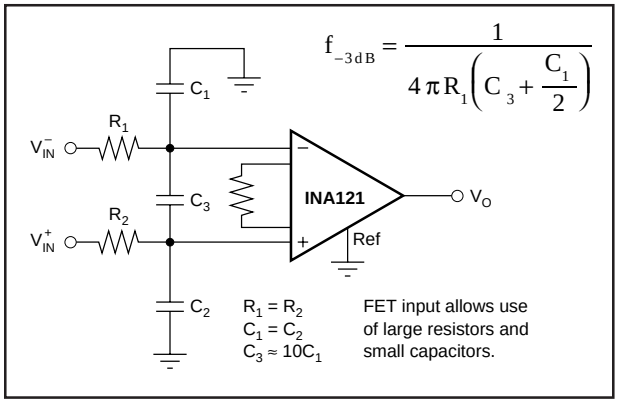


FIGURE 5. Input Low-Pass Filter.

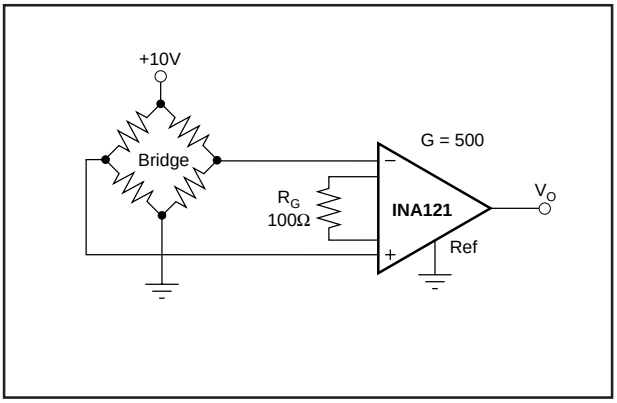


FIGURE 6. Bridge Transducer Amplifier.

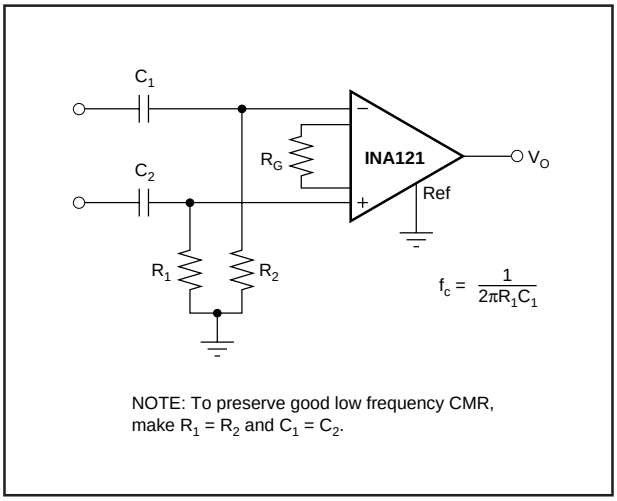


FIGURE 7. High-Pass Input Filter.

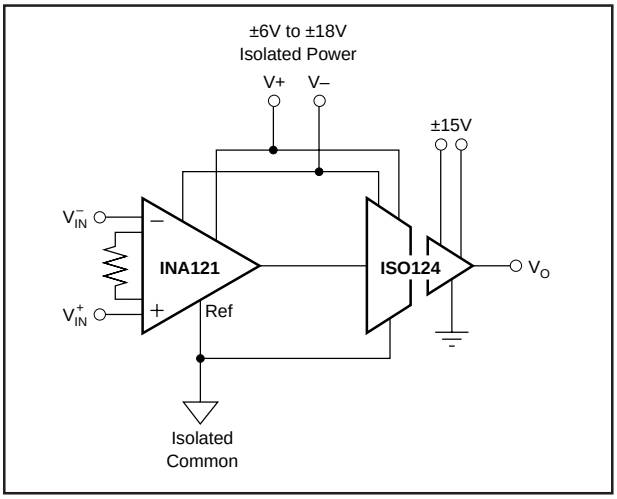


FIGURE 8. Galvanically Isolated Instrumentation Amplifier.

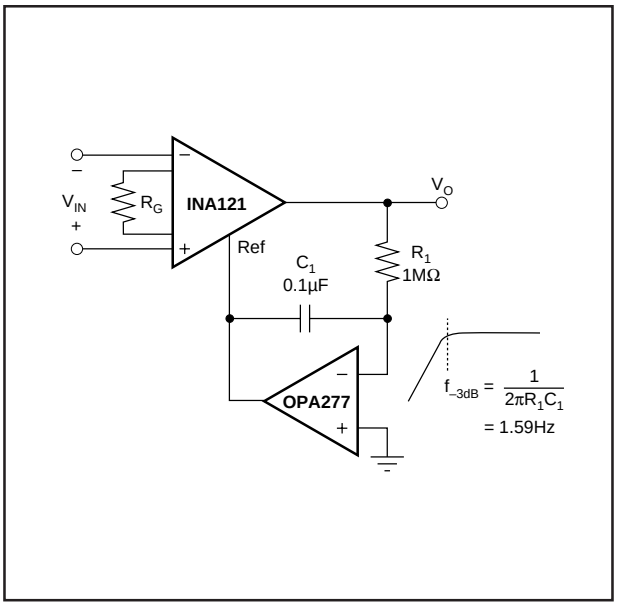


FIGURE 9. AC-Coupled Instrumentation Amplifier.

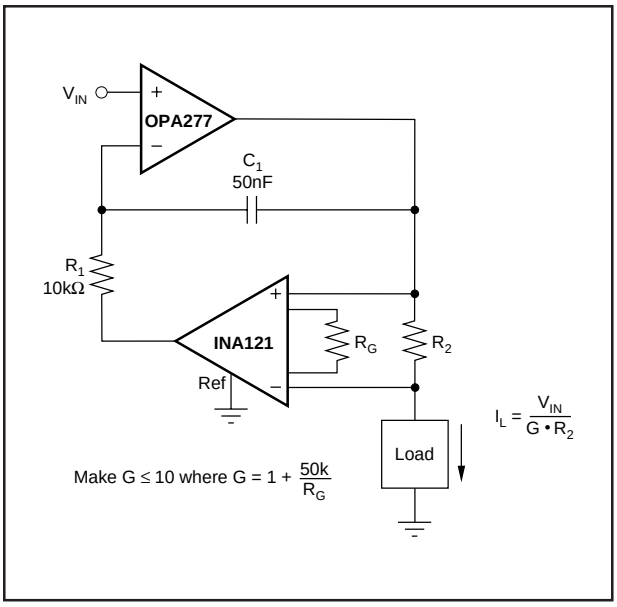


FIGURE 10. Voltage Controlled Current Source.

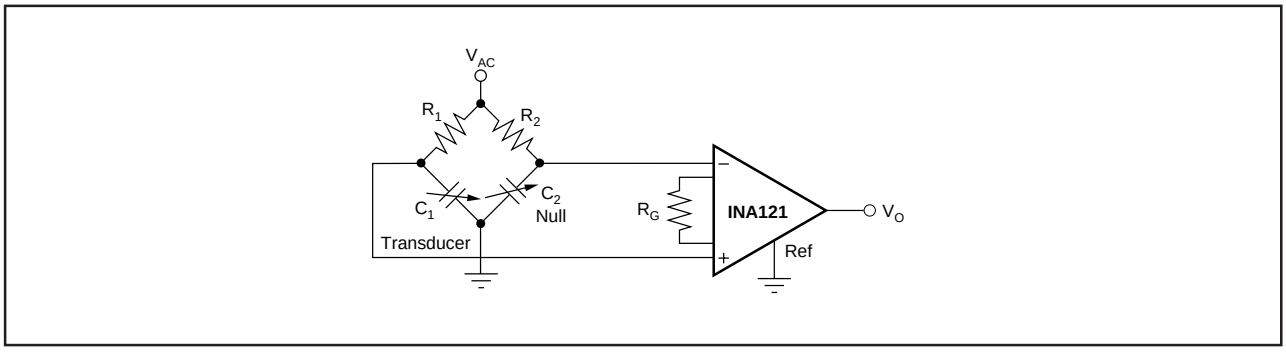


FIGURE 11. Capacitive Bridge Transducer Circuit.

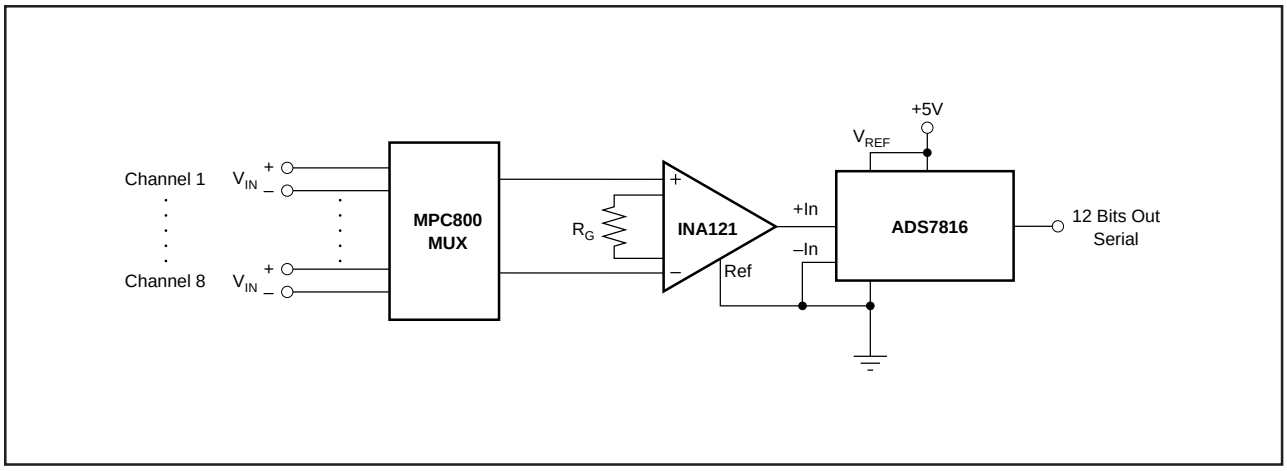


FIGURE 12. Multiplexed-Input Data Acquisition System.

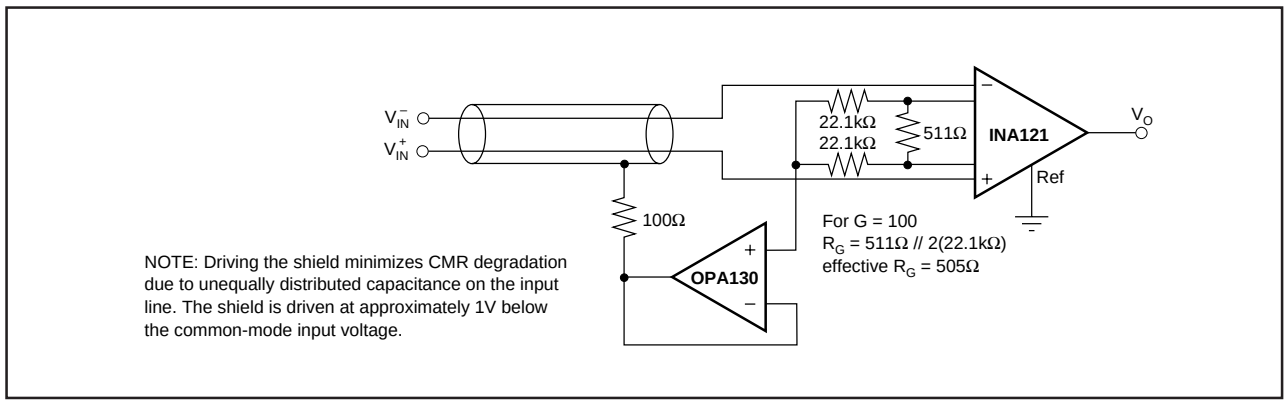


FIGURE 13. Shield Driver Circuit.

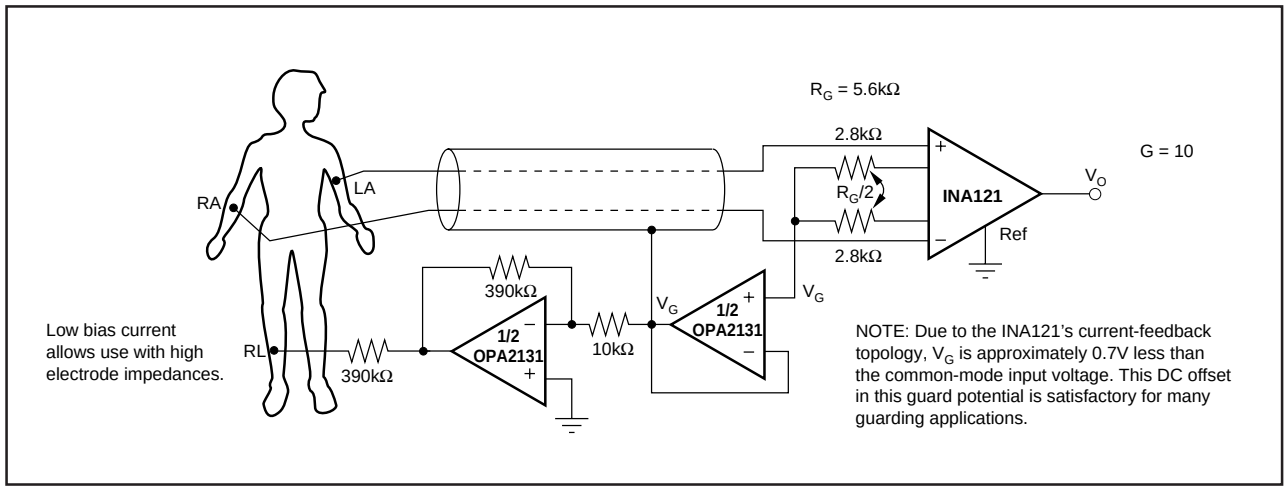


FIGURE 14. ECG Amplifier With Right-Leg Drive.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA121P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA121P A	Samples
INA121PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA121P A	Samples
INA121U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 121U	Samples
INA121U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 121U	Samples
INA121UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 121U A	Samples
INA121UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 121U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

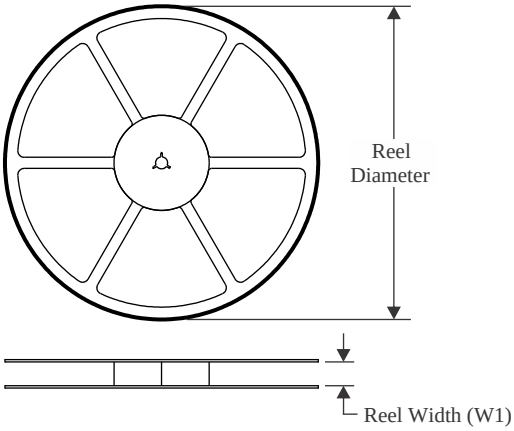
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

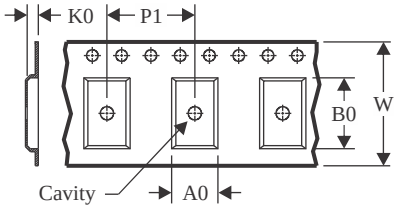
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

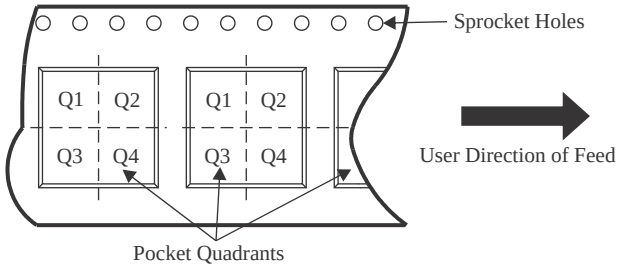


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

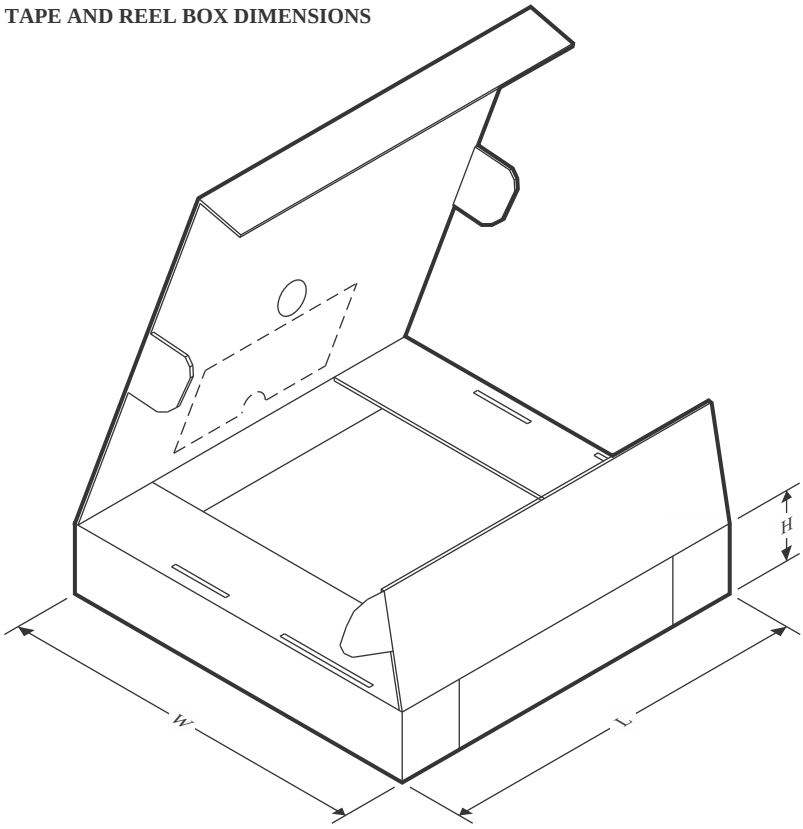
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA121U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA121UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

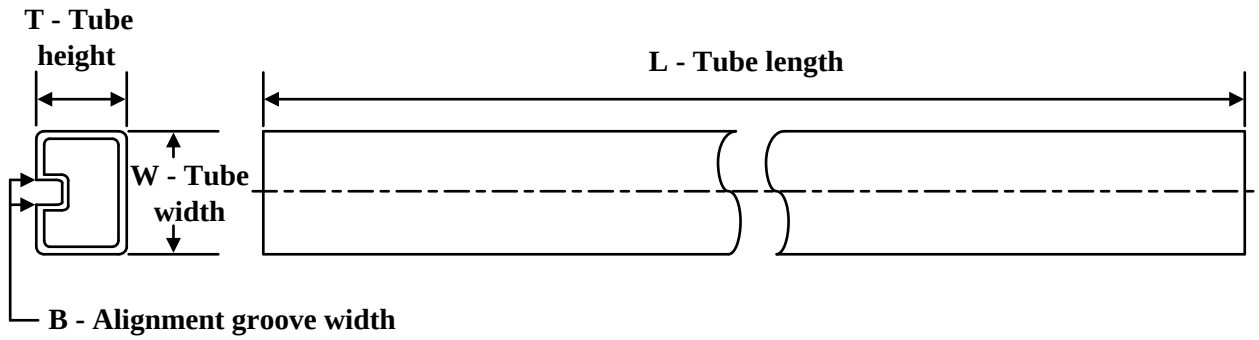
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

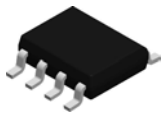
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA121U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA121UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA121P	P	PDIP	8	50	506	13.97	11230	4.32
INA121PA	P	PDIP	8	50	506	13.97	11230	4.32
INA121U	D	SOIC	8	75	506.6	8	3940	4.32
INA121UA	D	SOIC	8	75	506.6	8	3940	4.32

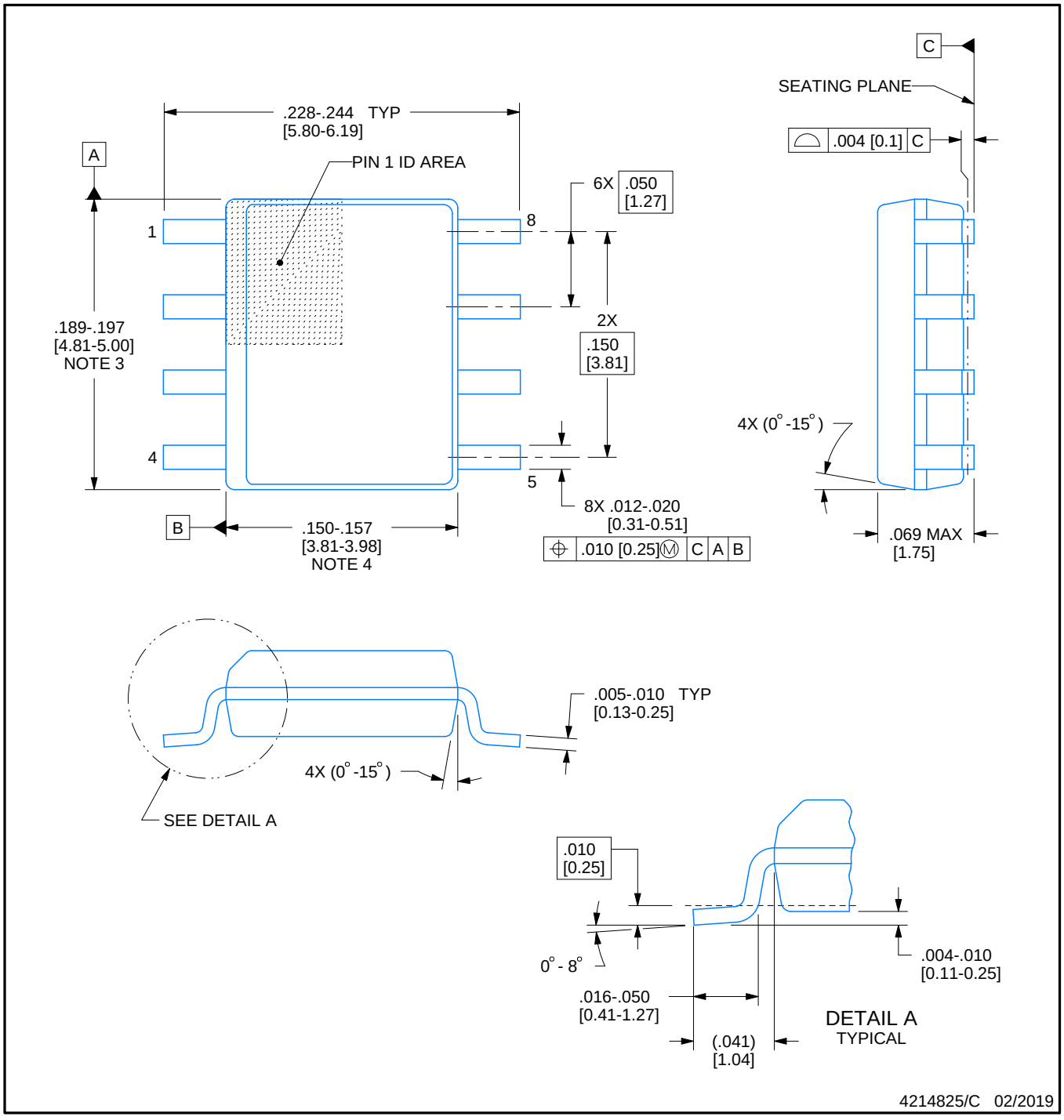


PACKAGE OUTLINE

D0008A

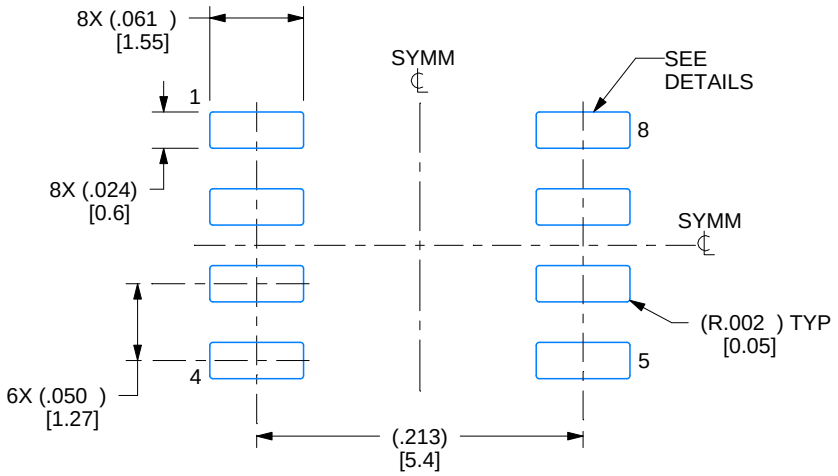
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

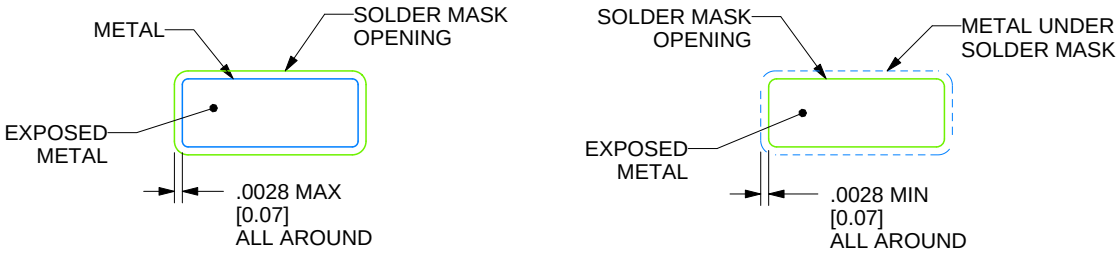


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

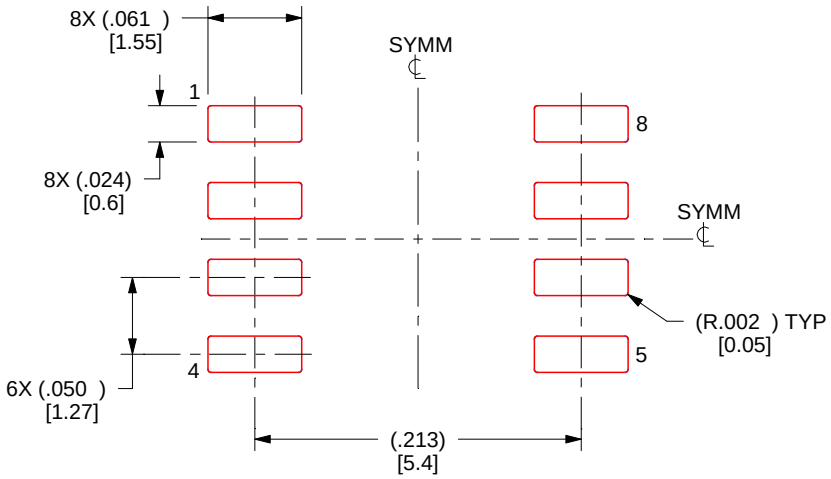
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



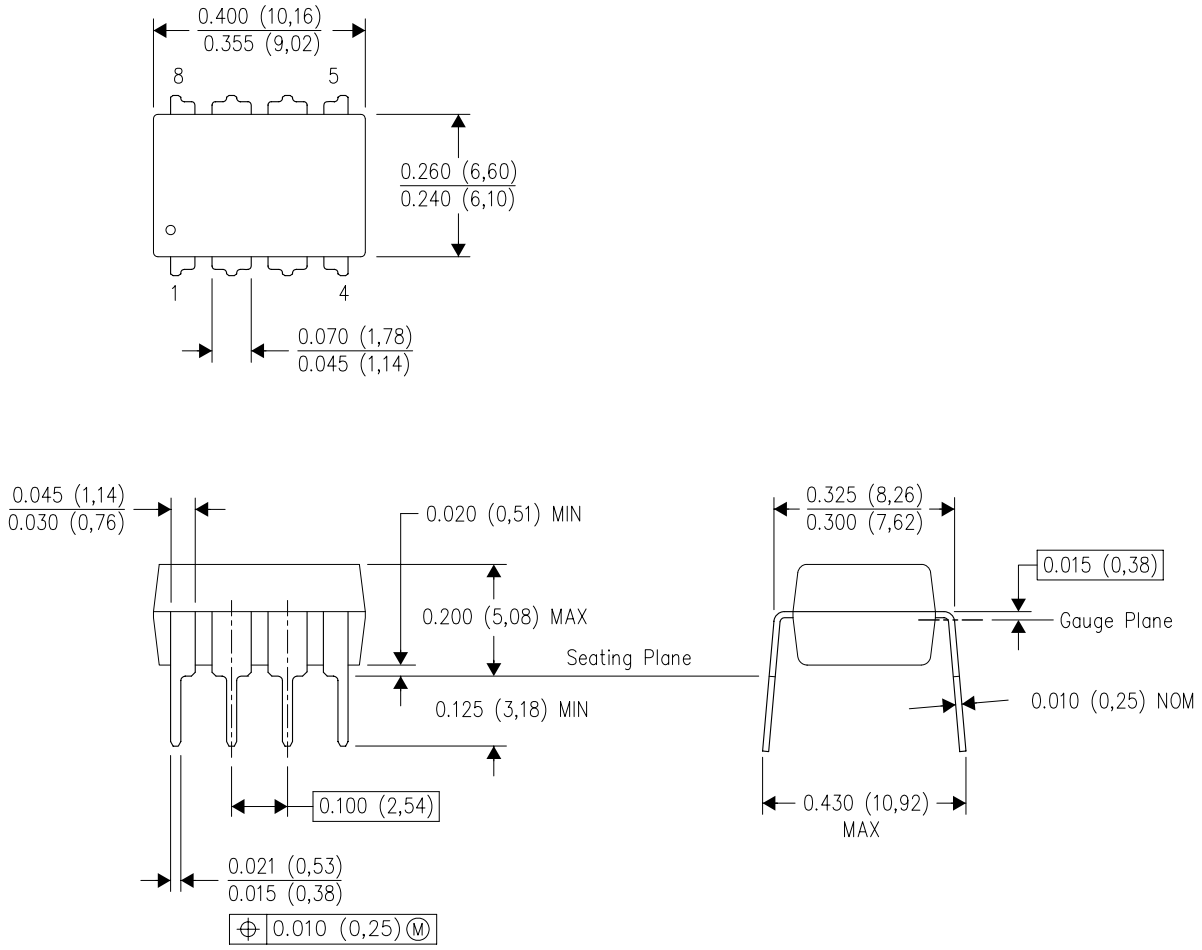
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265