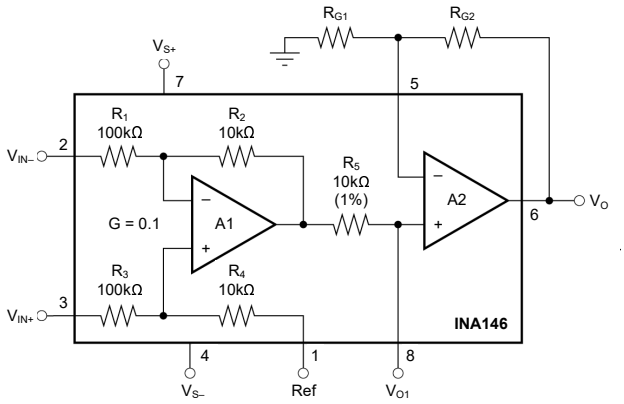
INA146 High-voltage, Programmable Gain Difference Amplifier

1 Features

- High common-mode voltage:
  - 40V at V_S = 5V
  - ±100V at V_S = ±15V
- Differential gain = 0.1V/V TO 100V/V:
  - Set with External Resistors
- Low quiescent current: 570µA
- Wide supply range:
  - Single Supply: 4.5V to 36V
  - Dual Supplies: ±2.25V to ±18V
- Low gain error: 0.025%
- High common-mode rejection: 80dB

2 Applications

- Battery cell formation & test equipment
- AC drive control module
- HVAC controller
- Professional audio amplifier (rack mount)
- Programmable DC power source
- Data acquisition (DAQ)



INA146 Simplified Block Diagram

3 Description

The INA146 is a precision difference amplifier that can be used to accurately attenuate high differential voltages and reject high common-mode voltages for compatibility with common signal processing voltage levels. High-voltage capability also affords inherent input protection. The input common-mode range extends beyond both supply rails, making the INA146 an excellent choice for both single and dual supply applications.

On-chip precision resistors are laser-trimmed to achieve accurate gain and high common-mode rejection. Excellent TCR tracking of these resistors provides continued high precision over temperature.

A 10:1 difference amplifier provides 0.1V/V gain when the output amplifier is used as a unity-gain buffer. In this configuration, input voltages up to ±100V can be measured. Gains greater than 0.1V/V can be set with an external resistor pair without affecting the common-mode input range.

The INA146 is available in the SO-8 surface-mount package specified for the extended industrial temperature range, –40°C to 85°C.

Package Information

PART NUMBER	PACKAGE(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE SIZE (2)
INA146	SOIC (8)	−40°C to 85°C	4.90mm × 6.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Pin Configuration and Functions

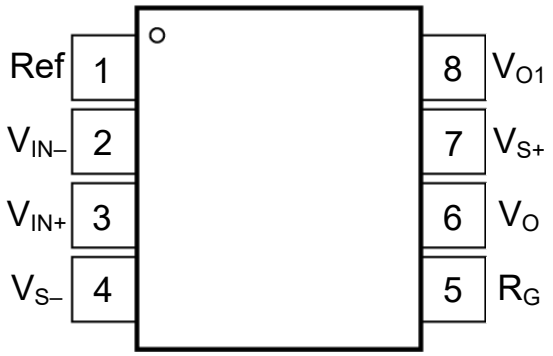


Figure 4-1. INA146D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Ref	1	I	Reference input. This pin must be driven by a low impedance source.
V_{IN-}	2	I	Negative (inverting) input
V_{IN+}	3	I	Positive (non-inverting) input
V_{S-}	4	–	Negative supply
R_G	5	I	Gain setting input. Place a resistor network between pin 1 and pin 5.
V_O	6	O	Output of amplifier A2
V_{S+}	7	–	Positive supply
V_{O1}	8	O	Output of amplifier A1

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 7.1.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, $V_S = (V_{S+}) – (V_{S–})$		±18	V
		Single supply, $V_S = (V_{S+}) – 0$ V		36	
V_{IN+}, $V_{IN–}$	Signal input voltage			±100	V
	Signal input current			±1	mA
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–55	125	°C
T_{stg}	Storage temperature		–55	125	°C
T_J	Junction temperature			150	°C
	Lead temperature (soldering, 10s)			240	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		INA146 SO-8 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25V to ±18V or 5V single supply, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = V_S / 2, and G = 0.1, all chips site origins (CSO), unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, V_O	RTI, V_S = ±15V, V_{CM} = 0V			±1	±5	mV
		RTI, V_S = 5V, V_{CM} = 0V			±3	±10	
	Offset voltage, V_{O1}	RTI			±1		
	Offset voltage drift	RTI, T_A = –40°C to 85°C			±10		µV/°C
PSRR	Power-supply rejection ratio	RTI, V_S = ±1.35V to ±18V			±100	±600	µV/V
V_{CM}	Common-mode voltage (1)	V_S = ±15V, V_{IN} = 0V		–100		100	V
		V_S = 5V, V_{IN} = 0V		–25		19	
CMRR	Common-mode voltage rejection	RTI, V_{CM} = [11($V_{S–}$)–10*V_{REF}] to [11*(V_{S+} -1)–10*V_{REF}] , R_S = 0Ω		70	80		dB
		T_A = –40°C to 85°C		64	74		
	Differential input impedance	Non-inverting input			110		kΩ
		Inverting input			91.7		
	Common-mode input impedance				55		kΩ
BIAS CURRENT							
I_B	Bias Current	V_{CM} = V_S / 2			±50		nA
I_{OS}	Offset Current				±5		nA
NOISE							
e_N	Voltage noise	RTI, f_B = 0.1Hz to 10Hz			12		μV_{PP}
		RTI, f = 1kHz			550		nV/√Hz
GAIN							
	Gain			0.1		100	V/V
GE	Gain error	V_O = ($V_{S–}$) + 0.15V to (V_{S+}) – 1V, R_L = 100kΩ, G = 1			±0.025	±0.1	%
		V_O = ($V_{S–}$) + 0.3V to (V_{S+}) – 1.25V, R_L = 10kΩ, G = 1			±0.025	±0.1	
	Gain error drift(2)	T_A = –40°C to 85°C	V_O = ($V_{S–}$) + 0.25V to (V_{S+}) – 1V, R_L = 100kΩ, G = 1		±1	±10	ppm/°C
			V_O = ($V_{S–}$) + 0.5V to (V_{S+}) – 1.25V, R_L = 10kΩ, G = 1		±1	±10	
	Gain nonlinearity	V_O = ($V_{S–}$) + 0.3V to (V_{S+}) – 1.25V, G = 1			±0.001	±0.01	% of FSR
OUTPUT							
	Output voltage	R_L = 100kΩ, G = 1		($V_{S–}$) + 0.15		(V_{S+}) – 1	V
			T_A = –40°C to 85°C	($V_{S–}$) + 0.25		(V_{S+}) – 1	
		R_L = 10kΩ, G = 1		($V_{S–}$) + 0.3		(V_{S+}) – 1.25	
			T_A = –40°C to 85°C	($V_{S–}$) + 0.5		(V_{S+}) – 1.25	
C_L	Load capacitance	Stable operation			1		nF
I_{SC}	Short-circuit current	Continuous to V_S / 2	CSO: SHE		±15		mA
			CSO: TID		±27		
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	G = 0.1			550		kHz
		G = 1			50		
SR	Slew rate	CSO: SHE			0.45		V/µs
		CSO: TID			0.3		
t_S	Settling time	To 0.1%	V_O = 10V-step		40		µs
		To 0.01%	V_O = 10V-step		80		

at T_A = 25°C, V_S = ±2.25V to ±18V or 5V single supply, R_L = 10kΩ, V_{REF} = V_S / 2, V_{CM} = V_S / 2, and G = 0.1, all chips site origins (CSO), unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Overload recovery	50% input overload	CSO: SHE		40		µs
			CSO: TID		2		
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0V	CSO: SHE		±570	±700	µA
			CSO: TID		±250	±700	µA
		T_A = –40°C to 85°C				±750	µA

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

5.6 Amplifier A1, A2 Performance

at T_A = 25°C, R_L = 10kΩ, V_{REF} = 0V, V_{CM} = V_S / 2, and G = 0.1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OS}	Offset voltage, V_O	RTI, V_S = ±15V, V_{CM} = V_O = 0V		±0.5		mV
	Offset voltage drift	RTI, T_A = –40°C to 85°C		±1		µV/°C
V_{CM}	Common-mode voltage (1)	V_{IN} = V_O = 0V		$V_{S–}$ to (V_{S+}) –1		V
CMRR	Common-mode voltage rejection	V_{CM} = $V_{S–}$ to (V_{S+}) –1		90		dB
GAIN						
A_{OL}	Open Loop Gain			110		dB
BIAS CURRENT						
I_B	Bias Current			±50		nA
I_{OS}	Offset Current			±5		nA
OUTPUT						
	Resistor at V_{O1}	Initial		10		kΩ
	Error at V_{O1}			±1		%
	Error drift at V_{O1}			±100		ppm/°C

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.

5.7 Typical Characteristics

at T_A = 25°C, V_S = ±15V, G = 0.1, R_L = 10kΩ connected to ground, V_{REF} = V_S / 2, all chips site origins (CSO), unless otherwise noted

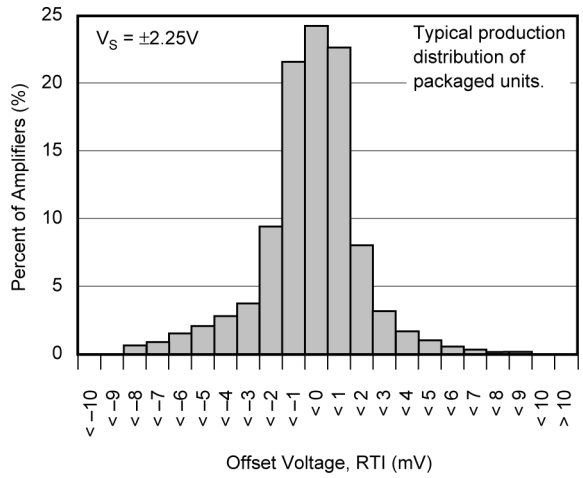


Figure 5-1. Offset Voltage Production Distribution

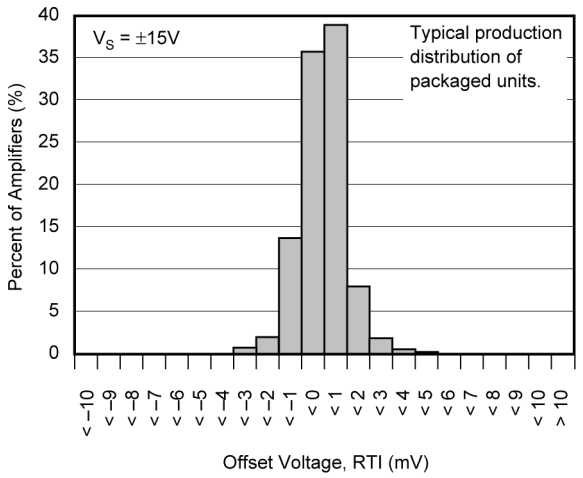


Figure 5-2. Offset Voltage Production Distribution

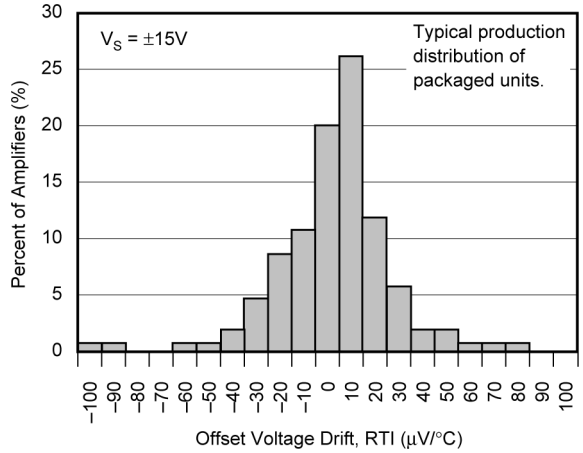


Figure 5-3. Offset Voltage Drift Production Distribution

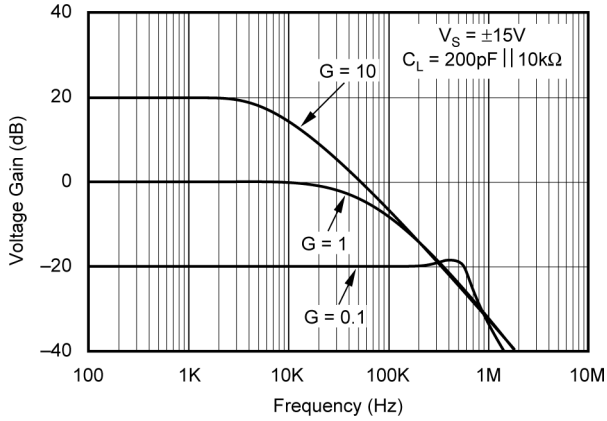
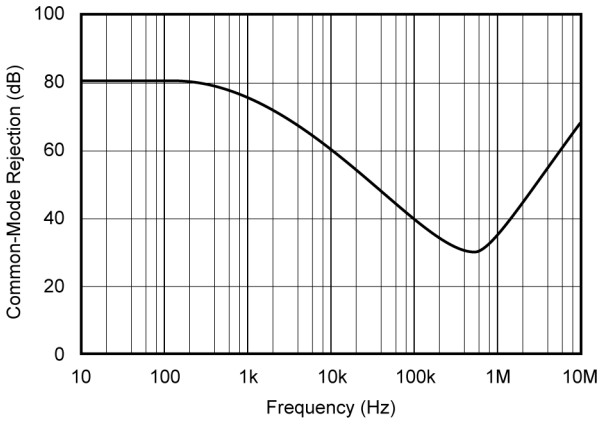
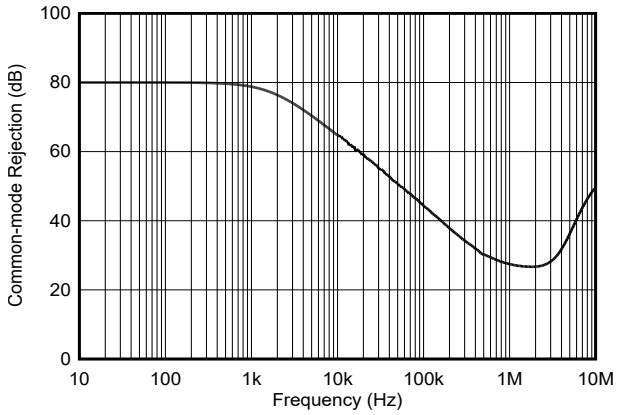


Figure 5-4. Gain vs Frequency



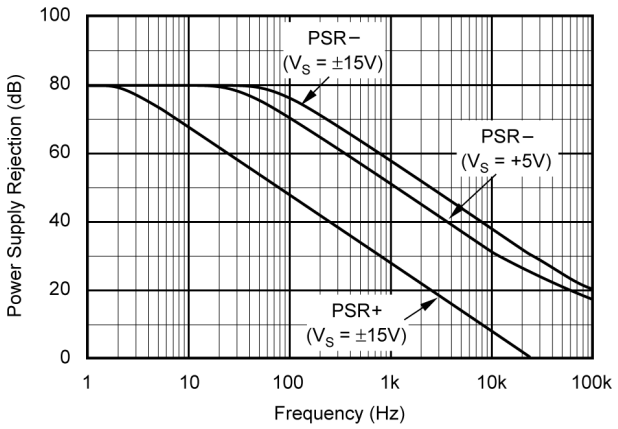
CSO: SHE

Figure 5-5. Common-mode Rejection vs Frequency



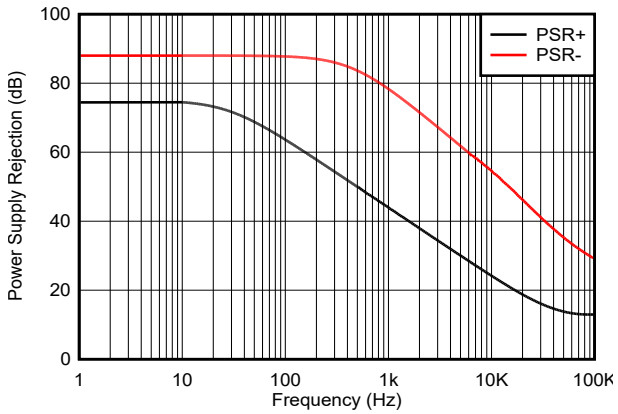
CSO: TID

Figure 5-6. Common-mode Rejection vs Frequency



CSO: SHE

Figure 5-7. Power Supply Rejection vs Frequency



CSO: TID

Figure 5-8. Power Supply Rejection vs Frequency

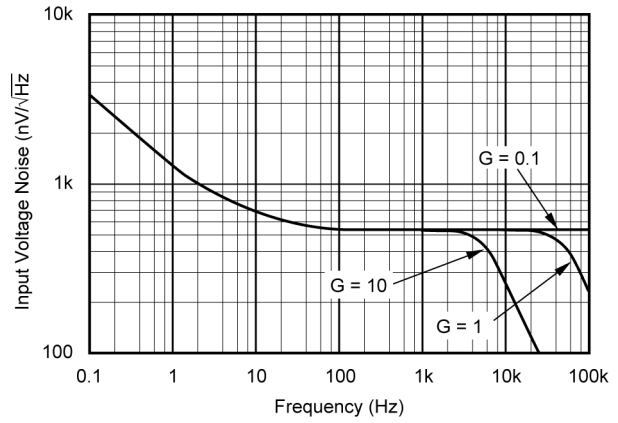


Figure 5-9. Input Voltage Noise Density

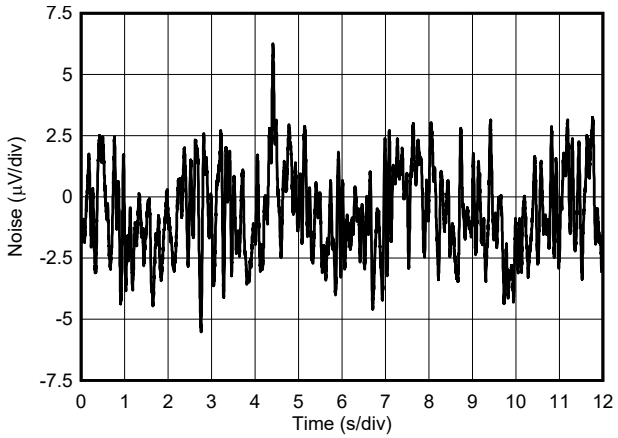
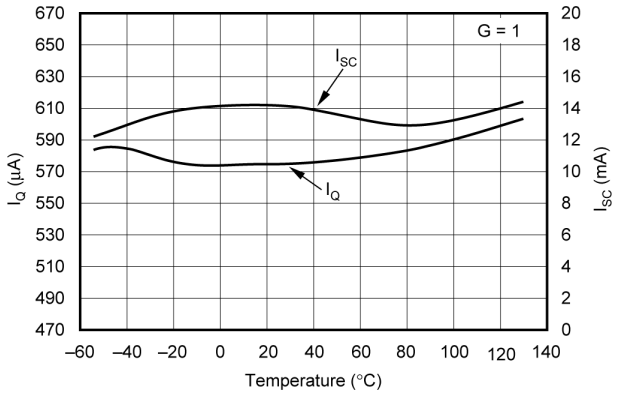
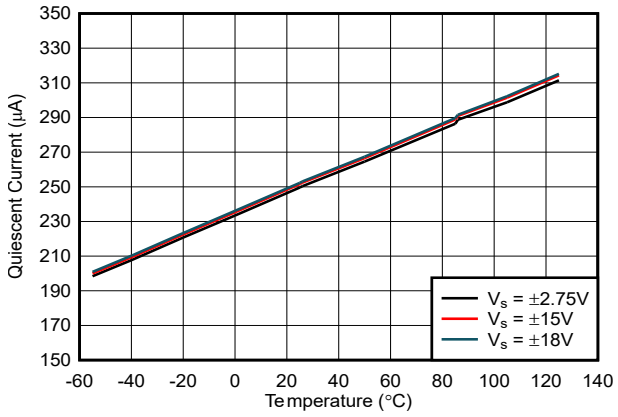


Figure 5-10. 0.1Hz to 10Hz Voltage Noise (Rti)



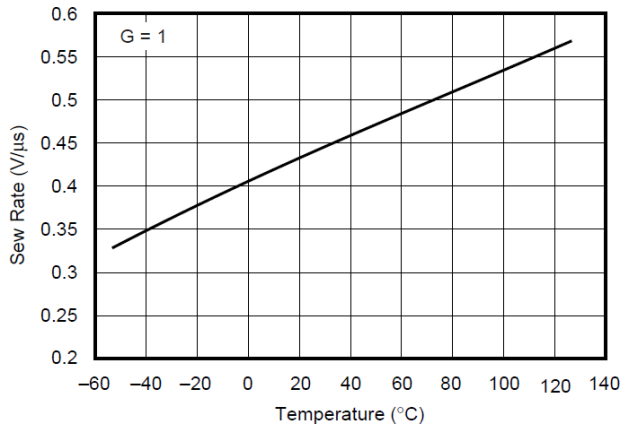
CSO: SHE

Figure 5-11. Quiescent Current and Short-circuit Current vs Temperature



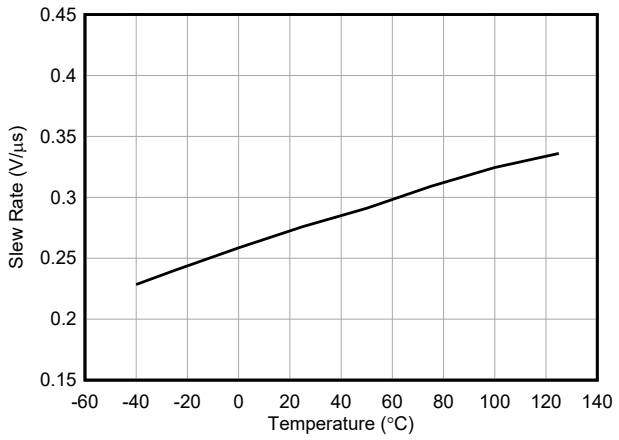
CSO: TID

Figure 5-12. Quiescent Current vs Temperature



CSO: SHE

Figure 5-13. Slew Rate vs Temperature



CSO: TID

Figure 5-14. Slew Rate vs Temperature

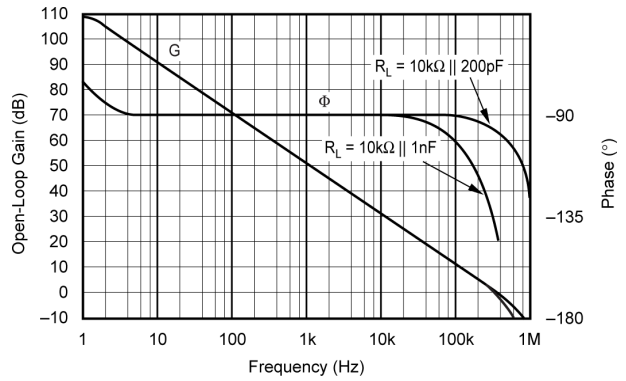


Figure 5-15. Gain and Phase vs Frequency Op Amp A1 and A2

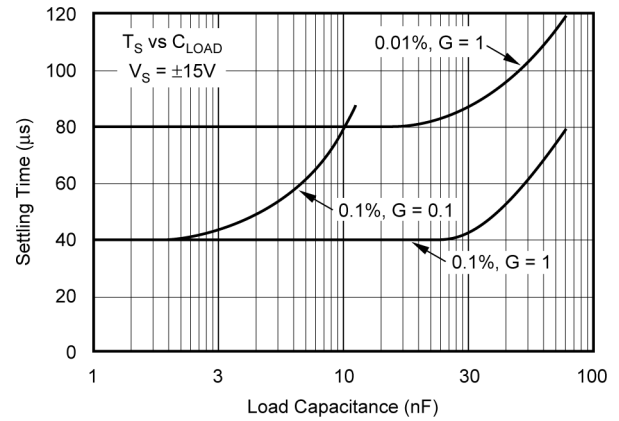
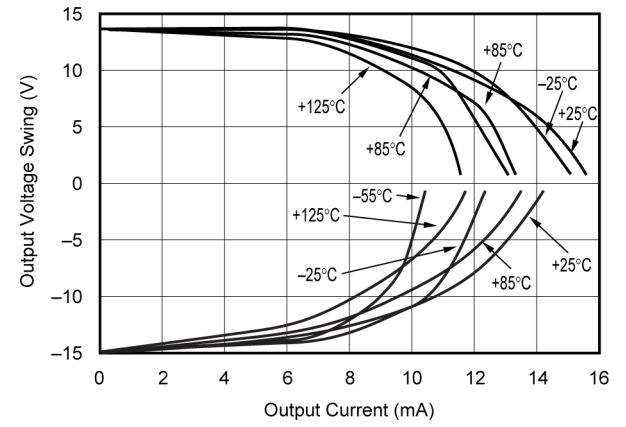
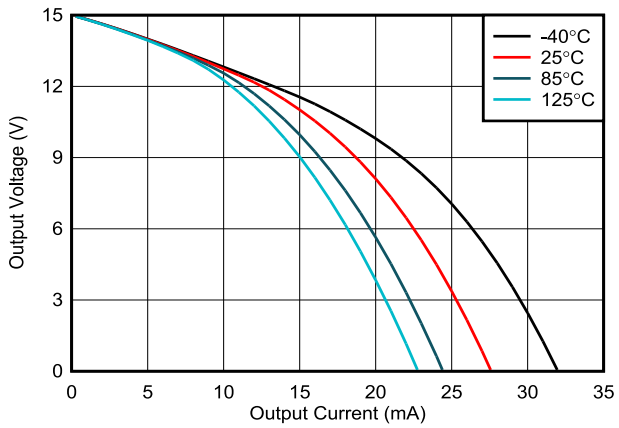


Figure 5-16. Settling Time vs Load Capacitance



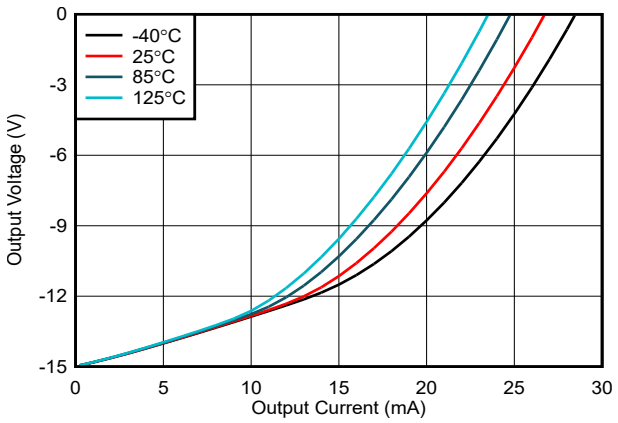
CSO: SHE

Figure 5-17. Maximum Output Voltage Swing vs Output Current



CSO: TID

Figure 5-18. Output Voltage Swing vs Output Current (Sourcing)



CSO: TID

Figure 5-19. Output Voltage Swing vs Output Current (Sinking)

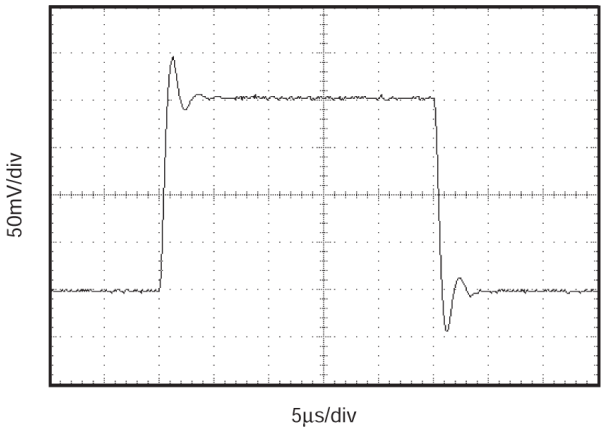


Figure 5-20. Small-signal Step Response (G = 0.1, R_L = 10kΩ, C_L = 200pF)

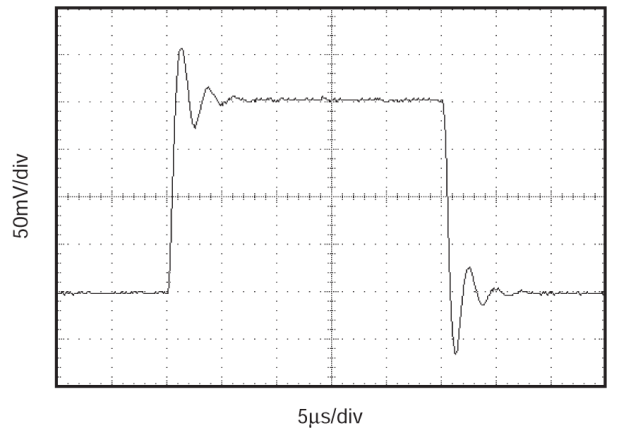


Figure 5-21. Small-signal Step Response (G = 0.1, C_L = 1000pF)

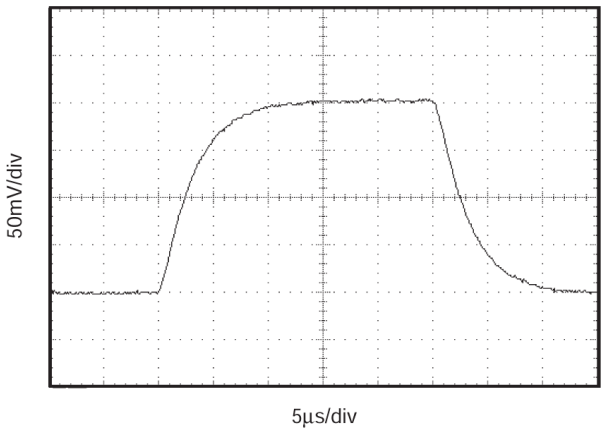
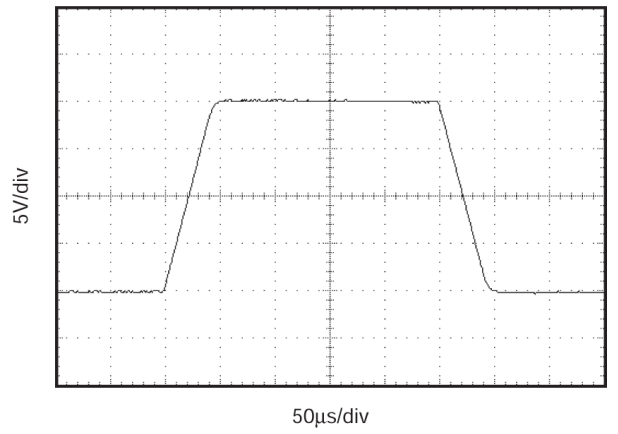
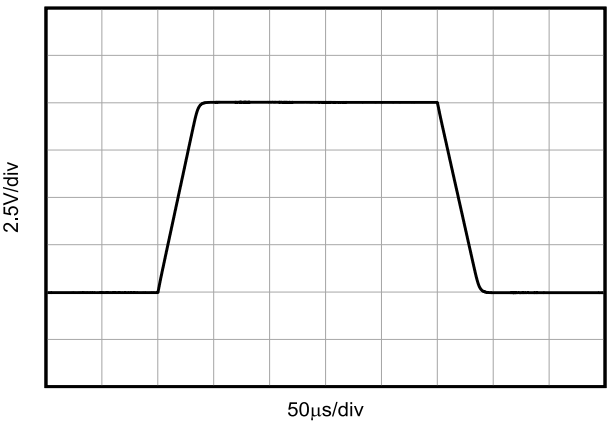


Figure 5-22. Small-signal Step Response (G = 1, C_L = 1000pF)



CSO: SHE

Figure 5-23. Large-signal Step Response (G = 1, R_L = 10kΩ, C_L = 200pF)



CSO: TID

Figure 5-24. Large-signal Step Response (G = 1, R_L = 10kΩ, C_L = 200pF)

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The INA146 is a programmable gain difference amplifier consisting of a gain of 0.1 difference amplifier and a programmable-gain output buffer stage. Basic circuit connections are shown in Figure 6-1. Power supply bypass capacitors must be connected close to pins 4 and 7, as shown. The amplifier is programmable in the range of G = 0.1 to G = 50 with two external resistors.

The output of A1 is connected to the noninverting input of A2 through a 10kΩ resistor which is trimmed to ±1% absolute accuracy. The A2 input is available for applications such as a filter or a precision current source. See application figures for examples.

6.1.1 Operating Voltage

The INA146 is fully specified for supply voltages from ±2.25 V to ±18 V with key parameters specified over the temperature range –40°C to 85°C. The INA146 can be operated with single or dual supplies with excellent performance. Parameters that vary significantly with operating voltage, load conditions or temperature are shown in the typical performance curves.

6.1.2 Setting the Gain

The gain of the INA146 is set by using two external resistors, R_{G1} and R_{G2}, according to the equation:

$G = 0.1 \times (1 + R_{G2}/R_{G1})$

For a total gain of 0.1, A2 is connected as a buffer amplifier with no R_{G1}. A feedback resistor, R_{G2} = 10kΩ, must be used in the buffer connection. This provides bias current cancellation (in combination with internal R_5) to provide the specified offset voltage performance. Commonly used values are shown in the table of Figure 6-1. Resistor values for other gains must be chosen to provide a 10kΩ parallel resistance.

6.1.3 Common-mode Range

The 10:1 input resistor ratio of the INA146 provides an input common-mode range that can extend well beyond the power supply rails. Exact range depends on the power supply voltage and the voltage applied to the Ref terminal (pin 1). For proper operation, the voltage at the non-inverting input of A1 (an internal node) must be within the linear operating range. The voltage is determined by the simple 10:1 voltage divider between pin 3 and pin 1. This voltage must be between V_{S-} and $(V_{S+}) – 1V$.

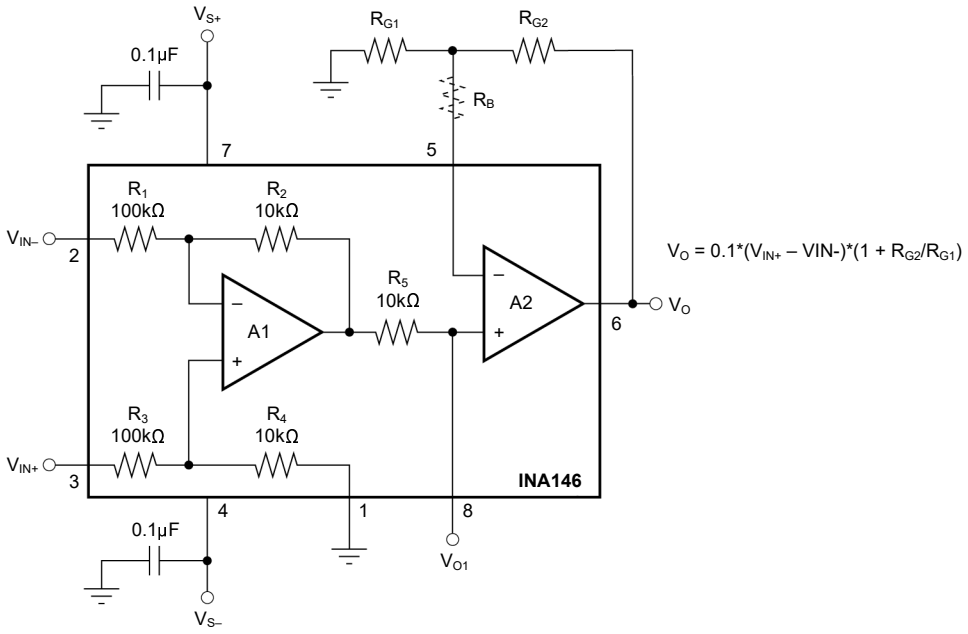


Figure 6-1. Basic Circuit Connections

Table 6-1. Basic Circuit External Resistor Values

Total Gain (V/V)	A2 Gain (V/V)	Standard 1% Resistors		
		R_{G1} (Ω)	R_{G2} (Ω)	R_B (Ω)
0.1	1	(None)	10k	–
0.2	2	20k	20k	–
0.5	5	12.4k	49.9k	–
1	10	11.0k	100k	–
2	20	10.5k	200k	–
5	50	10.2k	499k	–
10	100	10.2k	1M	–
20	200	499	100k	9.53k
50	500	100	49.9k	10k
100	1000	100	100k	10k

6.1.4 Offset Trim

The INA146 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the offset voltage. A voltage applied to the Ref terminal is summed with the output signal. This feature can be used to null offset voltage. To maintain good common-mode rejection, the source impedance of a signal applied to the Ref terminal must be less than 10Ω and a resistor added to the positive input terminal must be 10 times that, or 100Ω. Alternatively, the trim voltage can be buffered with an operational amplifier such as the OPA277.

6.1.5 Input Impedance

The input impedance of the INA146 is determined by the input resistor network and is approximately 100kΩ. The source impedance at the two input terminals must be nearly equal to maintain good common-mode rejection. A 12Ω mismatch in impedance between the two inputs causes the typical common-mode rejection to be degraded to approximately 72dB. Figure 6-7 shows a common application measuring power supply current through a

shunt resistor. The source impedance of the shunt resistor, R_S, is balanced by an equal compensation resistor, R_C.

Source impedances greater than 800Ω are not recommended, even if the source impedances are perfectly matched. Internal resistors are laser trimmed for accurate ratios, not to absolute values. Adding equal resistors greater than 800Ω can cause a mismatch in the total resistor ratios, degrading CMR.

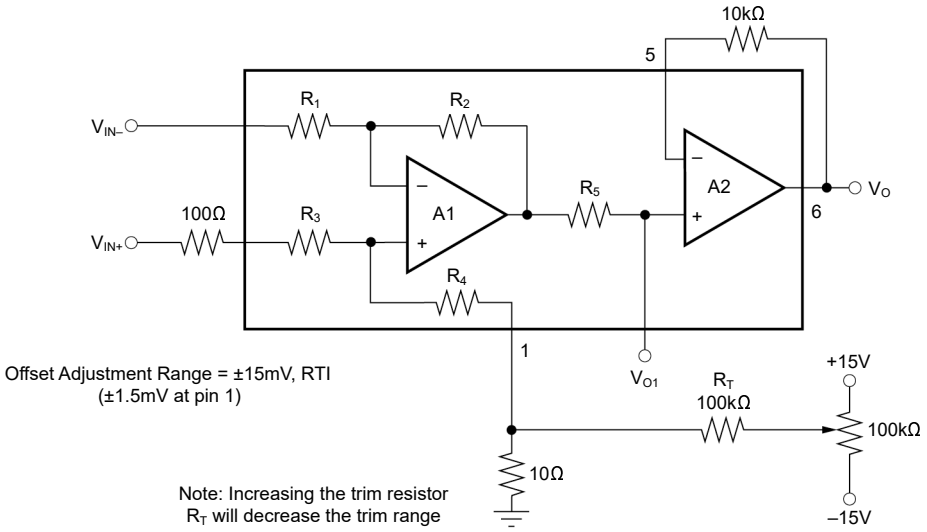


Figure 6-2. Optional Offset Trim Circuit

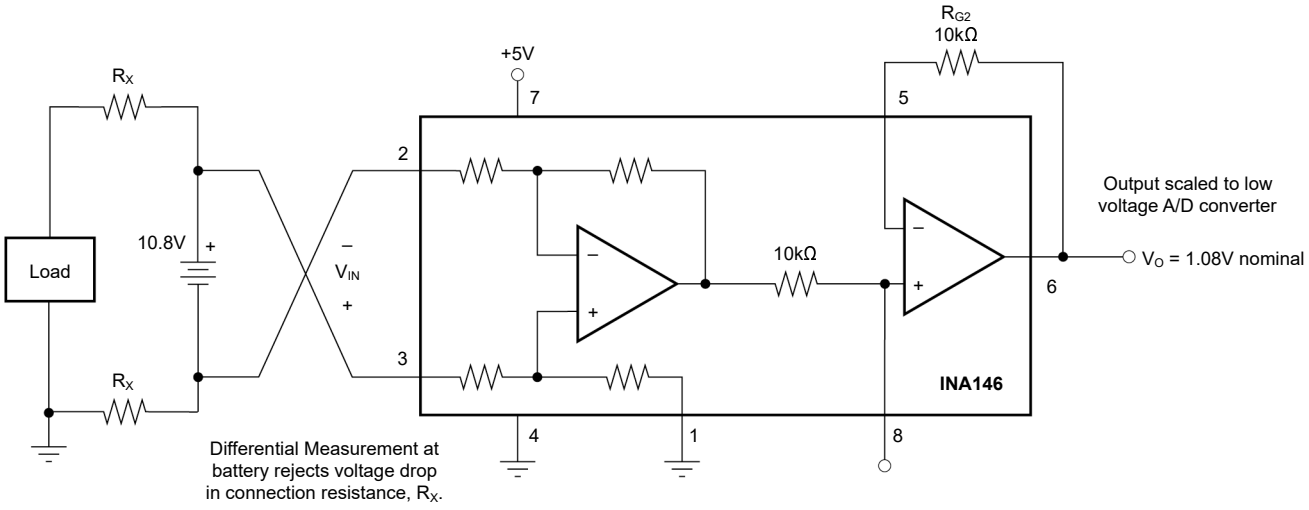


Figure 6-3. Measuring Voltages Greater Than Supply Voltage

Table 6-2. Measuring Voltage Greater Than Supply Voltage Values

V_{S+}	Max V_{IN}
+5V	40V
+7V	60V
+10V	95V
≥11V	100V

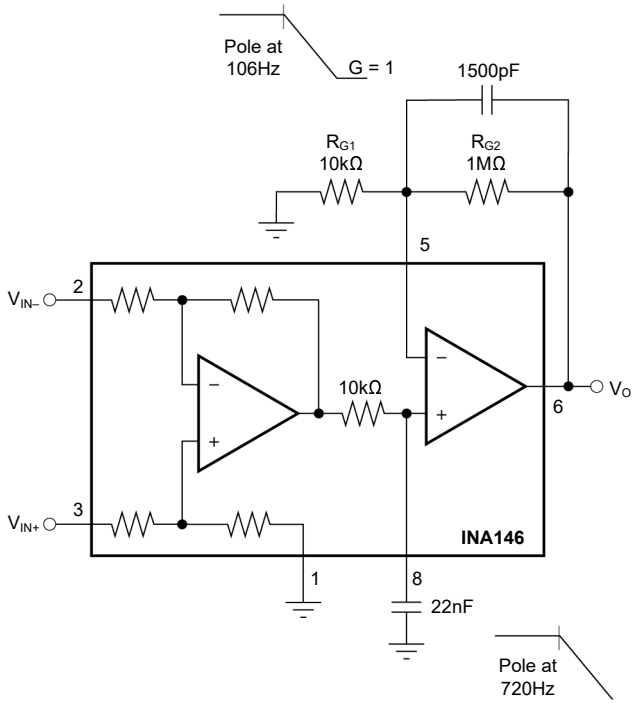


Figure 6-4. Noise Filtering

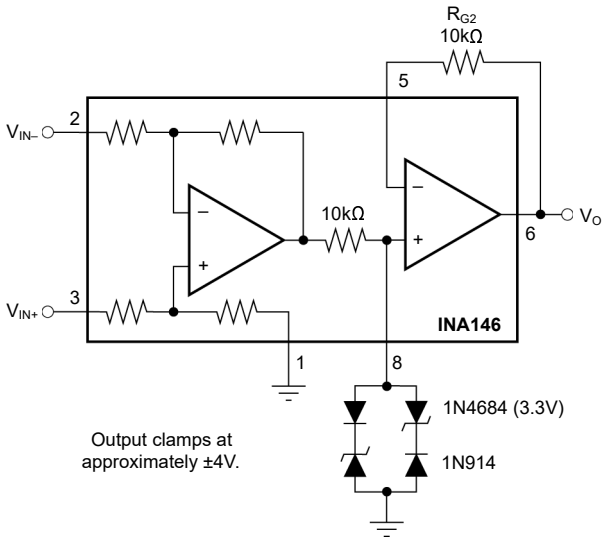
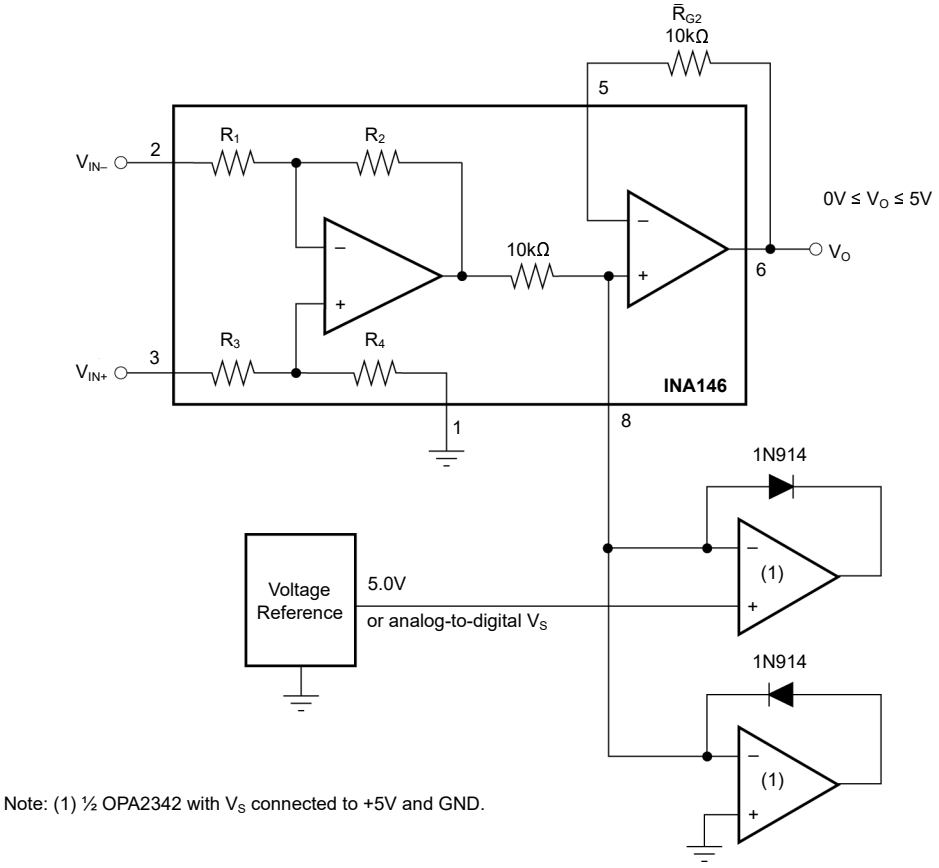


Figure 6-5. Output Clamp



Note: (1) ½ OPA2342 with V_S connected to +5V and GND.

Figure 6-6. Precision Clamp

For sense resistors (R_S) greater than 10Ω, use series compensation resistor (R_C) for good common-mode rejection. Sense resistors greater than 500Ω are not recommended.

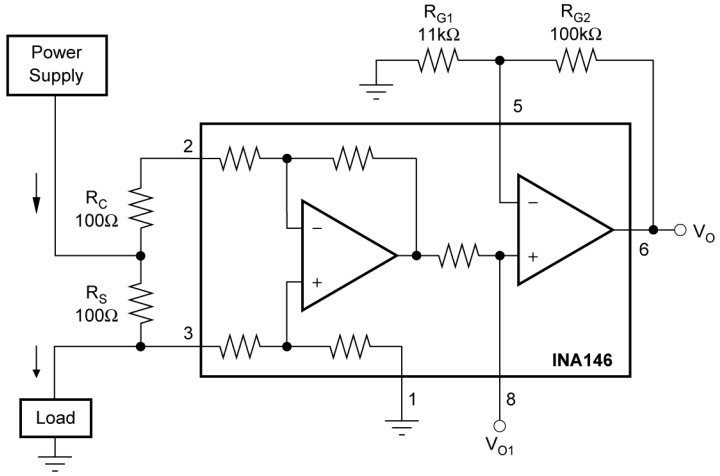


Figure 6-7. Current Monitor, G = 1

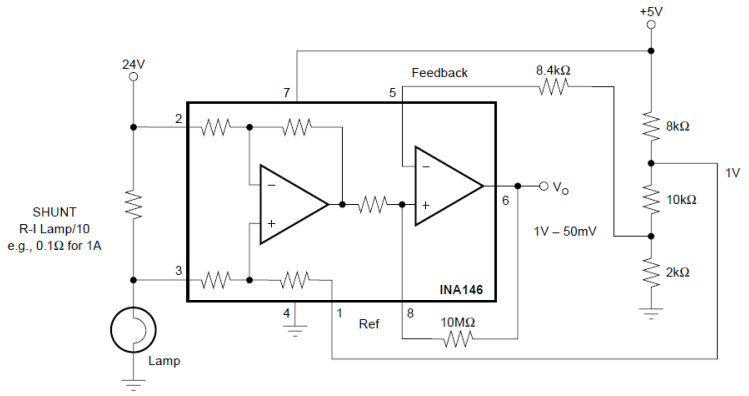


Figure 6-8. Comparator Output With Optional Hysteresis Application to Sense Lamp Burn-Out

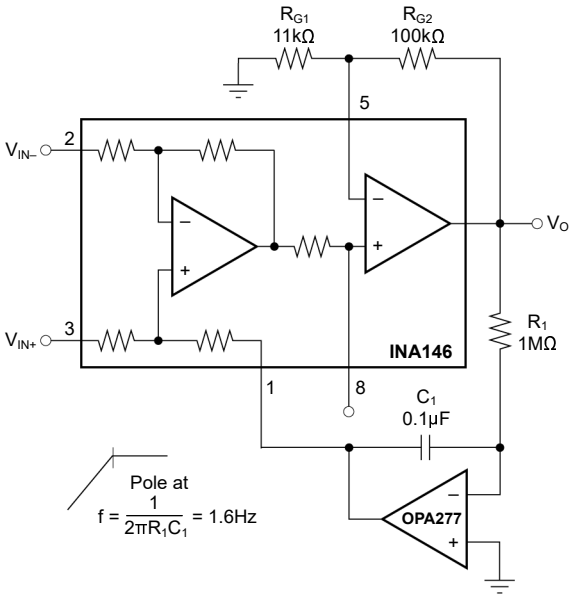


Figure 6-9. AC Coupling (DC Restoration)

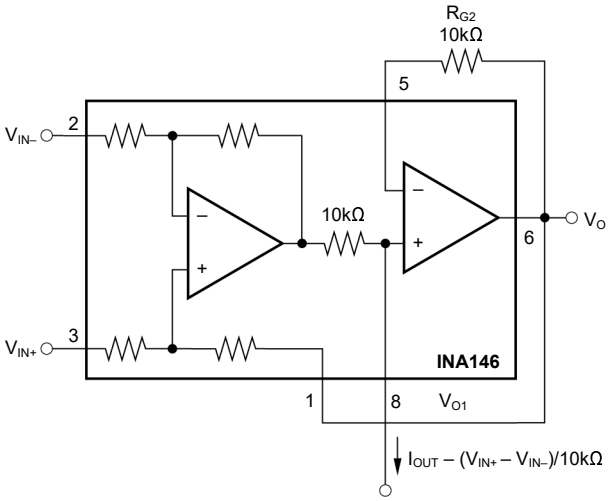


Figure 6-10. Precision Current Source

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Support

7.1.1 Device Nomenclature

Part Number	Definition
INA146UA, INA146UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.

7.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

7.3 Documentation Support

7.3.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers*, application note
- Texas Instruments, *High-Voltage Signal Conditioning for Low Voltage ADCs*, application note
- Texas Instruments, *Analog Engineer's Calculator,* application

7.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2023) to Revision B (December 2025)	Page
• Added description of device flow information in *Specifications*	4
• Merged *Electrical Characteristics* V_S = ±2.25V to ±18V and *Electrical Characteristics* V_S = 5V Single Supply into *Electrical Characteristics*	6
• Changed typical test condition V_{REF} = 0V to V_{REF} = V_S / 2 Added *all chips site origins (CSO)* condition to the typical test conditions in the *Electrical Characteristics*	6
• Change test condition V_{CM} formula to include V_{REF}	6
• Added different fabrication process specifications for Short-Circuit Current in the *Electrical Characteristics*	6
• Added different fabrication process specifications for Slew Rate in the *Electrical Characteristics*	6
• Added different fabrication process specifications for Overload Recovery in the *Electrical Characteristics*	6
• Added different fabrication process specifications for Quiescent Current in the *Electrical Characteristics*	6
• Added *all chips site origins (CSO)* condition to the typical test conditions in the *Typical Characteristics*	9
• Added CSO: SHE information to *Common-mode Rejection vs Frequency*, *Power Supply Rejection vs Frequency*, *Quiescent Current vs Temperature* and *Maximum Output Voltage Swing vs Output Current* curves in the *Typical Characteristics*	9
• Added *Slew Rate vs Temperature* and *Large-signal Step Response (G = 1, R_L = 10kΩ, C_L = 200pF* curves for CSO: SHE flow in the *Typical Characteristics*	9
• Added CSO: TID information to *Slew Rate vs Temperature* and *Large-signal Step Response (G = 1, R_L = 10kΩ, C_L = 200pF* curves in the *Typical Characteristics*	9
• Added *Common-mode Rejection vs Frequency*, *Power Supply Rejection vs Frequency*, *Output Voltage Swing vs Output Current (Sourcing)*, and *Output Voltage Swing vs Output Current (Sinking)* curves for CSO: TID in the *Typical Characteristics*	9
• Added Part Number flow information table to the *Device Nomenclature*	19

Changes from Revision * (September 1999) to Revision A (October 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 1
- Changed pin 7 from V+ to V_{S+} and pin 4 from V- to V_{S-} 3
- Added VREF = 0 V, VCM = VS / 2 "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity. 6
- Changed from Offset Voltage vs Power Supply to Power-supply rejection ratio for more clarity. 6
- Change test condition V_{CM} formula for more clarity. 6
- Added test condition "TA = –40°C to 85°C" for "Gain error vs temperature" in *Electrical Characteristics* and renamed to "Gain drift" for clarity. 6
- Added test condition "T_A = -40°C to 85°C" for Output over Temperature in Electrical Characteristics. 6
- Added test condition "Continuous to VS / 2" short-circuit current specification in *Electrical Characteristics* for clarity. 6
- Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics* 6
- Added V_{REF} = 0 V, V_{CM} = V_S / 2 to "unless otherwise noted" conditions in *Electrical Characteristics* and *Typical Characteristics* for clarity. 8

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA146UA	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	INA 146UA
INA146UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA
INA146UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 146UA
INA146UAE4	NRND	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

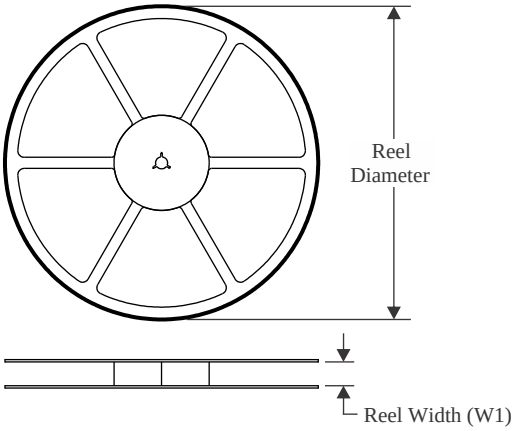
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

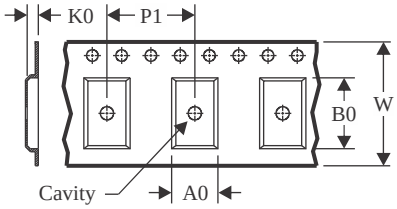
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

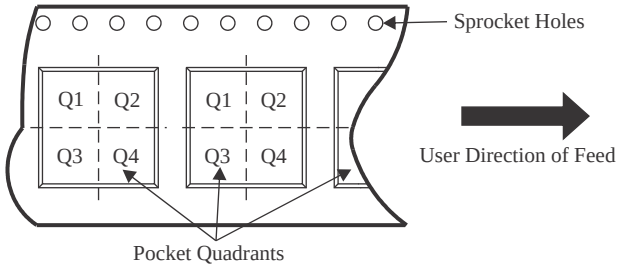


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

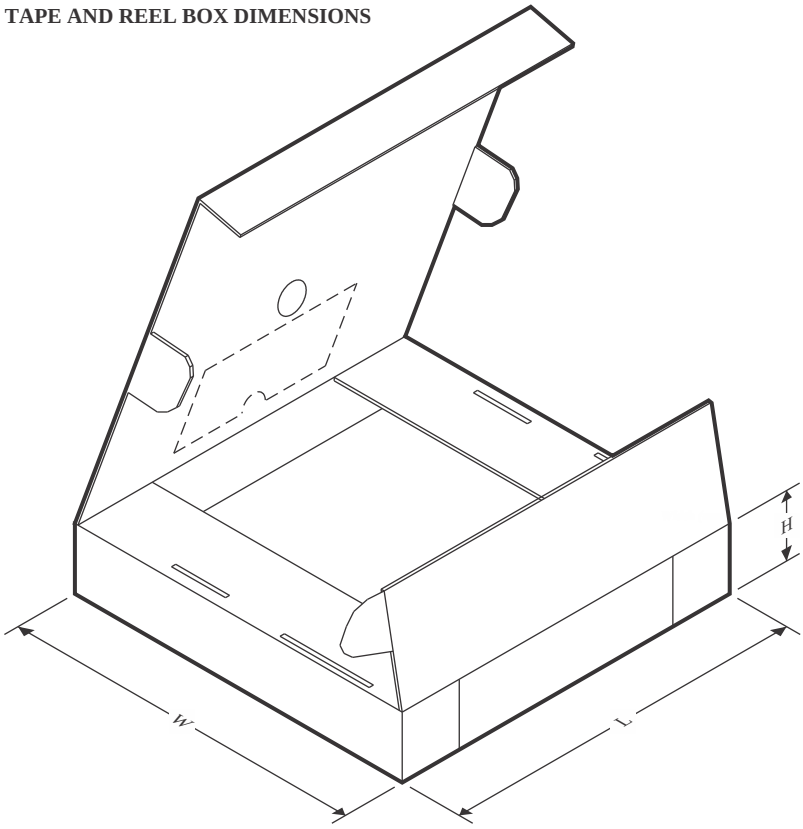
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

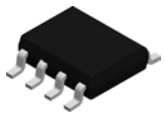
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA146UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA146UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

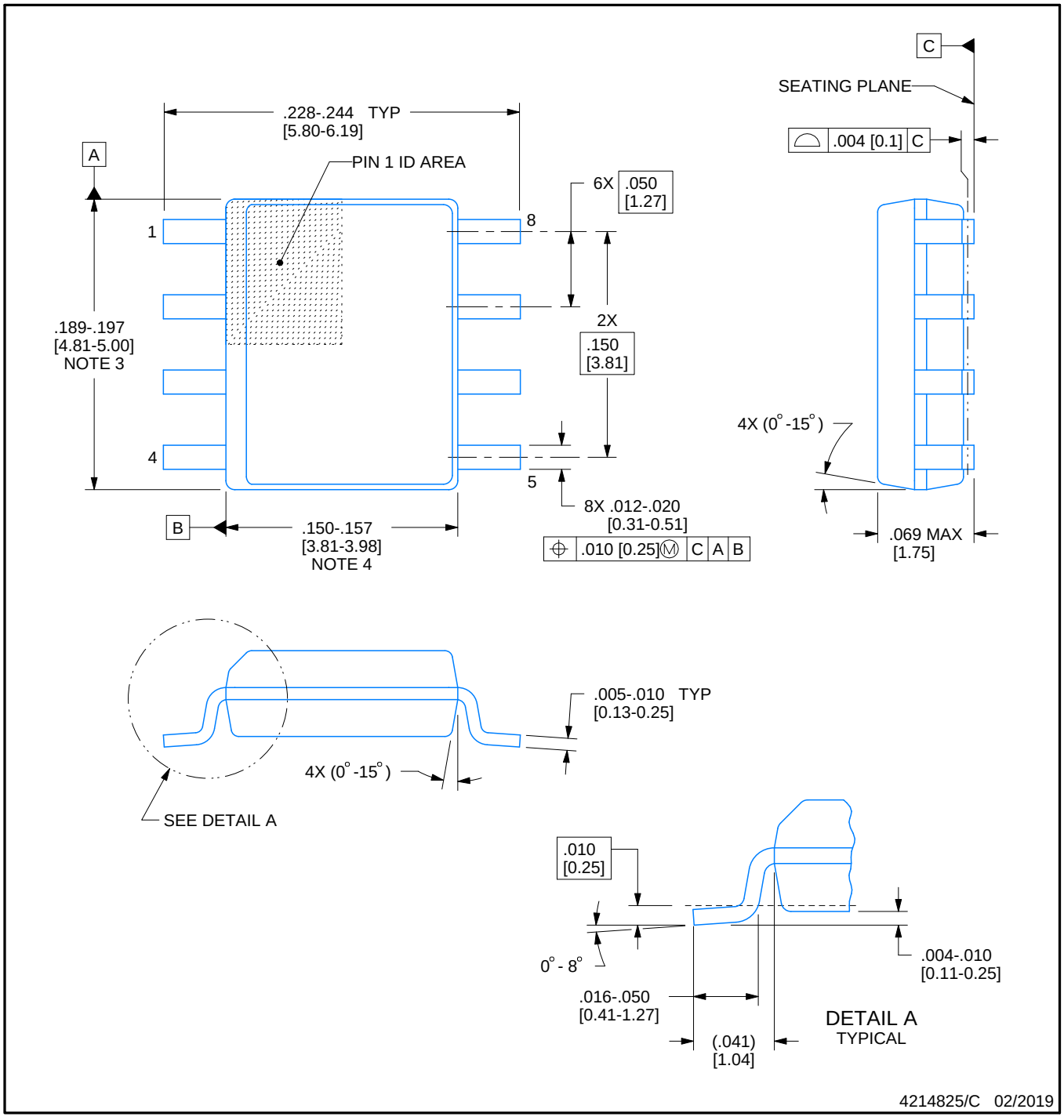


PACKAGE OUTLINE

D0008A

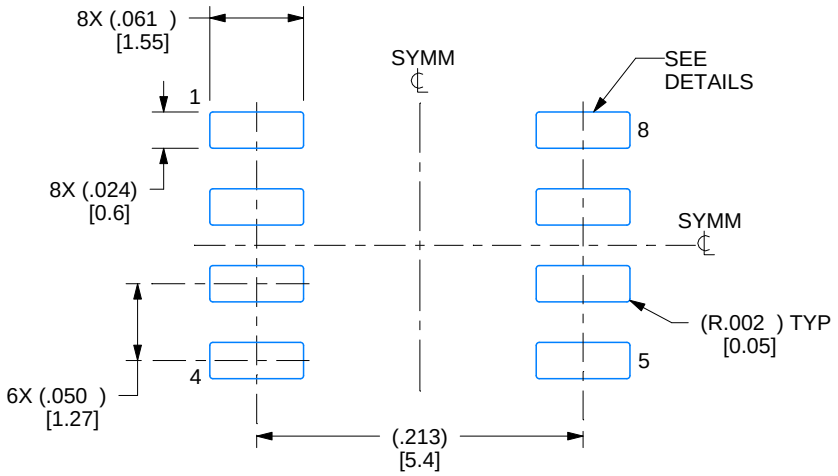
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

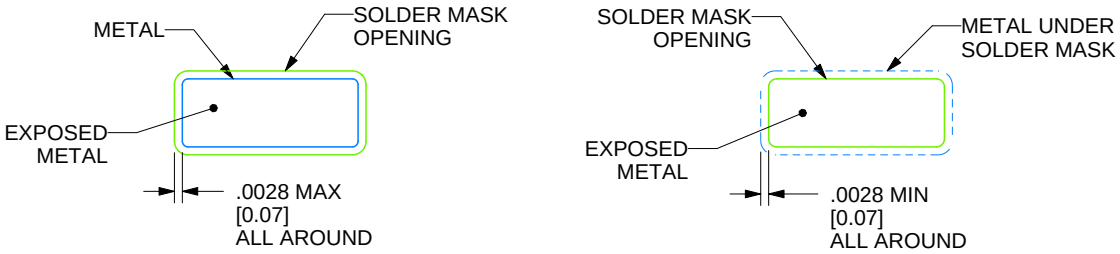


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

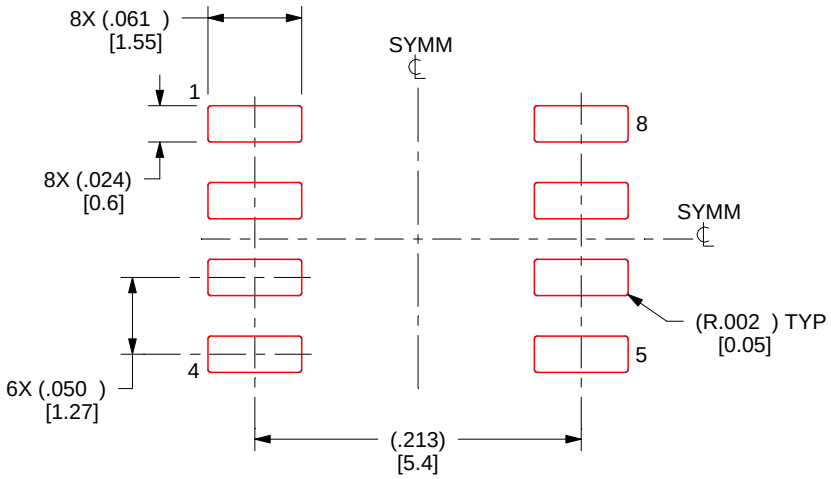
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025