

# INA239-Q1 AEC-Q100, 85-V, 16-Bit, High-Precision Power Monitor With SPI Interface

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- High-resolution, 16-bit delta-sigma ADC
- Current monitoring accuracy:
  - Offset voltage:  $\pm 5\ \mu\text{V}$  (maximum)
  - Offset drift:  $\pm 0.02\ \mu\text{V}/^{\circ}\text{C}$  (maximum)
  - Gain error:  $\pm 0.1\%$  (maximum)
  - Gain error drift:  $\pm 25\ \text{ppm}/^{\circ}\text{C}$  (maximum)
  - Common mode rejection: 140 dB (minimum)
- Power monitoring accuracy:
  - 0.7% full scale,  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (maximum)
- Fast alert response: 75  $\mu\text{s}$
- Wide common-mode range:  $-0.3\ \text{V}$  to  $+85\ \text{V}$
- Bus voltage sense input: 0 V to 85 V
- Shunt full-scale differential range:  $\pm 163.84\ \text{mV}$  /  $\pm 40.96\ \text{mV}$
- Input bias current: 2.5 nA (maximum)
- Temperature sensor:  $\pm 1^{\circ}\text{C}$  (maximum at  $25^{\circ}\text{C}$ )
- Programmable conversion time and averaging
- 10-MHz SPI communication interface
- Operates from a 2.7-V to 5.5-V supply:
  - Operational current: 640  $\mu\text{A}$  (typical)
  - Shutdown current: 5  $\mu\text{A}$  (maximum)

## 2 Applications

- [Automotive battery management systems](#)
- [EV / HEV A - KA sense applications](#)
- [DC/DC converters](#) and [power inverters](#)
- [ADAS domain controllers](#)

## 3 Description

The INA239-Q1 is an ultra-precise digital power monitor with a 16-bit delta-sigma ADC specifically designed for current-sensing applications. The device can measure a full-scale differential input of  $\pm 163.84\ \text{mV}$  or  $\pm 40.96\ \text{mV}$  across a resistive shunt sense element with common-mode voltage support from  $-0.3\ \text{V}$  to  $+85\ \text{V}$ .

The INA239-Q1 reports current, bus voltage, temperature, and power, all while performing the needed calculations in the background. The integrated temperature sensor is  $\pm 1^{\circ}\text{C}$  accurate for die temperature measurement and is useful in monitoring the system ambient temperature.

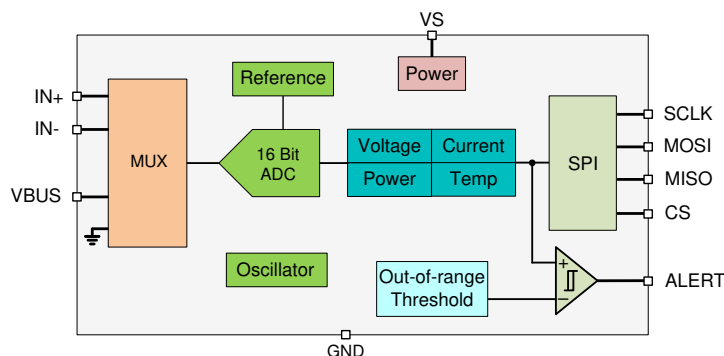
The low offset and gain drift design of the INA239-Q1 allows the device to be used in precise systems that do not undergo multi-temperature calibration during manufacturing. Further, the very low offset voltage and noise allow for use in A to kA sensing applications and provide a wide dynamic range without significant power dissipation losses on the sensing shunt element. The low input bias current of the device permits the use of larger current-sense resistors, thus providing accurate current measurements in the micro-amp range.

The device allows for selectable ADC conversion times from 50  $\mu\text{s}$  to 4.12 ms as well as sample averaging from 1x to 1024x, which further helps reduce the noise of the measured data.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA239-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



**Simplified Block Diagram**



## Table of Contents

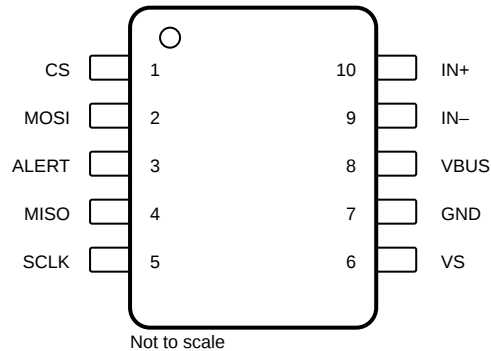
<b>1 Features</b> .....	1	7.4 Device Functional Modes.....	19
<b>2 Applications</b> .....	1	7.5 Programming.....	19
<b>3 Description</b> .....	1	7.6 Register Maps.....	21
<b>4 Revision History</b> .....	2	<b>8 Application and Implementation</b> .....	30
<b>5 Pin Configuration and Functions</b> .....	3	8.1 Application Information.....	30
<b>6 Specifications</b> .....	3	8.2 Typical Application.....	34
6.1 Absolute Maximum Ratings .....	3	<b>9 Power Supply Recommendations</b> .....	38
6.2 ESD Ratings .....	4	<b>10 Layout</b> .....	38
6.3 Recommended Operating Conditions .....	4	10.1 Layout Guidelines.....	38
6.4 Thermal Information .....	4	10.2 Layout Example.....	38
6.5 Electrical Characteristics .....	5	<b>11 Device and Documentation Support</b> .....	39
6.6 Timing Requirements (SPI) .....	7	11.1 Receiving Notification of Documentation Updates..	39
6.7 Timing Diagram .....	7	11.2 Support Resources.....	39
6.8 Typical Characteristics.....	8	11.3 Trademarks.....	39
<b>7 Detailed Description</b> .....	12	11.4 Electrostatic Discharge Caution.....	39
7.1 Overview.....	12	11.5 Glossary.....	39
7.2 Functional Block Diagram.....	12	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	39
7.3 Feature Description.....	12		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (May 2020) to Revision A (June 2021)</b>	<b>Page</b>
• Changed data sheet status from: Advanced Information to: Production Data.....	1
• Added Functional Safety bullets.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the figures and equations throughout the document to align with the commercial data sheet.....	1

## 5 Pin Configuration and Functions



**Figure 5-1. DGS Package 10-Pin VSSOP Top View**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CS	Digital input	SPI chip select (Active Low).
2	MOSI	Digital input	SPI digital data input.
3	ALERT	Digital output	Open-drain alert output, default state is active low.
4	MISO	Digital output	SPI digital data output (push-pull).
5	SCLK	Digital input	SPI clock input.
6	VS	Power supply	Power supply, 2.7 V to 5.5 V.
7	GND	Ground	Ground.
8	VBUS	Analog input	Bus voltage input.
9	IN-	Analog input	Negative input to the device. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
10	IN+	Analog input	Positive input to the device. For high-side applications, connect to power supply side of sense resistor. For low-side applications, connect to load side of sense resistor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_S$	Supply voltage		6	V
$V_{IN+}, V_{IN-}$ <sup>(2)</sup>	Differential ( $V_{IN+}$ ) – ( $V_{IN-}$ )	–40	40	V
	Common-mode	–0.3	85	V
$V_{VBUS}$		–0.3	85	V
$V_{IO}$	MOSI, MISO, SCLK, ALERT	GND – 0.3	vs. + 0.3	V
$I_{IN}$	Input current into any pin		5	mA
$I_{OUT}$	Digital output current		10	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)  $V_{IN+}$  and  $V_{IN-}$  are the voltages at the IN+ and IN– pins, respectively.

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins <sup>(1)</sup> HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011, all pins CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicated that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CM</sub>	Common-mode input range	−0.3		85	V
V <sub>S</sub>	Operating supply range	2.7		5.5	V
T <sub>A</sub>	Ambient temperature	−40		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA239-Q1	UNIT
		DGS	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	177.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	66.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	99.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	9.7	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	97.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-} = 0\text{ V}$ ,  $V_{\text{CM}} = V_{\text{IN}-} = 48\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{\text{CM}}$	Common-mode input range	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$	-0.3		85	V
$V_{\text{VBUS}}$	Bus voltage input range		0		85	V
CMRR	Common-mode rejection	$-0.3\text{ V} < V_{\text{CM}} < 85\text{ V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$	140	160		dB
$V_{\text{DIFF}}$	Shunt voltage input range	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , ADCRANGE = 0	-163.84		163.84	mV
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , ADCRANGE = 1	-40.96		40.96	mV
$V_{\text{os}}$	Shunt offset voltage	$V_{\text{CM}} = 48\text{ V}$		$\pm 1.5$	$\pm 5$	$\mu\text{V}$
		$V_{\text{CM}} = 0\text{ V}$		$\pm 1.5$	$\pm 5$	$\mu\text{V}$
$dV_{\text{os}}/dT$	Shunt offset voltage drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 2$	$\pm 20$	nV/ $^\circ\text{C}$
PSRR	Shunt offset voltage vs. power supply	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 0.1$	$\pm 1$	$\mu\text{V}/\text{V}$
$V_{\text{os\_bus}}$	$V_{\text{BUS}}$ offset voltage	$V_{\text{BUS}} = 20\text{ mV}$		$\pm 1$	$\pm 5$	mV
$dV_{\text{os}}/dT$	$V_{\text{BUS}}$ offset voltage drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 4$	$\pm 40$	$\mu\text{V}/^\circ\text{C}$
PSRR	$V_{\text{BUS}}$ offset voltage vs. power supply	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		$\pm 1.1$		mV/V
$I_B$	Input bias current	Either input, IN+ or IN-, $V_{\text{CM}} = 85\text{ V}$		0.1	2.5	nA
$Z_{\text{VBUS}}$	$V_{\text{BUS}}$ pin input impedance	Active mode	0.8	1	1.2	M $\Omega$
$I_{\text{VBUS}}$	$V_{\text{BUS}}$ pin leakage current	Shutdown mode, $V_{\text{BUS}} = 85\text{ V}$		10		nA
$R_{\text{DIFF}}$	Input differential impedance	Active mode, $V_{\text{IN}+} - V_{\text{IN}-} < 164\text{ mV}$		92		k $\Omega$
<b>DC ACCURACY</b>						
$G_{\text{SERR}}$	Shunt voltage gain error			$\pm 0.01$	$\pm 0.1$	%
$G_{\text{S\_DRFT}}$	Shunt voltage gain error drift				$\pm 25$	ppm/ $^\circ\text{C}$
$G_{\text{BERR}}$	$V_{\text{BUS}}$ voltage gain error			$\pm 0.01$	$\pm 0.1$	%
$G_{\text{B\_DRFT}}$	$V_{\text{BUS}}$ voltage gain error drift				$\pm 25$	ppm/ $^\circ\text{C}$
$P_{\text{TME}}$	Power total measurement error (TME)	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , at full scale			$\pm 0.7$	%
	ADC resolution			16		Bits
	1 LSB step size	Shunt voltage, ADCRANGE = 0		5		$\mu\text{V}$
		Shunt voltage, ADCRANGE = 1		1.25		$\mu\text{V}$
		Bus voltage		3.125		mV
		Temperature		125		$\text{m}^\circ\text{C}$
$T_{\text{CT}}$	ADC conversion-time <sup>(1)</sup>	Conversion time field = 0h		50		$\mu\text{s}$
		Conversion time field = 1h		84		
		Conversion time field = 2h		150		
		Conversion time field = 3h		280		
		Conversion time field = 4h		540		
		Conversion time field = 5h		1052		
		Conversion time field = 6h		2074		
		Conversion time field = 7h		4120		
INL	Integral Non-Linearity			$\pm 2$		m%
DNL	Differential Non-Linearity			0.2		LSB
<b>CLOCK SOURCE</b>						
$F_{\text{OSC}}$	Internal oscillator frequency			1		MHz
$F_{\text{OSC\_TOL}}$	Internal oscillator frequency tolerance	$T_A = 25\text{ }^\circ\text{C}$			$\pm 0.5$	%
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$			$\pm 1$	%

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-} = 0\text{ V}$ ,  $V_{\text{CM}} = V_{\text{IN}-} = 48\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TEMPERATURE SENSOR</b>						
	Measurement range		-40		+125	$^\circ\text{C}$
	Temperature accuracy	$T_A = 25\text{ }^\circ\text{C}$		$\pm 0.15$	$\pm 1$	$^\circ\text{C}$
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 0.2$	$\pm 2$	$^\circ\text{C}$
<b>POWER SUPPLY</b>						
$V_S$	Supply voltage		2.7		5.5	V
$I_Q$	Quiescent current	$V_{\text{SENSE}} = 0\text{ V}$		640	750	$\mu\text{A}$
		$V_{\text{SENSE}} = 0\text{ V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$			1.1	mA
$I_{\text{QSD}}$	Quiescent current, shutdown	Shutdown mode		2.8	5	$\mu\text{A}$
$T_{\text{POR}}$	Device start-up time	Power-up (NPOR)		300		$\mu\text{s}$
		From shutdown mode		60		
<b>DIGITAL INPUT / OUTPUT</b>						
$V_{\text{IH}}$	Logic input level, high		1.2		$V_S$	V
$V_{\text{IL}}$	Logic input level, low		GND		0.4	V
$V_{\text{OL}}$	Logic output level, low	$I_{\text{OL}} = 1\text{ mA}$	GND		0.4	V
$V_{\text{OH}}$	Logic output level, high	$I_{\text{OL}} = 1\text{ mA}$	$V_S - 0.4$		$V_S$	V
$I_{\text{IO\_LEAK}}$	Digital leakage input current	$0 \leq V_{\text{IN}} \leq V_S$	-1		1	$\mu\text{A}$

(1) Subject to oscillator accuracy and drift

## 6.6 Timing Requirements (SPI)

		MIN	NOM	MAX	UNIT
<b>SERIAL INTERFACE</b>					
$f_{\text{SPI}}$	SPI bit frequency			10	MHz
$t_{\text{SCLK\_H}}$	SCLK high time	40			ns
$t_{\text{SCLK\_L}}$	SCLK low time	40			ns
$t_{\text{CSF\_SCLKR}}$	CS fall to first SCLK rise time	10			ns
$t_{\text{SCLKF\_CSR}}$	Last SCLK fall to CS rise time	10			ns
$t_{\text{FRM\_DLY}}$	Sequential transfer delay <sup>(1)</sup>	50			ns
$t_{\text{MOSI\_RF}}$	MOSI Rise and Fall time, 10 MHz SCLK			15	ns
$t_{\text{MOSI\_ST}}$	MOSI data setup time	10			ns
$t_{\text{MOSI\_HLD}}$	MOSI data hold time	20			ns
$t_{\text{MISO\_RF}}$	MISO Rise and Fall time, $C_{\text{LOAD}} = 200 \text{ pF}$			15	ns
$t_{\text{MISO\_ST}}$	MISO data setup time	20			ns
$t_{\text{MISO\_HLD}}$	MISO data hold time	20			ns
$t_{\text{CS\_MISO\_DLY}}$	CS falling edge to MISO data valid delay time			25	ns
$t_{\text{CS\_MISO\_HIZ}}$	CS rising edge to MISO high impedance delay time			25	ns

(1) Optional. The SPI interface can operate without the CS pin assistance as long as the pin is held low.

## 6.7 Timing Diagram

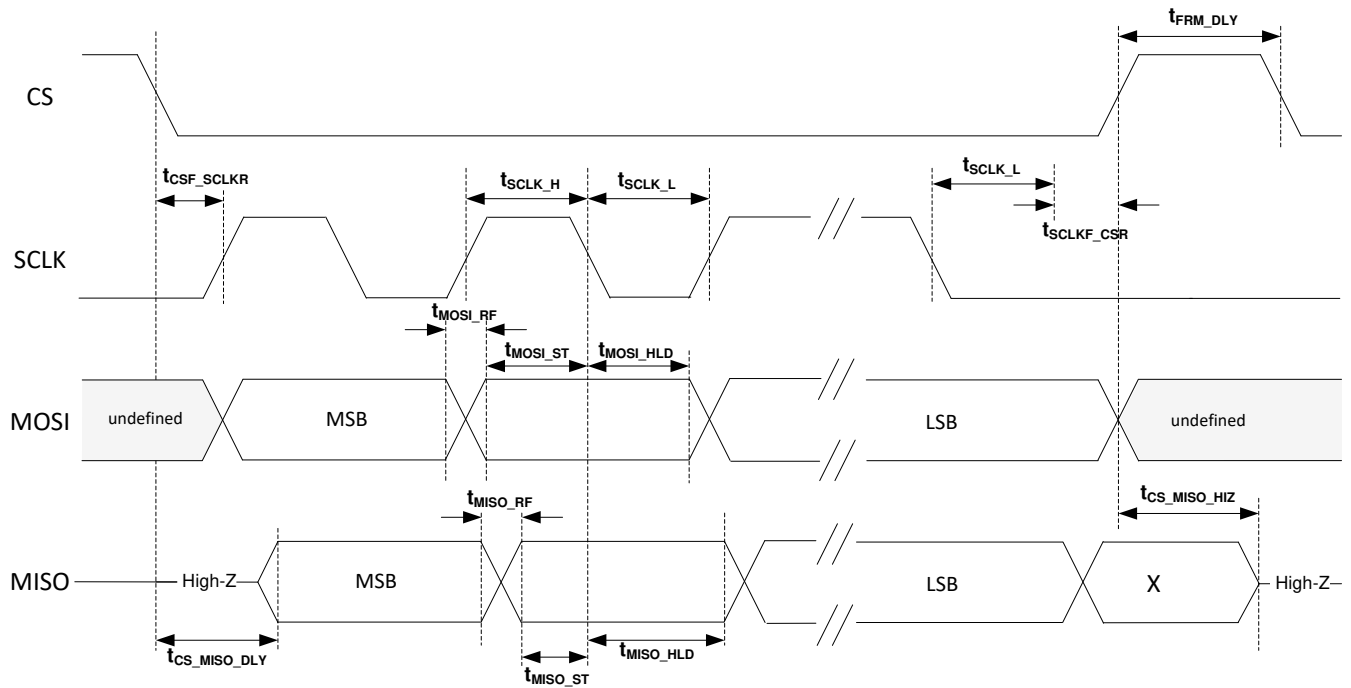


Figure 6-1. SPI Timing Diagram

## 6.8 Typical Characteristics

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{VS} = 3.3\text{ V}$ ,  $V_{CM} = 48\text{ V}$ ,  $V_{SENSE} = 0$ , and  $V_{VBUS} = 48\text{ V}$  (unless otherwise noted)

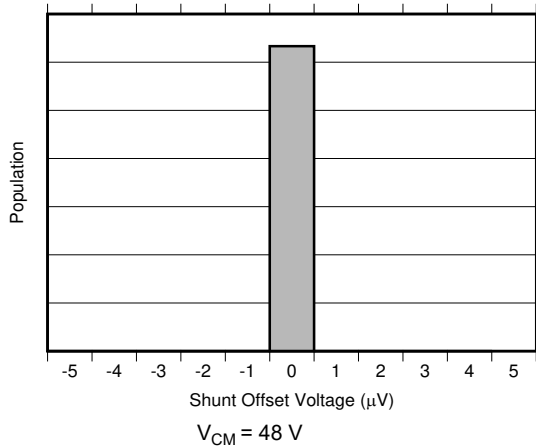


Figure 6-2. Shunt Input Offset Voltage Production Distribution

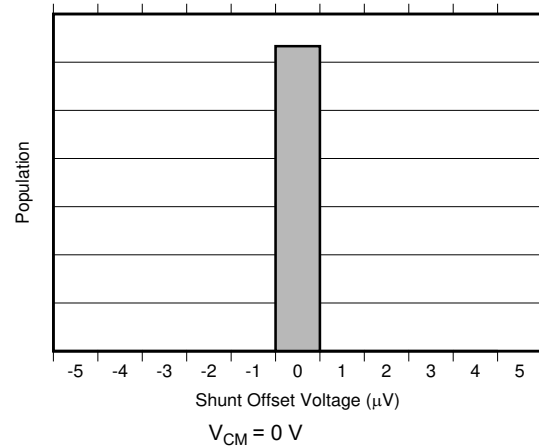


Figure 6-3. Shunt Input Offset Voltage Production Distribution

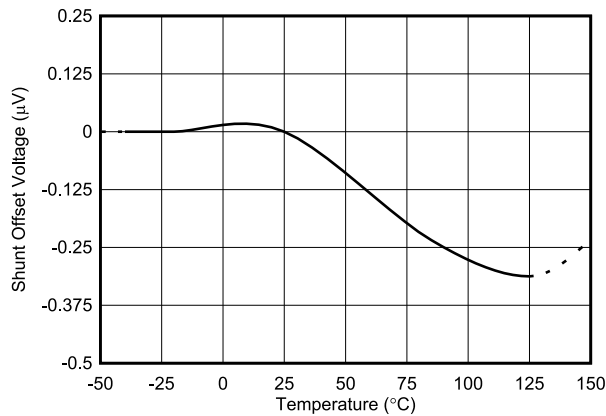


Figure 6-4. Shunt Input Offset Voltage vs. Temperature

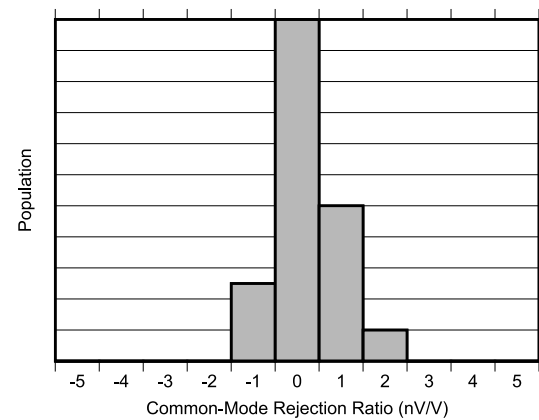


Figure 6-5. Common-Mode Rejection Ratio Production Distribution

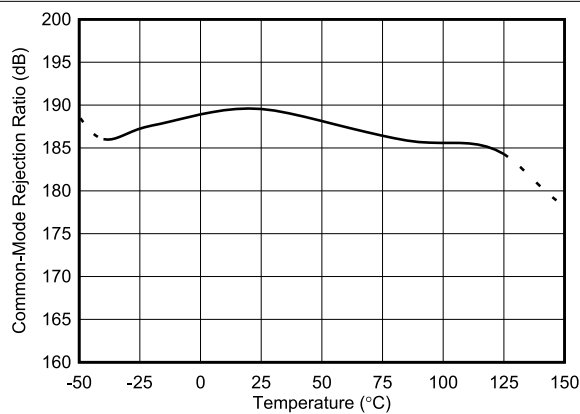


Figure 6-6. Shunt Input Common-Mode Rejection Ratio vs. Temperature

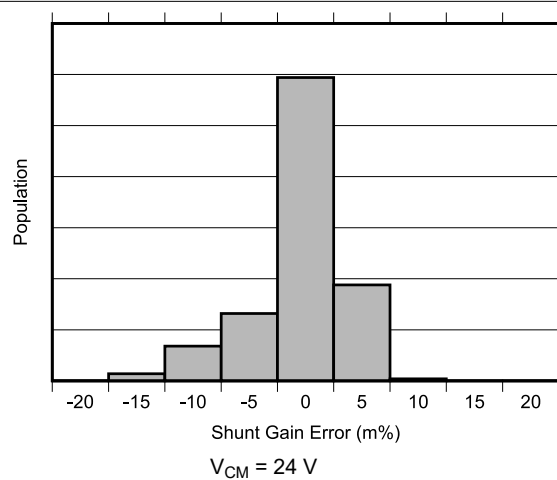
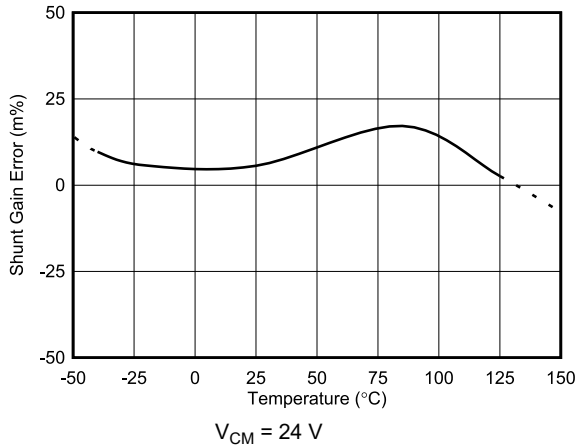


Figure 6-7. Shunt Input Gain Error Production Distribution

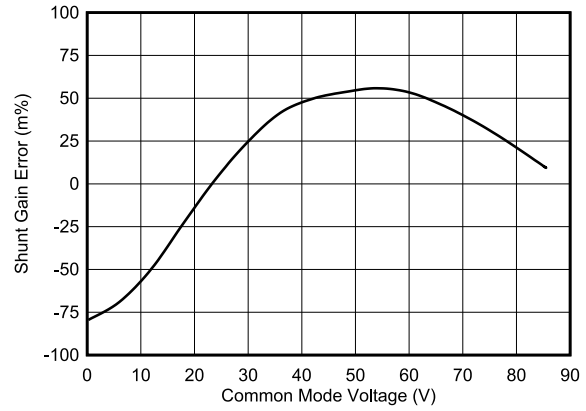


### 6.8 Typical Characteristics (continued)

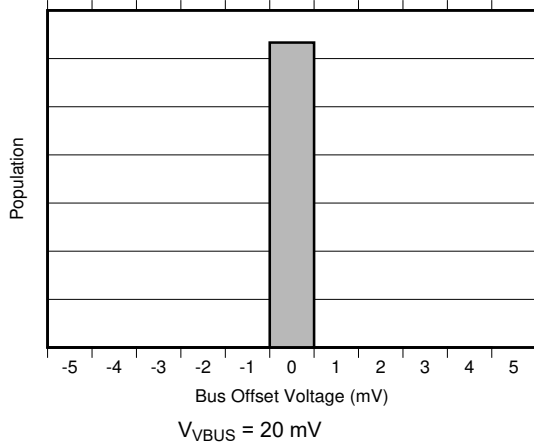
at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{VS} = 3.3\text{ V}$ ,  $V_{CM} = 48\text{ V}$ ,  $V_{SENSE} = 0$ , and  $V_{VBUS} = 48\text{ V}$  (unless otherwise noted)



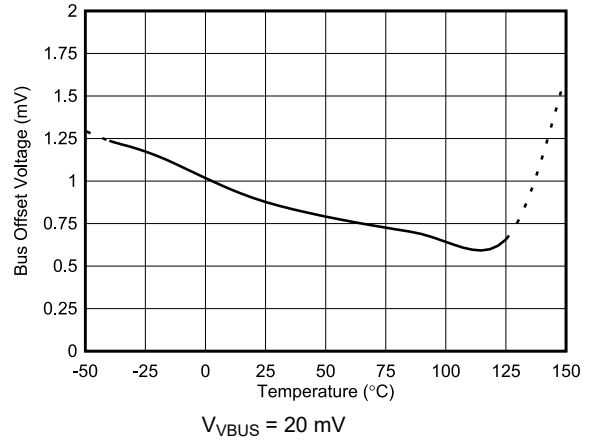
**Figure 6-8. Shunt Input Gain Error vs. Temperature**



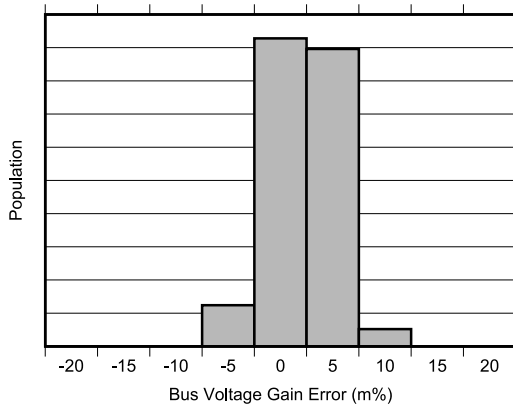
**Figure 6-9. Shunt Input Gain Error vs. Common-Mode Voltage**



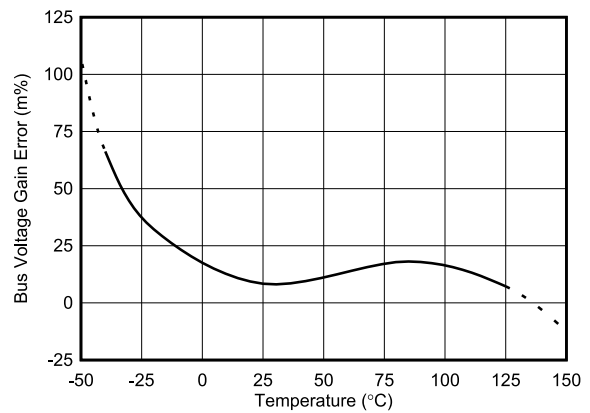
**Figure 6-10. Bus Input Offset Voltage Production Distribution**



**Figure 6-11. Bus Input Offset Voltage vs. Temperature**



**Figure 6-12. Bus Input Gain Error Production Distribution**



**Figure 6-13. Bus Input Gain Error vs. Temperature**

### 6.8 Typical Characteristics (continued)

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{VS} = 3.3\text{ V}$ ,  $V_{CM} = 48\text{ V}$ ,  $V_{SENSE} = 0$ , and  $V_{VBUS} = 48\text{ V}$  (unless otherwise noted)

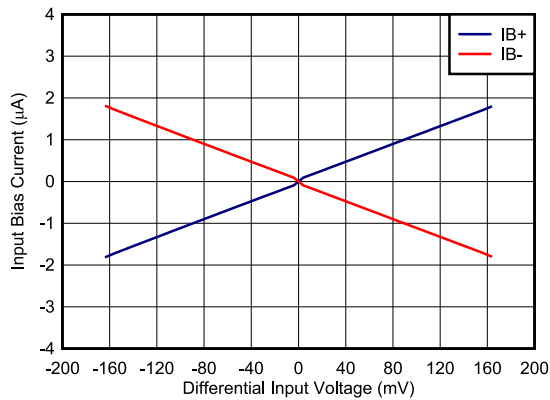


Figure 6-14. Input Bias Current vs. Differential Input Voltage

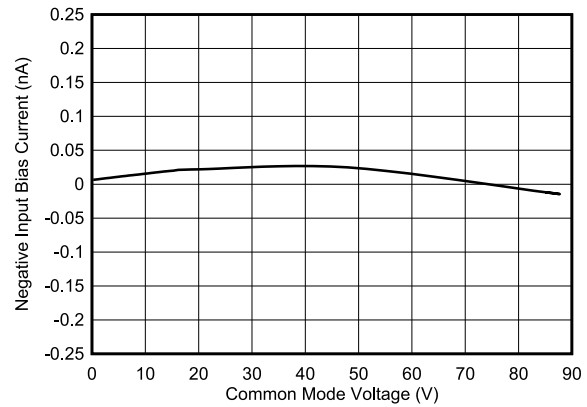


Figure 6-15. Input Bias Current (IB+ or IB-) vs. Common-Mode Voltage

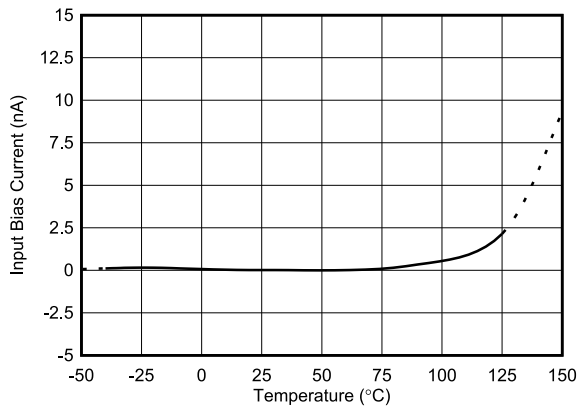


Figure 6-16. Input Bias Current vs. Temperature

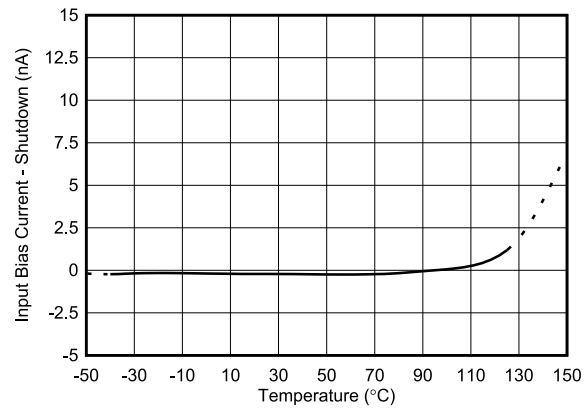


Figure 6-17. Input Bias Current vs. Temperature, Shutdown

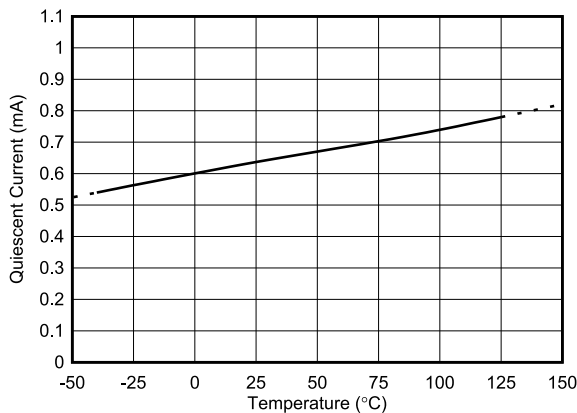


Figure 6-18. Active  $I_Q$  vs. Temperature

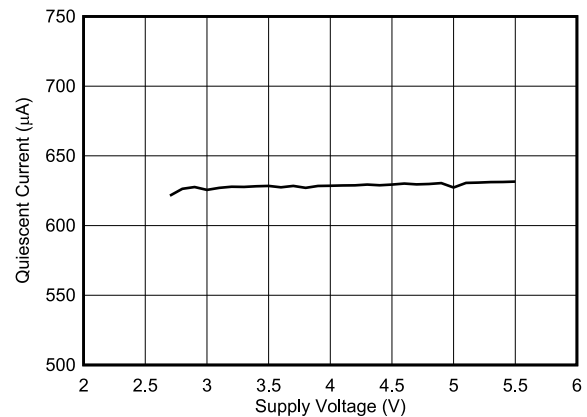


Figure 6-19. Active  $I_Q$  vs. Supply Voltage

### 6.8 Typical Characteristics (continued)

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{VS} = 3.3\text{ V}$ ,  $V_{CM} = 48\text{ V}$ ,  $V_{SENSE} = 0$ , and  $V_{VBUS} = 48\text{ V}$  (unless otherwise noted)

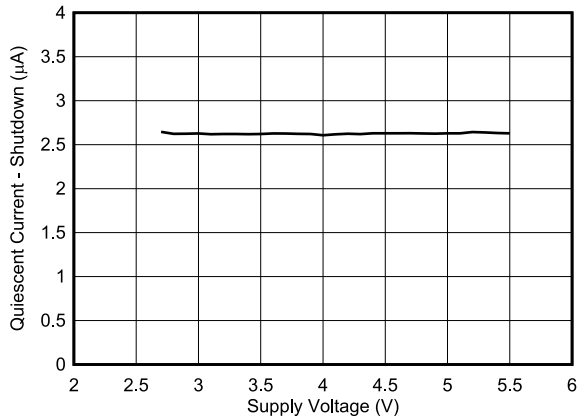


Figure 6-20. Shutdown  $I_Q$  vs. Supply Voltage

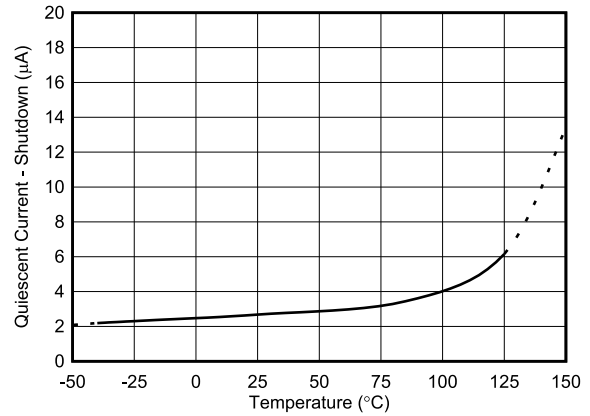


Figure 6-21. Shutdown  $I_Q$  vs. Temperature

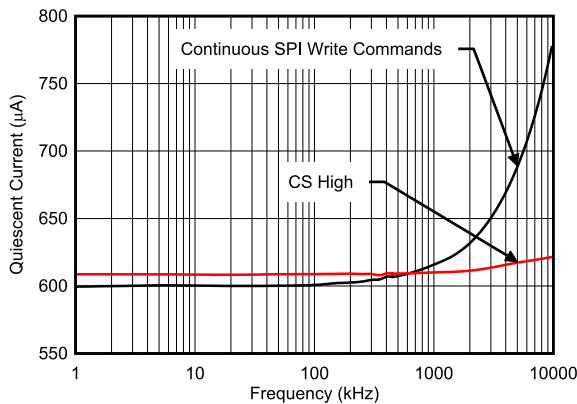


Figure 6-22. Active  $I_Q$  vs. Clock Frequency

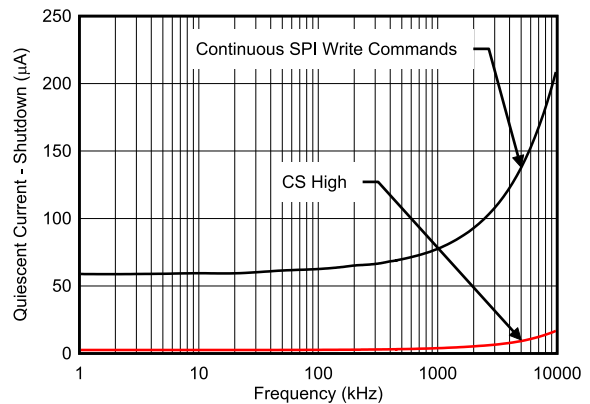


Figure 6-23. Shutdown  $I_Q$  vs. Clock Frequency

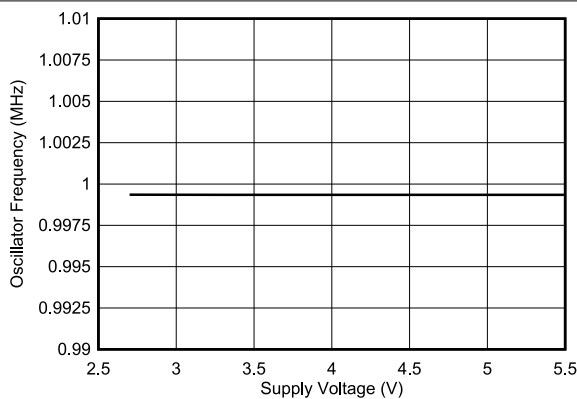


Figure 6-24. Internal Clock Frequency vs. Power Supply

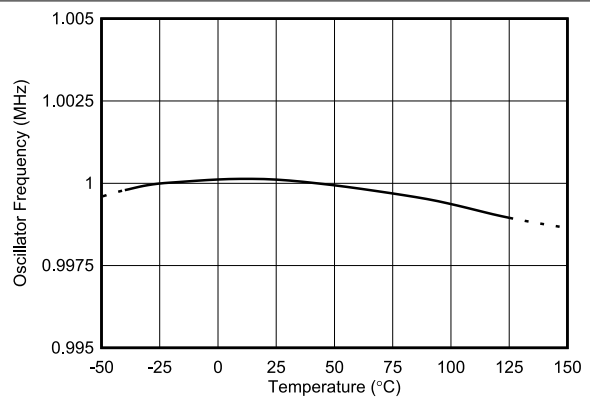


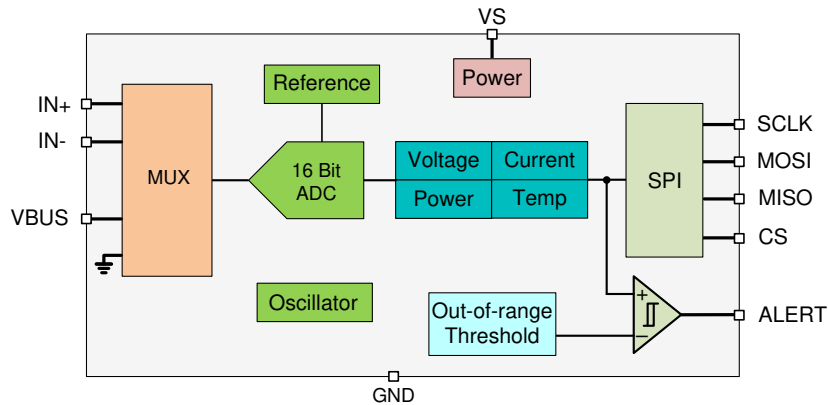
Figure 6-25. Internal Clock Frequency vs. Temperature

## 7 Detailed Description

### 7.1 Overview

The INA239-Q1 device is a digital current sense amplifier with a 4-wire SPI digital interface. It measures shunt voltage, bus voltage and internal temperature while calculating current, power necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation. Detailed register information is found in [Section 7.6](#).

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Versatile High Voltage Measurement Capability

The INA239-Q1 operates off a 2.7 V to 5.5 V supply but can measure voltage and current on rails as high as 85 V. The current is measured by sensing the voltage drop across an external shunt resistor at the IN+ and IN– pins. The input stage of the INA239-Q1 is designed such that the input common-mode voltage can be higher than the device supply voltage,  $V_S$ . The supported common-mode voltage range at the input pins is  $-0.3$  V to  $+85$  V, which makes the device well suited for both high-side and low-side current measurements. There are no special considerations for power-supply sequencing because the common-mode input range and device supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa without damaging the device.

The device also measures the bus supply voltage through the  $V_{BUS}$  pin and temperature through the integrated temperature sensor. The differential shunt voltage is measured between the IN+ and IN– pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0 V to 85 V, while monitored temperatures can range from  $-40$  °C to  $+125$  °C.

Shunt voltage, bus voltage, and temperature measurements are multiplexed internally to a single ADC as shown in [Figure 7-1](#).

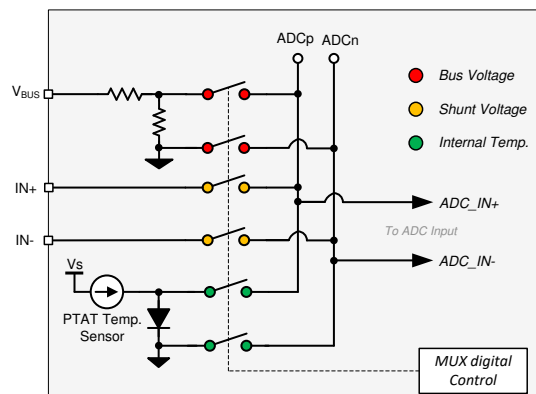
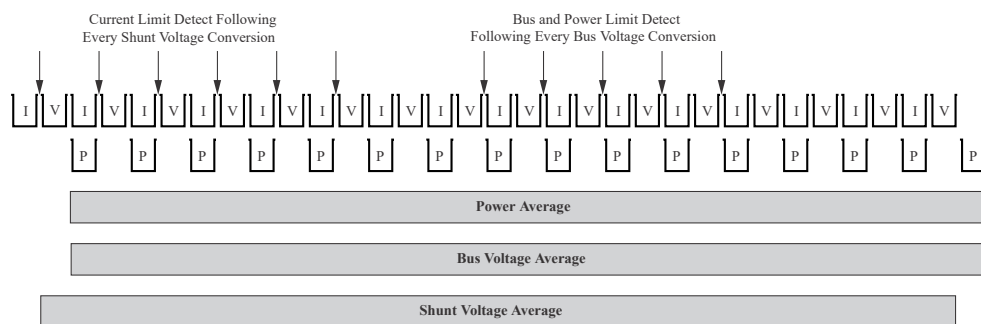


Figure 7-1. High-Voltage Input Multiplexer

### 7.3.2 Power Calculation

The current and power are calculated after a shunt voltage and bus voltage measurement as shown in [Figure 7-2](#). Power is calculated based on the previous current calculation and the latest bus voltage measurement. If the value loaded into the SHUNT\_CAL register is zero, the power value reported is also zero. The current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers where they can then be read. These calculations are performed in the background and do not add to the overall conversion time.



**Figure 7-2. Power Calculation Scheme**

### 7.3.3 Low Bias Current

The INA239-Q1 features very low input bias current which provides several benefits. The low input bias current of the INA239-Q1 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that it allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense amplifiers, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

The bias current in the INA239-Q1 is the smallest when the sensed current is zero. As the current starts to increase, the differential voltage drop across the shunt resistor increases which results in an increase in the bias current as shown in [Input Bias Current vs. Differential Input Voltage](#).

### 7.3.4 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current flow at the shunt voltage measurement channel. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs as shown in [Figure 7-1](#). The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across the common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0-V offset voltage that maximizes the useful dynamic range of the system.

The INA239-Q1 can measure the shunt voltage, bus voltage, and die temperature, or a combination of any based on the selected MODE bits setting in the ADC\_CONFIG register. This permits selecting modes to convert only the shunt voltage or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. When no averaging is selected, once an ADC conversion is completed, the converted values are independently updated in their corresponding registers where they can be read through the digital interface at the time of conversion end. The conversion time for shunt voltage, bus voltage, and temperature inputs are set independently from 50  $\mu$ s to 4.12ms depending on the values programmed in the ADC\_CONFIG register. Enabled measurement inputs are converted sequentially so the total time to convert all inputs depends on the conversion time for each input and the number of inputs enabled. When averaging is used, the intermediate values are subsequently stored in an averaging accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging has been completed, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—continuous and triggered—set by the MODE bits in ADC\_CONFIG register. In continuous-conversion mode, the ADC will continuously convert the input measurements and update the output registers as described above in an indefinite loop. In triggered-conversion mode, the ADC will convert the input measurements as described above, after which the ADC will go into shutdown mode until another single-shot trigger is generated by writing to the MODE bits. Writing the MODE bits will interrupt and restart triggered or continuous conversions that are in progress. Although the device can be read at any time, and the data from the last conversion remains available, the Conversion Ready flag (CNVRF bit in DIAG\_ALERT register) is provided to help coordinate triggered conversions. This bit is set after all conversions and averaging is completed.

The Conversion Ready flag (CNVRF) clears under these conditions:

- Writing to the ADC\_CONFIG register (except for selecting shutdown mode); or
- Reading the DIAG\_ALERT Register

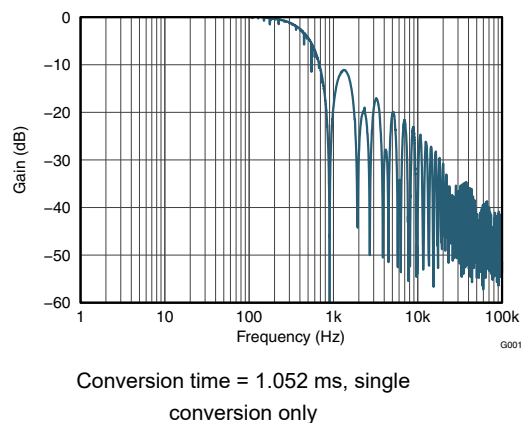
While the INA239-Q1 device is used in either one of the conversion modes, a dedicated digital engine is calculating the current and power values in the background as described in [Section 7.3.2](#). All of the calculations are performed in the background and do not contribute to conversion time.

For applications that must synchronize with other components in the system, the INA239-Q1 conversion can be delayed by programming the CONVDLY bits in CONFIG register in the range between 0 (no delay) and 510

ms. The resolution in programming the conversion delay is 2 ms. The conversion delay is set to 0 by default. Conversion delay can assist in measurement synchronization when multiple external devices are used for voltage or current monitoring purposes. In applications where an time aligned voltage and current measurements are needed, two devices can be used with the current measurement delayed such that the external voltage and current measurements will occur at approximately the same time. Keep in mind that even though the internal time base for the ADC is precise, synchronization will be lost over time due to internal and external time base mismatch.

#### 7.3.4.1 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods  $T_{CT}$  from 50  $\mu$ s to 4.12 ms. With this configuration the first amplitude notch appears at the Nyquist frequency of the output signal which is determined by the selected conversion time period and defined as  $f_{NOTCH} = 1 / (2 \times T_{CT})$ . This means that the filter cut-off frequency will scale proportionally with the data output rate as described. [ADC Frequency Response](#) shows the filter response when the 1.052 ms conversion time period is selected.



**Figure 7-3. ADC Frequency Response**

#### 7.3.4.2 Flexible Conversion Times and Averaging

ADC conversion times for shunt voltage, bus voltage and temperature can be set independently from 50  $\mu$ s to 4.12 ms. The flexibility in conversion time allows for robust operation in a variety of noisy environments. The device also allows for programmable averaging times from a single conversion all the way to an average of 1024 conversions. The amount of averaging selected applies uniformly to all active measurement inputs. The ADC\_CONFIG register shown in [Table 7-6](#) provides additional details on the supported conversion times and averaging modes. The INA239-Q1 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages. [Figure 7-4](#) and [Figure 7-5](#) shown below illustrate the effect of conversion time and averaging on a constant input signal.



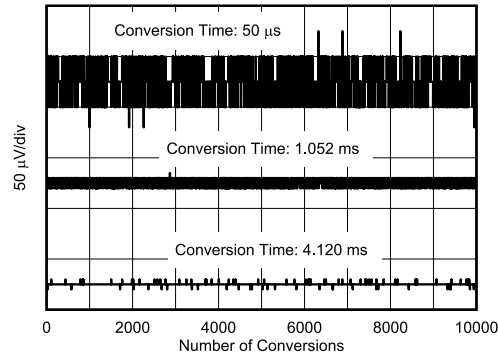


Figure 7-4. Noise vs. Conversion Time (Averaging = 1)

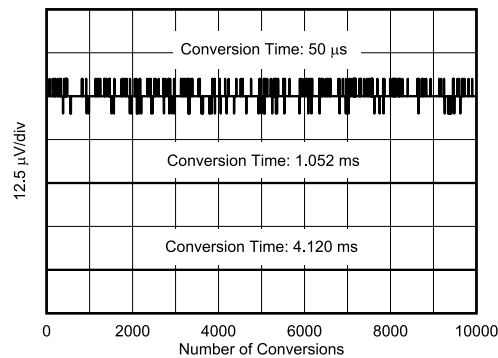


Figure 7-5. Noise vs. Conversion Time (Averaging = 128)

Settings for the conversion time and number of conversions averaged impact the effective measurement resolution. For more detailed information on how averaging reduces noise and increases the effective number of bits (ENOB) see [Section 8.1.3](#).

### 7.3.5 Integrated Precision Oscillator

The internal timebase of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions. The digital filter response varies with conversion time; therefore, the precise clock ensures filter response and notch frequency consistency across temperature. On power up, the internal oscillator and ADC take roughly 300 µs to reach <1% error stability. Once the clock stabilizes, the ADC data output will be accurate to the electrical specifications provided in [Section 6](#).

### 7.3.6 Multi-Alert Monitoring and Fault Detection

The INA239-Q1 includes a multipurpose, open-drain ALERT output pin that can be used to report multiple diagnostics or as an indicator that the ADC conversion is complete when the device is operating in both triggered and continuous conversion mode. The diagnostics listed in [Table 7-1](#) are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses its associated out-of-range threshold.

Table 7-1. ALERT Diagnostics Description

INA239-Q1 DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Shunt Under Voltage Limit	SHNTUL	SUVL	0x8000 h (two's complement)
Shunt Over Voltage Limit	SHNTOL	SOVL	0x7FFF h (two's complement)

**Table 7-1. ALERT Diagnostics Description (continued)**

INA239-Q1 DIAGNOSTIC	STATUS BIT IN DIAG_ALRT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (two's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

A read of the DIAG\_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register, shown in [Table 7-13](#), is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert latch enable — In case the ALERT pin is triggered, this function will hold the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG\_ALRT register will reset the status of the ALERT pin. This function is enabled by setting the ALATCH bit.
- Conversion ready enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise. However, the diagnostic will be delayed due to the time needed for averaging. This function is enabled by setting the SLOWALERT bit.
- Alert polarity — Allows the device to invert the active state of the ALERT pin. Note that the ALERT pin is an open-drain output that must be pulled-up by a resistor. The ALERT pin is active-low by default and can be configured for active high function using the APOL control bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG\_ALRT register:

- Math overflow — Indicated by the MATHOF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit should always read '1' when the device is operating properly.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. [Figure 7-6](#) shows an example where the device reports ADC conversion complete events while the INA239-Q1 device is subject to shunt over voltage (over current) event, bus under voltage event, over temperature event and over power-limit event.

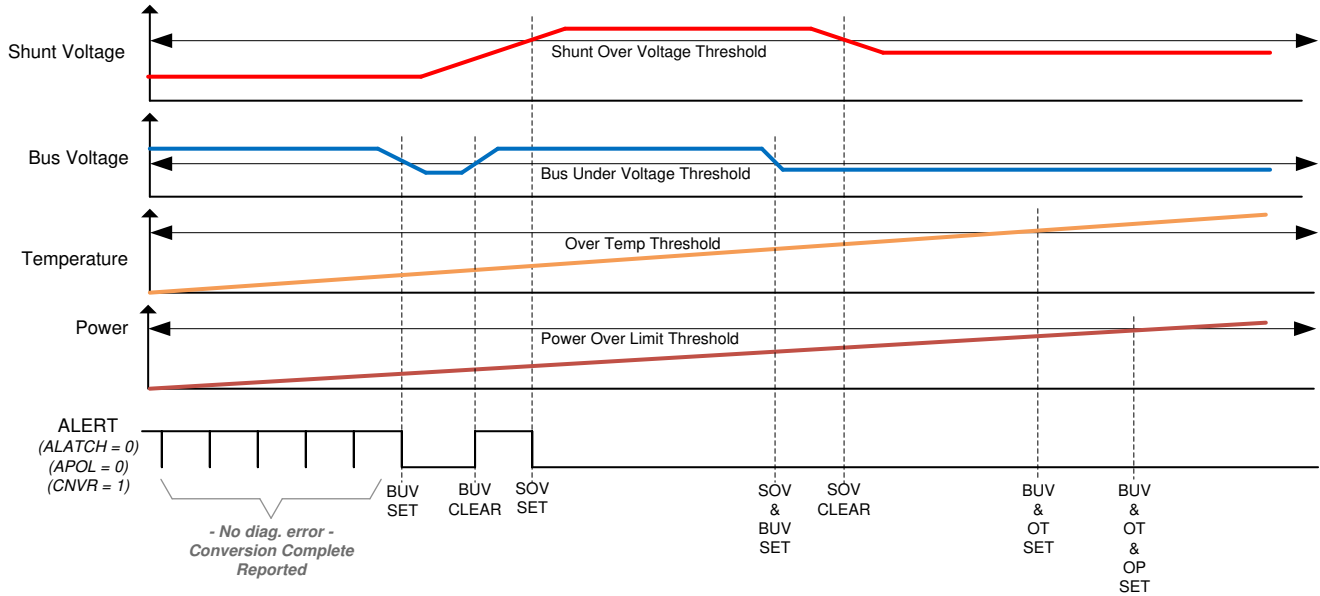


Figure 7-6. Multi-Alert Configuration

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

In addition to the two conversion modes (continuous and triggered), the device also has a shutdown mode (selected by the MODE bits in ADC\_CONFIG register) that reduces the quiescent current to less than 5  $\mu\text{A}$  and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. The registers of the device can be written to and read from while the device is in shutdown mode. The device remains in shutdown mode until another triggered conversion command or continuous conversion command is received.

The device can be triggered to perform conversions while in shutdown mode. When a conversion is triggered, the ADC will start conversion; once conversion completes the device will return to the shutdown state.

Note that the shutdown current is specified with an inactive communications bus. Active clock and data activity will increase the current consumption as a function of the bus frequency as shown in [Shutdown  \$I\_Q\$  vs. Clock Frequency](#).

### 7.4.2 Power-On Reset

Power-on reset (POR) is asserted when  $V_S$  drops below 1.26V (typical) at which all of the registers are reset to their default values. A manual device reset can be initiated by setting the RST bit in the CONFIG register. The default power-up register values are shown in the reset column for each register description. Links to the register descriptions are shown in [Section 7.6](#).

## 7.5 Programming

### 7.5.1 Serial Interface

The primary communication between the INA239-Q1 and the external MCU is through the SPI bus, which provides full-duplex communications in a main-secondary configuration. The external MCU is always the primary or main SPI device, sending command requests on the MOSI pin, and receiving device responses on the MISO pin. The INA239-Q1 is always an SPI secondary device, receiving command requests and sending responses (status, measured values) to the external MCU over the MISO pin.

- SPI is a 4-pin interface with pins as:
  - CS - SPI Chip Select (input)
  - SCLK - SPI Clock (input)
  - MOSI - SPI Secondary In / Main Out data (input)

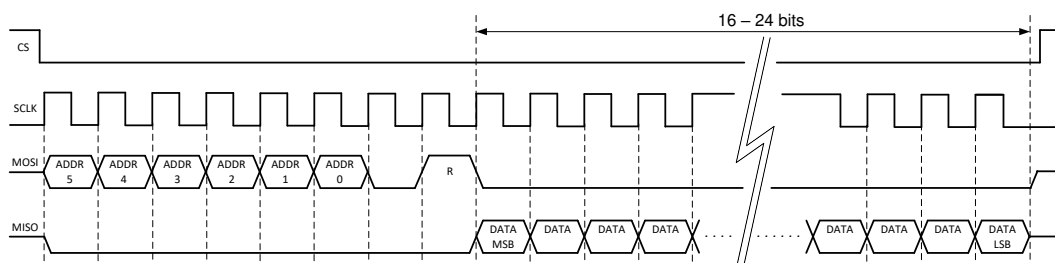
- MISO - SPI Secondary Out / Main In data (tri-state output)
- The SPI frame size is variable in length depending on the INA239-Q1 register accessed through the SPI interface as following:
  - Main to Secondary (MOSI): 6 bits for register Address; 1 bit low; 1 R/W bit (read / not write); variable length of low bits depending on the INA239-Q1 register length.
  - Secondary to Main (MISO): 8 bits low; variable length of bits depending on the INA239-Q1 register length.
- SPI bit-speed up to 10 Mbit/s
- Both Main commands and INA239-Q1 data are shifted MSB first, LSB last
- The data on the MOSI line is sampled on the falling edge of SCLK
- The data on the MISO line is shifted out on the rising edge of SCLK

The SPI communication starts with the CS falling edge, and ends with CS rising edge. The CS high level keeps secondary SPI interface in an idle state, and MISO output is tri-stated.

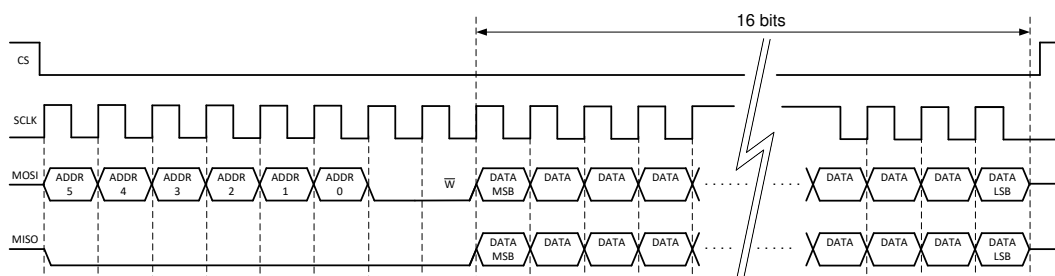
Since the MISO output is push-pull it is ideal to have the INA239-Q1 supply at the same voltage as the primary device I/O supply. If different supply voltages are used, level translation is recommended.

### 7.5.1.1 SPI Frame

SPI communication to the INA239-Q1 device is performed through register address access. Communication to every register starts with a 6-bit register address followed by a "0" and a R/W bit. Setting the R/W bit to "1" indicates that the current SPI frame will read from a device register while setting the R/W bit to "0" indicates the current SPI frame will write data to a device register.



**Figure 7-7. SPI Read Frame**



**Figure 7-8. SPI Write Frame**

Note that while the read frame can be variable in length due to the different length registers in the INA239-Q1 device, the write frame is fixed in length as all writable registers are 16 bits wide. During an SPI write frame, while new data is shifted into the INA239-Q1 register, the old data from the same register is shifted out on the MISO line.

The first 8-bits of each SPI frame are presented in [Table 7-2](#), which shows access to a certain register address on the MOSI line as well as read/write functionality. On an SPI read operation, the INA239-Q1 returns the data read in the same SPI frame.

**Table 7-2. First 8-MSB Bits of SPI Frame**

COMMAND	b7	b6	b5	b4	b3	b2	b1	b0
READ	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	0	1
WRITE								0

## 7.6 Register Maps

### 7.6.1 INA239-Q1 Registers

Table 7-3 lists the INA239-Q1 registers. All register locations not listed in Table 7-3 should be considered as reserved locations and the register contents should not be modified.

**Table 7-3. INA239-Q1 Registers**

Address	Acronym	Register Name	Register Size (bits)	Section
0h	CONFIG	Configuration	16	<a href="#">Go</a>
1h	ADC_CONFIG	ADC Configuration	16	<a href="#">Go</a>
2h	SHUNT_CAL	Shunt Calibration	16	<a href="#">Go</a>
4h	VSHUNT	Shunt Voltage Measurement	16	<a href="#">Go</a>
5h	VBUS	Bus Voltage Measurement	16	<a href="#">Go</a>
6h	DIETEMP	Temperature Measurement	16	<a href="#">Go</a>
7h	CURRENT	Current Result	16	<a href="#">Go</a>
8h	POWER	Power Result	24	<a href="#">Go</a>
Bh	DIAG_ALERT	Diagnostic Flags and Alert	16	<a href="#">Go</a>
Ch	SOVL	Shunt Overvoltage Threshold	16	<a href="#">Go</a>
Dh	SUVL	Shunt Undervoltage Threshold	16	<a href="#">Go</a>
Eh	BOVL	Bus Overvoltage Threshold	16	<a href="#">Go</a>
Fh	BUVL	Bus Undervoltage Threshold	16	<a href="#">Go</a>
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	<a href="#">Go</a>
11h	PWR_LIMIT	Power Over-Limit Threshold	16	<a href="#">Go</a>
3Eh	MANUFACTURER_ID	Manufacturer ID	16	<a href="#">Go</a>
3Fh	DEVICE_ID	Device ID	16	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. Table 7-4 shows the codes that are used for access types in this section.

**Table 7-4. INA239-Q1 Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

#### 7.6.1.1 Configuration (CONFIG) Register (Address = 0h) [reset = 0h]

The CONFIG register is shown in Table 7-5.

Return to the [Summary Table](#).

**Table 7-5. CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RESERVED	R/W	0h	Reserved. Always reads 0.
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2 ms. 0h = 0 s 1h = 2 ms FFh = 510 ms
5	RESERVED	R/W	0h	Reserved. Always reads 0.
4	ADCRANGE	R/W	0h	Shunt full scale range selection across IN+ and IN-. 0h = $\pm 163.84$ mV 1h = $\pm 40.96$ mV
3-0	RESERVED	R	0h	Reserved. Always reads 0.

### 7.6.1.2 ADC Configuration (ADC\_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC\_CONFIG register is shown in [Table 7-6](#).

Return to the [Summary Table](#).

**Table 7-6. ADC\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	<p>The user can set the MODE bits for continuous or triggered mode on bus voltage, shunt voltage or temperature measurement.</p> <p>0h = Shutdown</p> <p>1h = Triggered bus voltage, single shot</p> <p>2h = Triggered shunt voltage, single shot</p> <p>3h = Triggered shunt voltage and bus voltage, single shot</p> <p>4h = Triggered temperature, single shot</p> <p>5h = Triggered temperature and bus voltage, single shot</p> <p>6h = Triggered temperature and shunt voltage, single shot</p> <p>7h = Triggered bus voltage, shunt voltage and temperature, single shot</p> <p>8h = Shutdown</p> <p>9h = Continuous bus voltage only</p> <p>Ah = Continuous shunt voltage only</p> <p>Bh = Continuous shunt and bus voltage</p> <p>Ch = Continuous temperature only</p> <p>Dh = Continuous bus voltage and temperature</p> <p>Eh = Continuous temperature and shunt voltage</p> <p>Fh = Continuous bus voltage, shunt voltage and temperature</p>
11-9	VBUSCT	R/W	5h	<p>Sets the conversion time of the bus voltage measurement:</p> <p>0h = 50 <math>\mu</math>s</p> <p>1h = 84 <math>\mu</math>s</p> <p>2h = 150 <math>\mu</math>s</p> <p>3h = 280 <math>\mu</math>s</p> <p>4h = 540 <math>\mu</math>s</p> <p>5h = 1052 <math>\mu</math>s</p> <p>6h = 2074 <math>\mu</math>s</p> <p>7h = 4120 <math>\mu</math>s</p>
8-6	VSHCT	R/W	5h	<p>Sets the conversion time of the shunt voltage measurement:</p> <p>0h = 50 <math>\mu</math>s</p> <p>1h = 84 <math>\mu</math>s</p> <p>2h = 150 <math>\mu</math>s</p> <p>3h = 280 <math>\mu</math>s</p> <p>4h = 540 <math>\mu</math>s</p> <p>5h = 1052 <math>\mu</math>s</p> <p>6h = 2074 <math>\mu</math>s</p> <p>7h = 4120 <math>\mu</math>s</p>
5-3	VTCT	R/W	5h	<p>Sets the conversion time of the temperature measurement:</p> <p>0h = 50 <math>\mu</math>s</p> <p>1h = 84 <math>\mu</math>s</p> <p>2h = 150 <math>\mu</math>s</p> <p>3h = 280 <math>\mu</math>s</p> <p>4h = 540 <math>\mu</math>s</p> <p>5h = 1052 <math>\mu</math>s</p> <p>6h = 2074 <math>\mu</math>s</p> <p>7h = 4120 <math>\mu</math>s</p>

**Table 7-6. ADC\_CONFIG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

**7.6.1.3 Shunt Calibration (SHUNT\_CAL) Register (Address = 2h) [reset = 1000h]**

The SHUNT\_CAL register is shown in [Table 7-7](#).

Return to the [Summary Table](#).

**Table 7-7. SHUNT\_CAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved. Always reads 0.
14-0	SHUNT_CAL	R/W	1000h	The register provides the device with a conversion constant value that represents shunt resistance used to calculate current value in Amperes. This also sets the resolution for the <a href="#">CURRENT</a> register. Value calculation under <a href="#">Section 8.1.2</a> .

**7.6.1.4 Shunt Voltage Measurement (VSHUNT) Register (Address = 4h) [reset = 0h]**

The VSHUNT register is shown in [Table 7-8](#).

Return to the [Summary Table](#).

**Table 7-8. VSHUNT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0h	Differential voltage measured across the shunt output. Two's complement value. Conversion factor: 5 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 0 1.25 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 1

**7.6.1.5 Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]**

The VBUS register is shown in [Table 7-9](#).

Return to the [Summary Table](#).

**Table 7-9. VBUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 3.125 mV/LSB



### 7.6.1.6 Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in [Table 7-10](#).

Return to the [Summary Table](#).

**Table 7-10. DIETEMP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 125 m°C/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

### 7.6.1.7 Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in [Table 7-11](#).

Return to the [Summary Table](#).

**Table 7-11. CURRENT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Value description under <a href="#">Section 8.1.2</a> .

### 7.6.1.8 Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in [Table 7-12](#).

Return to the [Summary Table](#).

**Table 7-12. POWER Register Field Descriptions**

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in watts. Unsigned representation. Positive value. Value description under <a href="#">Section 8.1.2</a> .

### 7.6.1.9 Diagnostic Flags and Alert (DIAG\_ALERT) Register (Address = Bh) [reset = 0001h]

The DIAG\_ALERT register is shown in [Table 7-13](#).

Return to the [Summary Table](#).

**Table 7-13. DIAG\_ALERT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle state when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALERT Register has been read. 0h = Transparent 1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disable conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin

**Table 7-13. DIAG\_ALERT Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
13	SLOWALERT	R/W	0h	When enabled, ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (Active-low, open-drain) 1h = Inverted (active-high, open-drain )
11-10	RESERVED	R	0h	Reserved. Always read 0.
9	MATHOF	R	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. 0h = Normal 1h = Overflow Must be manually cleared by triggering another conversion.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R/W	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Over Temp Event When ALATCH =1 this bit is cleared by reading this register.
6	SHNTOL	R/W	0h	This bit is set to 1 if the shunt voltage measurement exceeds the threshold limit in the shunt over-limit register. 0h = Normal 1h = Over Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
5	SHNTUL	R/W	0h	This bit is set to 1 if the shunt voltage measurement falls below the threshold limit in the shunt under-limit register. 0h = Normal 1h = Under Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
4	BUSOL	R/W	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
3	BUSUL	R/W	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALATCH =1 this bit is cleared by reading this register.
2	POL	R/W	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
1	CNVRF	R/W	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion is complete When ALATCH =1 this bit is cleared by reading this register or starting a new triggered conversion.

**Table 7-13. DIAG\_ALRT Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
0	MEMSTAT	R/W	1h	This bit is set to 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

### 7.6.1.10 Shunt Overvoltage Threshold (SOVL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered in this register, then a shunt voltage measurement of 0 V will trip this alarm. When using negative values for the shunt under and overvoltage thresholds be aware that the over voltage threshold must be set to the larger (that is, less negative) of the two values. The SOVL register is shown in [Table 7-14](#).

Return to the [Summary Table](#).

**Table 7-14. SOVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	SOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Shunt Overvoltage (overcurrent protection). Two's complement value. Conversion Factor: 5 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 0 1.25 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 1.

### 7.6.1.11 Shunt Undervoltage Threshold (SUVL) Register (Address = Dh) [reset = 8000h]

The SUVL register is shown in [Table 7-15](#).

Return to the [Summary Table](#).

**Table 7-15. SUVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	SUVL	R/W	8000h	Sets the threshold for comparison of the value to detect Shunt Undervoltage (undercurrent protection). Two's complement value. Conversion Factor: 5 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 0 1.25 $\mu$ V/LSB when <a href="#">ADCRANGE</a> = 1.

### 7.6.1.12 Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in [Table 7-16](#).

Return to the [Summary Table](#).

**Table 7-16. BOVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

### 7.6.1.13 Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in [Table 7-17](#).

Return to the [Summary Table](#).

**Table 7-17. BUVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

#### 7.6.1.14 Temperature Over-Limit Threshold (TEMP\_LIMIT) Register (Address = 10h) [reset = 7FFh]

The TEMP\_LIMIT register is shown in [Table 7-18](#).

Return to the [Summary Table](#).

**Table 7-18. TEMP\_LIMIT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	TOL	R/W	7FFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. The value entered in this field compares directly against the value from the DIETEMP register to determine if an over temperature condition exists. Conversion factor: 125 m°C/LSB.
3-0	Reserved	R	0	Reserved, always reads 0

#### 7.6.1.15 Power Over-Limit Threshold (PWR\_LIMIT) Register (Address = 11h) [reset = FFFFh]

The PWR\_LIMIT register is shown in [Table 7-19](#).

Return to the [Summary Table](#).

**Table 7-19. PWR\_LIMIT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over power condition exists. Conversion factor: 256 × Power LSB.

#### 7.6.1.16 Manufacturer ID (MANUFACTURER\_ID) Register (Address = 3Eh) [reset = 5449h]

The MANUFACTURER\_ID register is shown in [Table 7-20](#).

Return to the [Summary Table](#).

**Table 7-20. MANUFACTURER\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5449h	Reads back TI in ASCII.

#### 7.6.1.17 Device ID (DEVICE\_ID) Register (Address = 3Fh) [reset = 2391h]

The DEVICE\_ID register is shown in [Table 7-21](#).

Return to the [Summary Table](#).

**Table 7-21. DEVICE\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DIEID	R	239h	Stores the device identification bits.
3-0	REV_ID	R	1h	Device revision identification.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Device Measurement Range and Resolution

The INA239-Q1 device supports two input ranges for the shunt voltage measurement. The supported full scale differential input across the IN+ and IN– pins can be either  $\pm 163.84$  mV or  $\pm 40.96$  mV depending on the ADCRANGE bit in CONFIG register. The range for the bus voltage measurement is from 0 V to 85 V. The internal die temperature sensor range extends from  $-256$  °C to  $+256$  °C but is limited by the package to  $-40$  °C to  $125$  °C.

Table 8-1 provides a description of full scale voltage on shunt, bus, and temperature measurements, along with their associated step size.

**Table 8-1. ADC Full Scale Values**

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	$\pm 163.84$ mV (ADCRANGE = 0)	5 $\mu$ V/LSB
	$\pm 40.96$ mV (ADCRANGE = 1)	1.25 $\mu$ V/LSB
Bus voltage	0 V to 85 V	3.125 mV/LSB
Temperature	$-40$ °C to $+125$ °C	125 m°C/LSB

The device shunt voltage measurements, bus voltage, and temperature measurements can be read through the VSHUNT, VBUS, and DIETEMP registers, respectively. The digital output in VSHUNT and VBUS registers is 16-bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in VSHUNT can be positive or negative. The VBUS data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by its respective resolution size. The digital output in the DIETEMP register is 12-bit and can be directly converted to °C by multiplying by the above resolution size. This output value can also be positive or negative.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts as described in [Section 8.1.2](#).

#### 8.1.2 Current and Power Calculations

For the INA239-Q1 device to report current values in Ampere units, a constant conversion value must be written in the SHUNT\_CAL register that is dependent on the maximum measured current and the shunt resistance used in the application. The SHUNT\_CAL register is calculated based on [Equation 1](#). The term CURRENT\_LSB is the LSB step size for the CURRENT register where the current in Amperes is stored. The value of CURRENT\_LSB is based on the maximum expected current as shown in [Equation 2](#), and it directly defines the resolution of the CURRENT register. While the smallest CURRENT\_LSB value yields highest resolution, it is common to select a higher round-number (no higher than 8x) value for the CURRENT\_LSB in order to simplify the conversion of the CURRENT.

The  $R_{SHUNT}$  term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use [Equation 1](#) for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT\_CAL must be multiplied by 4.

$$SHUNT\_CAL = 819.2 \times 10^6 \times CURRENT\_LSB \times R_{SHUNT} \quad (1)$$

where

- 819.2 x 10<sup>6</sup> is an internal fixed value used to ensure scaling is maintained properly.
- the value of SHUNT\_CAL must be multiplied by 4 for ADCRANGE = 1.

$$Current\_LSB = \frac{\text{Maximum Expected Current}}{2^{15}} \quad (2)$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT\_CAL register. If the value loaded into the SHUNT\_CAL register is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT\_CAL register with the calculated value, the measured current in Amperes can be read from the CURRENT register. The final value is scaled by CURRENT\_LSB and calculated in [Equation 3](#):

$$Current [A] = CURRENT\_LSB \times CURRENT \quad (3)$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as a 24-bit value and converted to Watts by using [Equation 4](#):

$$Power [W] = 0.2 \times CURRENT\_LSB \times POWER \quad (4)$$

where

- POWER is the value read from the POWER register.
- CURRENT\_LSB is the lsb size of the current calculation as defined by [Equation 2](#).

For a design example using these equations refer to [Section 8.2.2](#).

### 8.1.3 ADC Output Data Rate and Noise Performance

The INA239-Q1 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The INA239-Q1 effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

[Table 8-2](#) summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 50 μs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which assures that full noise distribution is taken into consideration.

**Table 8-2. INA239-Q1 Noise Performance**

ADC CONVERSION TIME PERIOD [μs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	1	0.05	12.5	9.9
84		0.084	12.7	10.5
150		0.15	13.4	11.4
280		0.28	13.7	12.2
540		0.54	14.1	12.4
1052		1.052	14.1	12.7
2074		2.074	15.7	13.1
4120		4.12	15.7	13.4
50	4	0.2	12.7	10.6
84		0.336	13.7	11.4
150		0.6	14.1	12.2
280		1.12	14.7	12.7
540		2.16	15.7	13.4
1052		4.208	15.7	14.1
2074		8.296	15.7	14.7
4120		16.48	15.7	14.7
50	16	0.8	13.7	11.5
84		1.344	15.7	12.7
150		2.4	15.7	13.4
280		4.48	15.7	13.7
540		8.64	15.7	14.1
1052		16.832	15.7	14.7
2074		33.184	15.7	15.7
4120		65.92	16.0	15.7
50	64	3.2	15.7	12.5
84		5.376	15.7	13.7
150		9.6	15.7	14.7
280		17.92	15.7	14.7
540		34.56	16.0	14.7
1052		67.328	16.0	15.7
2074		132.736	16.0	15.7
4120		263.68	16.0	15.7
50	128	6.4	15.7	13.1
84		10.752	15.7	14.1
150		19.2	15.7	14.7
280		35.84	16.0	15.7
540		69.12	16.0	15.7
1052		134.656	16.0	15.7
2074		265.472	16.0	15.7
4120		527.36	16.0	16.0



**Table 8-2. INA239-Q1 Noise Performance (continued)**

ADC CONVERSION TIME PERIOD [μs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±163.84-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±40.96-mV) (ADCRANGE = 1)
50	256	12.8	15.7	13.7
84		21.504	15.7	14.7
150		38.4	15.7	15.7
280		71.68	16.0	15.7
540		138.24	16.0	15.7
1052		269.312	16.0	16.0
2074		530.944	16.0	16.0
4120		1054.72	16.0	16.0
50	512	25.6	15.7	14.1
84		43	16.0	15.7
150		76.8	16.0	15.7
280		143.36	16.0	15.7
540		276.48	16.0	15.7
1052		538.624	16.0	16.0
2074		1061.888	16.0	16.0
4120		2109.44	16.0	16.0
50	1024	51.2	15.7	14.7
84		86.016	15.7	15.7
150		153.6	16.0	16.0
280		286.72	16.0	16.0
540		552.96	16.0	16.0
1052		1077.248	16.0	16.0
2074		2123.776	16.0	16.0
4120		4218.88	16.0	16.0

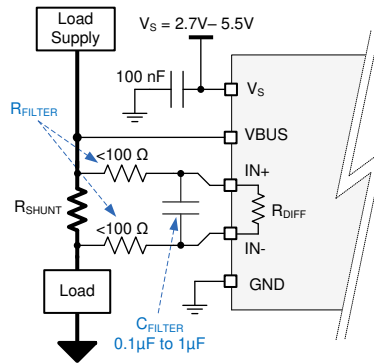
### 8.1.4 Input Filtering Considerations

As previously discussed, INA239-Q1 offers several options for noise filtering by allowing the user to select the conversion times and number of averages independently in the ADC\_CONFIG register. The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in monitoring of the power-supply bus.

The internal ADC has good inherent noise rejection; however, the transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating filtering at the input of the device. Filtering high frequency signals enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. For best results, filter using the lowest possible series resistance (typically 100 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 μF and 1 μF. [Figure 8-1](#) shows the device with a filter added at the input.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate ±40 V differential across the IN+ and IN– pins. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long as the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 40-V differential or 85-V common-mode absolute maximum rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called *transzorb*s) combined with sufficient energy storage capacitance. See the [Transient Robustness for Current Shunt Monitors](#) reference design which describes a high-side current shunt monitor used to measure the voltage developed across a current-sensing resistor when current passes through it.

In applications that do not have large energy storage, electrolytic capacitors on one or both sides of the shunt, an input overstress condition may result from an excessive  $dV/dt$  of the voltage applied to the input. A hard physical short is the most likely cause of this event. This problem occurs because an excessive  $dV/dt$  can activate the ESD protection in the device in systems where large currents are available. Testing demonstrates that the addition of 10- $\Omega$  resistors in series with each input of the device sufficiently protects the inputs against this  $dV/dt$  failure up to the 40-V maximum differential voltage rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

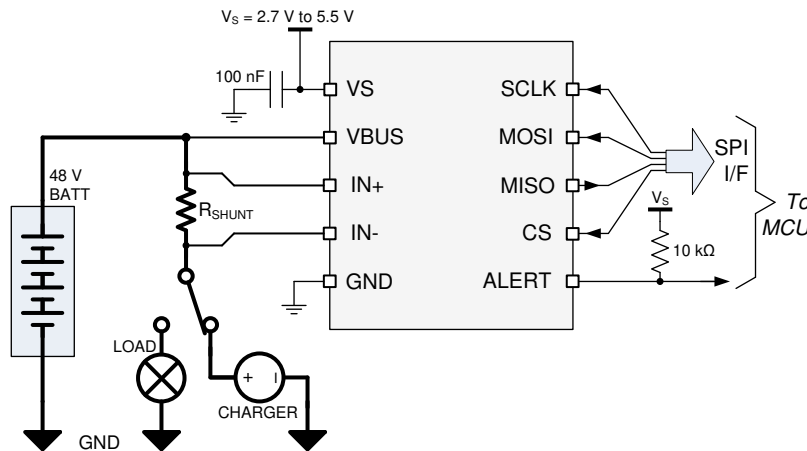


**Figure 8-1. Input Filtering**

Do not use values greater than 100 ohms for  $R_{FILTER}$ . Doing so will degrade gain error and increase non-linearity.

## 8.2 Typical Application

The low offset voltage and low input bias current of the INA239-Q1 allow accurate monitoring of a wide range of currents. To accurately monitor currents with high resolution, select the value of the shunt resistor so that the resulting sense voltage is close to the maximum allowable differential input voltage range (either  $\pm 163.84$  mV or  $\pm 40.96$  mV, depending on register settings). The circuit for monitoring currents in a high-side configuration is shown in [Figure 8-2](#).



**Figure 8-2. INA239-Q1 High-Side Sensing Application Diagram**

### 8.2.1 Design Requirements

The INA239-Q1 measures the voltage developed across a current-sensing resistor ( $R_{SHUNT}$ ) when current passes through it. The device also measures the bus supply voltage and calculates power when calibrated. It also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

The design requirements for the circuit shown in [Figure 8-2](#) are listed in [Table 8-3](#).

**Table 8-3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage ( $V_S$ )	5 V
Bus supply rail ( $V_{CM}$ )	48 V
Bus supply rail over voltage fault threshold	52 V
Average Current	6 A
Overcurrent fault threshold ( $I_{MAX}$ )	10 A
ADC Range Selection ( $V_{SENSE\_MAX}$ )	$\pm 163.84$ mV
Temperature	25 °C

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Select the Shunt Resistor

Using values from [Table 8-3](#), the maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed ( $I_{MAX}$ ) and the maximum allowable sense voltage ( $V_{SENSE\_MAX}$ ) for the chosen ADC range. When operating at the maximum current, the differential input voltage must not exceed the maximum full scale range of the device,  $V_{SENSE\_MAX}$ . Using [Equation 5](#) for the given design parameters, the maximum value for  $R_{SHUNT}$  is calculated to be 16.38 m $\Omega$ . The closest standard resistor value that is smaller than the maximum calculated value is 16.2 m $\Omega$ . Also keep in mind that  $R_{SHUNT}$  must be able to handle the power dissipated across it in the maximum load condition.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \quad (5)$$

### 8.2.2.2 Configure the Device

The first step to program the INA239-Q1 is to properly set the device and ADC configuration registers. On initial power up the CONFIG and ADC\_CONFIG registers are set to the reset values as shown in [Table 7-5](#) and [Table 7-6](#). In this default power on state the device is set to measured on the  $\pm 163.84$  mV range with the ADC continuously converting the shunt voltage, bus voltage, and temperature. If the default power up conditions do not meet the design requirements, these registers will need to be set properly after each  $V_S$  power cycle event.

### 8.2.2.3 Program the Shunt Calibration Register

The shunt calibration register needs to be correctly programmed at each  $V_S$  power up in order for the device to properly report any result based on current. The first step in properly setting this register is to calculate the LSB value for the current by using [Equation 2](#). Applying this equation with the maximum expected current of 10 A results in an LSB size of 305.1758  $\mu$ A. Applying [Equation 1](#) to the Current\_LSB and selected value for the shunt resistor results in a shunt calibration register setting of 4050d (FD2h). Failure to set the value of the shunt calibration register will result in a zero value for any result based on current.

### 8.2.2.4 Set Desired Fault Thresholds

Fault thresholds are set by programming the desired trip threshold into the corresponding fault register. The list of supported fault registers is shown in [Table 7-1](#).

An over current threshold is set by programming the shunt over voltage limit register (SOVL). The voltage that needs to be programmed into this register is calculated by multiplying the over current threshold by the shunt resistor. In this example the over current threshold is 10 A and the value of the current sense resistor is 16.2 m $\Omega$ , which give a shunt voltage limit of 162 mV. Once the shunt voltage limit is known, the value for the shunt over voltage limit register is calculated by dividing the shunt voltage limit by the shunt voltage LSB size.

In this example, the calculated value of the shunt over voltage limit register is 162 mV / 5  $\mu$ V = 32400d (7E90h).

An over voltage fault threshold on the bus voltage is set by programming the bus over voltage limit register (BOVL). In this example the desired over voltage threshold is 52 V. The value that needs to be programmed into this register is calculated by dividing the target threshold voltage by the bus voltage fault limit LSB value of 3.125 mV. For this example, the target value for the BOVL register is 52 V / 3.125 mV = 16640d (4100h).

When setting the power over-limit value, the LSB size used to calculate the value needed in the limit registers will be 256 times greater than the power LSB. This is because the power register is a 24 bits in length while the power fault limit register is 16 bits.

Values stored in the alert limit registers are set to the default values after  $V_S$  power cycle events and need to be reprogrammed each time power is applied.

### 8.2.2.5 Calculate Returned Values

Parametric values are calculated by multiplying the returned value by the LSB value. [Table 8-4](#) below shows the returned values for this application example assuming the design requirements shown in [Table 8-3](#).

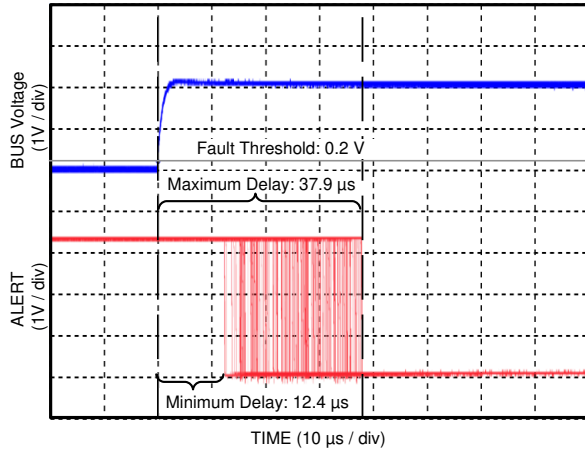
**Table 8-4. Calculating Returned Values**

PARAMETER	Returned Value	LSB Value	Calculated Value
Shunt voltage (V)	19440d	5 $\mu$ V/LSB	0.0972 V
Current (A)	19660d	10 A/ $2^{15}$ = 305.176 $\mu$ A/LSB	5.9997 A
Bus voltage (V)	15360d	3.125 mV/LSB	48 V
Power (W)	4718604d	Current LSB x 0.2 = 61.035156 $\mu$ W/LSB	288 W
Temperature ( $^{\circ}$ C)	200d	125 $m^{\circ}$ C/LSB	25 $^{\circ}$ C

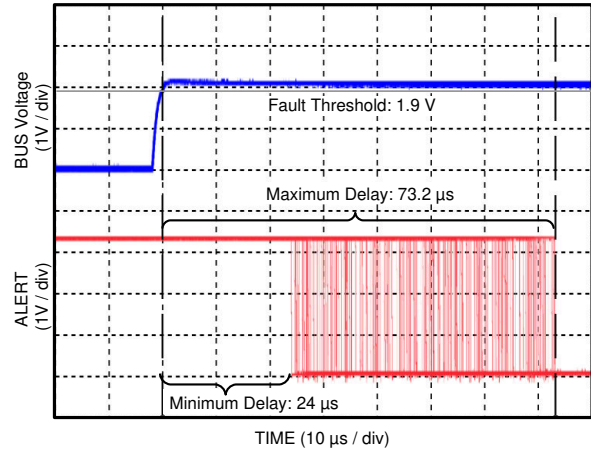
Shunt Voltage, Current, Bus Voltage (positive only), and Temperature return values in two's complement format. In two's complement format a negative value in binary is represented by having a 1 in the most significant bit of the returned value. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value should then be converted to decimal with the negative sign applied. For example, assume a shunt voltage reading returns 1011 0100 0001 0000. This is a negative value due to the MSB having a value of one. Inverting the bits and adding one results in 0100 1011 1111 0000 (19440d) which from the shunt voltage example in [Table 8-4](#) correlates to a voltage of 97.2 mV. Since the returned value was negative the measured shunt voltage value is -97.2 mV.

### 8.2.3 Application Curves

[Figure 8-3](#) and [Figure 8-4](#) show the ALERT pin response to a bus overvoltage fault with a conversion time of 50  $\mu$ s, averaging set to 1, and the SLOWALERT bit set to 0 for bus only conversions. For these scope shots, persistence was enabled on the ALERT channel to show the variation in the alert response for many sequential fault events. If the magnitude of the fault is sufficient the ALERT response can be as fast as one quarter of the ADC conversion time as shown in [Figure 8-3](#). For fault conditions that are just exceeding the limit threshold, the response time for the ALERT pin can vary from approximately 0.5 to 1.5 conversion cycles as shown in [Figure 8-4](#). Variation in the alert response exists because the external fault event is not synchronized to the internal ADC conversion start. Also the ADC is constantly sampling to get a result, so the response time for fault events starting from zero will slower than fault events starting from values near the set fault threshold. Since the timing of the alert can be difficult to predict, applications where the alert timing is critical should assume a alert response equal to 1.5 times the ADC conversion time for bus voltage or shunt voltage only conversions.



**Figure 8-3. Alert Response Time (Sampled Values Significantly Above Threshold)**



**Figure 8-4. Alert Response Time (Sampled Values Slightly Above Threshold)**

## 9 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power-supply voltage,  $V_S$ . For example, the voltage applied to the  $V_S$  power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as 85 V. Note that the device can also withstand the full 0 V to 85 V range at the input terminals, regardless of whether the device has power applied or not. Avoid applications where the GND pin is disconnected while device is actively powered.

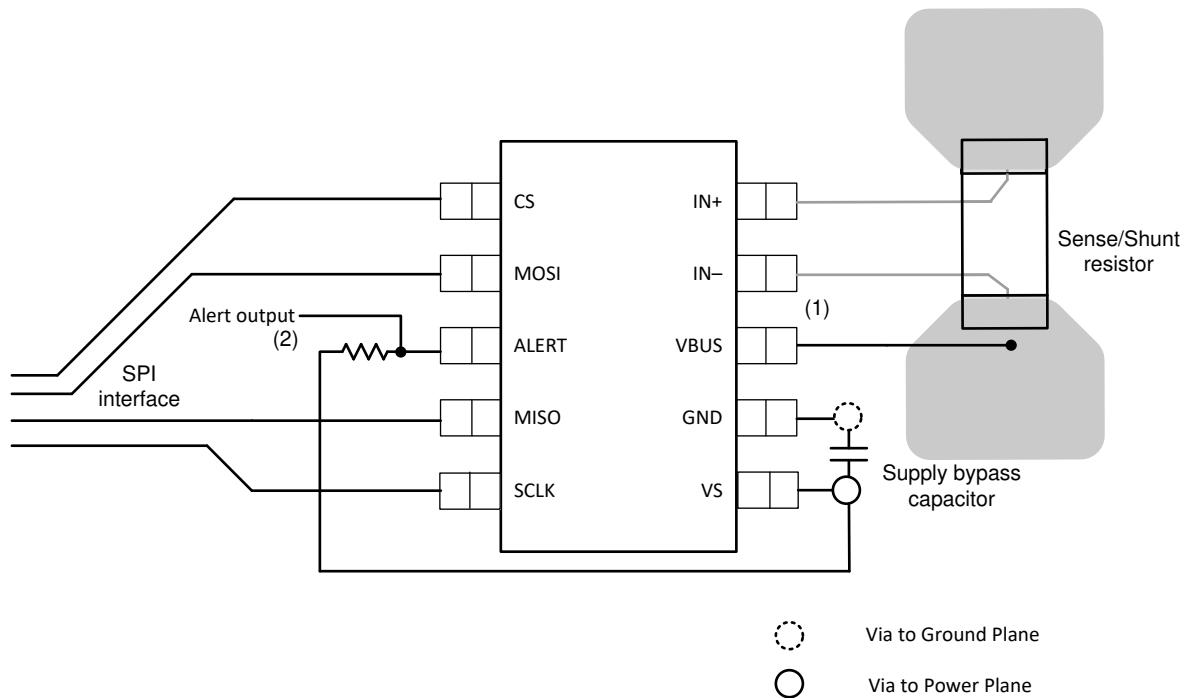
Place the required power-supply bypass capacitors as close as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1  $\mu\text{F}$ . Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

## 10 Layout

### 10.1 Layout Guidelines

Connect the input pins (IN+ and IN-) to the sensing resistor using a Kelvin connection or a 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is sensed between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

### 10.2 Layout Example



- (1) Connect the VBUS pin to the voltage powering the load for load power calculations..
- (2) Can be left floating if unused.

**Figure 10-1. INA239-Q1 Layout Example**

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA239AQDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	239Q	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA239-Q1 :**



- Catalog : [INA239](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA239AQDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA239AQDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated