FEATURES

- Wide Common-Mode Range: –16V to +80V
- CMRR: 78dB
- Accuracy:
  ±10mV Offset (max)
  ±7.5% Gain Error (max)
  100μV/°C Offset Drift (max)
- Bandwidth: Up to 130kHz
- Transfer Function: 20V/V
- Quiescent Current: 1600μA (max)
- Power Supply: +2.7V to +18V
- Provision for Filtering

APPLICATIONS

- Down-Hole Drilling
- High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extreme (–55°C/210°C) Temperature Range (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

(1) Custom temperature ranges available

DESCRIPTION

The INA271 is a current-shunt monitor with voltage output and can sense drops across current shunts at common-mode voltages from –16V to +80V, independent of the supply voltage. The INA271 pinouts readily enable filtering.

The INA271 is available with a 20V/V output voltage scale. The 130kHz bandwidth simplifies use in current-control loops.

The INA271 operates from a single +2.7V to +18V supply, drawing a maximum of 1600μA of supply current. This device is specified over the extended operating temperature range of –55°C to +210°C.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### BARE DIE INFORMATION

<table>
<thead>
<tr>
<th>DIE THICKNESS</th>
<th>BACKSIDE FINISH</th>
<th>BACKSIDE POTENTIAL</th>
<th>BOND PAD METALLIZATION COMPOSITION</th>
<th>BOND PAD THICKNESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>11 mils.</td>
<td>Silicon with backgrind</td>
<td>GND</td>
<td>Al-Cu (0.5%)</td>
<td>598 nm</td>
</tr>
</tbody>
</table>

![Diagram of bond pad coordinates](image)

Table 1. Bond Pad Coordinates in Microns

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PAD NUMBER</th>
<th>X min</th>
<th>Y min</th>
<th>X max</th>
<th>Y max</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN-</td>
<td>1</td>
<td>64.35</td>
<td>1012.41</td>
<td>139.41</td>
<td>1087.47</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>61.83</td>
<td>648.81</td>
<td>136.89</td>
<td>723.87</td>
</tr>
<tr>
<td>PRE OUT</td>
<td>3</td>
<td>61.83</td>
<td>520.29</td>
<td>136.89</td>
<td>595.35</td>
</tr>
<tr>
<td>BUF IN</td>
<td>4</td>
<td>70.92</td>
<td>152.37</td>
<td>145.98</td>
<td>227.43</td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>616.32</td>
<td>152.37</td>
<td>691.38</td>
<td>227.43</td>
</tr>
<tr>
<td>V+</td>
<td>6</td>
<td>621.99</td>
<td>386.55</td>
<td>697.05</td>
<td>461.61</td>
</tr>
<tr>
<td>NC</td>
<td>7</td>
<td>622.44</td>
<td>648.81</td>
<td>697.5</td>
<td>723.87</td>
</tr>
<tr>
<td>IN+</td>
<td>8</td>
<td>622.89</td>
<td>1012.41</td>
<td>697.95</td>
<td>1087.47</td>
</tr>
</tbody>
</table>
PIN CONFIGURATION

AHD OR HKJ PACKAGE
(TOP VIEW)

IN-
1
GND
2
PRE OUT
3
BUF IN
4
IN271
8
IN+
7
NC
6
V+
5
OUT
NC denotes no internal connection

HKQ PACKAGE
(TOP VIEW)

IN+
8
NC
7
GND
6
V+
5
PRE OUT
4
BUF IN
HKQ as formed or HKJ mounted dead bug

ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE(2)</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>–55°C to 175°C</td>
<td>AHD</td>
<td>INA271AHD</td>
<td>INA271AHD</td>
</tr>
<tr>
<td>–55°C to 210°C</td>
<td>KGD (bare die)</td>
<td>INA271SKGD1</td>
<td>INA271SKGD2</td>
</tr>
<tr>
<td></td>
<td>HKJ</td>
<td>INA271SHKJ</td>
<td>INA271SHKJ</td>
</tr>
<tr>
<td></td>
<td>HKQ</td>
<td>INA271SHKQ</td>
<td>INA271SHKQ</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_S)</td>
<td>+18</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Analog Inputs, V_IN+ , V_IN-</td>
<td>–18 to +18</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Differential, (V_IN+) – (V_IN-)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode</td>
<td>–16 to +80</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Analog Output</td>
<td>GND – 0.3 to (V+) + 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Current Into Any Pin</td>
<td>5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>–55 to +210</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>–65 to +210</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+210</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>ESD Ratings:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>3000</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Charged-Device Model</td>
<td>750</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>θ JC, Junction-to-case thermal resistance</td>
<td>to ceramic side of case</td>
<td>5.7</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>to top of case lid (metal side of case)</td>
<td>13.7</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

Copyright © 2010–2013, Texas Instruments Incorporated
ELECTRICAL CHARACTERISTICS

At $T_A = +25°C$, $V_S = +5V$, $V_{CM} = +12V$, $V_{SENSE} = 100mV$, and PRE OUT connected to BUF IN, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>$T_A = −55°C$ to $125°C$</th>
<th>$T_A = −55°C$ to $175°C$</th>
<th>$T_A = 210°C$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>INPUT</td>
<td>Full-Scale Input Voltage $V_{SENSE}$</td>
<td>$V_{SENSE} = (V_{IN}+) + (V_{IN}−)$&lt;br&gt;$V_{SENSE} = (V_{IN}−)/Gain$&lt;br&gt;$V_{SENSE} = (V_{IN}−)/Gain$</td>
<td>0.15</td>
<td>0.2</td>
</tr>
</tbody>
</table>
| Common-Mode Input Range $V_{CM}$ | $V_{IN}− = −16V$ to $+80V$
$V_{IN}− = +12V$ to $+80V$ | 80 | 120 | 8 | 70 | 8 | 81 | 9 | 8 | dB |
| Common-Mode Rejection Ratio $CMRR$ | $V_{SENSE} = +1.27V$ to $+18V$
$V_{CM} = +18V$ | 5 | 100 | 130 | 320 | μV/V |
| Offset Voltage, $V_{OS}$<br>vs Temperature $\Delta V_{OS}/dT$<br>vs Power-Supply PSD | ±0.6 | ±3 | ±5 | ±10 | mV |
| Input Bias Current, $I_B$<br>V$_{IN+}$ Pin | ±8 | ±16 | ±16 | ±25 | μA |
| PRE OUT Output Impedance <br>Buffer Input Bias Current | 96 | 96 | kΩ |
| Buffer Input Bias Current | −50 | −50 | nA |
| Temperature Coefficient | ±0.03 | nA/°C |
| OUTPUT ($V_{SENSE} ≥ 20mV$)<br>Gain: INA271 Total Gain | 20 | 20 | V/V |
| Output Buffer Gain $G_{BUF}$ | 2 | 2 | V/V |
| Total Gain Error $V_{SENSE} = 20mV$ to $100mV$ | ±0.2 | ±2 | ±1 | ±7.5 | % |
| vs Temperature | 50 | 300 | ppm/°C |
| Total Output Error<br>Nonlinearity Error $V_{SENSE} = 20mV$ to $100mV$ | ±1 | ±3 | ±4.6 | ±11.5 | % |
| Output Impedance $R_O$ | ±0.002 | ±0.002 | % |
| Maximum Capacitive Load | No Sustained Oscillation | 10 | 10 | nF |
| VOLTAGE OUTPUT<br>Swing to V+ Power-Supply Rail | $R_L = 10kΩ$ to GND | $(V+) − 0.05$ | $(V+) − 0.2$ | $(V+) − 0.13$ | $(V+) − 0.2$ | V |
| Swing to GND<br>$V_{GND} + 0.003$ | $V_{GND} + 0.05$ | $V_{GND} + 0.22$ | $V_{GND} + 0.42$ | V |
| FREQUENCY RESPONSE | $C_{LOAD} = 5pF$ | 130 | 130 | kHz |
| Bandwidth $BW$ | 40 | 40 | degrees |
| Phase Margin | 1 | 1 | V/μs |
| Slew Rate $SR$ | $C_{LOAD} < 10nF$ | 2 | 2 | μs |
| Settling Time (1%) $t_S$ | $V_{SENSE} = 10mV$ to $100mV_{PP}$<br>$C_{LOAD} = 5pF$ | 2 | μs |

(1) RTI means Referred-to-Input.
(2) Initial resistor variation is ±30% with an additional −2200ppm/°C temperature coefficient.
(3) For output behavior when $V_{SENSE} < 20mV$, see the Application Information section Accuracy Variations as A Result of $V_{SENSE}$ and Common-Mode Voltage.
(4) Total output error includes effects of gain error and $V_{OS}$.
(5) See typical characteristic curve Output Swing vs Output Current and Application Information section Accuracy Variations as A Result of $V_{SENSE}$ and Common-Mode Voltage.
(6) Ensured by design; not production tested.
ELECTRICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ$C, $V_S = +5\,\text{V}$, $V_{CM} = +12\,\text{V}$, $V_{SENSE} = 100\,\text{mV}$, and PRE OUT connected to BUF IN, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>$T_A = -55^\circ$C to 125$^\circ$C</th>
<th>$T_A = -55^\circ$C to 175$^\circ$C</th>
<th>$T_A = 210^\circ$C</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOISE &lt; RTI(^{(7)})</td>
<td>$e_n$</td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>Voltage Noise Density</td>
<td>40</td>
<td>40</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>Operating Range</td>
<td>$V_S$</td>
<td>2.7</td>
<td>18</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_Q$</td>
<td>740</td>
<td>1200</td>
<td>1160</td>
</tr>
<tr>
<td>VSENSE = 0mV</td>
<td>350</td>
<td>950</td>
<td>895</td>
<td>1600</td>
</tr>
<tr>
<td>TEMPERATURE RANGE</td>
<td>Specified Temperature Range</td>
<td>$-55$</td>
<td>125</td>
<td>$-55$</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$-55$</td>
<td>125</td>
<td>$-55$</td>
<td>210</td>
</tr>
</tbody>
</table>

(7) RTI means Referred-to-Input.

(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105$^\circ$C junction temperature (does not include package interconnect life).

Figure 1. INA271SKGD1/INA271SKGD2/INA271SHKJ/INA271SHKQ Operating Life Derating Chart
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $V_S = +12V$, $V_{CM} = 12V$, and $V_{SENSE} = 100mV$, unless otherwise noted.

GAIN vs FREQUENCY

Figure 2.

GAIN vs FREQUENCY

Figure 3.

GAIN PLOT

Figure 4.

COMMON-MODE AND POWER-SUPPLY REJECTION vs FREQUENCY

Figure 5.

TOTAL OUTPUT ERROR vs $V_{SENSE}$

Figure 6.

OUTPUT ERROR vs COMMON-MODE VOLTAGE

Figure 7.
TYPICAL CHARACTERISTICS (continued)

At \( T_A = +25^\circ C \), \( V_S = +12V \), \( V_{CM} = 12V \), and \( V_{SENSE} = 100mV \), unless otherwise noted.

**Figure 8.**

**Positive Output Voltage Swing vs Output Current**

Output stage is designed to source current. Current sinking capability is approximately 400mA.

**Figure 9.**

**Quiescent Current vs Output Voltage**

**Figure 10.**

**Quiescent Current vs Common-Mode Voltage**

**Figure 11.**

**Output Short-Circuit Current vs Supply Voltage**

**Figure 12.**

**Preout Output Resistance Production Distribution**

**Figure 13.**

**Buffer Gain vs Frequency**

**Figure 14.**
TYPICAL CHARACTERISTICS (continued)

At \( T_A = +25^\circ\text{C} \), \( V_S = +12\text{V} \), \( V_{CM} = 12\text{V} \), and \( V_{SENSE} = 100\text{mV} \), unless otherwise noted.

**SMALL-SIGNAL STEP RESPONSE**
**10mV TO 20mV INPUT**

![Small-Signal Step Response](image1)

**LARGE-SIGNAL STEP RESPONSE**
**10mV TO 100mV INPUT**

![Large-Signal Step Response](image2)
APPLICATIONS INFORMATION

BASIC CONNECTION

Figure 16 shows the basic connection of the INA271. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Minimum bypass capacitors of 0.01μF and 0.1μF in value should be placed close to the supply pins. Although not mandatory, an additional 10mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

Figure 16. INA271 Basic Connections

POWER SUPPLY

The input circuitry of the INA271 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5V, whereas the load power-supply voltage is up to +80V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

SELECTING RS

The value chosen for the shunt resistor, RS, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of RS provide better accuracy at lower currents by minimizing the effects of offset, while low values of RS minimize voltage loss in the supply line. For most applications, best performance is attained with an RS value that provides a full-scale shunt voltage range of 50mV to 100mV. Maximum input voltage for accurate measurements is (VS – 0.2)/Gain.
TRANSIENT PROTECTION

The \(-16\)V to \(+80\)V common-mode range of the INA271 is ideal for withstanding automotive fault conditions ranging from 12V battery reversal up to \(+80\)V transients, since no additional protective components are needed up to those levels. In the event that the INA271 is exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) will be necessary.

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA271 to be exposed to transients greater than 80V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA271 is not suited to using external resistors in series with the inputs since the internal gain resistors can vary up to \(\pm 30\)%, but is tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA271 inputs with two equal resistors on each input).

OUTPUT VOLTAGE RANGE

The output of the INA271 is accurate within the output voltage swing range set by the power-supply pin, \(V_+\).

The INA271 readily enables the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96k\(\Omega\) output impedance at \(\text{PRE OUT}\) on pin 3, as shown in Figure 17a.

The INA271 readily lends itself to second-order Sallen-Key configurations, as shown in Figure 17b. When designing these configurations consider that the PRE OUT 96k\(\Omega\) output impedance exhibits an initial variation of \(\pm 30\%\) with the addition of a –2200ppm/°C temperature coefficient.

![Figure 17](image-url)

**Figure 17.** The INA271 can be easily connected for first- or second-order filtering. Remember to use the appropriate buffer gain of 2 when designing Sallen-Key configurations.
ACCURACY VARIATIONS AS A RESULT OF V\text{SENSE} AND COMMON-MODE VOLTAGE

The accuracy of the INA271 current shunt monitor is a function of two main variables: V\text{SENSE} (V_{\text{IN}+} − V_{\text{IN}−}) and common-mode voltage, V\text{CM}, relative to the supply voltage, V\text{S}. V\text{CM} is expressed as (V_{\text{IN}+} + V_{\text{IN}−})/2; however, in practice, V\text{CM} is seen as the voltage at V_{\text{IN}+} because the voltage drop across V\text{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- **Normal Case 1:** V\text{SENSE} ≥ 20mV, V\text{CM} ≥ V\text{S}
- **Normal Case 2:** V\text{SENSE} ≥ 20mV, V\text{CM} < V\text{S}
- **Low V\text{SENSE} Case 1:** V\text{SENSE} < 20mV, –16V ≤ V\text{CM} < 0
- **Low V\text{SENSE} Case 2:** V\text{SENSE} < 20mV, 0V ≤ V\text{CM} ≤ V\text{S}
- **Low V\text{SENSE} Case 3:** V\text{SENSE} < 20mV, V\text{S} < V\text{CM} ≤ 80V

### Normal Case 1: V\text{SENSE} ≥ 20mV, V\text{CM} ≥ V\text{S}

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

\[
G = \frac{V_{\text{OUT1}} - V_{\text{OUT2}}}{100\text{mV} - 20\text{mV}}
\]

where:

\[
V_{\text{OUT1}} = \text{Output Voltage with } V_{\text{SENSE}} = 100\text{mV}
\]

\[
V_{\text{OUT2}} = \text{Output Voltage with } V_{\text{SENSE}} = 20\text{mV}
\]

Then the offset voltage is measured at V\text{SENSE} = 100mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

\[
V_{\text{OS RTI (Referred-To-Input)}} = \left(\frac{V_{\text{OUT1}}}{G}\right) - 100\text{mV}
\]

In the **Typical Characteristics**, the Output Error vs Common-Mode Voltage curve (Figure 7) shows the highest accuracy for this region of operation. In this plot, V\text{S} = 12V; for V\text{CM} ≥ 12V, the output error is at its minimum. This case is also used to create the V\text{SENSE} ≥ 20mV output specifications in the Electrical Characteristics table.

### Normal Case 2: V\text{SENSE} ≥ 20mV, V\text{CM} < V\text{S}

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode voltage, V\text{CM}, relative to the supply voltage, V\text{S}. V\text{CM} is expressed as (V_{\text{IN}+} + V_{\text{IN}−})/2; however, in practice, V\text{CM} is seen as the voltage at V_{\text{IN}+} because the voltage drop across V\text{SENSE} is usually small.

### Low V\text{SENSE} Case 1:

V\text{SENSE} < 20mV, –16V ≤ V\text{CM} < 0; and

### Low V\text{SENSE} Case 2:

V\text{SENSE} < 20mV, 0V ≤ V\text{CM} ≤ V\text{S}

### Low V\text{SENSE} Case 3:

V\text{SENSE} < 20mV, V\text{S} < V\text{CM} ≤ 80V

Although the INA271 is not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V\text{S} is still applied to the INA271, it is important to know what the behavior of the device will be in these regions.

As V\text{SENSE} approaches 0mV, in these V\text{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{\text{OUT}} = 60mV for V_{\text{SENSE}} = 0mV. As V_{\text{SENSE}} approaches 20mV, V_{\text{OUT}} returns to the expected output value with accuracy as specified in the Electrical Characteristics. Figure 18 shows this effect (Gain = 20).

![Figure 18. Example for Low V_{\text{SENSE}} Cases 1 and 3 (Gain = 20)](image-url)
**Low V\textsubscript{SENSE} Case 2: V\textsubscript{SENSE} < 20mV, 0V ≤ V\textsubscript{CM} ≤ V\textsubscript{S}**

This region of operation is the least accurate for the INA271. To achieve the wide input common-mode voltage range, this device uses two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V\textsubscript{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V\textsubscript{SENSE} approaches 0V. Within this region, as V\textsubscript{SENSE} approaches 20mV, device operation is closer to that described by Normal Case 2. Figure 19 illustrates this behavior for the INA271. The V\textsubscript{OUT} maximum peak for this case is determined by maintaining a constant V\textsubscript{S}, setting V\textsubscript{SENSE} = 0mV, and sweeping V\textsubscript{CM} from 0V to V\textsubscript{S}. The exact V\textsubscript{CM} at which V\textsubscript{OUT} peaks during this case varies from part to part. The maximum peak voltage for the INA271 is 0.4V.

![Graph](image-url)

**Figure 19. Example for Low V\textsubscript{SENSE} Case 2 (Gain = 20)**

**SHUTDOWN**

The INA271 does not provide a shutdown pin; however, because it consumes a quiescent current less than 1mA, it can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with 0.1\mu F bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate should have a supply voltage of 3V or greater because the INA271 requires a minimum supply greater than 2.7V. In addition to eliminating quiescent current, this gate also turns off the 10\mu A bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is illustrated in Figure 20.

**RFI/EMI**

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI/EMI sensitivity. PCB layout should locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA271 versus the INA193–INA198 may provide different EMI performance.
Figure 20. INA271 Example Shutdown Circuit

(1) 74HC04 is not tested or characterized at 210°C.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA271SHKJ</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>HKJ</td>
<td>8</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>INA271SHKJ</td>
<td>Samples</td>
</tr>
<tr>
<td>INA271SHKQ</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>HKQ</td>
<td>8</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>AU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>INA271SHKQ</td>
<td>Samples</td>
</tr>
<tr>
<td>INA271SKGD1</td>
<td>ACTIVE</td>
<td>XCEPT</td>
<td>KGD</td>
<td>0</td>
<td>252</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>INA271SKGD1</td>
<td>Samples</td>
</tr>
<tr>
<td>INA271SKGD2</td>
<td>ACTIVE</td>
<td>XCEPT</td>
<td>KGD</td>
<td>0</td>
<td>10</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>INA271SKGD2</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.**

(4) **There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.**

(5) **Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.**

(6) **Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.**

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA271-HT:

• Catalog: INA271

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product
### TUBE

- **L** - Tube length
- **T** - Tube height
- **W** - Tube width
- **B** - Alignment groove width

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA271SHKJ</td>
<td>HKJ</td>
<td>CFP</td>
<td>8</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
<tr>
<td>INA271SHKQ</td>
<td>HKQ</td>
<td>CFP</td>
<td>8</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
</tbody>
</table>
HKJ (R-CDFP-F8) CERAMIC DUAL FLATPACK

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
MECHANICAL DATA

HKQ (R-CDFP-G8) CERAMIC GULL WING

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

4212003/B 05/12
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated