INA27x Voltage Output, Unidirectional Measurement Current-Shunt Monitor

1 Features
- Wide Common-Mode Range: –16 V to +80 V
- CMRR: 120 dB
- Accuracy:
  ±0.5-mV Offset (typ)
  ±0.2% Gain Error (typ)
  2.5 μV/°C Offset Drift (typ)
  50 ppm/°C Gain Drift (max)
- Bandwidth: Up to 130 kHz
- Two Gain Options Available:
  14 V/V (INA270)
  20 V/V (INA271)
- Quiescent Current: 700 μA (typ)
- Power Supply: +2.7 V to +18 V
- Provision for Filtering

2 Applications
- Power Management
- Automotive
- Telecom Equipment
- Notebook Computers
- Battery Chargers
- Cell Phones
- Welding Equipment

3 Description
The INA270 and INA271 family of voltage-output, current-sense amplifiers can sense drops across shunt resistors at common-mode voltages from –16 V to +80 V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two gain options: 14 V/V and 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single +2.7-V to +18-V supply, drawing 700 μA (typical) of supply current. The devices are specified over the extended operating temperature range of –40°C to +125°C and are offered in an SOIC-8 package.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA27x</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................ 1
3 Description ............................................................ 1
4 Revision History ...................................................... 2
5 Device Comparison Table ........................................... 3
6 Pin Configuration and Functions ................................. 3
7 Specifications ........................................................... 3
  7.1 Absolute Maximum Ratings ..................................... 3
  7.2 ESD Ratings ........................................................ 4
  7.3 Recommended Operating Conditions ....................... 4
  7.4 Thermal Information ............................................. 4
  7.5 Electrical Characteristics ...................................... 5
  7.6 Typical Characteristics ......................................... 7
8 Detailed Description .................................................. 10
  8.1 Overview .......................................................... 10
  8.2 Functional Block Diagram ...................................... 10
  8.3 Feature Description .............................................. 11
9 Application and Implementation ................................ 15
  9.1 Application Information ......................................... 15
  9.2 Typical Application ............................................. 15
10 Power Supply Recommendations ............................. 17
  10.1 Shutdown ........................................................ 17
11 Layout .................................................................... 18
  11.1 Layout Guidelines .............................................. 18
  11.2 Layout Example ................................................ 18
12 Device and Documentation Support ........................... 19
  12.1 Documentation Support ....................................... 19
  12.2 Related Links .................................................. 19
  12.3 Community Resources ...................................... 19
  12.4 Trademarks ...................................................... 19
  12.5 Electrostatic Discharge Caution ............................. 19
  12.6 Glossary ........................................................ 19
13 Mechanical, Packaging, and Orderable Information ....... 19

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2014) to Revision E Page

- Added title to page 1 figure .................................................. 1
- Updated ESD Ratings table to current standards ..................... 4
- Changed Figure 16: changed op amp input to BUF IN pin from negative to positive ................ 12
- Added Community Resources section .................................. 19

Changes from Revision C (May 2010) to Revision D Page

- Changed format to meet latest data sheet standards .................. 1
- Added Handling Rating, Pin Descriptions, and Recommended Operating Conditions tables and Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections ........................................ 1
- Changed Accuracy and Quiescent Current Features bullets: changed from max specifications and values to typical ........... 1
- Changed wording in Two Gain Options Available Features bullet ............................................... 1
- Changed Description section for clarification .......................... 1
- Added Device Information table .............................................. 1
- Deleted Ordering Information table .......................................... 1
- Changed Input, Full-Scale Input Voltage parameter conditions in Electrical Characteristics table ......................... 5
- Changed title of First- or Second-Order Filtering section ......................... 12
- Changed title of Power Supply Recommendations section .................................................. 17

Changes from Revision B (July 2008) to Revision C Page

- Corrected Figure 17 y-axis .................................................. 14
- Corrected Figure 18 y-axis .................................................. 14
5 Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>GAIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA270</td>
<td>14 V/V</td>
</tr>
<tr>
<td>INA271</td>
<td>20 V/V</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

![D Package SOIC-8 Top View](IN27x.png)

NOTE (1): NC denotes no internal connection.

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF IN</td>
<td>4</td>
<td>Analog input: Connect to output of filter from PRE OUT</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Analog: Ground</td>
</tr>
<tr>
<td>IN–</td>
<td>1</td>
<td>Analog input: Connect to load side of shunt resistor</td>
</tr>
<tr>
<td>IN+</td>
<td>8</td>
<td>Analog input: Connect to supply side of shunt resistor</td>
</tr>
<tr>
<td>NC</td>
<td>7</td>
<td>— Connect to ground</td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>Analog output: Output voltage</td>
</tr>
<tr>
<td>PRE OUT</td>
<td>3</td>
<td>Analog output: Connect to input of filter to BUF IN</td>
</tr>
<tr>
<td>V+</td>
<td>6</td>
<td>Analog input: Power supply, +2.7 V to +18 V</td>
</tr>
</tbody>
</table>

7 Specifications

7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V_S)</td>
<td></td>
<td>+18</td>
<td>V</td>
</tr>
<tr>
<td>Analog inputs, ( V_{IN+}, V_{IN-} ):</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential, ( (V_{IN+}) - (V_{IN-}) )</td>
<td>-18</td>
<td>+18</td>
<td>V</td>
</tr>
<tr>
<td>Common-mode</td>
<td>-16</td>
<td>+80</td>
<td>V</td>
</tr>
<tr>
<td>Analog output: OUT and PRE OUT pins</td>
<td>GND – 0.3</td>
<td>((V+) + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Input current into any pin</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-55</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td></td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, ( T_{stg} )</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±3000</td>
<td>V</td>
</tr>
<tr>
<td>±750</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>–16</td>
<td>12</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>2.7</td>
<td>5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

THERMAL METRIC\(^{(1)}\)

<table>
<thead>
<tr>
<th>INA27x</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>D (SOIC) 8 PINS</td>
<td></td>
</tr>
<tr>
<td>R(_{JA})</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>R(_{JC(top)})</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>R(_{JB})</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>ψ(_{JT})</td>
<td>Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>ψ(_{JB})</td>
<td>Junction-to-board characterization parameter</td>
</tr>
<tr>
<td>R(_{JC(bot)})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

At \( T_A = +25^\circ C, V_S = +5 \, V, V_{CM} = +12 \, V, V_{SENSE} = 100 \, mV, \) and PRE OUT connected to BUF IN, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{SENSE} )</td>
<td>Full-scale input voltage</td>
<td>( V_{SENSE} = (V_{IN+}) - (V_{IN-}) )</td>
<td>0.15 ((V_S - 0.2) / \text{Gain})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Common-mode input range</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>–16</td>
<td>+80</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>( V_{IN+} = –16 , V ) to (+80 , V), ( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>80</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>CMRR over temperature</td>
<td>( V_{IN+} = +12 , V ) to (+80 , V), ( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>100</td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Offset voltage, RTI(1)</td>
<td>±0.5</td>
<td>2.5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( V_{OS} ) over temperature</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>±3</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( dV_{OS}/dT )</td>
<td>( V_{OS} ) vs temperature</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>2.5</td>
<td>20</td>
<td>( \mu V/^\circ C)</td>
</tr>
<tr>
<td>PSR</td>
<td>( V_{OS} ) vs power-supply</td>
<td>( V_S = +2.7 , V ) to (+18 , V), ( V_{CM} = +18 , V), ( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>5</td>
<td>100</td>
<td>( \mu V/V)</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input bias current, ( V_{IN+} ) pin</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>±8</td>
<td>±16</td>
<td>nA</td>
</tr>
<tr>
<td>PRE OUT output impedance(2)</td>
<td></td>
<td></td>
<td>96</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Buffer input bias current</td>
<td></td>
<td></td>
<td>–50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Buffer input bias current temperature coefficient</td>
<td></td>
<td></td>
<td>±0.03</td>
<td>nA/°C</td>
<td></td>
</tr>
<tr>
<td>OUTPUT (( V_{SENSE} \geq 20 , mV))(3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( G )</td>
<td>Gain</td>
<td>INA270 total gain</td>
<td>14</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INA271 total gain</td>
<td>20</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>( G_{BUF} )</td>
<td>Output buffer gain</td>
<td></td>
<td>2</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>Total gain error</td>
<td>( V_{SENSE} = 20 , mV ) to (100 , mV)</td>
<td>±0.2%</td>
<td>±1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total gain error over temperature</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>±2%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total gain error vs temperature</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>50</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total output error(4)</td>
<td></td>
<td></td>
<td>±0.75%</td>
<td>±2.2%</td>
<td></td>
</tr>
<tr>
<td>Total output error</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>±1.0%</td>
<td>±3.0%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nonlinearity error</td>
<td>( V_{SENSE} = 20 , mV ) to (100 , mV)</td>
<td>±0.002%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_O )</td>
<td>Output impedance, pin 5</td>
<td></td>
<td>1.5</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Maximum capacitive load</td>
<td>No sustained oscillation</td>
<td></td>
<td>10</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>VOLTAGE OUTPUT(5) (( R_L = 10 , k\Omega ) to GND)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Swing to V+ power-supply rail</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>((V+) – 0.05 )</td>
<td>((V+) – 0.2 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Swing to GND(6)</td>
<td>( T_A = –40^\circ C ) to (+125^\circ C)</td>
<td>( V_{GND} + 0.003 )</td>
<td>( V_{GND} + 0.05 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FREQUENCY RESPONSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( B_W )</td>
<td>Bandwidth</td>
<td>( C_{LOAD} = 5 , pF)</td>
<td>130</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Phase margin</td>
<td>( C_{LOAD} &lt; 10 , nF)</td>
<td>40</td>
<td>Degrees</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( S_R )</td>
<td>Slew rate</td>
<td></td>
<td>1</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>( t_S )</td>
<td>Settling time (1%)</td>
<td>( V_{SENSE} = 10 , mV ) to (100 , mV_{PP}), ( C_{LOAD} = 5 , pF)</td>
<td>2</td>
<td>μs</td>
<td></td>
</tr>
</tbody>
</table>

(1) RTI means Referred-to-Input.
(2) Initial resistor variation is ±30% with an additional –2200-ppm/°C temperature coefficient.
(3) For output behavior when \( V_{SENSE} < 20 \, mV\), see the Accuracy Variations as a Result of \( V_{SENSE} \) and Common-Mode Voltage section.
(4) Total output error includes effects of gain error and \( V_{OS}\).
(5) See typical characteristic curve Output Swing vs Output Current and the Accuracy Variations as a Result of \( V_{SENSE} \) and Common-Mode Voltage section.
(6) Ensured by design; not production tested.
Electrical Characteristics (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +5$ V, $V_{CM} = +12$ V, $V_{SENSE} = 100$ mV, and PRE OUT connected to BUF IN, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$e_n$</td>
<td>Voltage noise density</td>
<td>40</td>
<td></td>
<td></td>
<td>nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Operating range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = –40^\circ\text{C}$ to $+125^\circ\text{C}$</td>
<td>+2.7</td>
<td></td>
<td>+18</td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = 2$ V</td>
<td>700</td>
<td>900</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_Q$ over temperature</td>
<td>$V_{SENSE} = 0$ mV, $T_A = –40^\circ\text{C}$ to $+125^\circ\text{C}$</td>
<td>350</td>
<td>950</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Specified temperature range</td>
<td>−40</td>
<td></td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Operating temperature range</td>
<td>−55</td>
<td></td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal resistance, SO-8</td>
<td></td>
<td></td>
<td>150</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
7.6 Typical Characteristics
At $T_A = +25^\circ C$, $V_S = +12\, V$, $V_{CM} = 12\, V$, and $V_{SENSE} = 100\, mV$, unless otherwise noted.
Typical Characteristics (continued)

At $T_A = +25^\circ C$, $V_S = +12 \text{ V}$, $V_{CM} = 12 \text{ V}$, and $V_{SENSE} = 100 \text{ mV}$, unless otherwise noted.

Figure 7. Positive Output Voltage Swing vs Output Current

Figure 8. Quiescent Current vs Output Voltage

Figure 9. Quiescent Current vs Common-Mode Voltage

Figure 10. Output Short-Circuit Current vs Supply Voltage

Figure 11. PRE OUT Output Resistance Production Distribution

Figure 12. Buffer Gain vs Frequency
Typical Characteristics (continued)

At \( T_A = +25^\circ C \), \( V_S = +12 \) V, \( V_{CM} = 12 \) V, and \( V_{SENSE} = 100 \) mV, unless otherwise noted.

Figure 13. Small-Signal Step Response
(10-mV to 20-mV Input)

Figure 14. Large-Signal Step Response
(10-mV to 100-mV Input)
8 Detailed Description

8.1 Overview

The INA270 and INA271 family of current-shunt monitors with voltage output can sense drops across current shunts at common-mode voltages from –16 V to +80 V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two output voltage scales: 14 V/V and 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single +2.7-V to +18-V supply, drawing a maximum of 900 μA of supply current. The devices are specified over the extended operating temperature range of –40°C to +125°C and are offered in an SOIC-8 package.

8.2 Functional Block Diagram
8.3 Feature Description

8.3.1 Basic Connection

Figure 15 shows the basic connection of the INA270 and INA271. Connect the input pins (IN+ and IN−) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Place minimum bypass capacitors of 0.01 \( \mu \text{F} \) and 0.1 \( \mu \text{F} \) in value close to the supply pins. Although not mandatory, an additional 10-mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

![ INA270 Basic Connections Diagram ]

Figure 15. INA270 Basic Connections

8.3.2 Selecting \( R_S \)

The value chosen for the shunt resistor, \( R_S \), depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of \( R_S \) provide better accuracy at lower currents by minimizing the effects of offset, while low values of \( R_S \) minimize voltage loss in the supply line. For most applications, best performance is attained with an \( R_S \) value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is \( (V_S - 0.2) / \text{Gain} \).

8.3.3 Transient Protection

The –16-V to +80-V common-mode range of the INA270 and INA271 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to +80-V transients because no additional protective components are needed up to those levels. In the event that the INA270 and INA271 are exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzors) are necessary.
Feature Description (continued)

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows the INA270 and INA271 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA270 and INA271 are not suited to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30%, but are tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA270 and INA271 inputs with two equal resistors on each input).

8.4 Device Functional Modes

8.4.1 First- or Second-Order Filtering

The output of the INA270 and INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA270 and INA271 readily enable the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96-kΩ output impedance at PRE OUT on pin 3, as shown in Figure 16a.

The INA270 and INA271 readily lend themselves to second-order Sallen-Key configurations, as shown in Figure 16b. When designing these configurations consider that the PRE OUT 96-kΩ output impedance exhibits an initial variation of ±30% with the addition of a −2200-ppm/°C temperature coefficient.

Figure 16. The INA270–INA271 can be Easily Connected for First- or Second-Order Filtering

NOTE: Remember to use the appropriate buffer gain (INA270 = 1.4, INA271 = 2) when designing Sallen-Key configurations.
Device Functional Modes (continued)

8.4.2 Accuracy Variations as a Result of $V_{\text{SENSE}}$ and Common-Mode Voltage

The accuracy of the INA270 and INA271 current shunt monitors is a function of two main variables: $V_{\text{SENSE}}$ ($V_{\text{IN+}} - V_{\text{IN-}}$) and common-mode voltage ($V_{\text{CM}}$) relative to the supply voltage, $V_S$. $V_{\text{CM}}$ is expressed as $(V_{\text{IN+}} + V_{\text{IN-}}) / 2$; however, in practice, $V_{\text{CM}}$ is used as the voltage at $V_{\text{IN+}}$ because the voltage drop across $V_{\text{SENSE}}$ is usually small.

This section addresses the accuracy of these specific operating regions:

- **Normal Case 1**: $V_{\text{SENSE}} \geq 20 \text{ mV}, V_{\text{CM}} \geq V_S$
- **Normal Case 2**: $V_{\text{SENSE}} \geq 20 \text{ mV}, V_{\text{CM}} < V_S$
- **Low $V_{\text{SENSE}}$ Case 1**: $V_{\text{SENSE}} < 20 \text{ mV}, -16 \text{ V} \leq V_{\text{CM}} < 0$
- **Low $V_{\text{SENSE}}$ Case 2**: $V_{\text{SENSE}} < 20 \text{ mV}, 0 \text{ V} \leq V_{\text{CM}} \leq V_S$
- **Low $V_{\text{SENSE}}$ Case 3**: $V_{\text{SENSE}} < 20 \text{ mV}, V_S < V_{\text{CM}} \leq 80 \text{ V}$

### 8.4.2.1 Normal Case 1: $V_{\text{SENSE}} \geq 20 \text{ mV}, V_{\text{CM}} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{\text{OUT1}} - V_{\text{OUT2}}}{100\text{mV} - 20\text{mV}}$$

where
- $V_{\text{OUT1}}$ = Output voltage with $V_{\text{SENSE}} = 100 \text{ mV}$ and
- $V_{\text{OUT2}}$ = Output voltage with $V_{\text{SENSE}} = 20 \text{ mV}$.

Then the offset voltage is measured at $V_{\text{SENSE}} = 100 \text{ mV}$ and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{\text{OS}}\text{RTI (Referred-To-Input)} = \left(\frac{V_{\text{OUT1}}}{G}\right) - 100\text{mV}$$

In the *Typical Characteristics*, the *Output Error vs Common-Mode Voltage* curve (Figure 6) shows the highest accuracy for the this region of operation. In this plot, $V_S = 12 \text{ V}$; for $V_{\text{CM}} \geq 12 \text{ V}$, the output error is at its minimum. This case is also used to create the $V_{\text{SENSE}} \geq 20 \text{ mV}$ output specifications in the *Electrical Characteristics* table.

### 8.4.2.2 Normal Case 2: $V_{\text{SENSE}} \geq 20 \text{ mV}, V_{\text{CM}} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the device functions, as illustrated in the *Output Error vs Common-Mode Voltage* curve (Figure 6). As noted, for this graph $V_S = 12 \text{ V}$; for $V_{\text{CM}} < 12 \text{ V}$, the output error increases when $V_{\text{CM}}$ becomes less than 12 V, with a typical maximum error of 0.005% at the most negative $V_{\text{CM}} = -16 \text{ V}$.

### 8.4.2.3 Low $V_{\text{SENSE}}$ Case 1: $V_{\text{SENSE}} < 20 \text{ mV}, -16 \text{ V} \leq V_{\text{CM}} < 0$; and Low $V_{\text{SENSE}}$ Case 3: $V_{\text{SENSE}} < 20 \text{ mV}, V_S < V_{\text{CM}} \leq 80 \text{ V}$

Although the INA270 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while $V_S$ is still applied to the INA270 or INA271, knowing what the behavior of the devices is in these regions is important.
Device Functional Modes (continued)

When $V_{\text{SENSE}}$ approaches 0 mV, in these $V_{\text{CM}}$ regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of $V_{\text{OUT}} = 60$ mV for $V_{\text{SENSE}} = 0$ mV. When $V_{\text{SENSE}}$ approaches 20 mV, $V_{\text{OUT}}$ returns to the expected output value with accuracy as specified in the Electrical Characteristics. Figure 17 shows this effect using the INA271 (gain = 20).

![Figure 17. Example For Low $V_{\text{SENSE}}$ Cases 1 and 3 (INA271, Gain = 20)](image)

8.4.2.4 Low $V_{\text{SENSE}}$ Case 2: $V_{\text{SENSE}} < 20$ mV, $0 \leq V_{\text{CM}} \leq V_S$

This region of operation is the least accurate for the INA270 family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, $V_{\text{OUT}}$ approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer $V_{\text{SENSE}}$ approaches 0 V. Within this region, when $V_{\text{SENSE}}$ approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 18 shows this behavior for the INA271. The $V_{\text{OUT}}$ maximum peak for this case is determined by maintaining a constant $V_S$, setting $V_{\text{SENSE}} = 0$ mV, and sweeping $V_{\text{CM}}$ from 0 V to $V_S$. The exact $V_{\text{CM}}$ at which $V_{\text{OUT}}$ peaks during this case varies from device to device. The maximum peak voltage for the INA270 is 0.28 V; for the INA271, the maximum peak voltage is 0.4 V.

![Figure 18. Example for Low $V_{\text{SENSE}}$ Case 2 (INA271, Gain = 20)](image)

NOTE: (1) INA271 $V_{\text{OUT}}$ Limit = 0.4V. INA270 $V_{\text{OUT}}$ Limit = 0.28V.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The INA270 and INA271 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference terminal to adjust the functionality of the output signal offers multiple configurations discussed throughout this section. There is also a filtering feature to remove unwanted transients and smooth the output voltage.

9.2 Typical Application

9.2.1 Design Requirements
In this application, the device is configured to measure a triangular periodic current at 10 kHz with filtering. The average current through the shunt is the information that is desired. This current can be either solenoid current or inductor current where current is being pulsed through.

Selecting the capacitor size is based on the lowest frequency component to be filtered out. The amount of signal that is filtered out is dependant on this cutoff frequency. From the cutoff frequency, the attention is 20 dB per decade.
Typical Application (continued)

9.2.2 Detailed Design Procedure

Without this filtering capability, an input filter must be used. When series resistance is added to the input, large errors also come into play because the resistance must be large to create a low cutoff frequency. By using a 10-nF capacitor for the single-pole filter capacitor, the 10-kHz signal is averaged. The cutoff frequency made by the capacitor is set at 166 Hz frequency. This frequency is well below the periodic frequency and reduces the ripple on the output and the average current can easily be measured.

9.2.3 Application Curves

Figure 20 shows the output waveform without filtering. The output signal tracks the input signal with a large ripple. If this current is sampled by an ADC, many samples must be taken to average the current digitally. This process takes additional time to sample and average and is very time consuming, thus is unwanted for this application.

Figure 21 shows the output waveform with filtering. The output signal is filtered and the average can easily be measured with a small ripple. If this current is sampled by an ADC, only a few samples must be taken to average. Digital averaging is now not required and the time required is significantly reduced.
10 Power Supply Recommendations

The input circuitry of the INA270 and INA271 can accurately measure beyond its power-supply voltage, \( V^+ \). For example, the \( V^+ \) power supply can be 5 V, whereas the load power-supply voltage is up to +80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

10.1 Shutdown

The INA270 and INA271 do not provide a shutdown pin; however, because these devices consume a quiescent current less than 1 mA, they can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA270 and INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with a 0.1-\( \mu \)F bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate must have a supply voltage of 3 V or greater because the INA270 and INA271 require a minimum supply greater than 2.7 V. In addition to eliminating quiescent current, this gate also turns off the 10-\( \mu \)A bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is shown in Figure 22.

![Figure 22. INA270–INA271 Example Shutdown Circuit](image-url)
11 Layout

11.1 Layout Guidelines

• Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.

• Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.1.1 RFI and EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI and EMI sensitivity. PCB layout must locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA270 and INA271 versus the INA193 to INA198 may provide different EMI performance.

11.2 Layout Example

Figure 23. Example Layout
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation
For related documentation see the following:
INA270 TINA-TI Spice Model, SBOM306
INA270 PSpice Model, SBOM485
INA270 TINA-TI Reference Design, SBOC246

12.2 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>ORDER NOW</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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<tbody>
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12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
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12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA271:

NOTE: Qualified Version Definitions:
### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- K0: Dimension designed to accommodate the component thickness
- A0: Dimension designed to accommodate the component length
- B0: Overall width of the carrier tape
- W: Width of the component
- P1: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1
- Q2
- Q3
- Q4

**User Direction of Feed**

**Pocket Quadrants**

**Sprocket Holes**

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*All dimensions are nominal*

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**PACKAGE MATERIALS INFORMATION**

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**TAPE AND REEL BOX DIMENSIONS**

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*All dimensions are nominal*
TUBE

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*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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