INA28x-Q1 Automotive Grade, –14-V to +80-V, Bidirectional, High Accuracy, Low- or High-Side, Voltage Output, Current Shunt Monitor

1 Features
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C
  - Device Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide Common-Mode Range: –14 V to +80 V
- Offset Voltage: ±20 μV
- CMRR: 140 dB
- Accuracy:
  - ±1.4% Gain Error (Maximum)
  - 0.3 μV/°C Offset Drift
  - 0.005%/°C Gain Drift (Maximum)
- Available Gains:
  - 50 V/V: INA282-Q1
  - 100 V/V: INA286-Q1
  - 200 V/V: INA283-Q1
  - 500 V/V: INA284-Q1
  - 1000 V/V: INA285-Q1
- Quiescent Current: 900 μA (Maximum)

2 Applications
- EV and HEV Battery Management
- EV and HEV Chargers
- Electric Power Steering (EPS) Systems
- Body Control Modules
- Brake Systems
- Electronic Stability Control (ESC) Systems

3 Description
The INA28x-Q1 family includes the INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, and INA286-Q1 devices. These devices are voltage output current shunt monitors that can sense drops across shunts at common-mode voltages from –14 V to +80 V, independent of the supply voltage. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10 mV full-scale.

These current sense amplifiers operate from a single 2.7-V to 18-V supply, drawing a maximum of 900 μA of supply current. These devices are specified over the extended operating temperature range of –40°C to +125°C, and offered in SOIC-8 and VSSOP-8 packages.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA28x-Q1</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.

Detailed Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Revision B (December 2015) to Revision C (January 2021) Page
   • Updated the numbering format for tables, figures, and cross-references throughout the document ................. 1
   • Added Functional-Safety Capable bullets ........................................................................................................ 1

Changes from Revision A (July 2015) to Revision B (December 2015) Page
   • Changed VSSOP package from product preview to production data ............................................................... 1

Changes from Revision * (March 2012) to Revision A (May 2015) Page
   • Changed data sheet title from High-Accuracy, Wide Common-Mode Range, Bi-Directional CURRENT SHUNT MONITOR Zero-Drift Series to INA28x-Q1 Automotive Grade, –14-V to 80-V, Bidirectional, High Accuracy, Low- or High-Side, Voltage Output Current Shunt Monitor ................................................................. 1
   • Added DGK (VSSOP) package to data sheet ......................................................................................................... 1
   • Added Applications ............................................................................................................................................. 1
   • Changed front page diagram ............................................................................................................................. 1
   • Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 3
   • Added RVRR as symbol for reference rejection ratio .......................................................................................... 5
   • Changed order of figures in Typical Characteristics section ............................................................................... 7
   • Changed Figure 6-16 ........................................................................................................................................... 7
   • Changed V_DRIVE condition in Figure 6-20 and Figure 6-21 ........................................................................... 7
   • Added functional block diagram ........................................................................................................................ 13
   • Changed Figure 7-1 and Figure 7-2 .................................................................................................................... 15
   • Changed Figure 7-3 and Figure 7-4 .................................................................................................................... 16
   • Changed Figure 7-5 and Figure 7-6 .................................................................................................................... 16
   • Changed Figure 7-7 ........................................................................................................................................... 17
   • Changed Reference Common-Mode Rejection to Reference Voltage Rejection Ratio ................................... 18
   • Changed R_CM to RVRR in Table 7-1 and Table 7-2 ...................................................................................... 19
   • Changed Figure 8-1 ........................................................................................................................................... 20
   • Changed Figure 8-2 ........................................................................................................................................... 21
   • Changed Figure 8-4 ........................................................................................................................................... 23
5 Pin Configuration and Functions

A. NC: This pin is not internally connected. The NC pin should either be left floating or connected to GND.

Figure 5-1. D and DGK Package 8-Pin SOIC and VSSOP Top View

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>–IN</td>
<td>Analog</td>
<td>Connection to negative side of shunt resistor.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Analog</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>REF2</td>
<td>Analog</td>
<td>Reference voltage, 0 V to V+. See Section 7.4.1 for connection options.</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>—</td>
<td>This pin is not internally connected. The NC pin should either be left floating or connected to GND.</td>
</tr>
<tr>
<td>5</td>
<td>OUT</td>
<td>Analog output</td>
<td>Output voltage</td>
</tr>
<tr>
<td>6</td>
<td>V+</td>
<td>Analog</td>
<td>Power supply, 2.7 V to 18 V</td>
</tr>
<tr>
<td>7</td>
<td>REF1</td>
<td>Analog</td>
<td>Reference voltage, 0 V to V+. See Section 7.4.1 for connection options.</td>
</tr>
<tr>
<td>8</td>
<td>+IN</td>
<td>Analog input</td>
<td>Connection to positive side of shunt resistor.</td>
</tr>
</tbody>
</table>
## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.\(^{(1)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V^+ )</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Analog inputs, ( V_{+\text{IN}}, V_{-\text{IN}} )(^{(2)} )</td>
<td>(-5)</td>
<td>(5)</td>
</tr>
<tr>
<td>Differential ((V_{+\text{IN}}) - (V_{-\text{IN}}))(^{(3)} )</td>
<td>(-14)</td>
<td>(80)</td>
</tr>
<tr>
<td>Common-Mode</td>
<td>GND–0.3</td>
<td>((V^+) + 0.3)</td>
</tr>
<tr>
<td>Input current into any pin</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, ( T_{\text{stg}} )</td>
<td>(-65)</td>
<td>(150)</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) \( V_{+\text{IN}} \) and \( V_{-\text{IN}} \) are the voltages at the +IN and –IN pins, respectively.

\(^{(3)}\) Input voltages must not exceed common-mode rating.

### 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{(ESD)} ) Electrostatic discharge</td>
<td>Human body model (HBM), per AEC Q100-002(^{(1)} )</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per AEC Q100-011</td>
</tr>
</tbody>
</table>

\(^{(1)}\) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} ) Common-mode input voltage</td>
<td>12</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V^+ ) Operating supply voltage</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( T_A ) Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)} )</th>
<th>INA28x-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D (SOIC)</td>
</tr>
<tr>
<td>8 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>( R_{\text{JA}} ) Junction-to-ambient thermal resistance</td>
<td>134.9</td>
</tr>
<tr>
<td>( R_{\text{JC(top)}} ) Junction-to-case (top) thermal resistance</td>
<td>72.9</td>
</tr>
<tr>
<td>( R_{\text{JB}} ) Junction-to-board thermal resistance</td>
<td>61.3</td>
</tr>
<tr>
<td>( \psi_{\text{JT}} ) Junction-to-top characterization parameter</td>
<td>18.9</td>
</tr>
<tr>
<td>( \psi_{\text{JB}} ) Junction-to-board characterization parameter</td>
<td>54.3</td>
</tr>
<tr>
<td>( R_{\text{JC(bot)}} ) Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
6.5 Electrical Characteristics

at $T_A = 25^\circ C$, $V+ = 5 \, V$, $V_{\text{IN}} = 12 \, V$, $V_{\text{REF1}} = V_{\text{REF2}} = 2.048 \, V$ referenced to GND, and $V_{\text{SENSE}} = V_{\text{IN}} - V_{-\text{IN}}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{OS}}$</td>
<td>Offset Voltage, RTI$^{(1)}$</td>
<td>$V_{\text{SENSE}} = 0 , mV$</td>
<td>$\pm 20$</td>
<td>$\pm 70$</td>
<td>$\mu V$</td>
</tr>
<tr>
<td>$dV_{\text{OS}}/dT$</td>
<td>vs Temperature</td>
<td>$T_A = -40^\circ C$ to 125$^\circ C$</td>
<td>$\pm 0.3$</td>
<td>$\pm 1.5$</td>
<td>$\mu V/^\circ C$</td>
</tr>
<tr>
<td>PSRR</td>
<td>vs Power Supply</td>
<td>$V_S = 2.7 , V$ to 18 $V$, $V_{\text{SENSE}} = 0 , mV$</td>
<td>3</td>
<td></td>
<td>$\mu V/V$</td>
</tr>
<tr>
<td>$V_{\text{CM}}$</td>
<td>Common-Mode Input Range</td>
<td>$T_A = -40^\circ C$ to 125$^\circ C$</td>
<td>$-14$</td>
<td>$+80$</td>
<td>$V$</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection</td>
<td>$V_{\text{IN}} = -14 , V$ to 80 $V$, $V_{\text{SENSE}} = 0 , mV$</td>
<td>120</td>
<td>140</td>
<td>$dB$</td>
</tr>
<tr>
<td>$I_{\text{B}}$</td>
<td>Input Bias Current per Pin$^{(2)}$</td>
<td>$V_{\text{SENSE}} = 0 , mV$</td>
<td>25</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{\text{OS}}$</td>
<td>Input Offset Current</td>
<td>$V_{\text{SENSE}} = 0 , mV$</td>
<td>1</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td>Differential Input Impedance</td>
<td></td>
<td>6</td>
<td></td>
<td>$k\Omega$</td>
</tr>
</tbody>
</table>

REFERENCE INPUTS

| | | | | | |
| Reference Input Gain | | 1 | | | $V/V$ |
| Reference Input Voltage Range$^{(3)}$ | | $0$ | $V_{\text{GND}} + 9$ | $V$ |
| Divider Accuracy$^{(4)}$ | | $\pm 0.2\%$ | $\pm 0.5\%$ | | |

| RVRR | Reference Voltage Rejection Ratio ($V_{\text{REF1}} = V_{\text{REF2}} = 40 \, mV$ to 9 $V$; $V_{\text{IN}} = 18 \, V$) | | | | |
| INA282-Q1 | | $T_A = -40^\circ C$ to 125$^\circ C$ | $\pm 25$ | $\pm 75$ | $\mu V/V$ |
| INA283-Q1 | | $T_A = -40^\circ C$ to 125$^\circ C$ | $0.055$ | | $\mu V/V/^\circ C$ |
| INA284-Q1 | | $T_A = -40^\circ C$ to 125$^\circ C$ | $\pm 13$ | $\pm 30$ | $\mu V/V$ |
| INA285-Q1 | | $T_A = -40^\circ C$ to 125$^\circ C$ | $0.015$ | | $\mu V/V/^\circ C$ |
| INA286-Q1 | | $T_A = -40^\circ C$ to 125$^\circ C$ | $\pm 17$ | $\pm 45$ | $\mu V/V$ |

GAIN$^{(5)}$ ($G_{\text{N}} + 0.5 \, V \leq V_{\text{OUT}} \leq (V+) - 0.5 \, V$; $V_{\text{REF1}} = V_{\text{REF2}} = (V+) / 2$ for all devices)

| G | Gain | | | | |
| INA282-Q1, $V_{\text{IN}} = 5 \, V$ | | | 50 | | $V/V$ |
| INA283-Q1, $V_{\text{IN}} = 5 \, V$ | | | 200 | | $V/V$ |
| INA284-Q1, $V_{\text{IN}} = 5 \, V$ | | | 500 | | $V/V$ |
| INA285-Q1, $V_{\text{IN}} = 5 \, V$ | | | 1000 | | $V/V$ |
| INA286-Q1, $V_{\text{IN}} = 5 \, V$ | | | 100 | | $V/V$ |

| G | Gain Error | | | | |
| INA282-Q1, INA283-Q1, INA286-Q1 | | | $\pm 0.4\%$ | $\pm 1.4\%$ | | |
| INA284-Q1, INA285-Q1 | | | $\pm 0.4\%$ | $\pm 1.6\%$ | | |
| $T_A = -40^\circ C$ to 125$^\circ C$ | | | 0.0008 | 0.005 | $.%/^\circ C$ |
at $T_A = 25°C$, $V^+ = 5\, V$, $V_{\text{IN}} = 12\, V$, $V_{\text{REF1}} = V_{\text{REF2}} = 2.048\, V$ referenced to GND, and $V_{\text{SENSE}} = V_{\text{IN}} - V_{\text{IN}}$, unless otherwise noted.

## PARAMETERS TEST CONDITIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OUTPUT</strong></td>
<td>Nonlinearity Error</td>
<td>±0.01%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Impedance</td>
<td>1.5</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Maximum Capacitive Load</td>
<td>No sustained oscillation</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td><strong>VOLTAGE OUTPUT</strong></td>
<td>Swing to $V^+$ Power-Supply Rail</td>
<td>$V^+ = 5, V$, $R_{\text{LOAD}} = 10, kΩ$ to GND</td>
<td>$(V^+)-0.17$</td>
<td>$(V^+)-0.4$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Swing to GND</td>
<td>$T_A = -40°C$ to $125°C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
<td>Effective Bandwidth$^{(7)}$</td>
<td>INA282-Q1</td>
<td>10</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>INA283-Q1</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INA284-Q1</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INA285-Q1</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INA286-Q1</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NOISE, RTI$^{(1)}$</strong></td>
<td>Voltage Noise Density</td>
<td>1 kHz</td>
<td></td>
<td></td>
<td>110</td>
</tr>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td>Specified Voltage Range</td>
<td>$T_A = -40°C$ to $125°C$</td>
<td>2.7</td>
<td></td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>Quiescent Current</td>
<td></td>
<td></td>
<td>600</td>
<td>900</td>
</tr>
<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td>Specified Range</td>
<td></td>
<td></td>
<td></td>
<td>−40</td>
</tr>
</tbody>
</table>

1. RTI = referred-to-input.
2. See typical characteristic graph Figure 6-7.
3. The average of the voltage on pins REF1 and REF2 must be between $V_{\text{GND}}$ and the lesser of $(V_{\text{GND}} + 9\, V)$ and $V^+$.
4. Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 7-5.
5. See typical characteristic graphs Figure 6-16 through Figure 6-18.
6. See typical characteristic graph Figure 6-12.
7. See typical characteristic graph Figure 6-1 and Section 7.3.2 in the Applications Information.
6.6 Typical Characteristics

At $T_A = 25^\circ C$, $V_+ = 5\,V$, $V_{+\text{IN}} = 12\,V$, $V_{\text{REF1}} = V_{\text{REF2}} = 2.048\,V$ referenced to GND, and $V_{\text{SENSE}} = V_{+\text{IN}} - V_{-\text{IN}}$, unless otherwise noted.

![Figure 6-1. Gain vs Frequency](image1)

![Figure 6-2. INA282-Q1 PSRR (RTI) vs Frequency](image2)

![Figure 6-3. INA284-Q1 Common-Mode Rejection Ratio (RTI)](image3)

![Figure 6-4. INA282-Q1 Common-Mode Slew Rate Induced Offset](image4)

![Figure 6-5. INA286-Q1 Output Impedance vs Frequency](image5)

![Figure 6-6. INA282-Q1 Typical Nonlinearity vs Output Voltage](image6)
Figure 6-7. INA283-Q1 +IN BIAS Current vs Common-Mode Voltage

Figure 6-8. INA283-Q1 Quiescent Current vs Common-Mode Voltage

Figure 6-9. Quiescent Current vs Supply Voltage

Figure 6-10. Common-Mode Rejection Ratio vs Temperature

Figure 6-11. Quiescent Current vs Temperature

Figure 6-12. Deviation in Gain vs Temperature
**Figure 6-13. +IN BIAS Current vs Temperature**

![Graph showing +IN BIAS Current vs Temperature.](image)

**Figure 6-14. INA282-Q1 0.1-Hz to 10-Hz Voltage Noise, RTI**

![Graph showing Voltage Noise, RTI (200nV/div) vs Frequency.](image)

**Figure 6-15. INA282-Q1 Voltage Noise vs Frequency**

![Graph showing Voltage Noise, RTI (μV/Hz) vs Frequency.](image)

**Figure 6-16. INA284-Q1 Output Voltage Swing vs Output Current**

![Graph showing Output Voltage Swing vs Output Current.](image)

**Figure 6-17. INA283-Q1 Swing to Rail vs Output Current**

![Graph showing Swing to Rail vs Output Current.](image)

**Figure 6-18. INA283-Q1 Swing to Ground vs Output Current**

![Graph showing Swing to Ground vs Output Current.](image)
Figure 6-19. Start-Up Transient Response

Figure 6-20. Start-Up Transient Response

Figure 6-21. 12-V Common-Mode Step Response

Figure 6-22. 12-V Common-Mode Step Response

Figure 6-23. 12-V Common-Mode Step Response

Figure 6-24. 12-V Common-Mode Step Response
Figure 6-25. 50-V Common-Mode Step Response

Figure 6-26. 50-V Common-Mode Step Response

Figure 6-27. 100-mV Step Response

Figure 6-28. 500-mV Step Response

Figure 6-29. 4-V Step Response

Figure 6-30. 17-V Step Response
Figure 6-31. Input Overload
7 Detailed Description

7.1 Overview

The INA28x-Q1 family of voltage output current-sensing amplifiers are specifically designed to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the devices. This family features a common-mode range that extends 14 V less than the negative supply rail, as well as up to 80 V, allowing for either low-side or high-side current sensing while the device is powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 70 μV with a maximum temperature contribution of 1.5 μV/°C over the full temperature range of –40°C to 125°C.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Selecting Rs

The zero-drift offset performance of the INA28x-Q1 family offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift, current-shunt monitors typically require a full-scale range of 100 mV. The INA28x-Q1 family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude, with many additional benefits. Alternatively, applications that must measure current over a wide dynamic range can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA282-Q1, INA286-Q1, or INA283-Q1 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA282-Q1 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 55 mV, with only 70 μV of offset.

7.3.2 Effective Bandwidth

The extremely high DC CMRR of the INA28x-Q1 results from the switched capacitor input structure. Because of this architecture, the INA28x-Q1 exhibits discrete time system behaviors as illustrated in the gain versus frequency graph of Figure 6-3 and the step response curves of Figure 6-21 through Figure 6-28. The response to a step input depends somewhat on the phase of the internal INA28x-Q1 clock when the input step occurs. It is possible to overload the input amplifier with a rapid change in input common-mode voltage (see Figure 6-4). Errors as a result of common-mode voltage steps and/or overload situations typically disappear within 15 μs after the disturbance is removed.

7.3.3 Transient Protection

The –14-V to 80-V common-mode range of the INA28x-Q1 is ideal for withstanding automotive fault conditions that range from 12-V battery reversal up to 80-V transients; no additional protective components are needed up to those levels. In the event that the INA28x-Q1 is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (Zener or Transzorbs) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it cannot allow the INA28x-Q1 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage as a result of transient absorber dynamic impedance). Despite the use of internal zener-type electrostatic discharge (ESD) protection, the INA28x-Q1 does not lend itself to using external resistors in series with the inputs without degrading gain accuracy.
7.4 Device Functional Modes

7.4.1 Reference Pin Connection Options

Figure 7-1 illustrates a test circuit for reference divider accuracy. The output of the INA28x-Q1 can be connected for unidirectional or bidirectional operation. Neither the REF1 pin nor the REF2 pin may be connected to any voltage source lower than GND or higher than V+, and that the effective reference voltage (REF1 + REF2)/2 must be 9 V or less. This parameter means that the V+ reference output connection shown in Figure 7-3 is not allowed for V+ greater than 9 V. However, the split-supply reference connection shown in Figure 7-5 is allowed for all values of V+ up to 18 V.

A. Reference divider accuracy is determined by measuring the output with the reference voltage applied to alternate reference resistors, and calculating a result such that the amplifier offset is cancelled in the final measurement.

**Figure 7-1. Test Circuit for Reference Divider Accuracy**

### 7.4.1.1 Unidirectional Operation

Unidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in one direction. In the case of unidirectional operation, the output could be set at the negative rail (near ground, and the most common connection) or at the positive rail (near V+) when the differential input is 0V. The output moves to the opposite rail when a correct polarity differential input voltage is applied.

The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to move the output down. If the output is set at ground, the polarity is positive to move the output up.

The following sections describe how to configure the output for unidirectional operation.

#### 7.4.1.1.1 Ground Referenced Output

When using the INA28x-Q1 in this mode, both reference inputs are connected to ground; this configuration takes the output to the negative rail when there is 0V differential at the input (as Figure 7-2 shows).
7.4.1.1.2 V+ Referenced Output

This mode is set when both reference pins are connected to the positive supply. It is typically used when a diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (as shown in Figure 7-3).

![Figure 7-3. V+ Referenced Output](image)

7.4.1.2 Bidirectional Operation

Bidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, from 0 V to 9 V, but never to exceed the supply voltage). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage(s) to the reference inputs. REF1 and REF2 are connected to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

7.4.1.2.1 External Reference Output

Connecting both pins together and to a reference produces an output at the reference voltage when there is no differential input; this configuration is illustrated in Figure 7-4. The output moves down from the reference voltage when the input is negative relative to the –IN pin and up when the input is positive relative to the –IN pin. This technique is the most accurate way to bias the output to a precise voltage.

![Figure 7-4. External Reference Output](image)

7.4.1.2.2 Splitting the Supply

By connecting one reference pin to V+ and the other to the ground pin, the output is set at half of the supply when there is no differential input, as shown in Figure 7-5. This method creates a midscale offset that is
ratiometric to the supply voltage; thus, if the supply increases or decreases, the output remains at half the supply.

**Figure 7-5. Split-Supply Output**

7.4.1.2.3 Splitting an External Reference

In this case, an external reference is divided by 2 with an accuracy of approximately 0.5% by connecting one REF pin to ground and the other REF pin to the reference (as Figure 7-6 illustrates).

**Figure 7-6. Split Reference Output**

7.4.2 Shutdown

While the INA28x-Q1 family does not provide a shutdown pin, the quiescent current of 600 μA enables the device to be powered from the output of a logic gate. Take the gate low to shut down the INA28x-Q1 family devices.

7.4.3 Extended Negative Common-Mode Range

Using a negative power supply can extend the common-mode range 14 V more negative than the supply used. For instance, a –10 V supply allows up to –24-V negative common-mode. Remember to keep the total voltage between the GND pin and V+ pin to less than 18 V. The positive common-mode decreases by the same amount.

The reference input simplifies this type of operation because the output quiescent bias point is always based on the reference connections. **Figure 7-7** shows a circuit configuration for common-mode ranges from –24 V to 70 V.
A. Connect the REF pins as desired; however, they cannot exceed 9 V greater than the GND pin voltage.

Figure 7-7. Circuit Configuration for Common-Mode Ranges from –24 V to 70 V

7.4.4 Calculating Total Error

The electrical specifications for the INA28x-Q1 family of devices include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in Section 6.5. To accurately calculate the expected error of the device, the operating conditions of the device must first be known. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them to calculate the total error value for the device under any normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode rejection ratio, gain error, and nonlinearity error. For the INA28x-Q1, an additional error source referred to as reference voltage rejection ratio is also included in the total error value.

The nonlinearity error of the INA28x-Q1 is relatively low compared to the gain error specification. This low error results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA28x-Q1 decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal resulting in an increase in error in the measurement. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The relatively low input offset voltages present in the INA28x-Q1 devices limit the amount of contribution the offset voltage has on the total error term.

The term reference voltage rejection ratio refers to the amount of error induced by applying a reference voltage to the INA28x-Q1 device that deviates from the inherent bias voltage present at the output of the first stage of the device. The output of the switched-capacitor network and first-stage amplifier has an inherent bias voltage of approximately 2.048 V. Applying a reference voltage of 2.048 V to the INA28x-Q1 reference pins results in no additional error term contribution. Applying a voltage to the reference pins that differs from 2.048 V creates a voltage potential in the internal difference amplifier, resulting in additional current flowing through the resistor network. As a result of resistor tolerances, this additional current flow causes additional error at the output because of resistor mismatches. Additionally, as a result of resistor tolerances, this additional current flow causes additional error at the output based on the common-mode rejection ratio of the output stage amplifier. This error term is referred back to the input of the device as additional input offset voltage. Increasing the difference between the 2.048-V internal bias and the external reference voltage results in a higher input offset voltage. Also, as the error at the output is referred back to the input, there is a larger impact on the input-referred offset, $V_{OS}$, for the lower-gain versions of the device.
Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well, to provide the user more information on how much error variance is present from device to device.

### 7.4.4.1 Example 1 INA282-Q1

**Table 7-1.** $V^+ = 5 \text{ V}; \ V_{CM} = 12 \text{ V}; \ V_{REF1} = V_{REF2} = 2.048 \text{ V}; \ V_{SENSE} = 10 \text{ mV}

<table>
<thead>
<tr>
<th>TERM</th>
<th>SYMBOL</th>
<th>EQUATION</th>
<th>TYPICAL VALUE</th>
<th>MAXIMUM VALUE</th>
</tr>
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<tbody>
<tr>
<td>Initial input offset voltage</td>
<td>$V_{OS}$</td>
<td>—</td>
<td>20 μV</td>
<td>70 μV</td>
</tr>
<tr>
<td>Added input offset voltage because of common-mode voltage</td>
<td>$V_{OS_CM}$</td>
<td>$\frac{1}{10 (CMRR_{db})} \times (V_{CM} - 12 \text{ V})$</td>
<td>0 μV</td>
<td>0 μV</td>
</tr>
<tr>
<td>Added input offset voltage because of reference voltage</td>
<td>$V_{OS_REF}$</td>
<td>$RVRR \times (2.048 \text{ V} - V_{REF})$</td>
<td>0 μV</td>
<td>0 μV</td>
</tr>
<tr>
<td>Total input offset voltage</td>
<td>$V_{OS_Total}$</td>
<td>$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$</td>
<td>20 μV</td>
<td>70 μV</td>
</tr>
<tr>
<td>Error from input offset voltage</td>
<td>$Error_{V_{OS}}$</td>
<td>$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$</td>
<td>0.20%</td>
<td>0.70%</td>
</tr>
<tr>
<td>Gain error</td>
<td>$Error_{Gain}$</td>
<td>—</td>
<td>0.40%</td>
<td>1.40%</td>
</tr>
<tr>
<td>Nonlinearity error</td>
<td>$Error_{Lin}$</td>
<td>—</td>
<td>0.01%</td>
<td>0.01%</td>
</tr>
<tr>
<td><strong>Total error</strong></td>
<td>—</td>
<td>$\sqrt{(Error_{V_{OS}})^2 + (Error_{Gain})^2 + (Error_{Lin})^2}$</td>
<td>0.45%</td>
<td>1.56%</td>
</tr>
</tbody>
</table>

### 7.4.4.2 Example 2 INA286-Q1

**Table 7-2.** $V^+ = 5 \text{ V}; \ V_{CM} = 24 \text{ V}; \ V_{REF1} = V_{REF2} = 0 \text{ V}; \ V_{SENSE} = 10 \text{ mV}

<table>
<thead>
<tr>
<th>TERM</th>
<th>SYMBOL</th>
<th>EQUATION</th>
<th>TYPICAL VALUE</th>
<th>MAXIMUM VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial input offset voltage</td>
<td>$V_{OS}$</td>
<td>—</td>
<td>20 μV</td>
<td>70 μV</td>
</tr>
<tr>
<td>Added input offset voltage because of common-mode voltage</td>
<td>$V_{OS_CM}$</td>
<td>$\frac{1}{10 (CMRR_{db})} \times (V_{CM} - 12 \text{ V})$</td>
<td>1.2 μV</td>
<td>12 μV</td>
</tr>
<tr>
<td>Added input offset voltage because of reference voltage</td>
<td>$V_{OS_REF}$</td>
<td>$RVRR \times (2.048 \text{ V} - V_{REF})$</td>
<td>34.8 μV</td>
<td>92.2 μV</td>
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<tr>
<td>Total input offset voltage</td>
<td>$V_{OS_Total}$</td>
<td>$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$</td>
<td>40.2 μV</td>
<td>116.4 μV</td>
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<td>Error from input offset voltage</td>
<td>$Error_{V_{OS}}$</td>
<td>$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$</td>
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<td>Gain error</td>
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<td>0.40%</td>
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<td>Nonlinearity error</td>
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<td>0.01%</td>
<td>0.01%</td>
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<td>0.57%</td>
<td>1.82%</td>
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</table>
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA28x-Q1 family of devices measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pins to adjust the functionality of the output signal is shown in multiple configurations.

8.1.1 Basic Connections

Figure 8-1 shows the basic connection of an INA28x-Q1 family device. Connect the input pins, +IN and –IN, as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.
8.2 Typical Applications
8.2.1 Current Summing

The outputs of multiple INA28x-Q1 family devices are easily summed by connecting the output of one INA28x-Q1 family device to the reference input of a second INA28x-Q1 family device. The circuit configuration shown in Figure 8-1 is an easy way to achieve current summing.

NOTE: The voltage applied to the reference inputs must not exceed 9 V.

Figure 8-2. Summing the Outputs of Multiple INA28x-Q1 Family Devices
8.2.1.1 Design Requirements

In order to sum multiple load currents, multiple INA28x-Q1 devices must be connected. Figure 8-2 shows summing for two devices. Summing beyond two devices is possible by repeating this connection. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

8.2.1.2 Detailed Design Procedures

Connect the output of one INA28x-Q1 family device to the reference input of the next INA28x-Q1 family device in the chain. Use the reference input of the first circuit to set the reference of the final summed output. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

8.2.1.3 Application Curve

Figure 8-3 shows an example output response of a summing configuration. The reference pins of the first circuit are connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.

![Figure 8-3. Current Summing Application Output Response](image-url)
8.2.2 Current Differencing

Occasionally, the need arises to confirm that the current into a load is identical to the current out of a load, usually as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing except that the two amplifiers have the inputs connected opposite of each other.

**NOTE:** The voltage applied to the reference inputs must not exceed 9 V.

**Figure 8-4. Current Differencing Using an INA28x-Q1 Device**
8.2.2.1 Design Requirements

For current differencing, connect two INA28x-Q1 devices, and connect the inputs opposite to each other, as shown in Figure 8-4. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

8.2.2.2 Detailed Design Procedure

Connect the output of one INA28x-Q1 family device to the reference input of the second INA28x-Q1 family device. The reference input of the first circuit sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current into and out of a load do not match.

8.2.2.3 Application Curve

Figure 8-5 shows an example output response of a difference configuration. The reference pins of the first circuit are connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out of phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.

![Diagram of Current Differencing Application Output Response](image)

}\text{Figure 8-5. Current Differencing Application Output Response}
9 Power Supply Recommendations

The INA28x-Q1 can make accurate measurements well outside of its own power-supply voltage, V+, because its inputs (+IN and –IN) may operate anywhere from –14 V to 80 V independent of V+. For example, the V+ power supply can be 5 V while the common-mode voltage being monitored by the shunt may be as high as 80 V. Of course, the output voltage range of the INA28x-Q1 is constrained by the supply voltage that powers it on V+. When the power to the INA28x-Q1 is off (that is, no voltage is supplied to the V+ pin), the input pins (+IN and –IN) are high impedance with respect to ground and typically leak less than ±1 μA over the full common-mode range of –14 V to 80 V.

10 Layout

10.1 Layout Guidelines

Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor with a value of 0.1 uF. Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

![Figure 10-1. Layout Example](image-url)
11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
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<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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<td>286Q1</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **_OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based
  flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, INA286-Q1:
- Catalog: INA282, INA283, INA284, INA285, INA286

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**TAPE DIMENSIONS**

- **K0** Dimension designed to accommodate the component thickness
- **B0** Dimension designed to accommodate the component length
- **A0** Dimension designed to accommodate the component width
- **P1** Pitch between successive cavity centers
- **W** Overall width of the carrier tape

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

*All dimensions are nominal

<table>
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<th>Package Type</th>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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