Burr-Brown Products from Texas Instruments

INA326 INA327

SBOS222D – NOVEMBER 2001 – REVISED NOVEMBER 2004

Precision, Rail-to-Rail I/O INSTRUMENTATION AMPLIFIER

FEATURES

- **PRECISION**
  - **LOW OFFSET: 100µV (max)**
  - **LOW OFFSET DRIFT: 0.4µV/°C (max)**
  - **EXCELLENT LONG-TERM STABILITY**
  - **VERY-LOW 1/f NOISE**
- **TRUE RAIL-TO-RAIL I/O**
  - **INPUT COMMON-MODE RANGE: 20mV Below Negative Rail to 100mV Above Positive Rail**
  - **WIDE OUTPUT SWING: Within 10mV of Rails**
  - **SUPPLY RANGE: Single +2.7V to +5.5V**
- **SMALL SIZE**
  - ***micro*PACKAGE: MSOP-8, MSOP-10**
- **LOW COST**

APPLICATIONS

- **LOW-LEVEL TRANSDUCER AMPLIFIER FOR BRIDGES, LOAD CELLS, THERMOCOUPLES**
- **WIDE DYNAMIC RANGE SENSOR MEASUREMENTS**
- **HIGH-RESOLUTION TEST SYSTEMS**
- **WEIGH SCALES**
- **MULTI-CHANNEL DATA ACQUISITION SYSTEMS**
- **MEDICAL INSTRUMENTATION**
- **GENERAL-PURPOSE**

DESCRIPTION

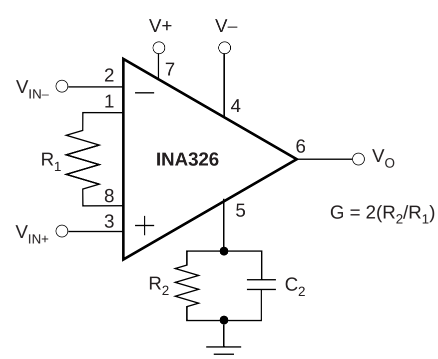
The INA326 and INA327 (with shutdown) are high-performance, low-cost, precision instrumentation amplifiers with rail-to-rail input and output. They are true single-supply instrumentation amplifiers with very low DC errors and input common-mode ranges that extends beyond the positive and negative rails. These features make them suitable for applications ranging from general-purpose to high-accuracy.

Excellent long-term stability and very low 1/f noise assure low offset voltage and drift throughout the life of the product.

The INA326 (without shutdown) comes in the MSOP-8 package. The INA327 (with shutdown) is offered in an MSOP-10. Both are specified over the industrial temperature range, –40°C to +85°C, with operation from –40°C to +125°C.

INA326 AND INA327 RELATED PRODUCTS

PRODUCT	FEATURES
INA337	**Precision, 0.4µV/°C Drift, Specified –40°C to +125°C**
INA114	50µV V_{OS}, 0.5nA I_B, 115dB CMR, 3mA I_Q, 0.25µV/°C Drift
INA118	50µV V_{OS}, 1nA I_B, 120dB CMR, 385µA I_Q, 0.5µV/°C Drift
INA122	250µV V_{OS}, –10nA I_B, 85µA I_Q, Rail-to-Rail Output, 3µV/°C Drift
INA128	50µV V_{OS}, 2nA I_B, 125dB CMR, 750µA I_Q, 0.5µV/°C Drift
INA321	500µV V_{OS}, 0.5pA I_B, 94dB CMRR, 60µA I_Q, Rail-to-Rail Output



PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
INA326	MSOP-8	DGK	–40°C to +85°C	B26	INA326EA/250	Tape and Reel, 250
"	"	"	"	"	INA326EA/2K5	Tape and Reel, 2500
INA327	MSOP-10	DGS	–40°C to +85°C	B27	INA327EA/250	Tape and Reel, 250
"	"	"	"	"	INA327EA/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, download the latest version of this data sheet and see the Package Option Addendum located at the end of the data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals: Voltage(2)	–0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit	Continuous
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

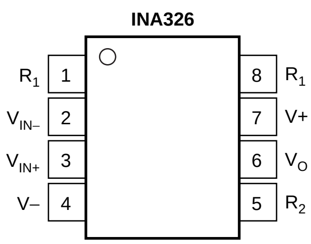
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

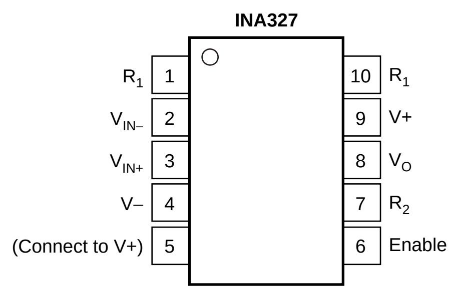
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View



MSOP- 8



MSOP- 10

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +85°C

At T_A = +25°C, R_L = 10kΩ, G = 100 (R_1 = 2kΩ, R_2 = 100kΩ), external gain set resistors, and IA_{COMMON} = V_S/2, with external equivalent filter corner of 1kHz, unless otherwise noted.

PARAMETER		CONDITION	INA326EA, INA327EA MIN	TYP	MAX	UNITS
INPUT						
Offset Voltage, RTI	V_{OS}	V_S = +5V, V_{CM} = V_S/2		±20	±100	µV
Over Temperature					**±124**	**µV**
vs Temperature	**dV_{OS}/dT**			**±0.1**	**±0.4**	**µV/°C**
vs Power Supply	PSR	V_S = +2.7V to +5.5V, V_{CM} = V_S/2	±20	±3		µV/V
Long-Term Stability				See Note (1)		
Input Impedance, Differential				10^{10} || 2		Ω || pF
Common-Mode				10^{10} || 14		Ω || pF
Input Voltage Range			**(V–) – 0.02**		**(V+) + 0.1**	**V**
Safe Input Voltage			(V–) – 0.5		(V+) + 0.5	V
Common-Mode Rejection	CMR	V_S = +5V, V_{CM} = (V–) – 0.02V to (V+) + 0.1V	100	114		dB
Over Temperature			**94**			**dB**
INPUT BIAS CURRENT		V_{CM} = V_S/2				
Bias Current	I_B	V_S = +5V		±0.2	±2	nA
vs Temperature				**See Typical Characteristics**		
Offset Current	I_{OS}	V_S = +5V		±0.2	±2	nA
NOISE						
Voltage Noise, RTI		R_S = 0Ω, G = 100, R_1 = 2kΩ, R_2 = 100kΩ				
f = 10Hz				33		nV/√Hz
f = 100Hz				33		nV/√Hz
f = 1kHz				33		nV/√Hz
f = 0.01Hz to 10Hz				0.8		µVp-p
Voltage Noise, RTI		R_S = 0Ω, G = 10, R_1 = 20kΩ, R_2 = 100kΩ				
f = 10Hz				120		nV/√Hz
f = 100Hz				97		nV/√Hz
f = 1kHz				97		nV/√Hz
f = 0.01Hz to 10Hz				4		µVp-p
Current Noise, RTI						
f = 1kHz				0.15		pA/√Hz
f = 0.01Hz to 10Hz				4.2		pAp-p
Output Ripple, V_O Filtered(2)				See Applications Information		
GAIN						
Gain Equation				G = 2(R_2/R_1)		
Range of Gain			< 0.1		> 10000	V/V
Gain Error(3)		G = 10, 100, V_S = +5V, V_O = 0.075V to 4.925V		±0.08	±0.2	%
vs Temperature		**G = 10, 100, V_S = +5V, V_O = 0.075V to 4.925V**		**±6**	**±25**	**ppm/°C**
Nonlinearity		G = 10, 100, V_S = +5V, V_O = 0.075V to 4.925V		±0.004	±0.01	% of FS
OUTPUT						
Voltage Output Swing from Rail		R_L = 100kΩ		5		mV
		R_L = 10kΩ, V_S = +5V	75	10		mV
Over Temperature			**75**			**mV**
Capacitive Load Drive				500		pF
Short-Circuit Current	I_{SC}			±25		mA
INTERNAL OSCILLATOR						
Frequency of Auto-Correction				90		kHz
Accuracy				±20		%
FREQUENCY RESPONSE						
Bandwidth(4), –3dB	BW	G = 1 to 1k		1		kHz
Slew Rate(4)	SR	V_S = +5V, All Gains, C_L = 100pF		Filter Limited		
Settling Time(4), 0.1%	t_S	1kHz Filter, G = 1 to 1k, V_O = 2V step, C_L = 100pF		0.95		ms
0.01%				1.3		ms
0.1%		10kHz Filter, G = 1 to 1k, V_O = 2V step, C_L = 100pF		130		µs
0.01%				160		µs
Overload Recovery(4)		1kHz Filter, 50% Output Overload, G = 1 to 1k		30		µs
		10kHz Filter, 50% Output Overload, G = 1 to 1k		5		µs

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (Cont.)

BOLDFACE limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 10kΩ, G = 100 (R_1 = 2kΩ, R_2 = 100kΩ), external gain set resistors, and IA_{COMMON} = V_S/2, with external equivalent filter corner of 1kHz, unless otherwise noted.

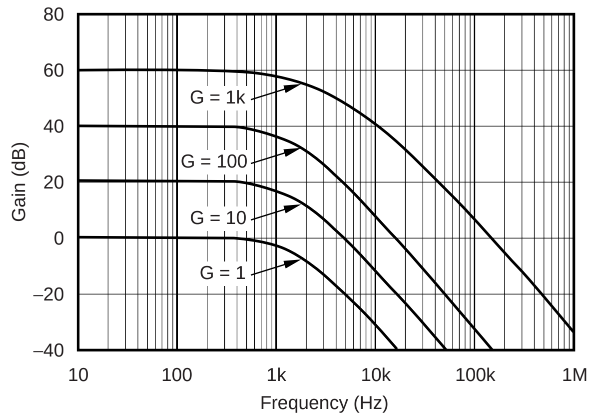
PARAMETER		CONDITION	INA326EA, INA327EA			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
Specified Voltage Range			+2.7		+5.5	V
Quiescent Current	I_Q	I_O = 0, Diff V_{IN} = 0V, V_S = +5V		2.4	3.4	mA
Over Temperature					**3.7**	**mA**
SHUTDOWN						
Disable (Logic Low Threshold)					0.25	V
Enable (Logic High Threshold)			1.6			V
Enable Time(5)				75		µs
Disable Time				100		µs
Shutdown Current and Enable Pin Current		V_S = +5V, Disabled		2	5	µA
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range			–40		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}	MSOP-8, MSOP-10 Surface-Mount		150		°C/W

NOTES: (1) 1000-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately 10µV. (2) See Applications Information section, and Figures 1 and 3. (3) Does not include error and TCR of external gain-setting resistors. (4) Dynamic response is limited by filtering. Higher bandwidths can be achieved by adjusting the filter. (5) See Typical Characteristics, “Input Offset Voltage vs Warm-Up Time”.

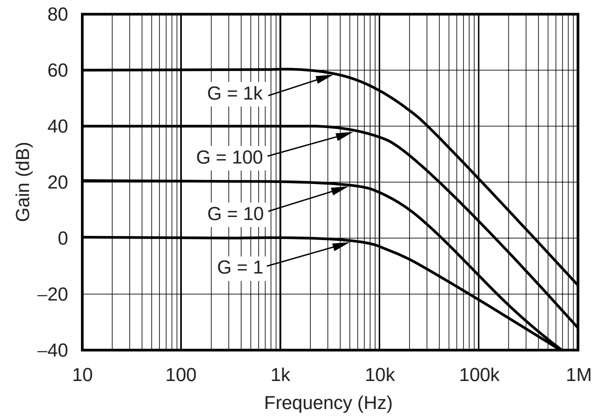
TYPICAL CHARACTERISTICS

At $T_A = 25°C$, $V_S = +5V$, Gain = 100, and $R_L = 10kΩ$ with external equivalent filter corner of 1kHz, unless otherwise noted.

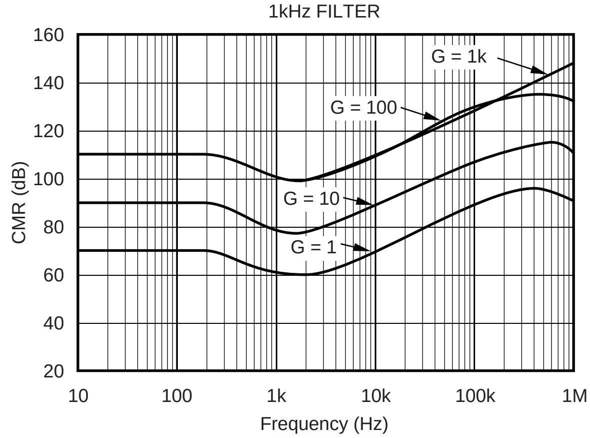
GAIN vs FREQUENCY
1kHz FILTER



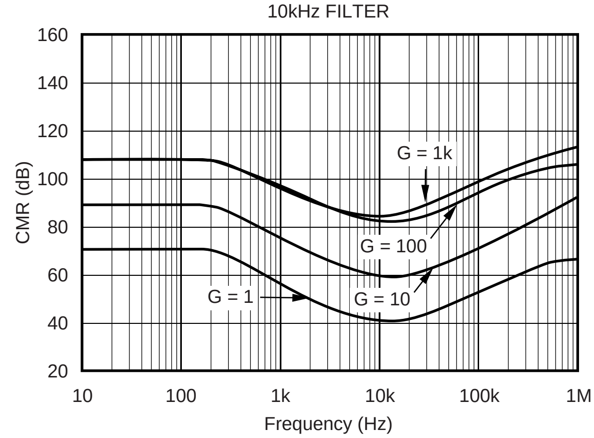
GAIN vs FREQUENCY
10kHz FILTER



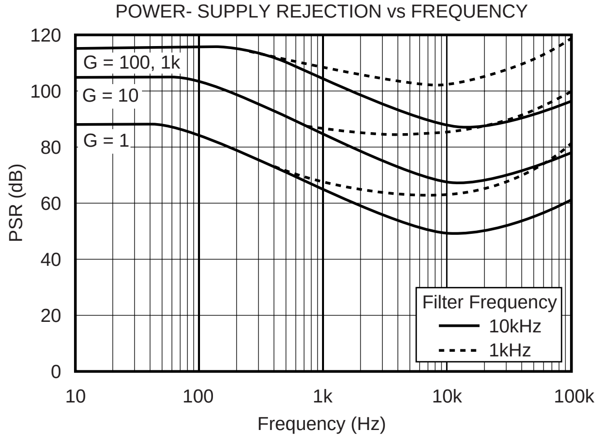
COMMON- MODE REJECTION vs FREQUENCY
1kHz FILTER



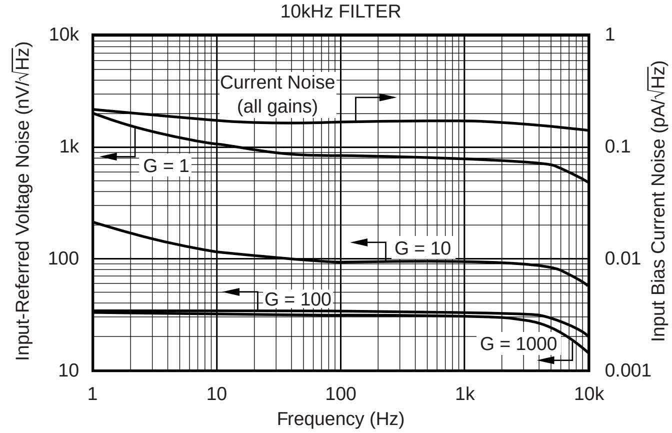
COMMON- MODE REJECTION vs FREQUENCY
10kHz FILTER



POWER- SUPPLY REJECTION vs FREQUENCY

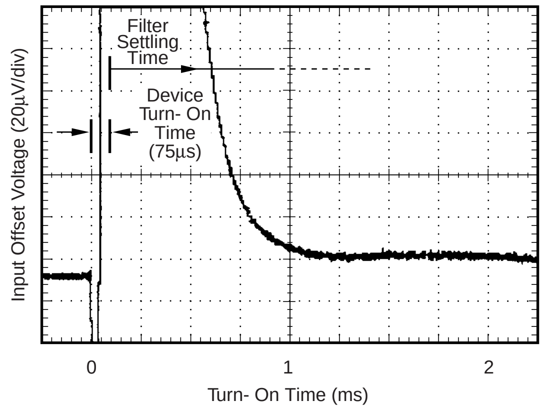


INPUT- REFERRED VOLTAGE NOISE AND
INPUT BIAS CURRENT NOISE vs FREQUENCY
10kHz FILTER

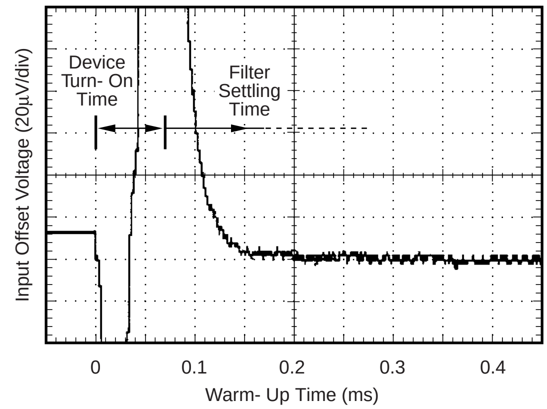


At $T_A = 25°C$, $V_S = +5V$, Gain = 100, and $R_L = 10k\Omega$ with external equivalent filter corner of 1kHz, unless otherwise noted.

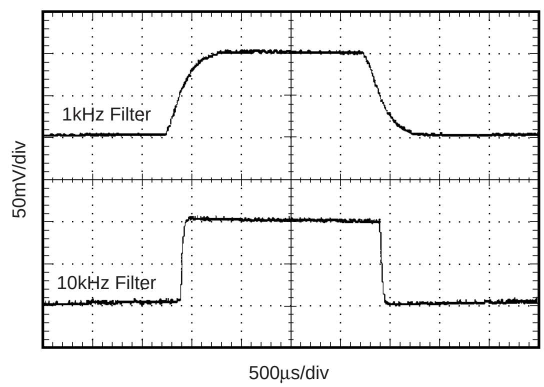
INPUT OFFSET VOLTAGE vs TURN- ON TIME
1kHz FILTER, G = 100



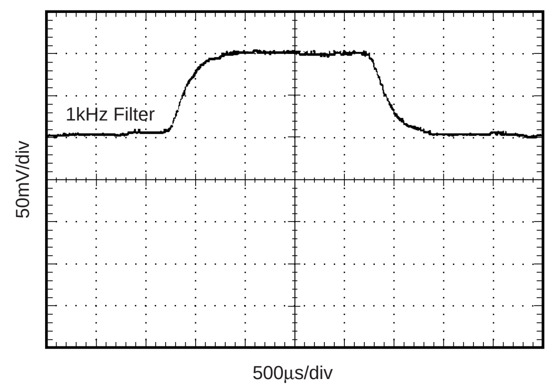
INPUT OFFSET VOLTAGE vs WARM- UP TIME
10kHz FILTER, G = 100



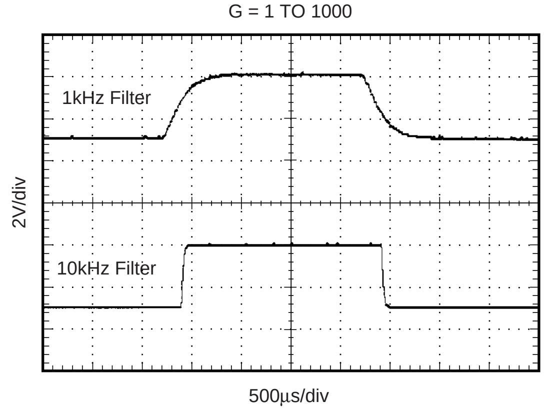
SMALL- SIGNAL RESPONSE
G = 1, 10, AND 100



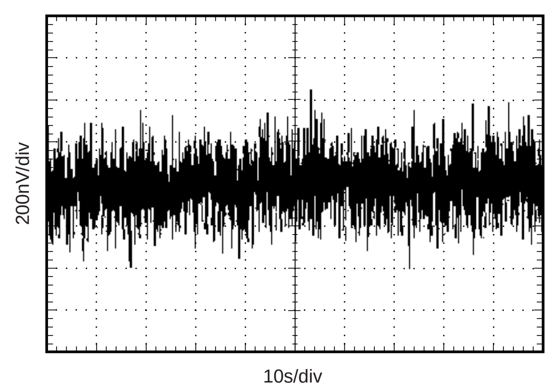
SMALL- SIGNAL STEP RESPONSE
G = 1000



LARGE- SIGNAL RESPONSE
G = 1 TO 1000

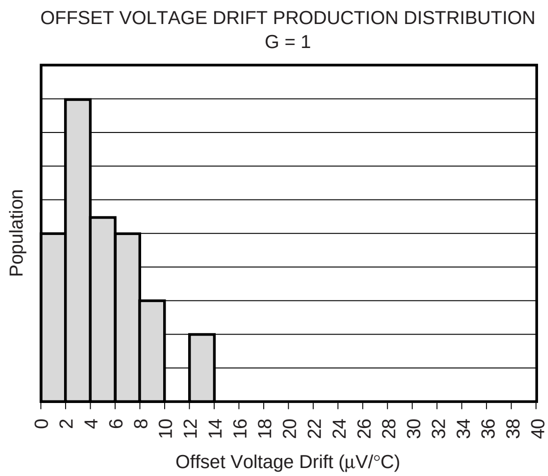


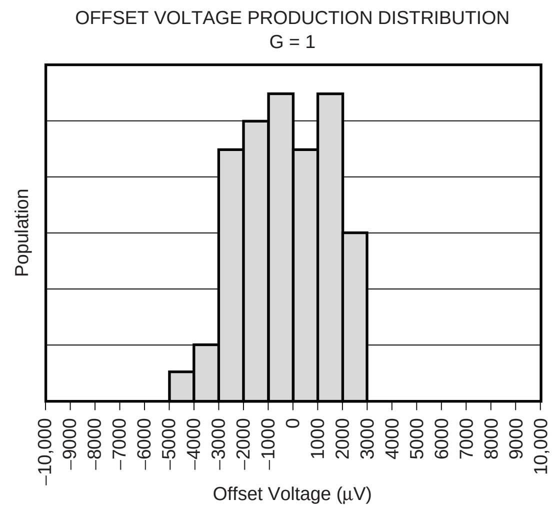
0.01Hz TO 10Hz VOLTAGE NOISE

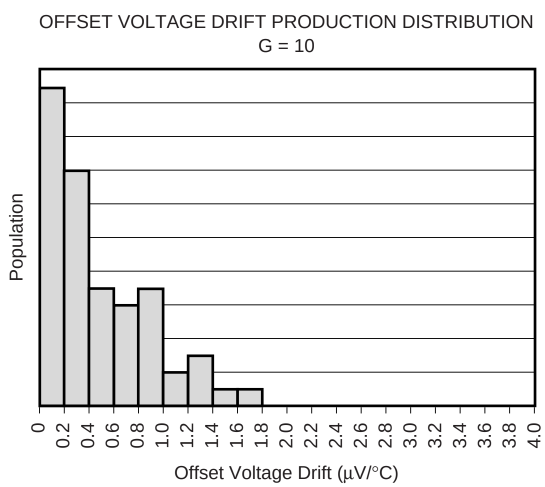


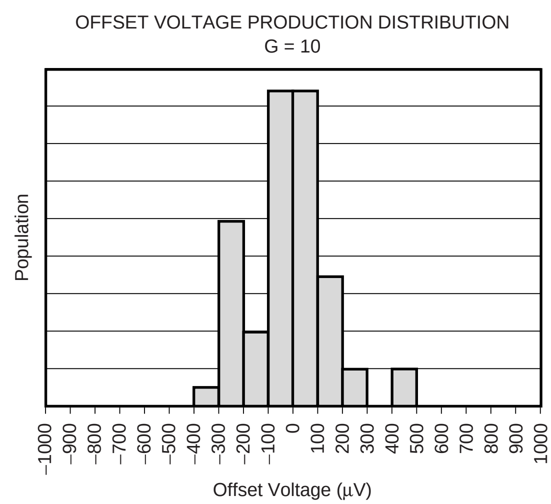
TYPICAL CHARACTERISTICS (Cont.)

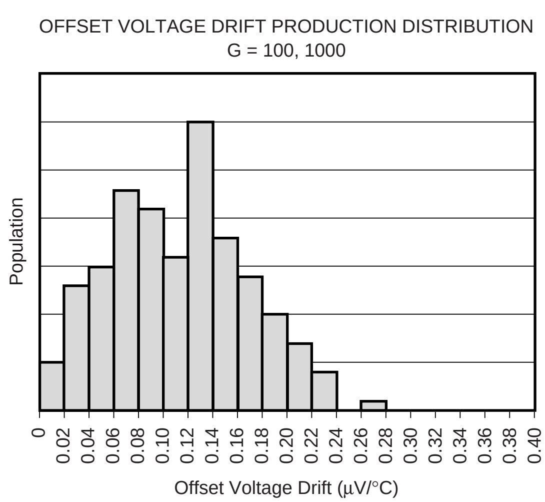
At $T_A = 25°C$, $V_S = +5V$, Gain = 100, and $R_L = 10k\Omega$ with external equivalent filter corner of 1kHz, unless otherwise noted.

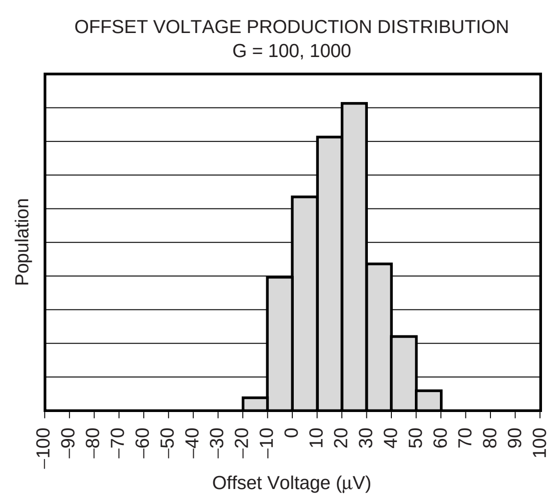






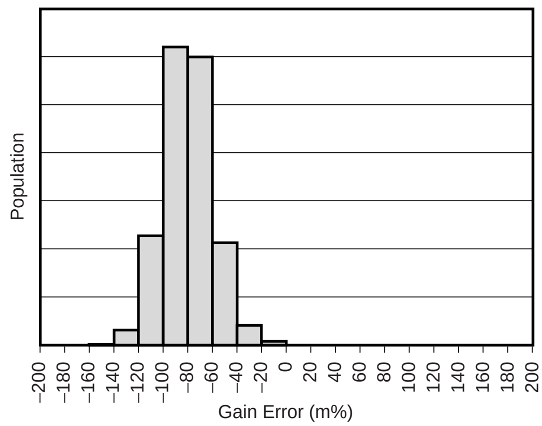




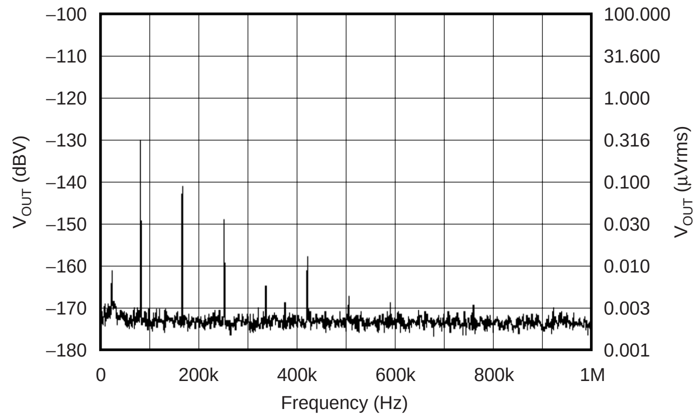


At T_A = 25°C, V_S = +5V, Gain = 100, and R_L = 10kΩ with external equivalent filter corner of 1kHz, unless otherwise noted.

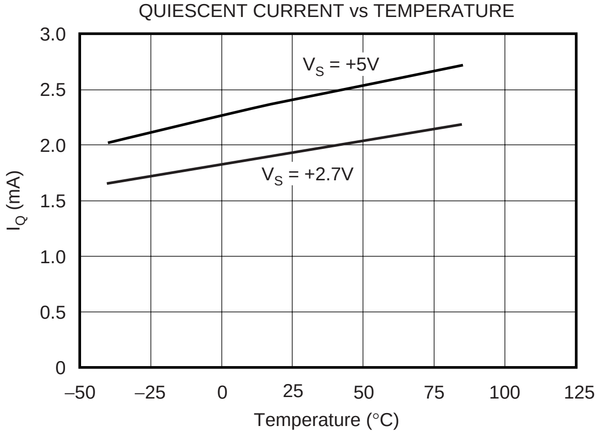
GAIN ERROR PRODUCTION DISTRIBUTION
G = 100



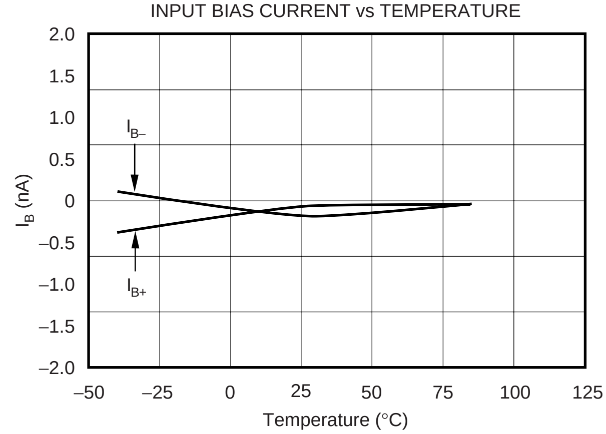
INPUT- REFERRED RIPPLE SPECTRUM
G = 100



QUIESCENT CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA326. A 0.1µF capacitor, placed close to and across the power-supply pins is strongly recommended for highest accuracy. R_oC_o is an output filter that minimizes auto-correction circuitry noise. This output filter may also serve as an anti-aliasing filter ahead of an Analog-to-Digital (A/D) converter. It is also optional based on desired precision.

The output reference terminal is taken at the low side of R_2 (IA_{COMMON}).

The INA326 uses a unique internal topology to achieve excellent Common-Mode Rejection (CMR). Unlike conventional instrumentation amplifiers, CMR is not affected by resistance in the reference connections or sockets. See "Inside the INA326" for further detail. To achieve best high-frequency CMR, minimize capacitance on pins 1 and 8.

SETTING THE GAIN

The INA326 is a 2-stage amplifier with each stage gain set by R_1 and R_2, respectively (see Figure 5, "Inside the INA326", for details). Overall gain is described by the equation:

$$G = 2\frac{R_2}{R_1} \quad (1)$$

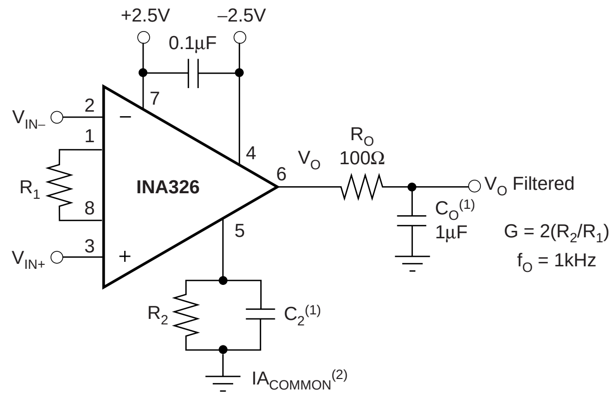
The stability and temperature drift of the external gain-setting resistors will affect gain by an amount that can be directly inferred from the gain equation (1).

Resistor values for commonly used gains are shown in Figure 1. Gain-set resistor values for best performance are different for +5V single-supply and for ±2.5V dual-supply operation. Optimum value for R_1 can be calculated by:

$$R_1 = V_{IN,\ MAX}/12.5\mu A \quad (2)$$

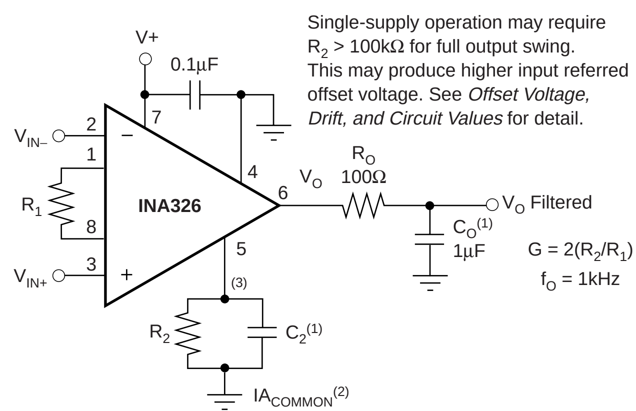
where R_1 must be no less than 2kΩ.

DESIRED GAIN	R_1 (Ω)	$R_2 \parallel C_2$ (Ω ǁ nF)
0.1	400k	20k ǁ 5
0.2	400k	40k ǁ 2.5
0.5	400k	100k ǁ 1
1	200k	100k ǁ 1
2	100k	100k ǁ 1
5	40k	100k ǁ 1
10	20k	100k ǁ 1
20	10k	100k ǁ 1
50	4k	100k ǁ 1
100	2k	100k ǁ 1
200	2k	200k ǁ 0.5
500	2k	500k ǁ 0.2
1000	2k	1M ǁ 0.1
2000	2k	2M ǁ 0.05
5000	2k	5M ǁ 0.02
10000	2k	10M ǁ 0.01



(1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz.
(2) Output voltage is referenced to IA_{COMMON} (see text).

DESIRED GAIN	R_1 (Ω)	$R_2 \parallel C_2$ (Ω ǁ nF)
0.1	400k	20k ǁ 5
0.2	400k	40k ǁ 2.5
0.5	400k	100k ǁ 1
1	400k	200k ǁ 0.5
2	200k	200k ǁ 0.5
5	80k	200k ǁ 0.5
10	40k	200k ǁ 0.5
20	20k	200k ǁ 0.5
50	8k	200k ǁ 0.5
100	4k	200k ǁ 0.5
200	2k	200k ǁ 0.5
500	2k	500k ǁ 0.2
1000	2k	1M ǁ 0.1
2000	2k	2M ǁ 0.05
5000	2k	5M ǁ 0.02
10000	2k	10M ǁ 0.01



(1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz.
(2) Output voltage is referenced to IA_{COMMON} (see text).
(3) Output offset voltage required for measurement near zero (see Figure 28).

NOTES: (1) C_2 and C_O combine to form a 2-pole response that is –3dB at 1kHz. Each individual pole is at 1.5kHz. (2) Output voltage is referenced to IA_{COMMON} (see text). (3) Output offset voltage required for measurement near zero (see Figure 6).

FIGURE 1. Basic Connections. NOTE: Connections for INA327 differ—see Pin Configuration for detail.

Following this design procedure for R_1 produces the maximum possible input stage gain for best accuracy and lowest noise.

Circuit layout and supply bypassing can affect performance. Minimize the stray capacitance on pins 1 and 8. Use recommended supply bypassing, including a capacitor directly from pin 7 to pin 4 (V+ to V–), even with dual (split) power supplies (see Figure 1).

OFFSET VOLTAGE, DRIFT, AND CIRCUIT VALUES

As with other multi-stage instrumentation amplifiers, input-referred offset voltage depends on gain and circuit values. The specified offset and drift performance is rated at $R_1 = 2k\Omega$, $R_2 = 100k\Omega$, and $V_S = \pm2.5V$. Offset voltage and drift for other circuit values can be estimated from the following equations:

$$V_{OS} = 10\mu V + (50nA)(R_2)/G \quad (3)$$

$$dV_{OS}/dT = 0.12\mu V/°C + (0.16nA/°C)(R_2)/G \quad (4)$$

These equations might imply that offset and drift can be minimized by making the value of R_2 much lower than the values indicated in Figure 1. These values, however, have been chosen to assure that the output current into R_2 is kept less than or equal to ±25µA, while maintaining R_1's value greater than or equal to 2kΩ. Some applications with limited output voltage swing or low power-supply voltage may allow lower values for R_2, thus providing lower input-referred offset voltage and offset voltage drift.

Conversely, single-supply operation with R_2 grounded requires that R_2 values be made larger to assure that current remains under 25µA. This will increase the input-referred offset voltage and offset voltage drift.

Circuit conditions that cause more than 25µA to flow in R_2 will not cause damage, but may produce more nonlinearity.

INA327 ENABLE FUNCTION

The INA327 adds an enable/shutdown function to the INA326. Its pinout differs from the INA326—see the Pin Configuration for detail.

The INA327 can be enabled by applying a logic HIGH voltage level to the Enable pin. Conversely, a logic LOW voltage level will disable the amplifier, reducing its supply current from 2.4mA to typically 2µA. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. This pin should be connected to a valid high or low voltage or driven, not left open circuit. The Enable pin can be modeled as a CMOS input gate as in Figure 2.

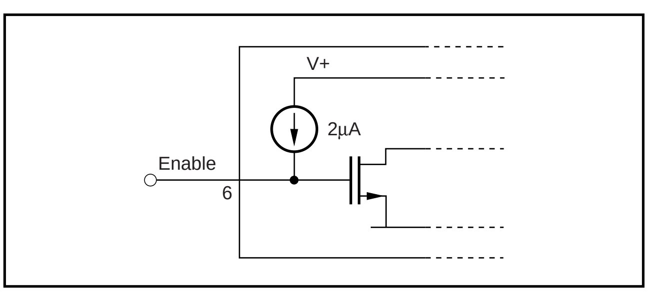


FIGURE 2. Enable Pin Model.

The enable time following shutdown is 75µs plus the settling time due to filters (see Typical Characteristics, "Input Offset Voltage vs Warm-up Time"). Disable time is 100µs. This allows the INA327 to be operated as a "gated" amplifier, or to have its output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

INA327 PIN 5

Pin 5 of the INA327 should be connected to V+ to ensure proper operation.

DYNAMIC PERFORMANCE

The typical characteristic "Gain vs Frequency" shows that the INA326 has nearly constant bandwidth regardless of gain. This results from the bandwidth limiting from the recommended filters.

NOISE PERFORMANCE

Internal auto-correction circuitry eliminates virtually all 1/f noise (noise that increases at low frequency) in gains of 100 or greater. Noise performance is affected by gain-setting resistor values. Follow recommendations in the "Setting Gain" section for best performance.

Total noise is a combination of input stage noise and output stage noise. When referred to the input, the total mid-band noise is:

$$V_N = 33nV/\sqrt{Hz} + \frac{800nV/\sqrt{Hz}}{G} \quad (5)$$

The output noise has some 1/f components that affect performance in gains less than 10. See typical characteristic "Input-Referred Voltage Noise vs Frequency."

High-frequency noise is created by internal auto-correction circuitry and is highly dependent on the filter characteristics chosen. This may be the dominant source of noise visible when viewing the output on an oscilloscope. Low cutoff frequency filters will provide lowest noise. Figure 3 shows the typical noise performance as a function of cutoff frequency.

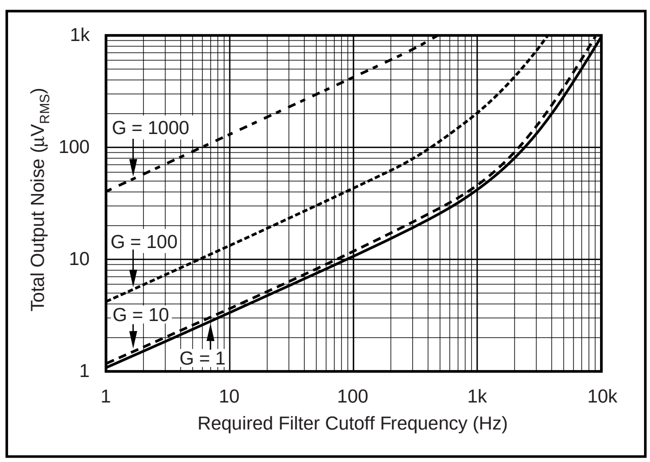


FIGURE 3. Total Output Noise vs Required Filter Cutoff Frequency.

Applications sensitive to the spectral characteristics of high-frequency noise may require consideration of the spurious frequencies generated by internal clocking circuitry. “Spurs” occur at approximately 90kHz and its harmonics (see typical characteristic “Input-Referred Ripple Spectrum”) which may be reduced by additional filtering below 1kHz.

Insufficient filtering at pin 5 can cause nonlinearity with large output voltage swings (very near the supply rails). Noise must be sufficiently filtered at pin 5 so that noise peaks do not “hit the rail” and change the average value of the signal. Figure 3 shows guidelines for filter cutoff frequency.

HIGH-FREQUENCY NOISE

C_2 and C_O form filters to reduce internally generated auto-correction circuitry noise. Filter frequencies can be chosen to optimize the trade-off between noise and frequency response of the application, as shown in Figure 3. The cutoff frequencies of the filters are generally set to the same frequency. Figure 3 shows the typical output noise for four gains as a function of the –3dB cutoff frequency of each filter response. Small signals may exhibit the addition of internally generated auto-correction circuitry noise at the output. This noise, combined with broadband noise, becomes most evident in higher gains with filters of wider bandwidth.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA326 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±0.2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 4 shows provision for an input bias current path in a thermocouple application. Without a bias current path, the inputs will float to an undefined potential and the output voltage may not be valid.

INPUT COMMON-MODE RANGE

Common instrumentation amplifiers do not respond linearly with common-mode signals near the power-supply rails, even if “rail-to-rail” op amps are used. The INA326 uses a unique topology to achieve true rail-to-rail input behavior (see Figure 5, “Inside the INA326”). The linear input voltage range of each input terminal extends to 20mV below the negative rail, and 100mV above the positive rail.

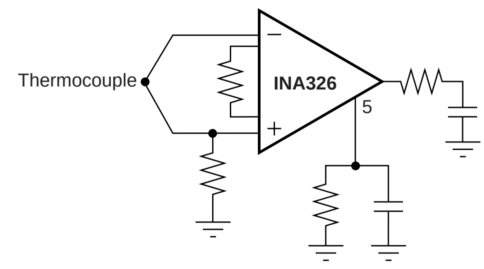


FIGURE 4. Providing Input Bias Current Return Path.

INPUT PROTECTION

The inputs of the INA326 are protected with internal diodes connected to the power-supply rails. These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.5V, the input signal current should be limited to less than 10mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

FILTERING

Filtering can be adjusted through selection of R_2C_2 and R_OC_O for the desired trade-off of noise and bandwidth. Adjustment of these components will result in more or less ripple due to auto-correction circuitry noise and will also affect broadband noise. Filtering limits slew rate, settling time, and output overload recovery time.

It is generally desirable to keep the resistance of R_O relatively low to avoid DC gain error created by the subsequent stage loading. This may result in relatively high values for C_O to produce the desired filter response. The impedance of R_OC_O can be scaled higher to produce smaller capacitor values if the load impedance is very high.

Certain capacitor types greater than 0.1µF may have dielectric absorption effects that can significantly increase settling time in high-accuracy applications (settling to 0.01%). Polypropylene, polystyrene, and polycarbonate types are generally good. Certain “high-K” ceramic types may produce slow settling “tails.” Settling time to 0.1% is not generally affected by high-K ceramic capacitors. Electrolytic types are not recommended for C_2 and C_O.

INSIDE THE INA326

The INA326 uses a new, unique internal circuit topology that provides true rail-to-rail input. Unlike other instrumentation amplifiers, it can linearly process inputs up to 20mV below the negative power-supply rail, and 100mV above the positive power-supply rail. Conventional instrumentation amplifier circuits cannot deliver such performance, even if rail-to-rail op amps are used.

The ability to reject common-mode signals is derived in most instrumentation amplifiers through a combination of amplifier CMR and accurately matched resistor ratios. The INA326 converts the input voltage to a current. Current-mode signal processing provides rejection of common-mode input voltage and power-supply variation without accurately matched resistors.

A simplified diagram shows the basic circuit function. The differential input voltage, (V_{IN+}) – (V_{IN-}) is applied across R_1. The signal-generated current through R_1 comes from A1 and A2's output stages. A2 combines the current in R_1 with a mirrored replica of the current from A1. The resulting current in A2's output and associated current mirror is two times the current in R_1. This current flows in (or out) of pin 5 into R_2. The resulting gain equation is:

$$G = 2\frac{R_2}{R_1}$$

Amplifiers A1, A2, and their associated mirrors are powered from internal charge-pumps that provide voltage supplies that are beyond the positive and negative supply rails. As a result, the voltage developed on R_2 can actually swing 20mV *below* the negative power-supply rail, and 100mV *above* the positive supply rail. A3 provides a buffered output of the voltage on R_2. A3's input stage is also operated from the charge-pumped power supplies for true rail-to-rail operation.

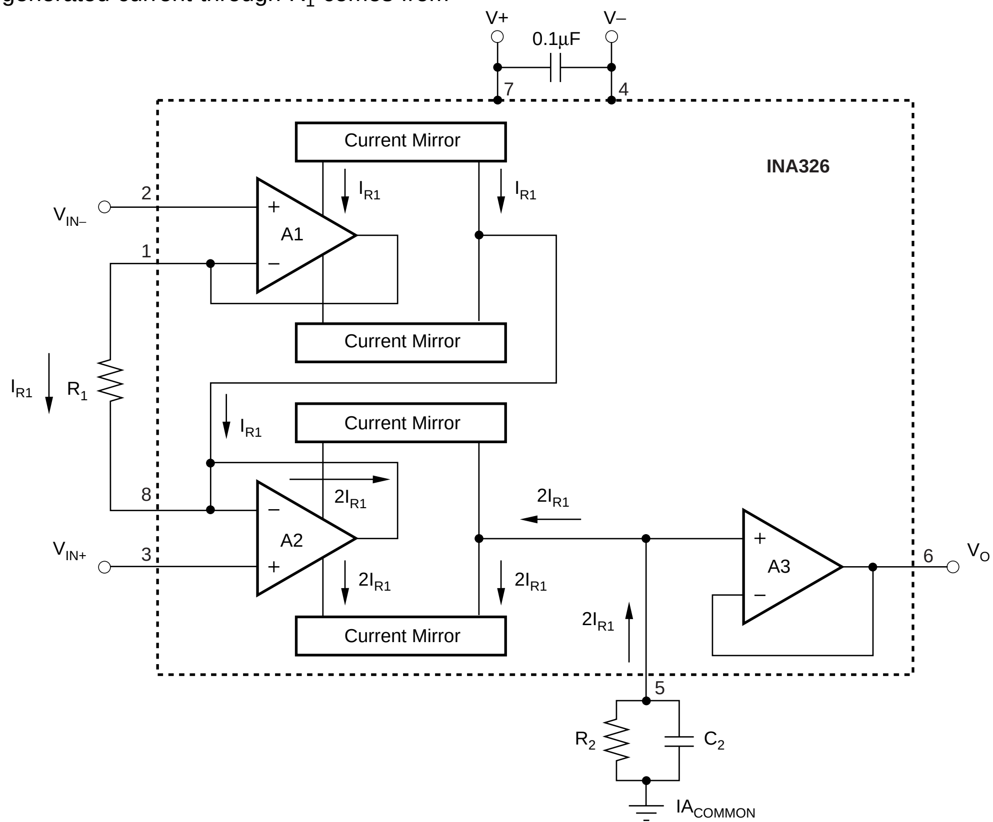


FIGURE 5. Simplified Circuit Diagram.

APPLICATION CIRCUITS

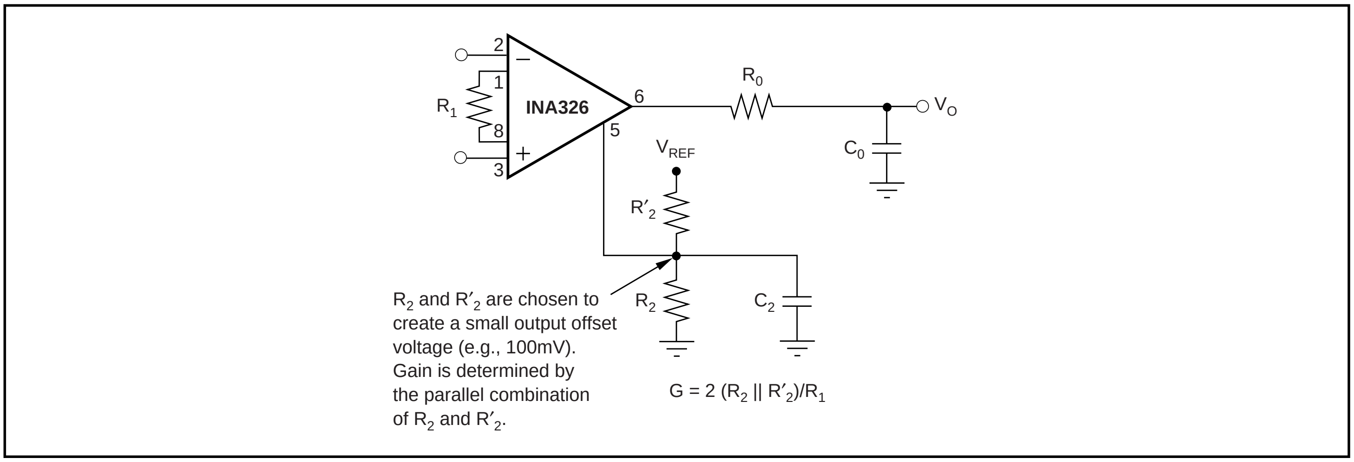


FIGURE 6. Generating Output Offset Voltage.

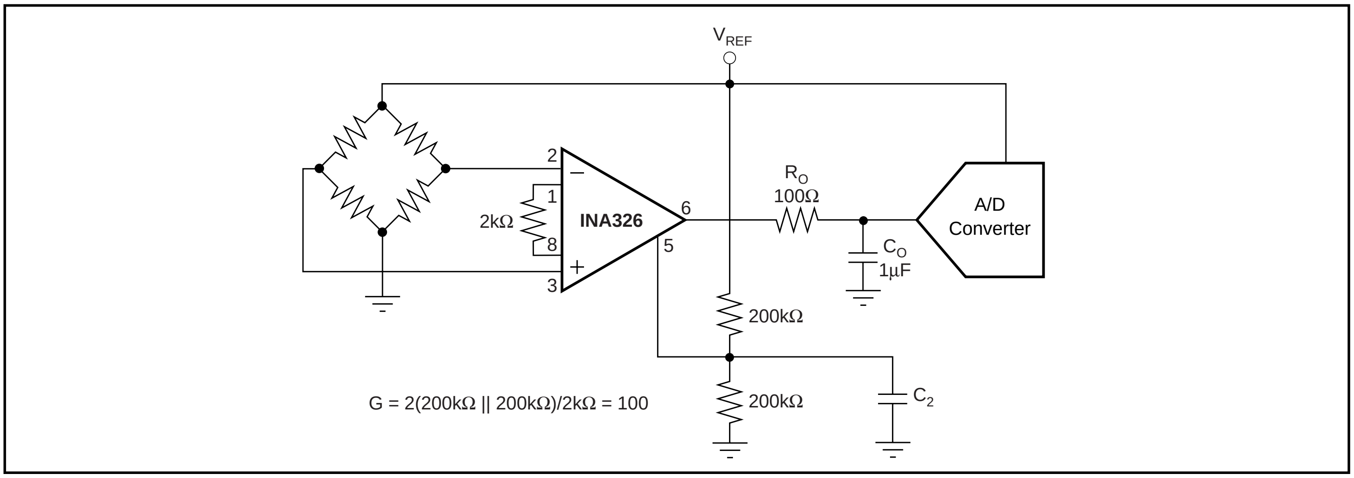


FIGURE 7. Output Referenced to $V_{REF}/2$.

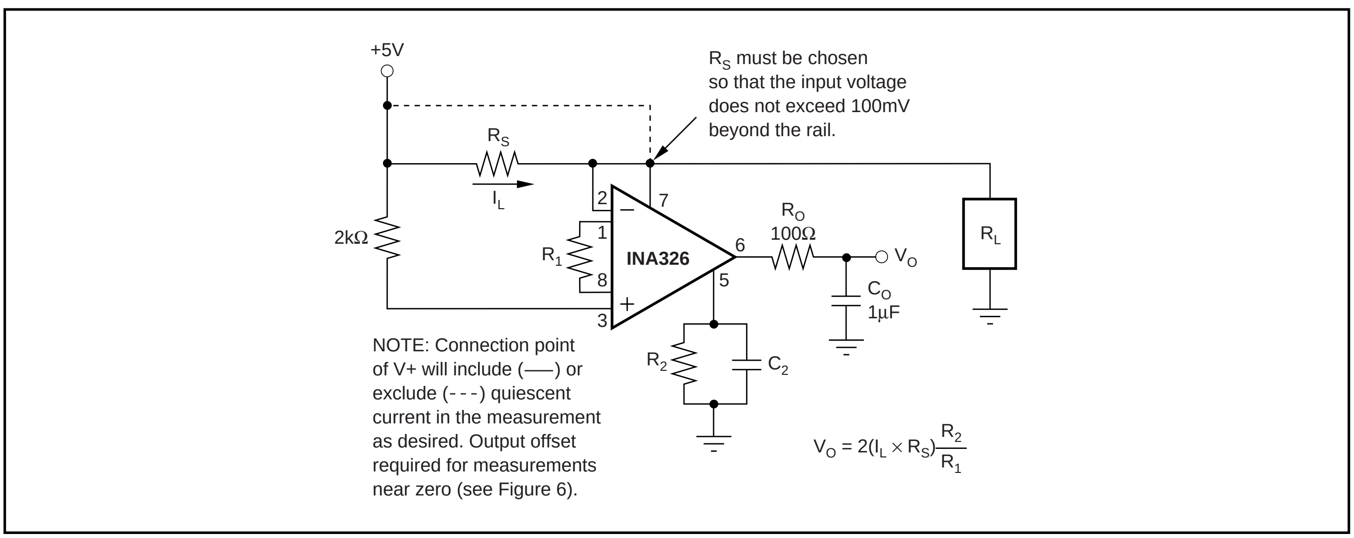


FIGURE 8. High-Side Current Shunt Measurement.

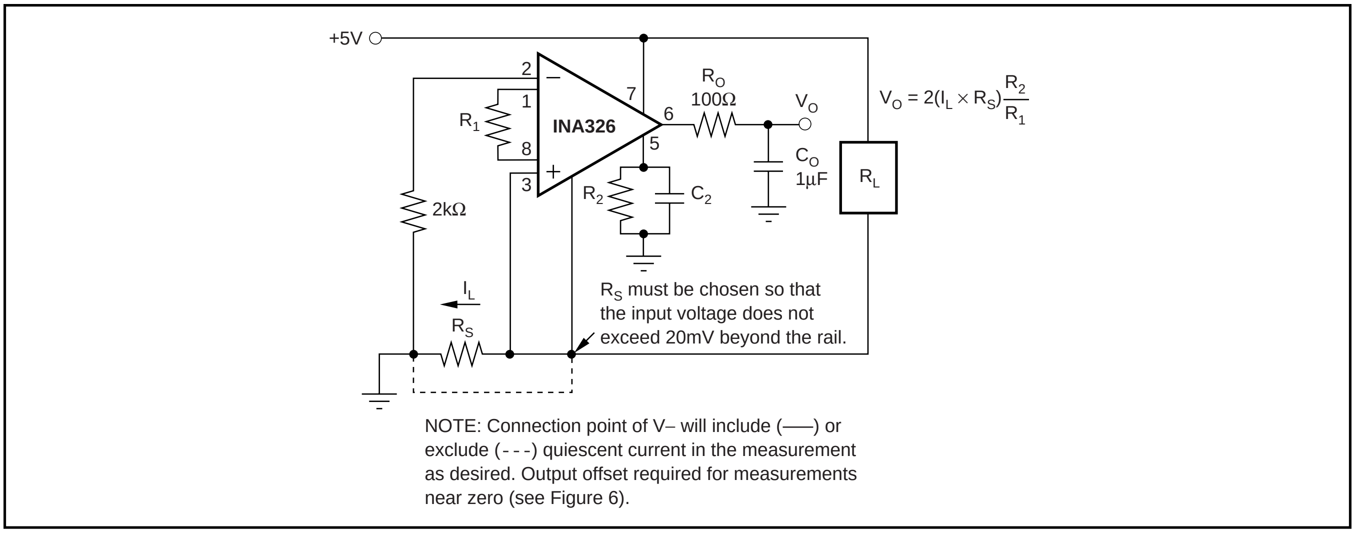


FIGURE 9. Low-Side Current Shunt Measurement.

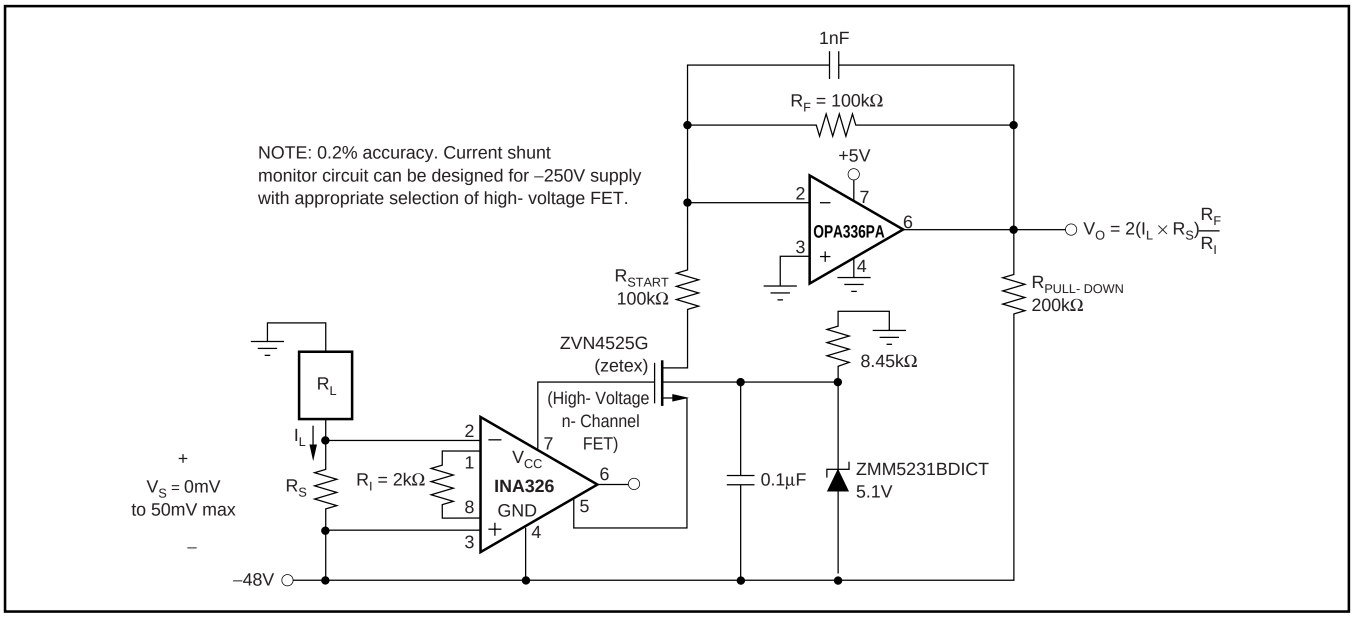


FIGURE 10. Low-Side –48V Current Shunt Monitor.

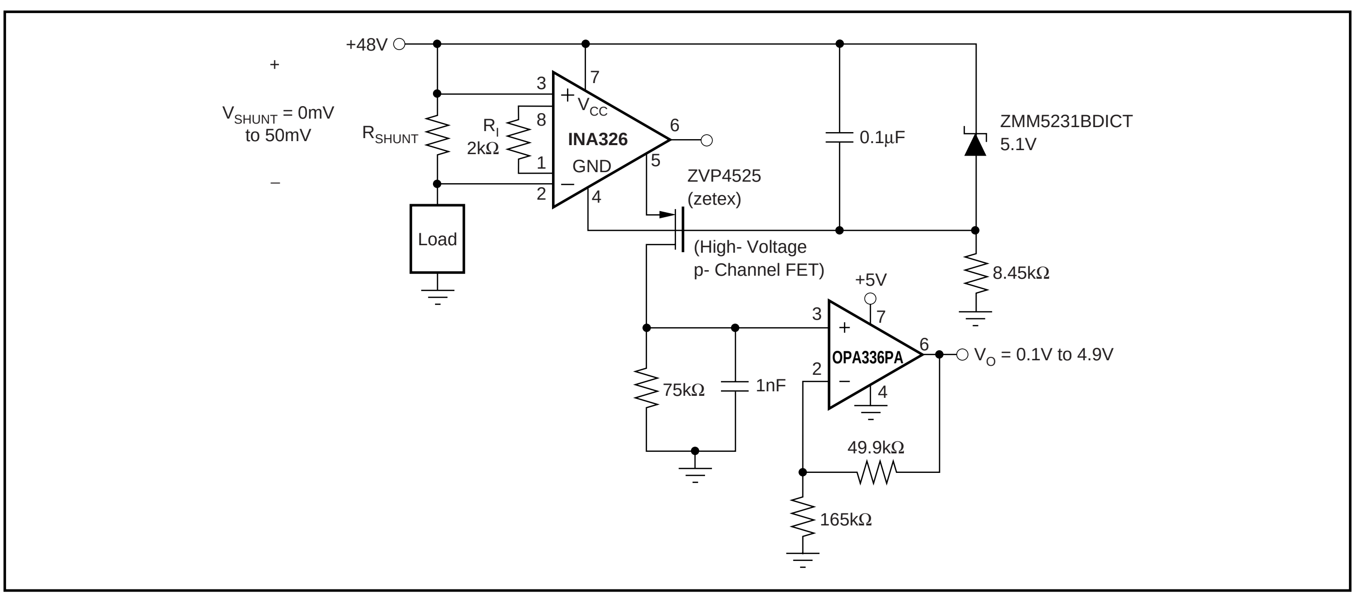


FIGURE 11. High-Side +48V Current Shunt Monitor.

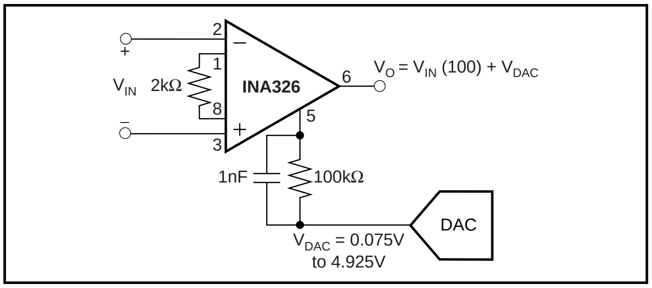


FIGURE 12. Output Offset Adjustment.

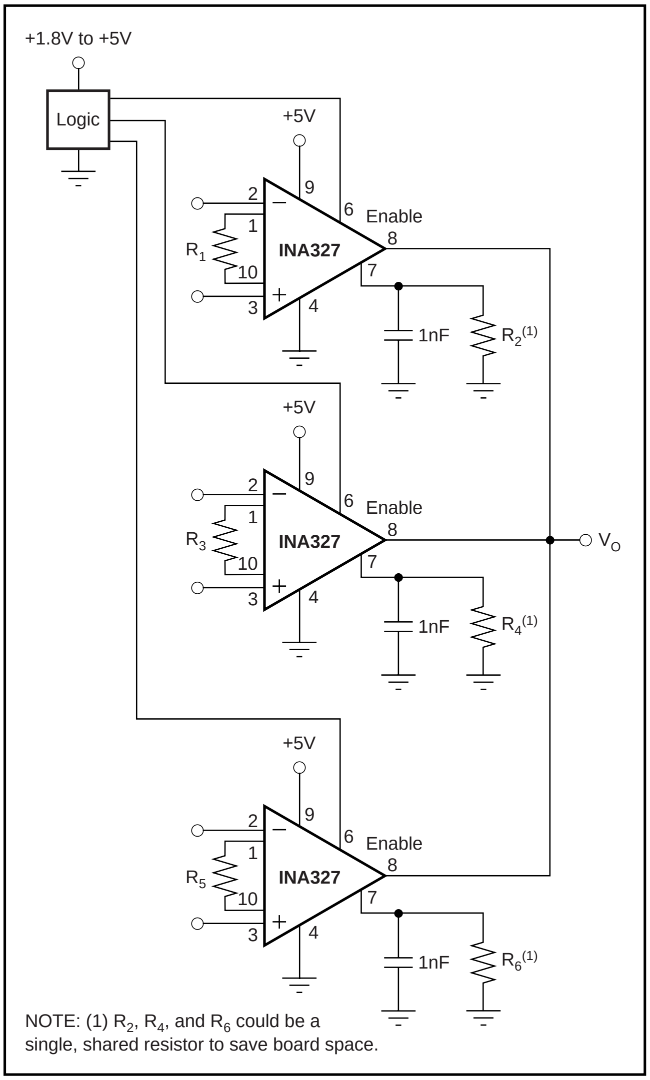


FIGURE 13. Multiplexed Output.

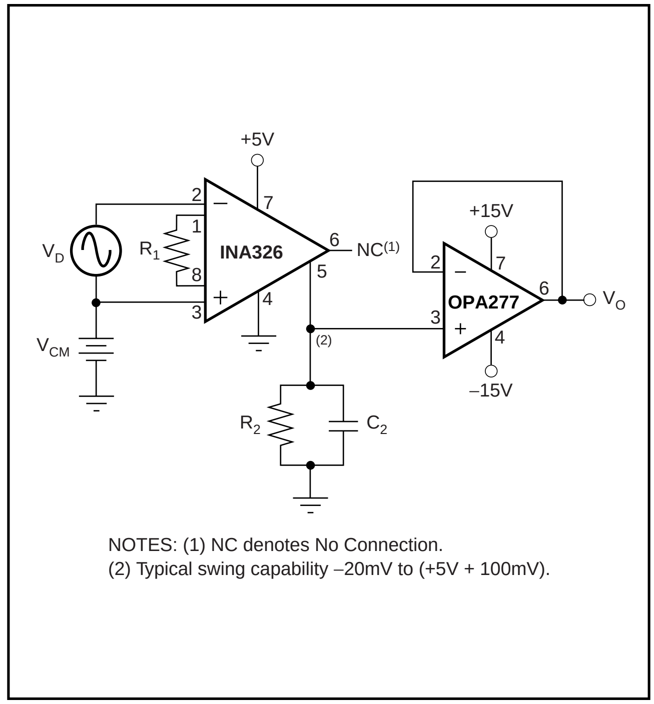


FIGURE 14. Output from Pin 5 to Allow Swing Beyond the Rail.

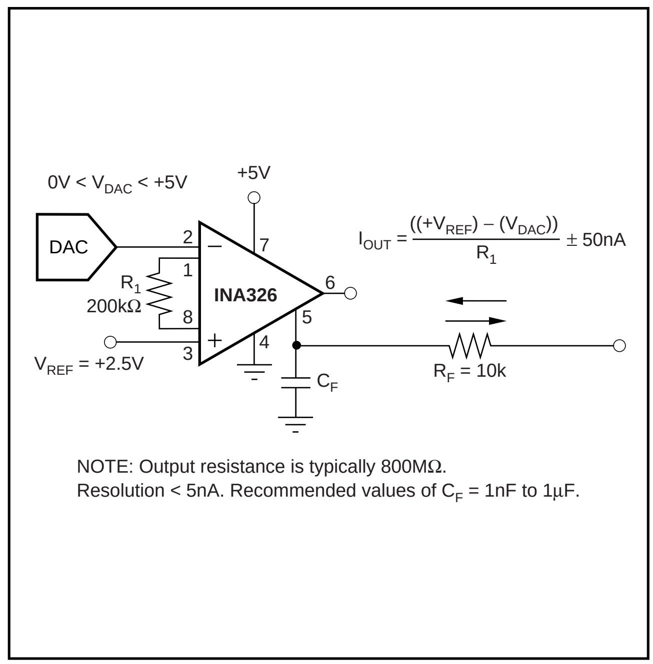


FIGURE 15. Programmable ±25µA Current Source with High Output Resistance.

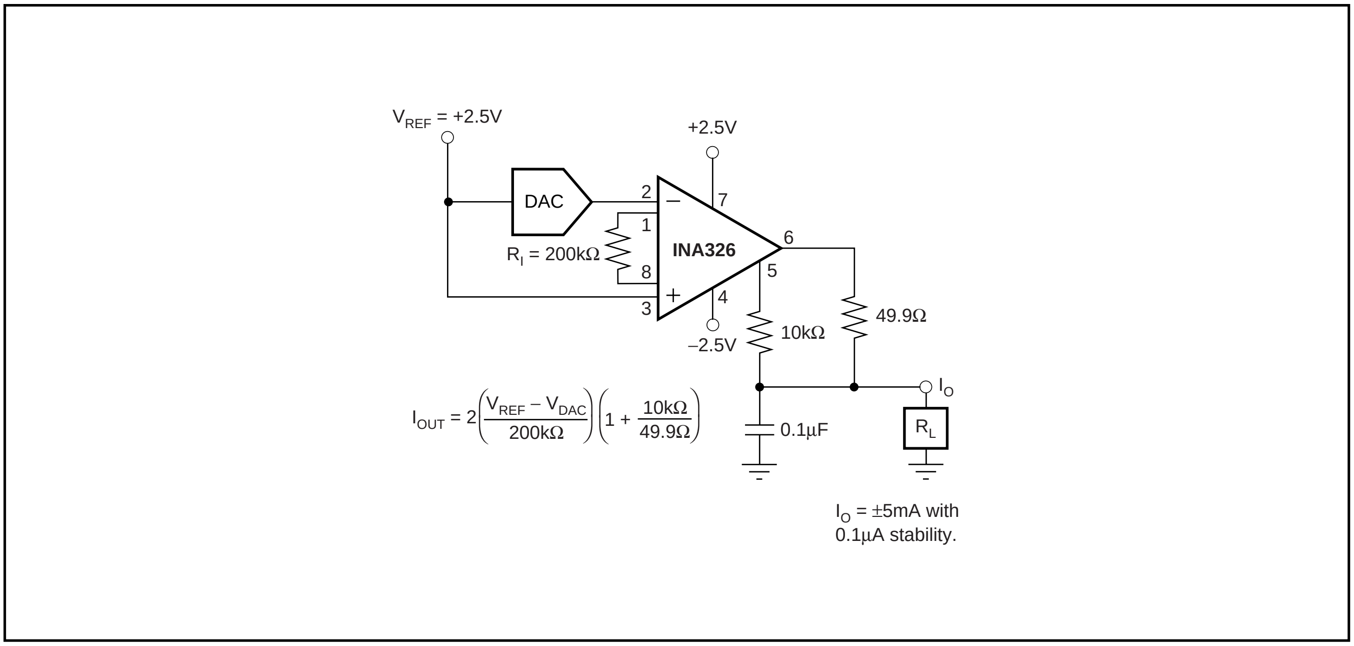


FIGURE 16. Programmable ±5mA Current Source.

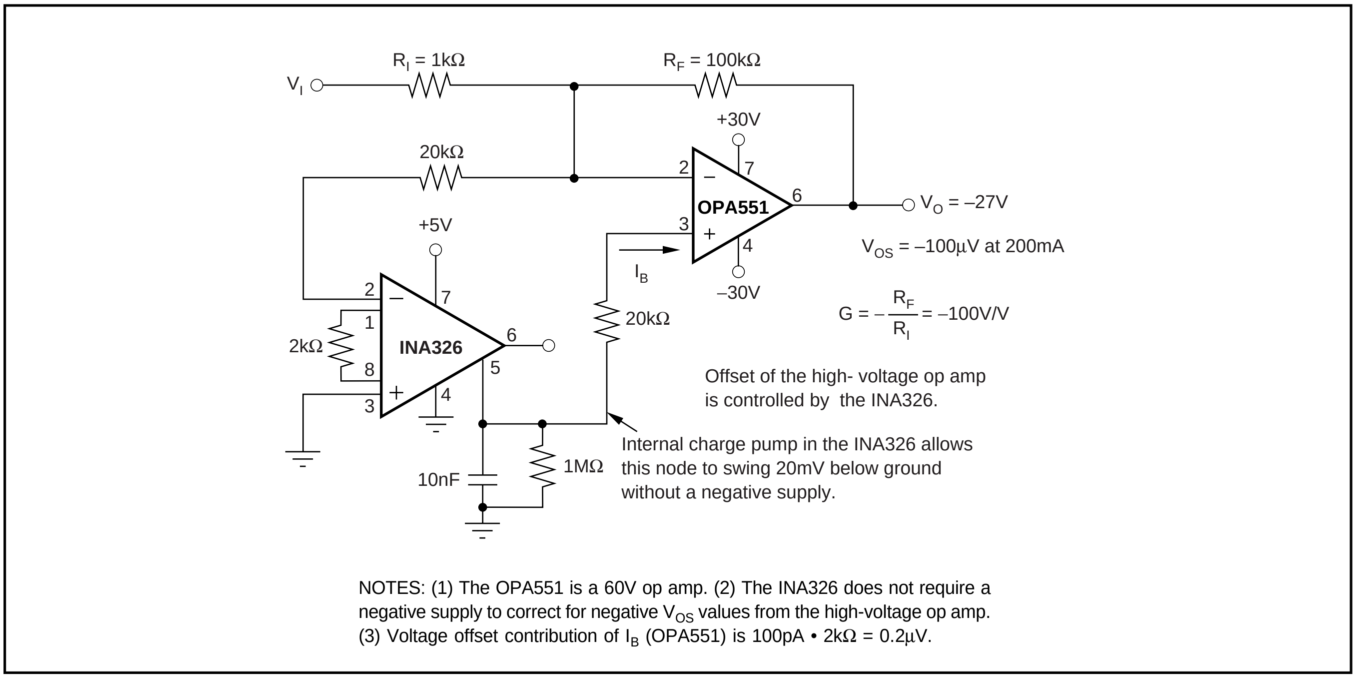


FIGURE 17. ±27V Output at 200mA Amplifier with 100µV Offset.

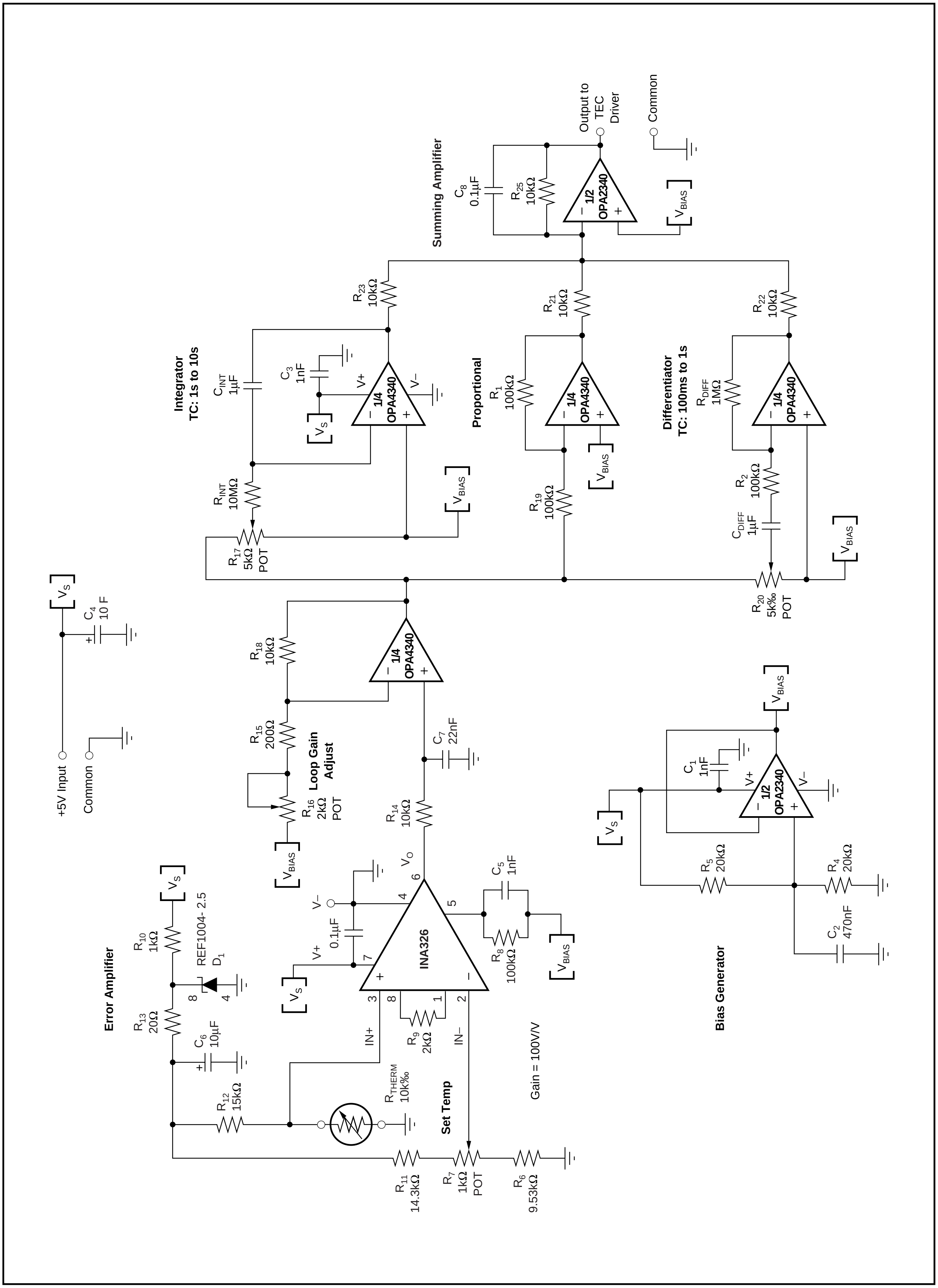


FIGURE 18. Single-Supply PID Temperature Control Loop.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA326EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	B26	Samples
INA326EA/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	B26	Samples
INA326EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	B26	Samples
INA327EA/250	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B27	Samples
INA327EA/250G4	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	B27	Samples
INA327EA/2K5	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B27	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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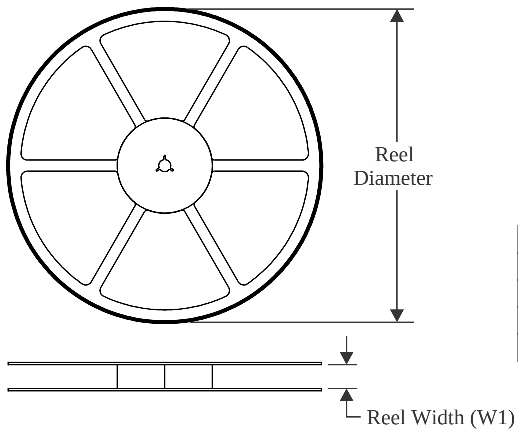
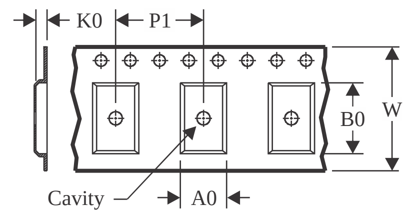
TAPE AND REEL INFORMATION

REEL DIMENSIONS

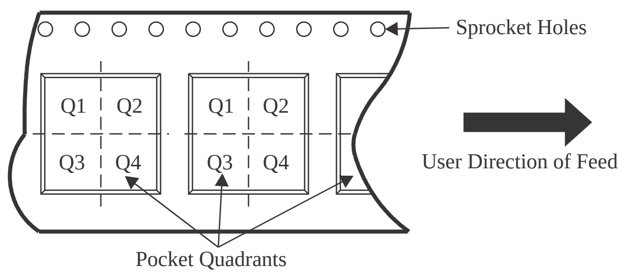


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

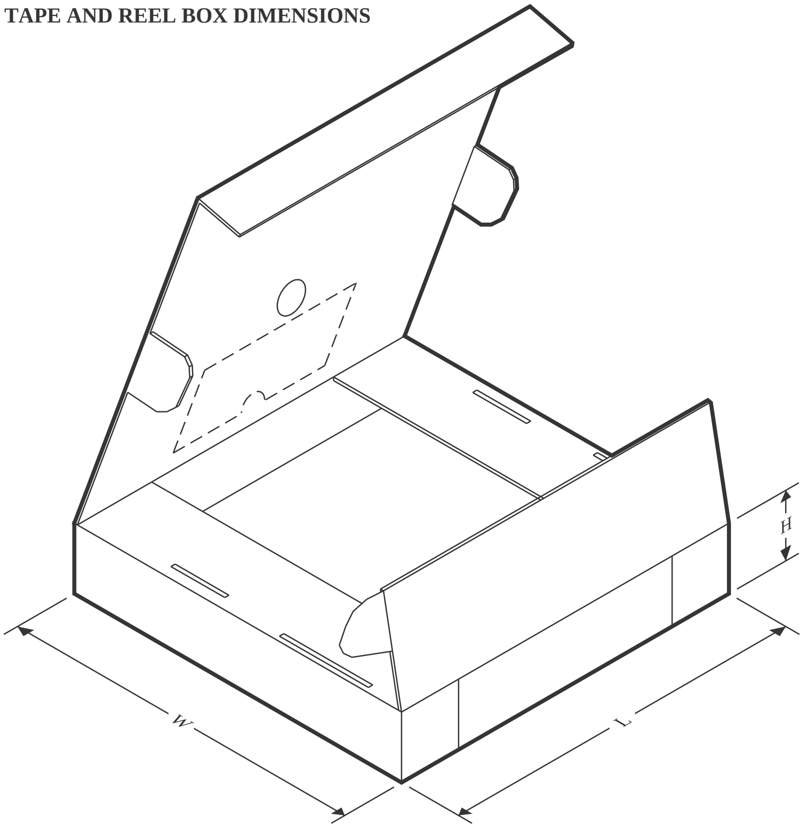
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

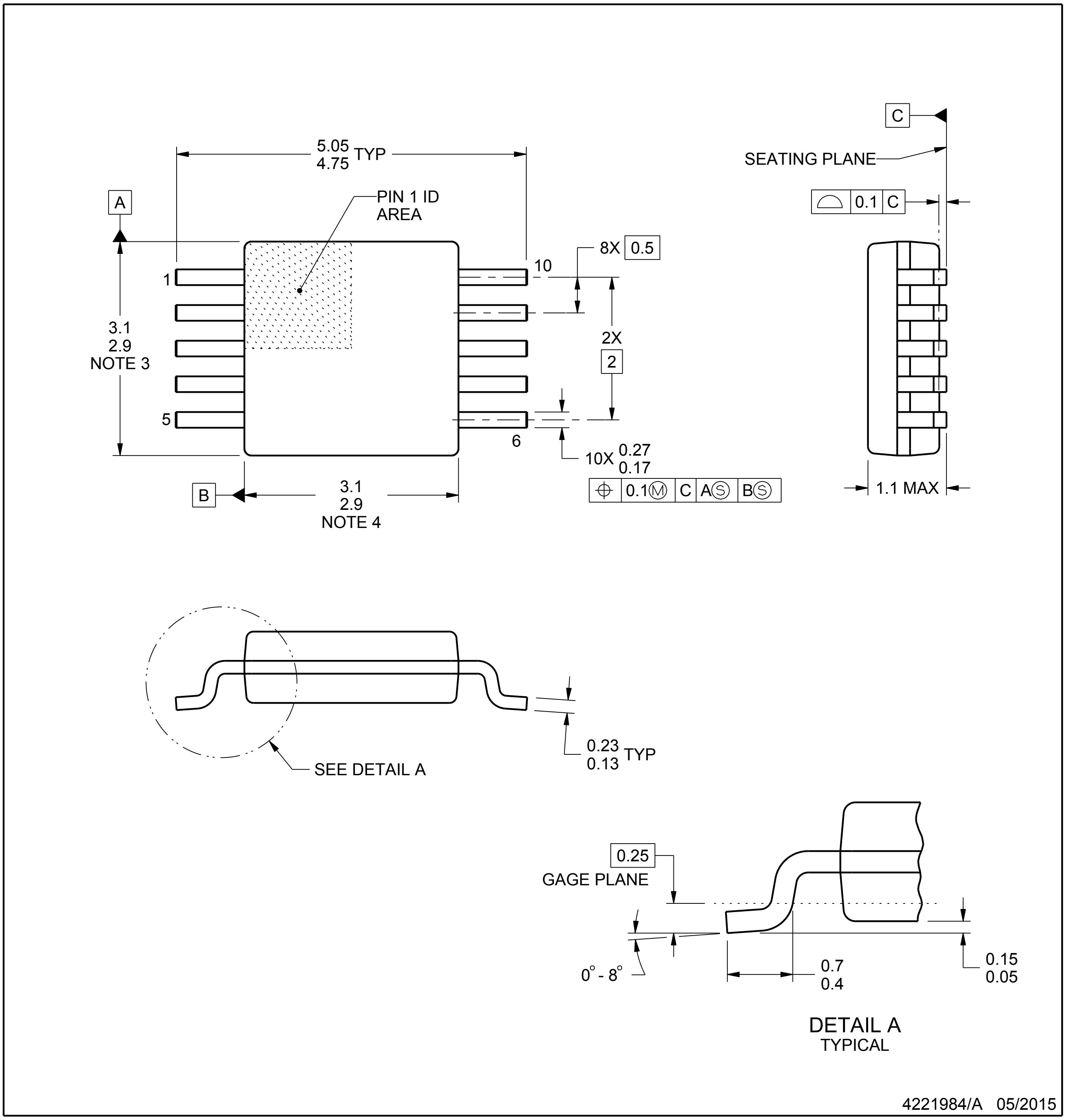
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA326EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA326EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



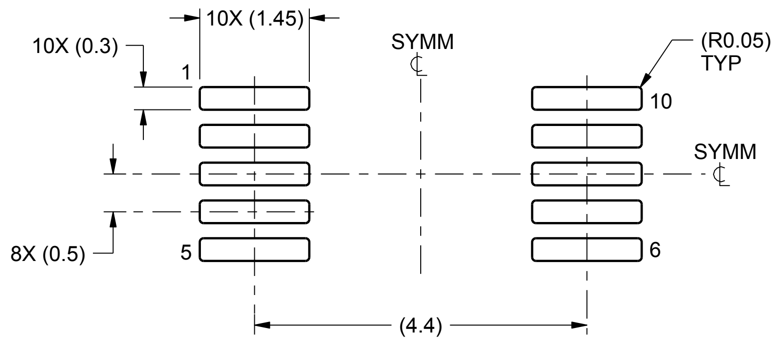
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA326EA/250	VSSOP	DGK	8	250	366.0	364.0	50.0
INA326EA/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0

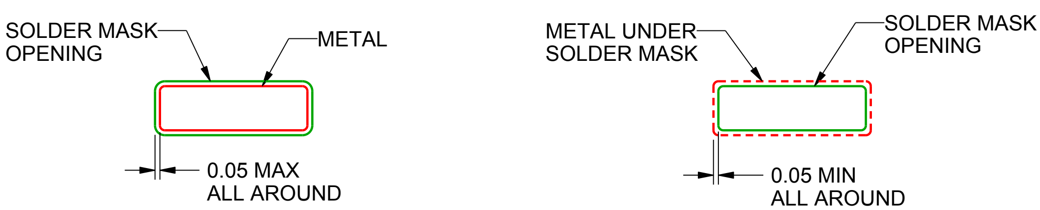


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

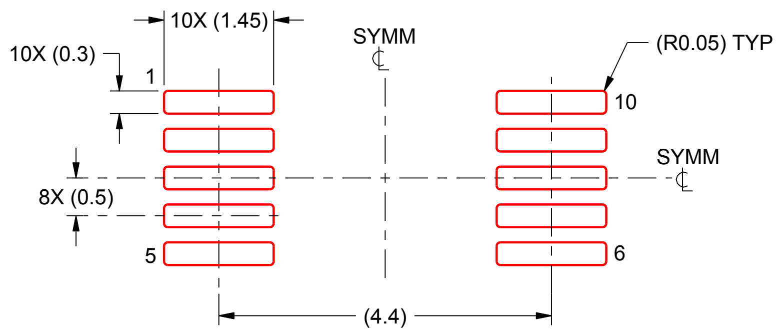
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



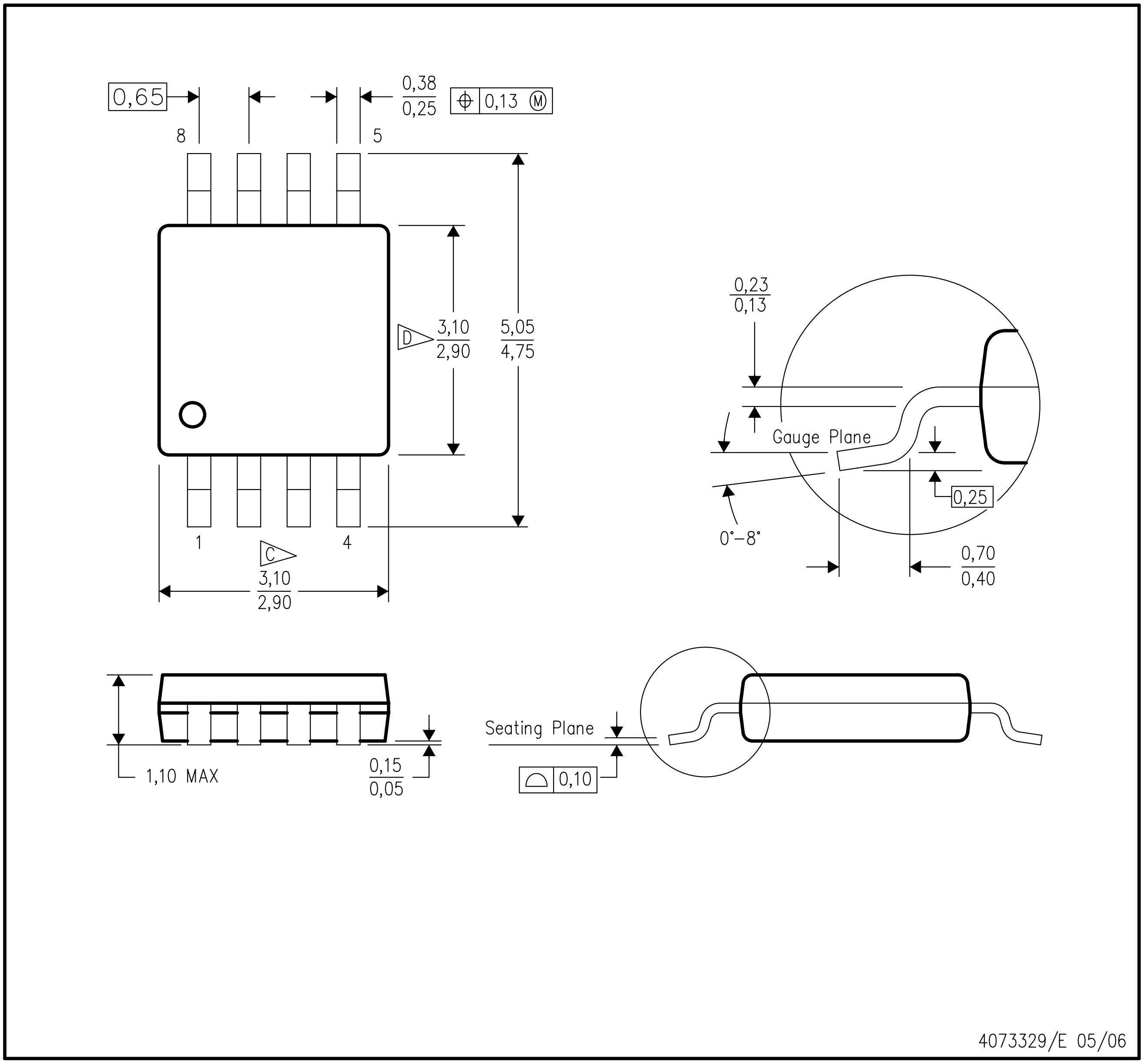
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

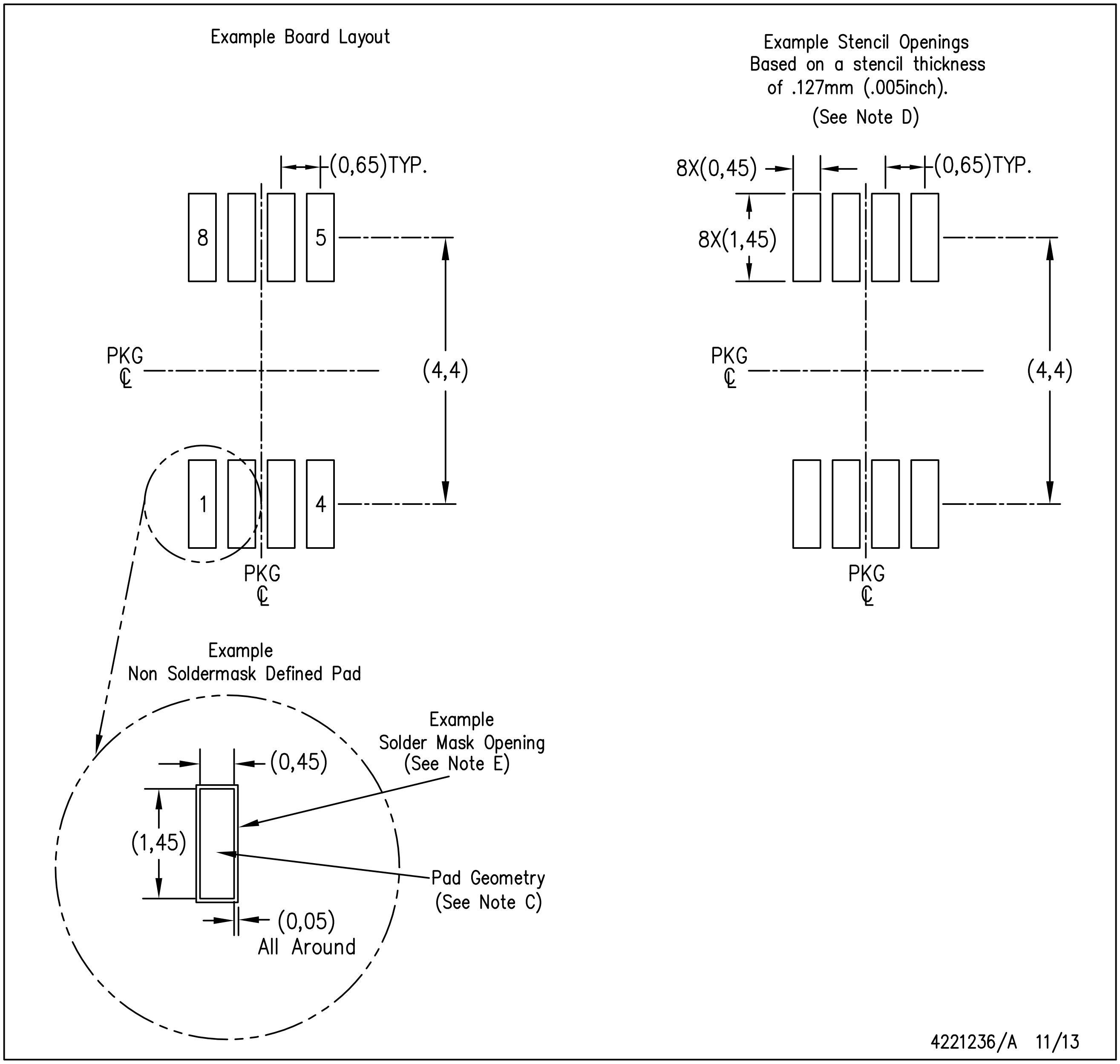
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.