INA901-SP Radiation Hardened, –15-V to 65-V Common Mode, Unidirectional Current-Shunt Monitor

1 Features

- 5962-1821001
  - Radiation Hardness Assured (RHA) 50 krad(Si) at Low Dose Rate
  - Single Event Latch-up (SEL) Immune to 75 MeV-cm^2/mg at 125 °C
    - See Radiation Reports
  - Qualified Over the Military Temperature Range (–55 °C to 125 °C)
  - High-Performance 8-Pin Ceramic Flat Pack Package (HKX)
- Wide Common-Mode Range: –15 V to 65 V
- CMRR: 120 dB
- Accuracy:
  - ±0.5-mV Offset
  - ±0.2% Gain Error
  - 2.5-µV/°C Offset Drift
  - 50-ppm/°C Gain Drift
- Bandwidth: Up to 130 kHz
- Gain: 20 V/V
- Quiescent Current: 700 µA
- Power Supply: 2.7 V to 16 V
- Provision for Filtering

2 Applications

- Power Supervision
- Overcurrent and Undercurrent Detection
- Satellites Telemetry
- Space Signal Conditioning
- Motor Control Loops

3 Description

The INA901-SP is a voltage-output, current-sense amplifier that can sense drops across shunt resistors at common-mode voltages from –15 V to 65 V, independent of the supply voltage. The INA901-SP operates from a single 2.7-V to 16-V supply, drawing 700 µA (typical) of supply current.

The gain of the INA901-SP is 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops. The pinouts readily enable filtering.

The device is specified over the extended operating temperature range of –55 °C to 125 °C and is offered in an 8-pin CFP package.

Device Information(1)

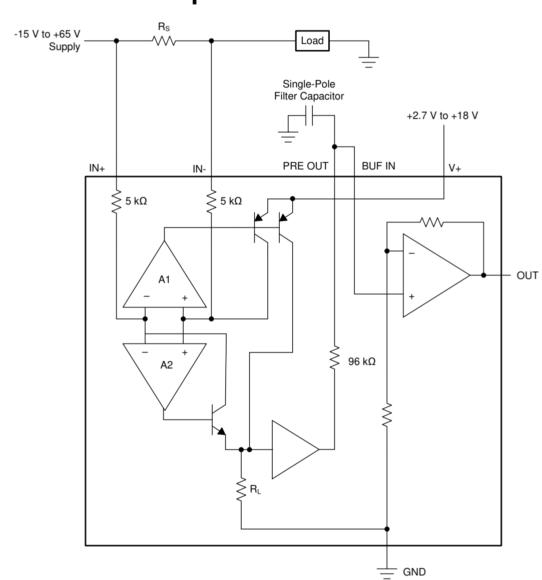
PART NUMBER	GRADE	PACKAGE
5962L1821001VXC	QMLV RHA [50 krad(Si)]	8-lead CFP [HKX] 6.48 × 6.48 mm Weight: 0.39 g(3)
5962-1821001VXC	QMLV	
INA901HKX/EM	Engineering Samples(2)	
INA901EVM-CVAL	Ceramic Evaluation Board	—

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55 °C to 125 °C or operating life.

(3) Weight is accurate to ±10%.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

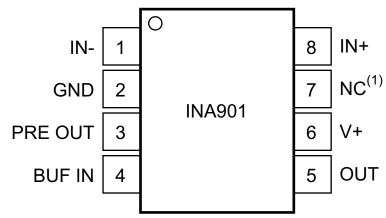
Changes from Revision B (December 2018) to Revision C — **Page**

- Changed Radiation Hardness Assured (RHA) at the low dose rate from: 100 krad(Si) to: 50 krad(Si)... 1
- Changed Single Event Latch-up (SEL) immunity at 125 °C from: 93 MeV-cm^2/mg to: 75 MeV-cm^2/mg... 1
- Changed common-mode input voltage maximum from: 80 V to: 65 V ... 1
- Changed recommended V_{CM} minimum from: –16 V to: –15 V throughout data sheet... 5
- Removed C_{LOAD} = 1000 pF text condition from the *Gain vs Frequency* graph ... 7

Changes from Revision A (December 2018) to Revision B — **Page**

- Changed the device status from *Advance Information* to *Production Data*... 1

5 Pin Configuration and Functions



NOTE (1): NC denotes no internal connection.

Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NAME	NO.			
BUF IN	4	I	A	Connect to output of filter from PRE OUT.
GND	2	—	GND	Ground.
IN–	1	I	A	Connect to load side of shunt resistor.
IN+	8	I	A	Connect to supply side of shunt resistor.
NC	7	—	—	Recommend connect to ground.
OUT	5	O	A	Output voltage.
PRE OUT	3	O	A	Connect to input of filter to BUF IN.
V+	6	—	P	Power supply, 2.7 V to 18 V.

(1) A = analog, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage (V_S)			18	V
Analog inputs, V_{IN+}, $V_{IN–}$	Differential, (V_{IN+}) – ($V_{IN–}$)	–18	18	V
	Common-mode	–16	65	
Analog output: OUT and PRE OUT pins		GND – 0.3	(V+) + 0.3	V
Input current into any pin			5	mA
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CM}	Common-mode input voltage	–15	65	V
V_S	Operating supply voltage	2.7	16	V
T_A	Operating free-air temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA901-SP HKX (CFP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	26.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_S = 2.7 V and 16 V, V_{CM} = –15 V, 12 V and 65 V, V_{SENSE} = 100 mV, and PRE OUT connected to BUF IN, unless otherwise noted. T_A is as shown in SUBGROUP column.

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
INPUT							
V_{SENSE}	Full-scale input voltage	$V_{SENSE} = (V_{IN+}) – (V_{IN–})$	[1, 2, 3]		0.15	(V_S – 0.2) / Gain	V
V_{CM}	Common-mode input range		[1, 2, 3]	–15		65	V
CMRR	Common-mode rejection ratio	V_{IN+} = –15 V to 65 V	[1]	80	120		dB
			[2, 3]	70	120		
V_{OS}	Offset voltage, RTI		[1]		±0.5	±2.5	mV
			[2, 3]			±3.5	
dV_{OS}/dT					2.5		µV/°C
PSR	V_{OS} vs power-supply		[1, 2, 3]		5	250	µV/V
I_B	Input bias current, $V_{IN–}$ pin		[1]		±8	±16	µA
			[2, 3]			±19	
	PRE OUT output impedance				96		kΩ
	Buffer input bias current				–50		nA
	Buffer input bias current temperature coefficient				±0.03		nA/°C
OUTPUT (V_{SENSE} ≥ 20 mV)(2)							
G	Gain				20		V/V
G_{BUF}	Output buffer gain				2		V/V
	Total gain error	V_{SENSE} = 20 mV to 100 mV	[4, 5, 6]		±0.2%	±1.5%	
	Total gain error vs temperature	T_A = –55 °C to 125 °C			50		ppm/°C
	Total output error(3)		[4]		±0.75%	±2%	
			[5, 6]			±3%	
	Nonlinearity error	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance, pin 5				1.5		Ω
	Maximum capacitive load	No sustained oscillation			10		nF
VOLTAGE OUTPUT (R_L = 10 kΩ to GND)							
	Swing to V+ power-supply rail		[1, 2, 3]		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND		[1, 2, 3]		V_{GND} + 0.003	V_{GND} + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 5 pF			130		kHz
	Phase margin	C_{LOAD} < 10 nF			40		°
SR	Slew rate				1		V/µs
t_S	Settling time (1%)	V_{SENSE} = 10 mV to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs

(1) For subgroup definitions, see the *Quality Conformance Inspection* table.
(2) For output behavior when V_{SENSE} < 20 mV, see the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section.
(3) Total output error includes effects of gain error and V_{OS}.

Electrical Characteristics (continued)

V_S = 2.7 V and 16 V, V_{CM} = –15 V, 12 V and 65 V, V_{SENSE} = 100 mV, and PRE OUT connected to BUF IN, unless otherwise noted. T_A is as shown in SUBGROUP column.

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
NOISE, RTI(4)							
e_n	Voltage noise density				40		nV/√Hz
POWER SUPPLY							
V_S	Operating range		[1, 2, 3]	2.7		16	V
I_Q	Quiescent current	V_{OUT} = 2 V	[1]		700	900	µA
			[2, 3]		700	1200	
		V_{SENSE} = 0 mV	[1]		350	500	
			[2, 3]		350	650	

(4) RTI means *Referred-to-Input*.

6.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55
12	Setting time at	25
13	Setting time at	125
14	Setting time at	–55

6.7 Typical Characteristics

At T_A = 25 °C, V_S = 12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

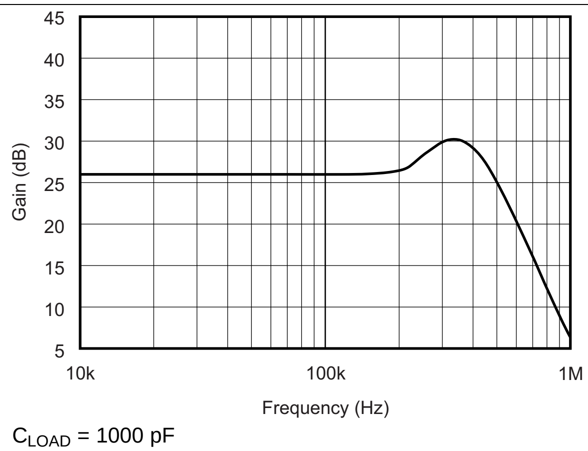


Figure 1. Gain vs Frequency

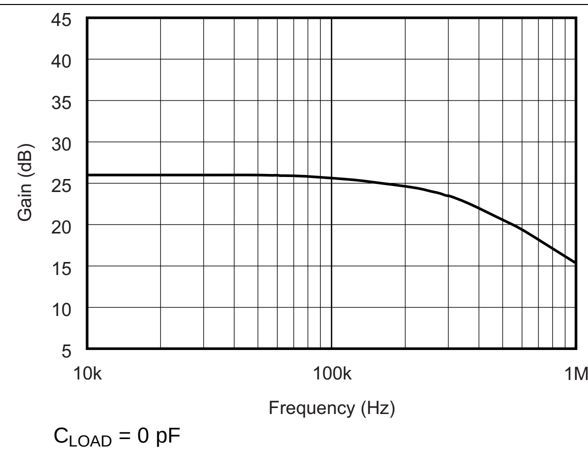


Figure 2. Gain vs Frequency

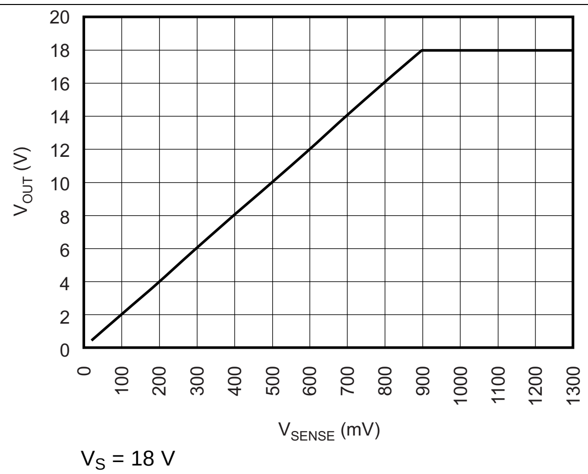


Figure 3. Gain Plot

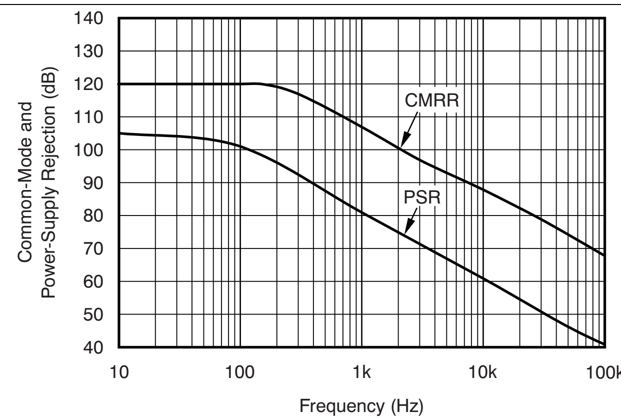


Figure 4. Common-Mode and Power-Supply Rejection vs Frequency

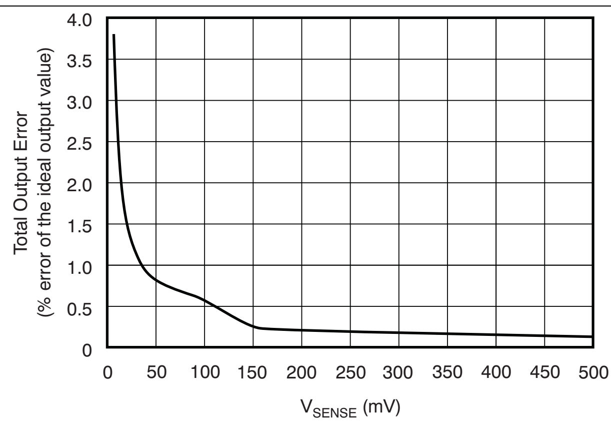


Figure 5. Total Output Error vs V_{SENSE}

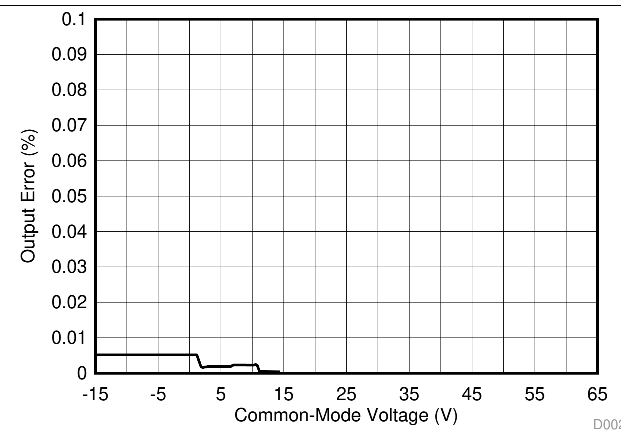


Figure 6. Output Error vs Common-Mode Voltage

Typical Characteristics (continued)

At T_A = 25 °C, V_S = 12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

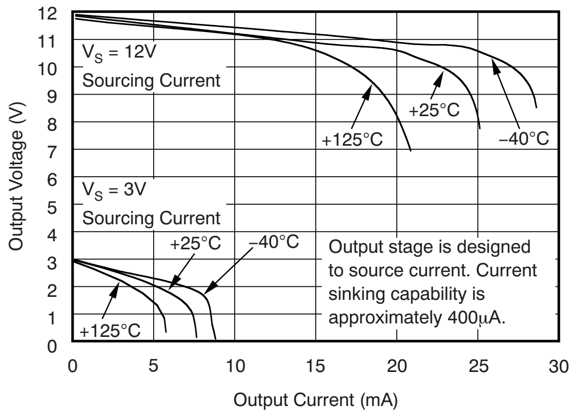


Figure 7. Positive Output Voltage Swing vs Output Current

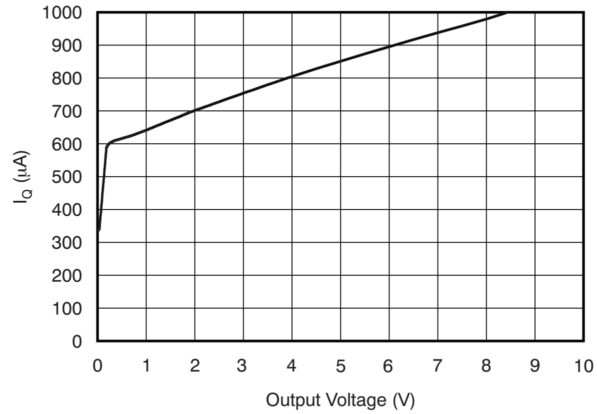


Figure 8. Quiescent Current vs Output Voltage

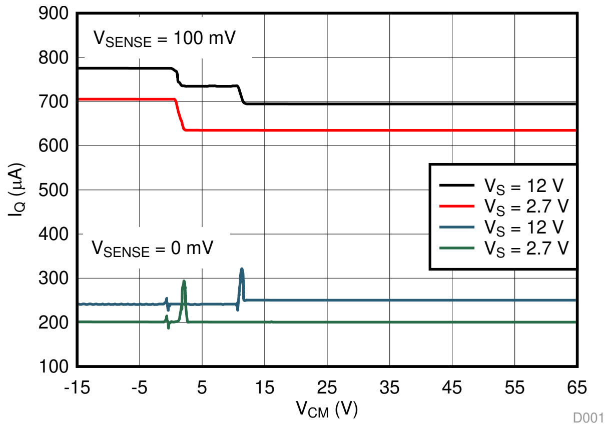


Figure 9. Quiescent Current vs Common-Mode Voltage

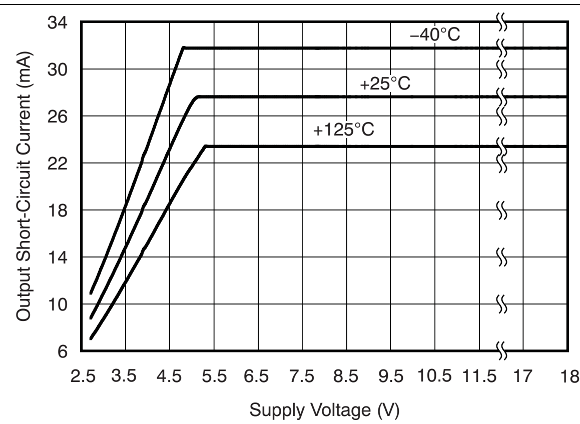


Figure 10. Output Short-Circuit Current vs Supply Voltage

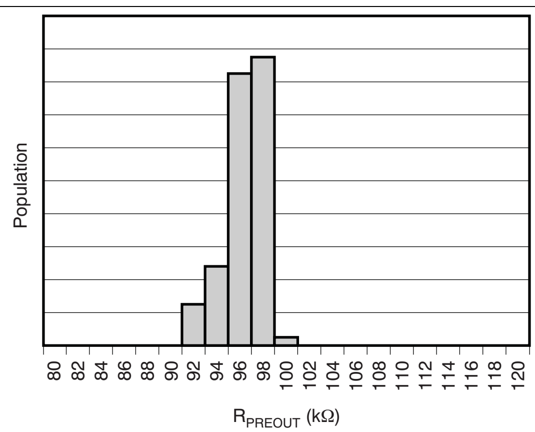


Figure 11. PRE OUT Output Resistance Production Distribution

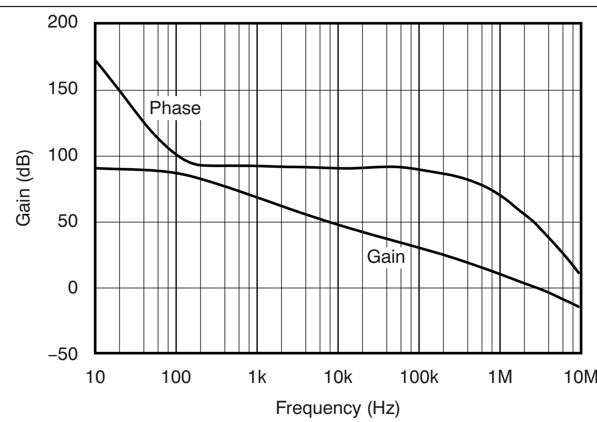


Figure 12. Buffer Gain vs Frequency

Typical Characteristics (continued)

At T_A = 25 °C, V_S = 12 V, V_{CM} = 12 V, and V_{SENSE} = 100 mV, unless otherwise noted.

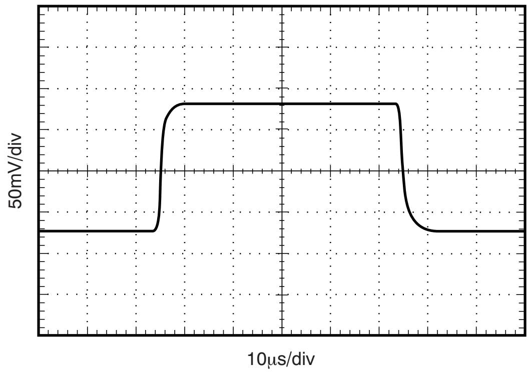


Figure 13. Small-Signal Step Response (10-mV to 20-mV Input)

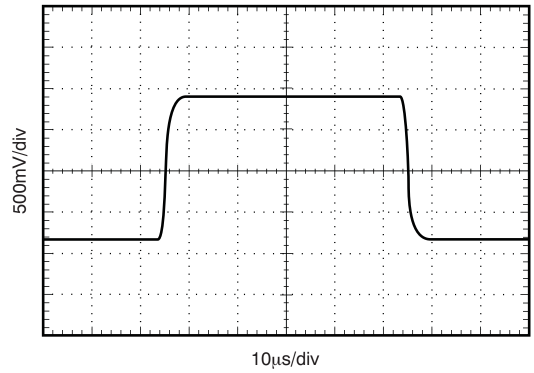


Figure 14. Large-Signal Step Response (10-mV to 100-mV Input)

7 Detailed Description

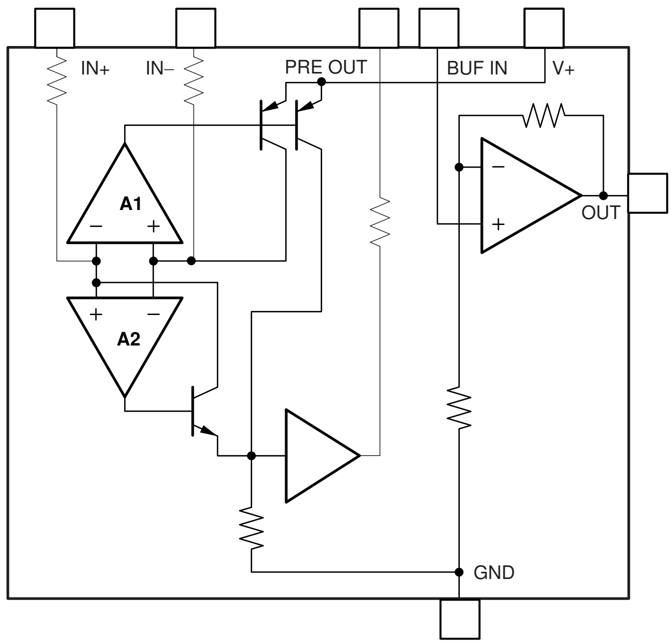
7.1 Overview

The INA901-SP current-shunt monitor with voltage output can sense drops across current shunts at common-mode voltages from –15 V to 65 V, independent of the supply voltage. The INA901-SP pinout readily enables filtering.

The INA901-SP is available with a 20-V/V output voltage scale. The 130-kHz bandwidth simplifies use in current-control loops.

The INA901-SP operates from a single 2.7-V to 18-V supply, drawing a maximum of 1200 μA of supply current. The device is specified over the extended operating temperature range of –55 °C to 125 °C and is offered in an 8-pin CFP package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connection

Figure 15 shows the basic connection of the INA901-SP. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Place minimum bypass capacitors of 0.01 µF and 0.1 µF in value close to the supply pins. Although not mandatory, an additional 10-mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

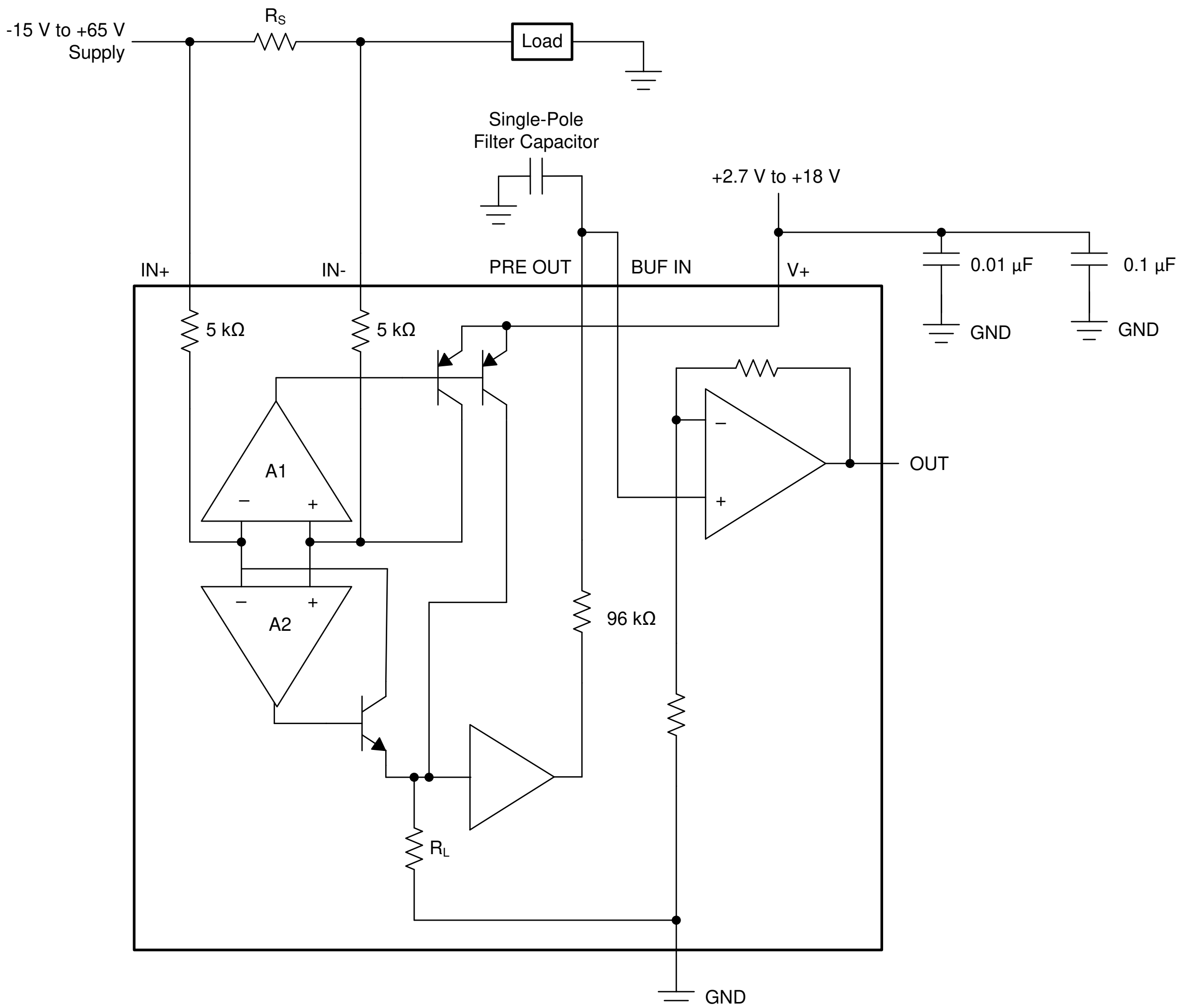


Figure 15. INA901-SP Basic Connections

7.3.2 Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_S – 0.2) / Gain.

Feature Description (continued)

7.3.3 Transient Protection

The –15-V to 65-V common-mode range of INA901-SP is ideal for withstanding fault conditions ranging from 12-V battery reversal up to 65-V transients because no additional protective components are needed up to those levels. In the event that the INA901-SP is exposed to transients on the inputs in excess of its ratings, external transient absorption with semiconductor transient absorbers (Zeners or Transzorbs) are necessary.

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it never allows the INA901-SP to be exposed to transients greater than 65 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal Zener-type ESD protection, the INA901-SP is not suited to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30%, but are tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA901-SP inputs with two equal resistors on each input).

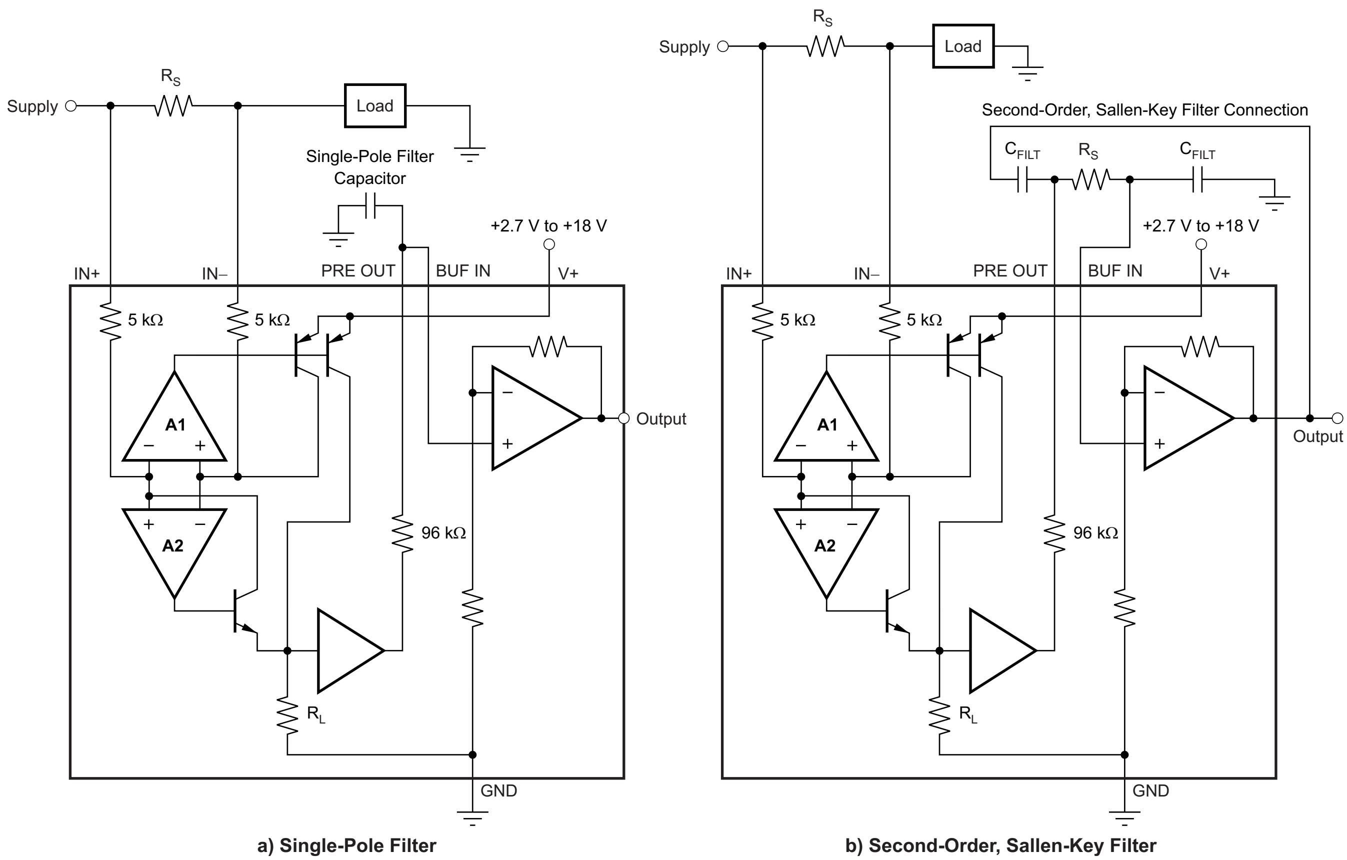
7.4 Device Functional Modes

7.4.1 First- or Second-Order Filtering

The output of the INA901-SP is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA901-SP readily enables the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96-kΩ output impedance at PRE OUT on pin 3, as shown in Figure 16a.

The INA901-SP readily lends itself to second-order Sallen-Key configurations, as shown in Figure 16b. When designing these configurations consider that the PRE OUT 96-kΩ output impedance exhibits an initial variation of ±30% with the addition of a –2200-ppm/°C temperature coefficient.



NOTE: Remember to use the appropriate buffer gain = 2 when designing Sallen-Key configurations.

Figure 16. The INA901-SP Can Be Easily Connected for First- or Second-Order Filtering

7.4.2 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA901-SP current shunt monitor is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$) and common-mode voltage (V_{CM}) relative to the supply voltage, V_S. V_{CM} is expressed as ($V_{IN+} + V_{IN–}$) / 2; however, in practice, V_{CM} is used as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$

Low V_{SENSE} Case 1:

$V_{SENSE} < 20$ mV, $–15\text{ V} \leq V_{CM} < 0$

Low V_{SENSE} Case 2:

$V_{SENSE} < 20$ mV, $0\text{ V} \leq V_{CM} \leq V_S$

Device Functional Modes (continued)

Low V_{SENSE} Case 3:
V_{SENSE} < 20 mV, $V_S < V_{CM} \leq 65$ V

7.4.2.1 Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV}$$

where

- V_{OUT1} = Output voltage with V_{SENSE} = 100 mV and
- V_{OUT2} = Output voltage with V_{SENSE} = 20 mV. (1)

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left[\frac{V_{OUT1}}{G}\right] - 100mV \tag{2}$$

In the *Typical Characteristics* section, the *Output Error vs Common-Mode Voltage* curve (Figure 6) shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for $V_{CM} \geq 12$ V, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq$ 20-mV output specifications in the *Electrical Characteristics* table.

7.4.2.2 Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the device functions, as illustrated in the *Output Error vs Common-Mode Voltage* curve (Figure 6). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases when V_{CM} becomes less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –15 V.

7.4.2.3 Low V_{SENSE} Case 1: V_{SENSE} < 20 mV, –15 V ≤ V_{CM} < 0; and Low V_{SENSE} Case 3: V_{SENSE} < 20 mV, $V_S < V_{CM} \leq 65$ V

Although the INA901-SP is not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA901-SP, knowing what the behavior of the device is in these regions is important.

Device Functional Modes (continued)

When V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 60 mV for V_{SENSE} = 0 mV. When V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in the *Electrical Characteristics* table. Figure 17 shows this effect using the INA901-SP (gain = 20).

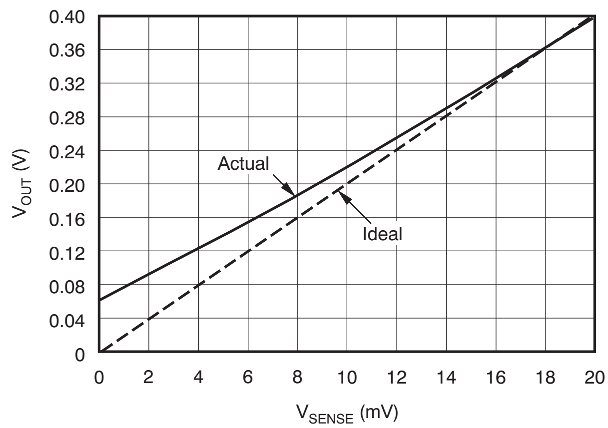


Figure 17. Example For Low V_{SENSE} Cases 1 and 3 (INA901-SP Gain = 20)

7.4.2.4 Low V_{SENSE} Case 2: V_{SENSE} < 20 mV, 0 V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA901-SP. To achieve the wide input common-mode voltage range, this device uses two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, when V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 18 shows this behavior for the INA901-SP. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S, setting V_{SENSE} = 0 mV, and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this case varies from device to device. The maximum peak voltage for the INA901-SP is 0.4 V.

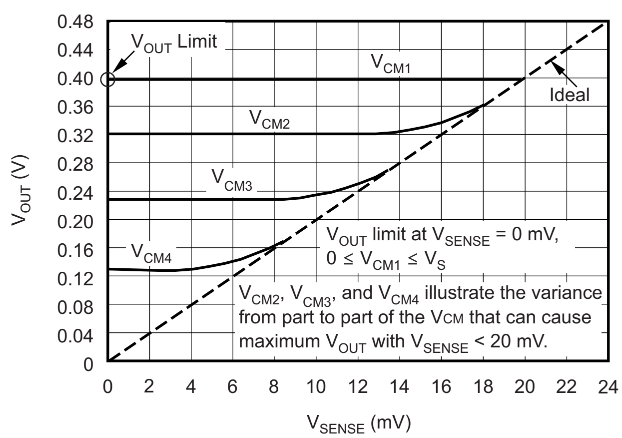


Figure 18. Example for Low V_{SENSE} Case 2 (INA901-SP, Gain = 20)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA901-SP measures the voltage developed across a current-sensing resistor when current passes through it. There is also a filtering feature to remove unwanted transients and smooth the output voltage.

8.2 Typical Application

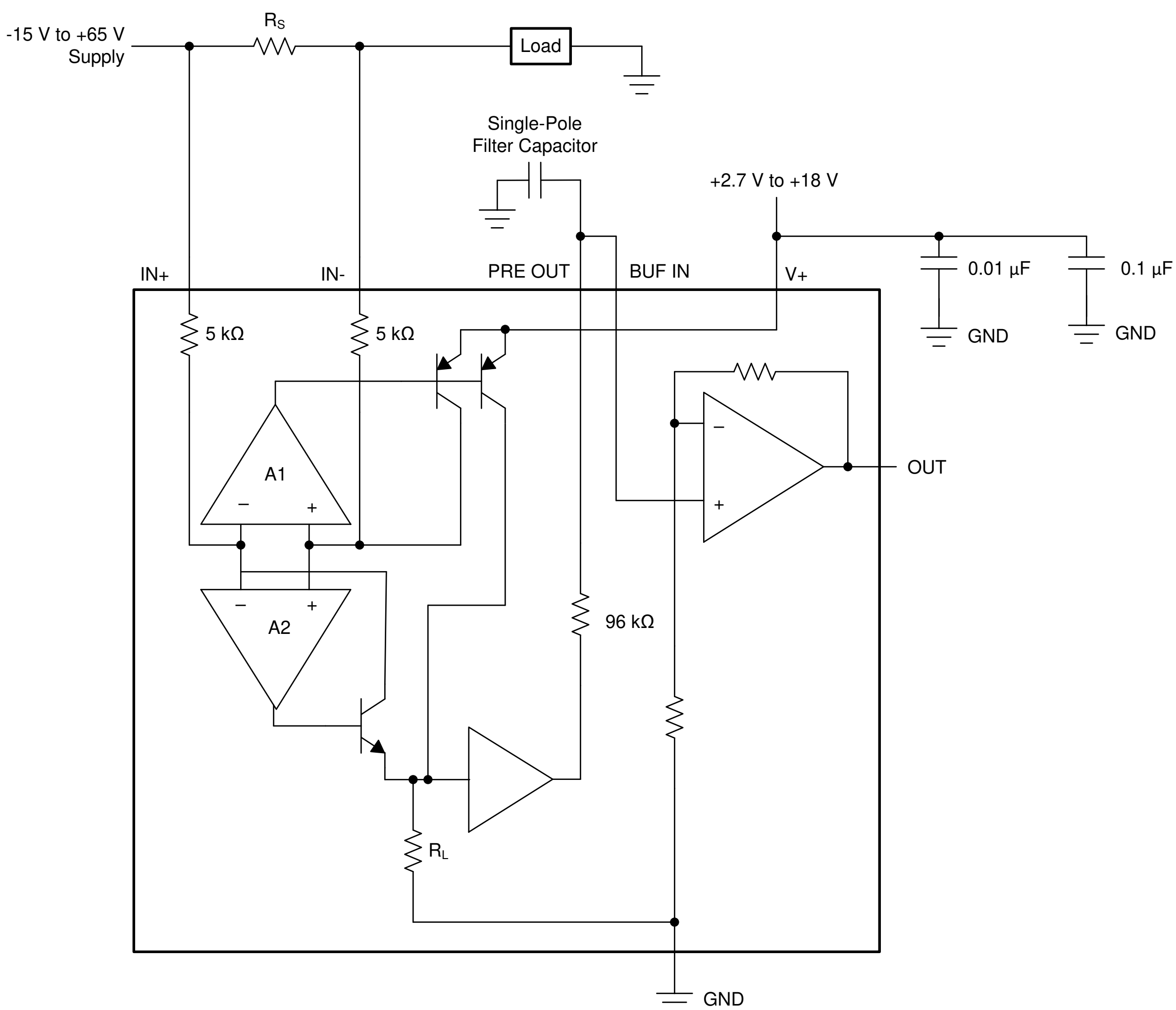


Figure 19. Filtering Configuration

8.2.1 Design Requirements

In this application, the device is configured to measure a triangular periodic current at 10 kHz with filtering. The average current through the shunt is the information that is desired. This current can be either solenoid current or inductor current where current is being pulsed through.

Typical Application (continued)

Selecting the capacitor size is based on the lowest frequency component to be filtered out. The amount of signal that is filtered out is dependant on this cutoff frequency. From the cutoff frequency, the attenuation is 20 dB per decade.

8.2.2 Detailed Design Procedure

Without this filtering capability, an input filter must be used. When series resistance is added to the input, large errors also come into play because the resistance must be large to create a low cutoff frequency. By using a 10-nF capacitor for the single-pole filter capacitor, the 10-kHz signal is averaged. The cutoff frequency made by the capacitor is set at 166-Hz frequency. This frequency is well below the periodic frequency and reduces the ripple on the output and the average current can easily be measured.

8.2.3 Application Curves

Figure 20 shows the output waveform without filtering. The output signal tracks the input signal with a large ripple. If this current is sampled by an ADC, many samples must be taken to average the current digitally. This process requires additional time for sampling or operating at a higher sampling rate, which may be undesirable for the application.

Figure 21 shows the output waveform with filtering. shows the output waveform with filtering. The average value of the current with a small ripple can now be easily sampled by the converter without the need for digital averaging.

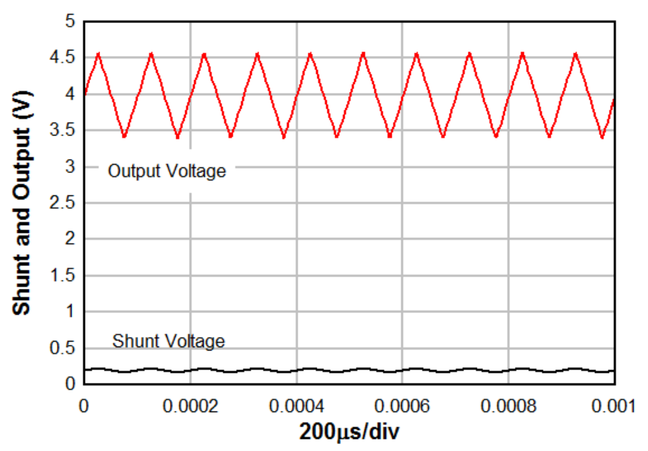


Figure 20. Without Filtering

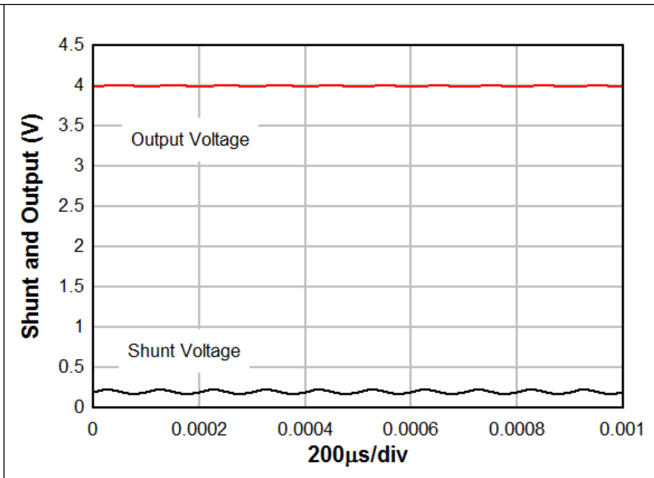


Figure 21. With Filtering

9 Power Supply Recommendations

The input circuitry of the INA901-SP can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage is up to 65 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Place minimum bypass capacitors of 0.01 μF and 0.1 μF in value close to the supply pins. Although not mandatory, an additional 10-mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.1.1 RFI and EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI and EMI sensitivity. PCB layout must locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields.

10.2 Layout Example

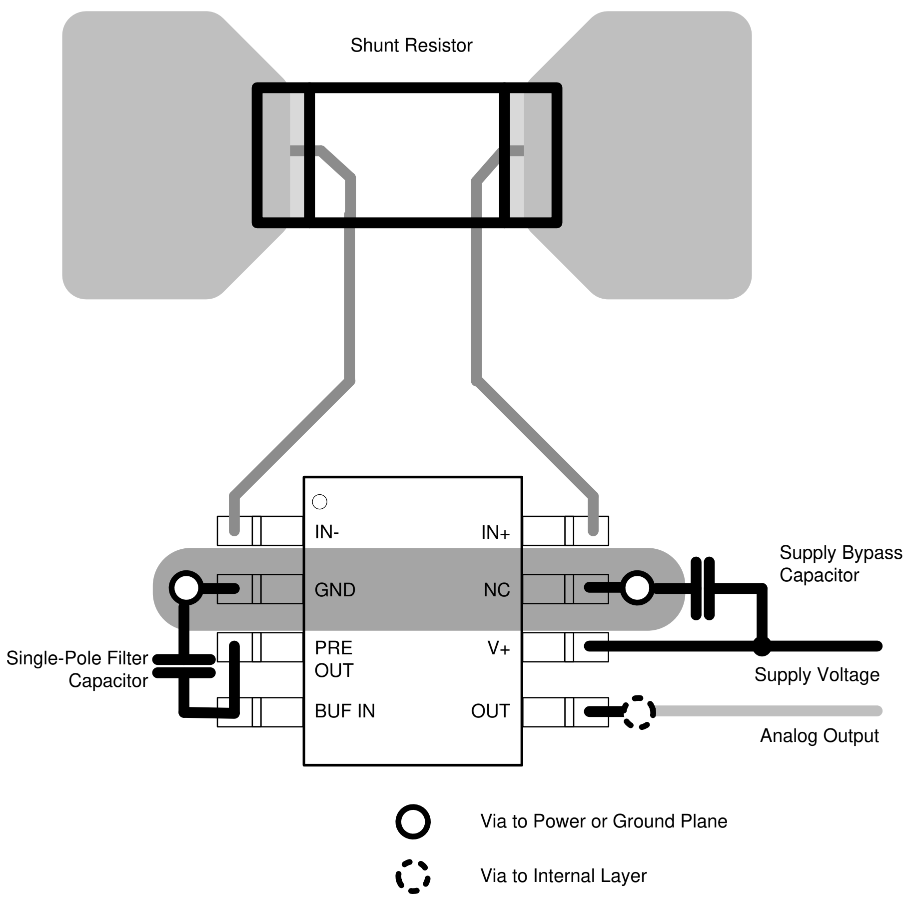


Figure 22. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *INA901EVM-CVAL Evaluation Board User's Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1821001VXC	ACTIVE	CFP	HKX	8	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	1821001VXC INA901-SP	Samples
5962L1821001VXC	ACTIVE	CFP	HKX	8	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	5962L1821001VXC INA901-SP	Samples
INA901HKX/EM	ACTIVE	CFP	HKX	8	25	RoHS & Green	NIAU	N / A for Pkg Type	25 to 25	INA901HKX/EM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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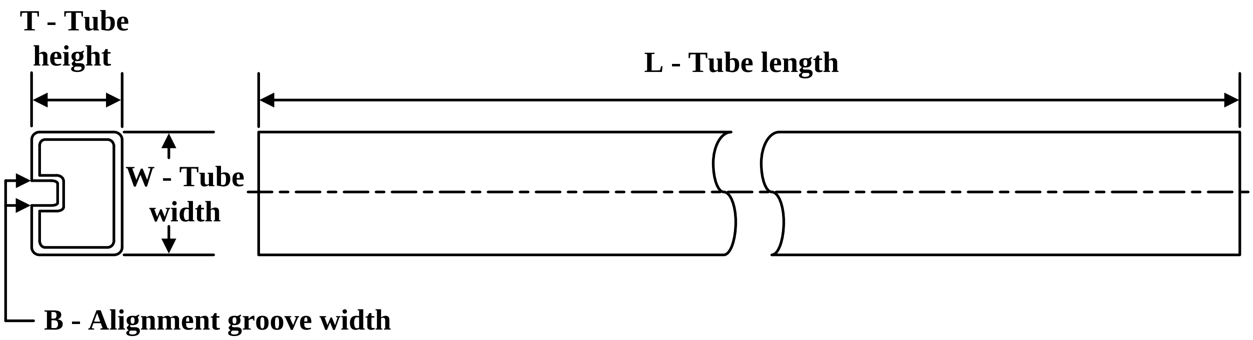
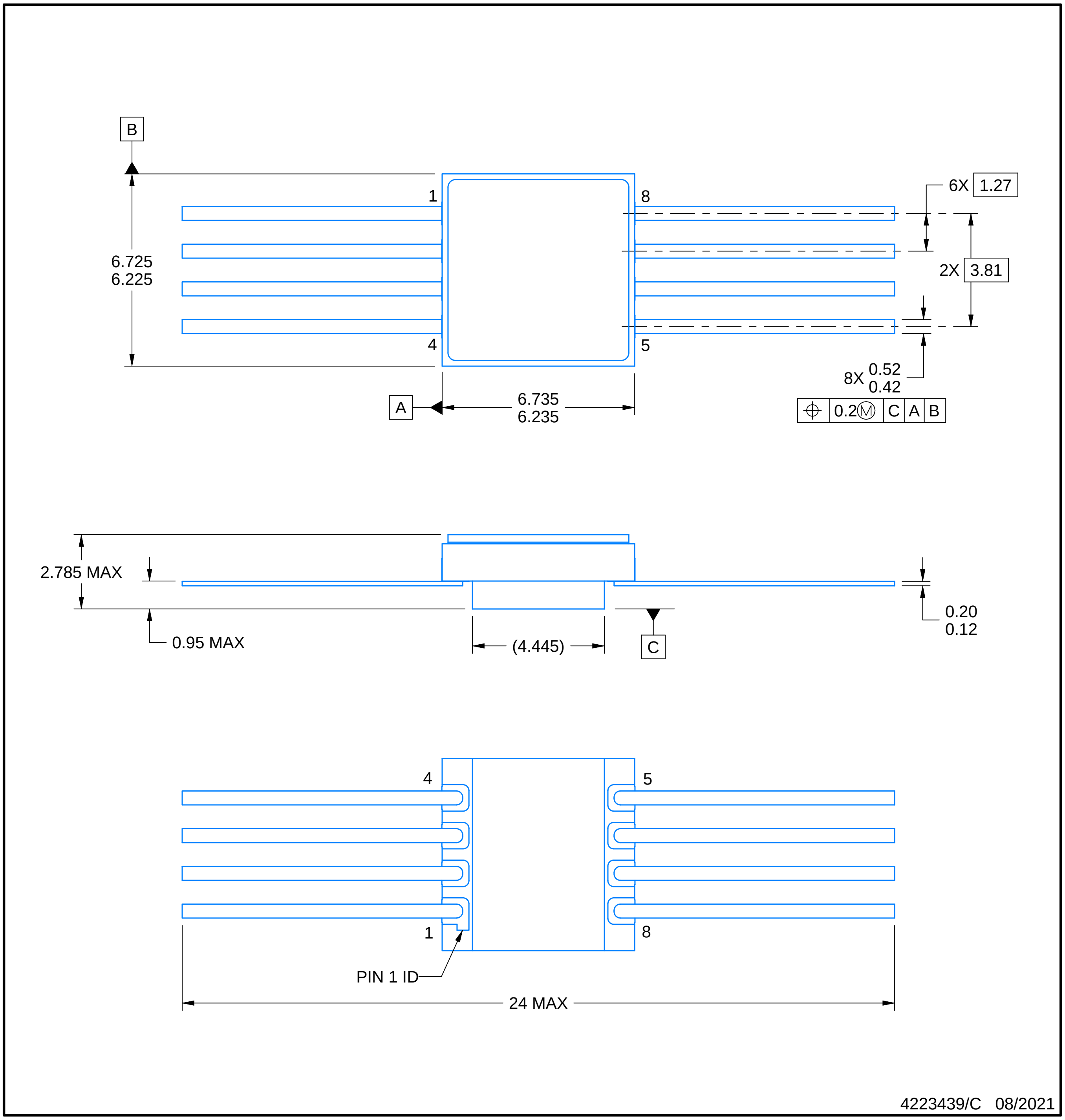
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1821001VXC	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA
5962L1821001VXC	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA
INA901HKX/EM	HKX	CFP (HSL)	8	25	506.98	26.16	6220	NA



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated.

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