ISO5451-Q1 High-CMTI 2.5-A and 5-A Isolated IGBT, MOSFET Gate Driver
With Active Protection Features

Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 3A
  - Device CDM Classification Level C6
- 50-kV/µs Minimum and 100-kV/µs Typical Common-Mode Transient Immunity (CMTI) at $V_{CM} = 1500$ V
- 2.5-A Peak Source and 5-A Peak Sink Currents
- Short Propagation Delay: 76 ns (Typ), 110 ns (Max)
- 2-A Active Miller Clamp
- Output Short-Circuit Clamp
- Fault Alarm upon Desaturation Detection is Signaled on FLT and Reset Through RST
- Input and Output Under Voltage Lock-Out (UVLO) with Ready (RDY) Pin Indication
- Active Output Pull-down and Default Low Outputs with Low Supply or Floating Inputs
- 3-V to 5.5-V Input Supply Voltage
- 15-V to 30-V Output Driver Supply Voltage
- CMOS Compatible Inputs
- Rejects Input Pulses and Noise Transients Shorter Than 20 ns
- Isolation Surge Withstand Voltage 10000-$V_{PK}$
- Safety-Related Certifications:
  - $8000-V_{PK}$ $V_{IOTM}$ and $1420-V_{PK}$ $V_{IDRM}$
  - Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - $5700-V_{RMS}$ Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950–1 and IEC 60601–1 End Equipment Standards
  - TUV Certification per EN 61010-1 and EN 60950-1
  - GB4943.1-2011 CQC Certification
  - All Certifications Complete per UL, VDE, CQC, TUV and Planned for CSA

Applications

- Isolated IGBT and MOSFET Drives in:
  - HEV and EV Power Modules
  - Industrial Motor Control Drives
  - Industrial Power Supplies
  - Solar Inverters
  - Induction Heating

Description

The ISO5451-Q1 is a 5.7-$kV_{RMS}$, reinforced isolated gate driver for IGBTs and MOSFETs with 2.5-A source and 5-A sink current. The input side operates from a single 3-V to 5.5-V supply. The output side allows for a supply range from minimum 15 V to maximum 30 V. Two complementary CMOS inputs control the output stage of the gate driver. The short propagation time of 76 ns assures accurate control of the output stage.

An internal desaturation (DESAT) fault detection recognizes when the IGBT is in an overload condition. Upon a DESAT detect, the gate driver output is driven low to $V_{EE2}$ potential, turning the IGBT immediately off.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO5451-Q1</td>
<td>SOIC (16)</td>
<td>10.30 mm × 7.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram
Table of Contents

1 Features ....................................................... 1
2 Applications .................................................. 1
3 Description .................................................... 1
4 Revision History ............................................. 2
5 Description (continued) ..................................... 3
6 Pin Configuration and Function .......................... 3
7 Specifications .................................................. 4
  7.1 Absolute Maximum Ratings ......................... 4
  7.2 ESD Ratings ................................................. 4
  7.3 Recommended Operating Conditions ............... 4
  7.4 Thermal Information ..................................... 5
  7.5 Power Ratings .............................................. 5
  7.6 Insulation Characteristics ............................. 6
  7.7 Safety-Related Certifications ....................... 7
  7.8 Safety Limiting Values .................................. 7
  7.9 Electrical Characteristics ............................. 8
  7.10 Switching Characteristics ......................... 9
  7.11 Insulation Characteristics Curves ................. 10
  7.12 Typical Characteristics ............................. 11
8 Parameter Measurement Information .................... 17
9 Detailed Description ....................................... 19
9.1 Overview .................................................. 19
9.2 Functional Block Diagram .............................. 19
9.3 Feature Description ...................................... 20
9.4 Device Functional Modes .............................. 21
10 Application and Implementation ....................... 22
  10.1 Application Information .............................. 22
  10.2 Typical Applications ................................... 22
11 Power Supply Recommendations ........................ 30
12 Layout ....................................................... 30
  12.1 Layout Guidelines ...................................... 30
  12.2 PCB Material ............................................ 30
  12.3 Layout Example ......................................... 30
13 Device and Documentation Support ..................... 31
  13.1 Documentation Support ............................... 31
  13.2 Receiving Notification of Documentation Updates . 31
  13.3 Community Resources ............................... 31
  13.4 Trademarks .............................................. 31
  13.5 Electrostatic Discharge Caution .................... 31
  13.6 Glossary ................................................. 31
14 Mechanical, Packaging, and Orderable Information .... 31

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to Revision A Page

• Changed the title of the data sheet from Active Safety Features to Active Protection Features ................. 1
• Changed the Electrostatic Discharge Caution section ................................................................. 31
5 Description (continued)

When desaturation is active, a fault signal is sent across the isolation barrier, pulling the FLT output at the input side low and blocking the isolator input. The FLT output condition is latched and can be reset through a low-active pulse at the RST input.

When the IGBT is turned off during normal operation with bipolar output supply, the output is hard clamp to \( V_{EE2} \). If the output supply is unipolar, an active Miller clamp can be used, allowing Miller current to sink across a low impedance path, preventing IGBT to be dynamically turned on during high voltage transient conditions.

The readiness for the gate driver to be operated is under the control of two undervoltage-lockout circuits monitoring the input side and output side supplies. If either side has insufficient supply the RDY output goes low, otherwise this output is high.

The ISO5451-Q1 is available in a 16-pin SOIC package. Device operation is specified over a temperature range from \(-40^\circ C\) to \(+125^\circ C\) ambient.

6 Pin Configuration and Function

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLAMP</td>
<td>O</td>
<td>Miller clamp output</td>
</tr>
<tr>
<td>DESAT</td>
<td>I</td>
<td>Desaturation voltage input</td>
</tr>
<tr>
<td>FLT</td>
<td>O</td>
<td>Fault output, low-active during DESAT condition</td>
</tr>
<tr>
<td>GND1</td>
<td>—</td>
<td>Input ground</td>
</tr>
<tr>
<td>GND2</td>
<td>—</td>
<td>Gate drive common. Connect to IGBT emitter</td>
</tr>
<tr>
<td>IN+</td>
<td>I</td>
<td>Non-inverting gate drive voltage control input</td>
</tr>
<tr>
<td>IN–</td>
<td>I</td>
<td>Inverting gate drive voltage control input</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>Not connected</td>
</tr>
<tr>
<td>OUT</td>
<td>O</td>
<td>Gate drive voltage output</td>
</tr>
<tr>
<td>RDY</td>
<td>O</td>
<td>Power-good output, active high when both supplies are good</td>
</tr>
<tr>
<td>RST</td>
<td>I</td>
<td>Reset input, apply a low pulse to reset fault latch</td>
</tr>
<tr>
<td>( V_{CC1} )</td>
<td>—</td>
<td>Positive input supply (3 V to 5.5 V)</td>
</tr>
<tr>
<td>( V_{CC2} )</td>
<td>—</td>
<td>Most positive output supply potential</td>
</tr>
<tr>
<td>( V_{EE2} )</td>
<td>—</td>
<td>Output negative supply. Connect to GND2 for unipolar-supply application</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

| V\(_{CC1}\) | Supply voltage input side | GND1 – 0.3 | 6 | V |
| V\(_{CC2}\) | Positive supply voltage output side \(\left( V_{CC2} - \text{GND2} \right) \) | –0.3 | 35 | V |
| V\(_{EE2}\) | Negative supply voltage output side \(\left( V_{EE2} - \text{GND2} \right) \) | –17.5 | 0.3 | V |
| V\(_{\text{SUP2}}\) | Total supply output voltage \(\left( V_{CC2} - V_{EE2} \right) \) | –0.3 | 35 | V |
| V\(_{OUT}\) | Gate driver output voltage \(\left( V_{EE2} - 0.3 \right) \left( V_{CC2} + 0.3 \right) \) | –0.3 | V |
| I\(_{O(\text{H})}\) | Gate driver high output current \(\text{max pulse width} = 10 \mu\text{s}, \text{max duty cycle} = 0.2\%\) | 2.7 | A |
| I\(_{O(L)}\) | Gate driver low output current \(\text{max pulse width} = 10 \mu\text{s}, \text{max duty cycle} = 0.2\%\) | 5.5 | A |
| V\(_{\text{LIP}}\) | Voltage at IN+, IN–, FLT, RDY, RST | GND1 – 0.3 | \( V_{CC1} + 0.3 \) | V |
| I\(_{\text{LOP}}\) | Output current of FLT, RDY | 10 | mA |
| V\(_{\text{DESAT}}\) | Voltage at DESAT | GND2 – 0.3 | \( V_{CC2} + 0.3 \) | V |
| V\(_{\text{CLAMP}}\) | Clamp voltage \(\left( V_{EE2} - 0.3 \right) \left( V_{CC2} + 0.3 \right) \) | –0.3 | V |
| T\(_{J}\) | Junction temperature | –40 | 150 | °C |
| T\(_{STG}\) | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| V\(_{\text{ESD}}\) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002\(^{(1)}\) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

| V\(_{CC1}\) | Supply voltage input side | 3 | 5.5 | V |
| V\(_{CC2}\) | Positive supply voltage output side \(\left( V_{CC2} - \text{GND2} \right) \) | 15 | 30 | V |
| V\(_{EE2}\) | Negative supply voltage output side \(\left( V_{EE2} - \text{GND2} \right) \) | –15 | 0 | V |
| V\(_{\text{SUP2}}\) | Total supply voltage output side \(\left( V_{CC2} - V_{EE2} \right) \) | 15 | 30 | V |
| V\(_{IH}\) | High-level input voltage \(\left( \text{IN+}, \text{IN–}, \text{RST} \right) \) \(0.7 \times V_{CC1}\) | \( V_{CC1} \) | V |
| V\(_{IL}\) | Low-level input voltage \(\left( \text{IN+}, \text{IN–}, \text{RST} \right) \) \(0 \) | \( 0.3 \times V_{CC1} \) | V |
| I\(_{P}\) | Pulse width at \(\text{IN+}, \text{IN–}\) for full output \((C_{LOAD} = 1 \, \text{nF})\) | 40 | ns |
| I\(_{RST}\) | Pulse width at \(\text{RST}\) for resetting fault latch | 800 | ns |
| T\(_{A}\) | Ambient temperature | –40 | 25 | 125 | °C |
7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>ISO5451-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DW (SOIC)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16 PINS</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{JA}}$ (Junction-to-ambient thermal resistance)</td>
<td>99.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{JC(top)}}$ (Junction-to-case (top) thermal resistance)</td>
<td>48.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\text{JB}}$ (Junction-to-board thermal resistance)</td>
<td>56.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JT}}$ (Junction-to-top characterization parameter)</td>
<td>29.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{\text{JB}}$ (Junction-to-board characterization parameter)</td>
<td>56.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Power Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{D}$</td>
<td>Maximum power dissipation (1)</td>
<td>1255</td>
<td>mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{ID}$</td>
<td>Maximum input power dissipation</td>
<td>175</td>
<td>mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{OD}$</td>
<td>Maximum output power dissipation</td>
<td>1080</td>
<td>mW</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Full chip power dissipation is de-rated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.
## 7.6 Insulation Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SPECIFICATION</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>Shortest terminal-to-terminal distance through air</td>
<td>&gt;8</td>
<td>mm</td>
</tr>
<tr>
<td>CPG</td>
<td>Shortest terminal-to-terminal distance across the package surface</td>
<td>&gt;8</td>
<td>mm</td>
</tr>
<tr>
<td>DTI</td>
<td>Minimum internal gap (internal clearance)</td>
<td>&gt;21</td>
<td>μm</td>
</tr>
<tr>
<td>CTI</td>
<td>DIN EN 60112 (VDE 0303-11); IEC 60112;</td>
<td>&gt;600</td>
<td>V</td>
</tr>
<tr>
<td>Material Group</td>
<td>According to IEC 60664-1; UL 746A</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>Overvoltage category (according to IEC 60664-1)</td>
<td>Rated Mains Voltage ≤ 300 V&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>I-IV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rated Mains Voltage ≤ 600 V&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>I-III</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rated Mains Voltage ≤ 1000 V&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>I-II</td>
<td></td>
</tr>
</tbody>
</table>

### DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)

- **V<sub>IORM</sub>** Maximum repetitive peak isolation voltage
  - AC voltage (bipolar)
  - Specification: 1420 V<sub>PK</sub>
- **V<sub>IO</sub>** Isolation resistance, input to output
  - V<sub>IO</sub> = 500 V, T<sub>A</sub> = 25°C
  - Specification: > 10<sup>12</sup> Ω
- **C<sub>IO</sub>** Barrier capacitance, input to output
  - V<sub>IO</sub> = 0.4 × sin (2πf), f = 1 MHz
  - Specification: 1 pF
- **Pollution degree**
  - Specification: 2

### ISO5451-Q1

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

2. This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

4. Apparent charge is electrical discharge caused by a partial discharge (pd).

5. All pins on each side of the barrier tied together creating a two-terminal device.
7.7 Safety-Related Certifications

<table>
<thead>
<tr>
<th>VDE</th>
<th>CSA</th>
<th>UL</th>
<th>CQC</th>
<th>TUV</th>
</tr>
</thead>
</table>

Reinforced Insulation
Maximum Transient isolation voltage, 8000 VPK;
Maximum surge isolation voltage, 6250 VPK;
Maximum repetitive peak isolation voltage, 1420 VPK

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;S&lt;/sub&gt;</td>
<td>Safety input, output or supply current</td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 3.6 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>349</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 5.5 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>228</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 15 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>84</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 30 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>42</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

P<sub>S</sub> Safety input, output, or total power

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>1255(1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

T<sub>S</sub> Maximum ambient safety temperature

| | | | | | |
| | | | | | |

(1) Production tested ≥ 6840 V<sub>RMS</sub> for 1 second in accordance with UL 1577.

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;S&lt;/sub&gt;</td>
<td>Safety input, output or supply current</td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 3.6 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>349</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 5.5 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>228</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 15 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>84</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R&lt;sub&gt;UA&lt;/sub&gt; = 99.6°C/W, V&lt;sub&gt;I&lt;/sub&gt; = 30 V, T&lt;sub&gt;J&lt;/sub&gt; = 150°C, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>42</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.
### 7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25^\circ C$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} – GND2 = 15 \text{ V}$, $GND2 – V_{EE2} = 8 \text{ V}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VOLTAGE SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT+/(UVLO1)}$</td>
<td>Positive-going UVLO1 threshold voltage input side ($V_{CC1} – GND1$)</td>
<td>2.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IT-/(UVLO1)}$</td>
<td>Negative-going UVLO1 threshold voltage input side ($V_{CC1} – GND1$)</td>
<td>1.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{HYS(UVLO1)}$</td>
<td>UVLO1 Hysteresis voltage ($V_{IT–} - V_{IT+}$) input side</td>
<td>0.24</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IT+/(UVLO2)}$</td>
<td>Positive-going UVLO2 threshold voltage output side ($V_{CC2} – GND2$)</td>
<td>12</td>
<td>13</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IT-/(UVLO2)}$</td>
<td>Negative-going UVLO2 threshold voltage output side ($V_{CC2} – GND2$)</td>
<td>9.5</td>
<td>11</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{HYS(UVLO2)}$</td>
<td>UVLO2 Hysteresis voltage ($V_{IT–} - V_{IT+}$) output side</td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{Q1}$</td>
<td>Input supply quiescent current</td>
<td>2.8</td>
<td>4.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{Q2}$</td>
<td>Output supply quiescent current</td>
<td>3.6</td>
<td>6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>LOGIC I/O</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT+(IN,RST)}$</td>
<td>Positive-going input threshold voltage ($IN+, IN–, RST$)</td>
<td>$0.7 \times V_{CC1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT–(IN,RST)}$</td>
<td>Negative-going input threshold voltage ($IN+, IN–, RST$)</td>
<td>$0.3 \times V_{CC1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HYS(IN,RST)}$</td>
<td>Input hysteresis voltage ($IN+, IN–, RST$)</td>
<td>$0.15 \times V_{CC1}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High-level input leakage at ($IN+$) (1)</td>
<td>$IN+ = V_{CC1}$</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low-level input leakage at ($IN–, RST$) (2)</td>
<td>$IN– = GND1, RST = GND1$</td>
<td>-100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{PU}$</td>
<td>Pull-up current of FLT, RDY</td>
<td>$V_{FLT} = GND1, V_{RDY} = GND1$</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage at FLT, RDY</td>
<td>$I_{FLT} = 5 \text{ mA}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GATE DRIVER STAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUTPD}$</td>
<td>Active output pulldown voltage</td>
<td>$I_{OUT} = 200 \text{ mA}, V_{CC2} = \text{open}$</td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUTH}$</td>
<td>High-level output voltage</td>
<td>$I_{OUT} = -20 \text{ mA}$</td>
<td>$V_{CC2} = 0.5, V_{CC2} = 0.24$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUTH}$</td>
<td>High-level output peak current</td>
<td>$IN+ = \text{high}, IN– = \text{low}, V_{OUT} = V_{CC2} - 15 \text{ V}$</td>
<td>1.5</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>$I_{OUTL}$</td>
<td>Low-level output peak current</td>
<td>$IN+ = \text{low}, IN– = \text{high}, V_{OUT} = V_{EE2} + 15 \text{ V}$</td>
<td>3.4</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td><strong>ACTIVE MILLER CLAMP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ICL}$</td>
<td>Low-level clamp voltage</td>
<td>$I_{CL} = 20 \text{ mA}$</td>
<td>$V_{EE2} + 0.015, V_{EE2} + 0.08$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{ICL}$</td>
<td>Low-level clamp current</td>
<td>$V_{ICLAMP} = V_{EE2} + 2.5 \text{ V}$</td>
<td>1.6</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>$V_{CLTH}$</td>
<td>Clamp threshold voltage</td>
<td></td>
<td>1.6</td>
<td>2.1</td>
<td>2.5</td>
</tr>
<tr>
<td><strong>SHORT CIRCUIT CLAMPING</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ICL,OUT}$</td>
<td>Clamping voltage ($V_{OUT} - V_{CC2}$)</td>
<td>$IN+ = \text{high}, IN– = \text{low}, I_{CL} = 10 \mu\text{A}, I_{OUT} = 500 \text{ mA}$</td>
<td>0.8</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>$V_{ICL,CLAMP}$</td>
<td>Clamping voltage ($V_{CLAMP} - V_{CC2}$)</td>
<td>$IN+ = \text{high}, IN– = \text{low}, I_{CL} = 10 \mu\text{A}, I_{CLAMP} = 500 \text{ mA}$</td>
<td>1.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ICL,CLAMP}$</td>
<td>Clamping voltage at CLAMP</td>
<td>$IN+ = \text{High}, IN– = \text{Low}, I_{CLAMP} = 20 \mu\text{A}$</td>
<td>0.7</td>
<td>1.1</td>
<td></td>
</tr>
<tr>
<td><strong>DESAT PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DCHG}$</td>
<td>Blanking capacitor charge current</td>
<td>$V_{DESAT} - GND2 = 2 \text{ V}$</td>
<td>0.42</td>
<td>0.5</td>
<td>0.58</td>
</tr>
<tr>
<td>$I_{DCHG}$</td>
<td>Blanking capacitor discharge current</td>
<td>$V_{DESAT} - GND2 = 6 \text{ V}$</td>
<td>9</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>$V_{DSTH}$</td>
<td>DESAT threshold voltage with respect to GND2</td>
<td></td>
<td>8.3</td>
<td>9</td>
<td>9.5</td>
</tr>
<tr>
<td>$V_{DSL}$</td>
<td>DESAT voltage with respect to GND2, when OUT is driven low</td>
<td></td>
<td>0.4</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

(1) $I_{IH}$ for $IN–, RST$ pin is zero as they are pulled high internally.
(2) $I_{IL}$ for $IN+$ is zero, as it is pulled low internally.
### 7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - \text{GND2} = 15\text{ V}$, $\text{GND2} - V_{EE2} = 8\text{ V}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_r$</td>
<td>Output signal rise time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Output signal fall time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{p_{LH} - p_{HL}}$</td>
<td>Propagation Delay</td>
<td>C_{LOAD} = 1 nF, see Figure 38, Figure 39 and Figure 40</td>
<td>12</td>
<td>20</td>
<td>35</td>
</tr>
<tr>
<td>$t_{sk-p}$</td>
<td>Pulse Skew $t_{p_{HL} - p_{LH}}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{sk-pp}$</td>
<td>Part-to-part skew</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{GF}$</td>
<td>Glitch filter on IN+, IN–, RST</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DESAT (10%)}$</td>
<td>DESAT sense to 10% OUT delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DESAT (GF)}$</td>
<td>DESAT glitch filter delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DESAT (FLT)}$</td>
<td>DESAT sense to FLT-low delay</td>
<td>see Figure 40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{LEB}$</td>
<td>Leading edge blanking time</td>
<td>see Figure 38 and Figure 39</td>
<td>330</td>
<td>400</td>
<td>500</td>
</tr>
<tr>
<td>$t_{GF(RSTFLT)}$</td>
<td>Glitch filter on RST for resetting FLT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_i$</td>
<td>Input capacitance(2)</td>
<td>$V_1 = V_{CC1}/2 + 0.4 \times \sin (2\pi f t)$, $f = 1\text{ MHz}$, $V_{CC1} = 5\text{ V}$</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMTI</td>
<td>Common-mode transient immunity</td>
<td>$V_{CM} = 1500\text{ V}$, see Figure 41</td>
<td>50</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

1. Measured at same supply voltage and temperature condition
2. Measured from input pin to ground.
7.11 Insulation Characteristics Curves

Figure 1. Reinforced High-Voltage Capacitor Lifeime Projection

Figure 2. Thermal Derating Curve for Limiting Current per VDE

Figure 3. Thermal Derating Curve for Limiting Power per VDE
### 7.12 Typical Characteristics

![Graph 1](image1.png)

**Figure 4. Output High Drive Current vs Temperature**

![Graph 2](image2.png)

**Figure 5. Output Low Drive Current vs Temperature**

![Graph 3](image3.png)

**Figure 6. Output High Drive Current vs Output Voltage**

![Graph 4](image4.png)

**Figure 7. Output Low Drive Current vs Output Voltage**

![Graph 5](image5.png)

**Figure 8. DESAT Threshold Voltage vs Temperature**

Unipolar: $V_{CC2} - V_{EE2} = V_{CC2} - GND2$
Typical Characteristics (continued)

<table>
<thead>
<tr>
<th>Circuit Configuration</th>
<th>Figure Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L = 1 \text{nF}$, $R_G = 0 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 9</td>
<td>Output Transient Waveform</td>
</tr>
<tr>
<td>$C_L = 1 \text{nF}$, $R_G = 10 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 10</td>
<td>Output Transient Waveform</td>
</tr>
<tr>
<td>$C_L = 10 \text{nF}$, $R_G = 0 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 11</td>
<td>Output Transient Waveform</td>
</tr>
<tr>
<td>$C_L = 10 \text{nF}$, $R_G = 10 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 12</td>
<td>Output Transient Waveform</td>
</tr>
<tr>
<td>$C_L = 100 \text{nF}$, $R_G = 0 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 13</td>
<td>Output Transient Waveform</td>
</tr>
<tr>
<td>$C_L = 100 \text{nF}$, $R_G = 10 \Omega$, $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND} = 20 \text{V}$</td>
<td>Figure 14</td>
<td>Output Transient Waveform</td>
</tr>
</tbody>
</table>
Typical Characteristics (continued)

Figure 15. Output Transient Waveform DESAT and FLT

\[ C_L = 100 \text{ nF} \quad R_G = 10 \Omega \]

\[ V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V} \]

Figure 16. \( I_{CC1} \) Supply Current vs Temperature

\[ V_{CC1} = 3 \text{ V} \quad V_{CC1} = 3.3 \text{ V} \quad V_{CC1} = 5 \text{ V} \quad V_{CC1} = 5.5 \text{ V} \]

Figure 17. \( I_{CC1} \) Supply Current vs Temperature

\[ I_{CC1} = \text{Low} \quad I_{CC1} = \text{Low} \]

Figure 18. \( I_{CC2} \) Supply Current vs Temperature

\[ V_{CC2} = 15 \text{ V} \quad V_{CC2} = 20 \text{ V} \quad V_{CC2} = 30 \text{ V} \]

Figure 19. \( I_{CC1} \) Supply Current vs Input Frequency

\[ V_{CC1} = 3 \text{ V} \quad V_{CC1} = 5.5 \text{ V} \]

Figure 20. \( I_{CC2} \) Supply Current vs Input Frequency

\[ V_{CC2} = 15 \text{ V} \quad V_{CC2} = 20 \text{ V} \quad V_{CC2} = 30 \text{ V} \]
Typical Characteristics (continued)

Figure 21. $I_{CC2}$ Supply Current vs Load Capacitance

Figure 22. $V_{CC1}$ Propagation Delay vs Temperature

Figure 23. $V_{CC2}$ Propagation Delay vs Temperature

Figure 24. Propagation Delay vs Load Capacitance

Figure 25. $t_r$ Rise Time vs Load Capacitance

Figure 26. $t_f$ Fall Time vs Load Capacitance
Typical Characteristics (continued)

![Figure 27. \( t_r \) Rise Time vs Load Capacitance](image)

![Figure 28. \( t_f \) Fall Time vs Load Capacitance](image)

![Figure 29. Leading Edge Blanking Time With Temperature](image)

![Figure 30. DESAT Sense to \( V_{OUT} \) 10\% Delay vs Temperature](image)

![Figure 31. DESAT Sense to FLT Low Delay vs Temperature](image)

![Figure 32. Reset to Fault Delay Across Temperature](image)
Typical Characteristics (continued)

Figure 33. Miller Clamp Current vs Temperature

Figure 34. Active Pull Down Voltage vs Temperature

Figure 35. V_{CLP\_CLAMP} - Short Circuit Clamp Voltage on Clamp Across Temperature

Figure 36. V_{OUT\_CLAMP} - Short Circuit Clamp Voltage on OUT Across Temperature

Figure 37. Blanking Capacitor Charging Current vs Temperature
8 Parameter Measurement Information

Figure 38. OUT Propagation Delay, Non-Inverting Configuration

Figure 39. OUT Propagation Delay, Inverting Configuration
Parameter Measurement Information (continued)

Figure 40. DESAT, OUT, FLT, RST Delay

Figure 41. Common-Mode Transient Immunity Test Circuit
9 Detailed Description

9.1 Overview

The ISO5451-Q1 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a capacitive, silicon dioxide ($SiO_2$), isolation barrier.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET (RST) inputs, READY (RDY) and FAULT (FLT) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5451-Q1 also contains under voltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5451-Q1 also has an active Miller clamp function which can be used to prevent parasitic turnon of the external power transistor, because of Miller effect, for unipolar supply operation.

9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 Supply and Active Miller Clamp

The ISO5451-Q1 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of $V_{CC2}$ and $V_{EE2}$ for bipolar operation are 15 V and -8 V with respect to GND2.

For operation with unipolar supply, typically, $V_{CC2}$ is connected to 15 V with respect to GND2, and $V_{EE2}$ is connected to GND2. In this use case, the IGBT can turn-on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sank through a low impedance CLAMP transistor. Miller CLAMP is designed for miller current up to 2 A. When the IGBT is turned-off and the gate voltage transitions below 2 V the CLAMP current output is activated.

9.3.2 Active Output Pull-down

The Active output pulldown feature ensures that the IGBT gate OUT is clamped to $V_{EE2}$ to ensure safe IGBT off-state when the output side is not connected to the power supply.

9.3.3 Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication Output

Undervoltage Lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply $V_{CC1}$ drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN– and RST input till $V_{CC1}$ goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned-off, if the supply $V_{CC2}$ drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN– and RST input till $V_{CC2}$ goes above $V_{IT+(UVLO2)}$.

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply ($V_{CC1}$ or $V_{CC2}$), the RDY pin output goes low; otherwise, RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

9.3.4 Fault (FLT) and Reset (RST)

During IGBT overload condition, to report desaturation error FLT goes low. If RST is held low for the specified duration, FLT is cleared at rising edge of RST. RST has an internal filter to reject noise and glitches. By asserting RST for at-least the specified minimum duration, device input logic can be enabled or disabled.

9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUT and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUT and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.
9.4 Device Functional Modes

For ISO5451-Q1 OUT to follow IN+ in normal functional mode, RST and RDY must be in high state.

Table 1. Function Table\(^{(1)}\)

<table>
<thead>
<tr>
<th>(V_{CC1})</th>
<th>(V_{CC2})</th>
<th>(IN+)</th>
<th>(IN–)</th>
<th>(RST)</th>
<th>(RDY)</th>
<th>(OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PU</td>
<td>PD</td>
<td>X</td>
<td>X</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>PD</td>
<td>PU</td>
<td>X</td>
<td>X</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>PU</td>
<td>Open</td>
<td>X</td>
<td>X</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>PU</td>
<td>PU</td>
<td>Low</td>
<td>X</td>
<td>X</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>PU</td>
<td>PU</td>
<td>X</td>
<td>High</td>
<td>X</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>PU</td>
<td>PU</td>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

\(^{(1)}\) PU: Power Up \((V_{CC1} \geq 2.25 \text{ V}, V_{CC2} \geq 13 \text{ V})\), PD: Power Down \((V_{CC1} \leq 1.7 \text{ V}, V_{CC2} \leq 9.5 \text{ V})\), X: Irrelevant
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
The ISO5451-Q1 is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a microcontroller, and are at low voltage levels such as 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30 V (using unipolar output supply) to 15 V (using bipolar output supply), and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive needs to be applied with reference to the Emitter of the IGBT (source for MOSFET), and by construction, the Emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several hundreds of volts in magnitude.

The ISO5451-Q1 is thus used to level shift the incoming 3.3-V and 5-V control signals from the microcontroller to the 30-V (using unipolar output supply) to 15-V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

10.2 Typical Applications
Figure 42 shows the typical application of a three-phase inverter using six ISO5451-Q1 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as High-Voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5451-Q1. The switches are driven on and off at high switching frequency with specific patterns that to converter dc bus voltage to three-phase AC voltages.
Typical Applications (continued)

Figure 42. Typical Motor Drive Application

10.2.1 Design Requirements

Unlike optocoupler based gate drivers which need external current drivers and biasing circuitry to provide the input control signals, the input control to the device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain FLT output signal and RST input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. Table 2 shows the allowed range for Input and Output supply voltage, and the typical current output available from the gate-driver.

Table 2. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input supply voltage</td>
<td>3-V to 5.5-V</td>
</tr>
<tr>
<td>Unipolar output supply voltage (Vcc2 – GND2 = Vdc2 – Vee2)</td>
<td>15-V to 30-V</td>
</tr>
<tr>
<td>Bipolar output supply voltage (Vcc2 – Vee2)</td>
<td>15-V to 30-V</td>
</tr>
<tr>
<td>Bipolar output supply voltage (GND2 – Vee2)</td>
<td>0-V to 15-V</td>
</tr>
<tr>
<td>Output current</td>
<td>2.5-A</td>
</tr>
</tbody>
</table>

10.2.2 Detailed Design Procedure

10.2.2.1 Recommended ISO5451-Q1 Application Circuit

The ISO5451-Q1 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in Figure 43 shows a typical gate driver implementation with Unipolar Output Supply and Figure 44 shows a typical gate driver implementation with Bipolar Output Supply using the ISO5451-Q1.
A 0.1-μF bypass capacitor, recommended at input supply pin \( V_{CC1} \) and 1-μF bypass capacitor, recommended at output supply pin \( V_{CC2} \), provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode (\( D_{DST} \)) and its 1-kΩ series resistor are external protection components. The \( R_G \) gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain FLT output and RDY output has a passive 10-kΩ pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

**Figure 43. Unipolar Output Supply**

**Figure 44. Bipolar Output Supply**

### 10.2.2.2 FLT and RDY Pin Circuitry

There is 50k pullup resistor internally on FLT and RDY pins. The FLT and RDY pin is an open-drain output. A 10-kΩ pullup resistor can be used to make it faster rise and to provide logic high when FLT and RDY is inactive, as shown in Figure 45.

Fast common mode transients can inject noise and glitches on FLT and RDY pins due to parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the FLT and RDY pins.

**Figure 45. FLT and RDY Pin Circuitry for High CMTI**
10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5451-Q1. For maximum CMTI performance, the digital control inputs, IN+ and IN–, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5451-Q1 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. There is a 20 ns glitch filter which can filter a glitch up to 20 ns on IN+ or IN–.

10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the FLT output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

![Diagram of Local Shutdown and Reset](image)

Figure 46. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

10.2.2.5 Global- Shutdown and Reset

When configured for inverting operation, the ISO5451-Q1 can be configured to shutdown automatically in the event of a fault condition by tying the FLT output to IN+. For high reliability drives, the open drain FLT outputs of multiple ISO5451-Q1 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low FLT output disables all six gate drivers simultaneously.
10.2.2.6 Auto-Reset

In this case, the gate control signal at IN+ is also applied to the RST input to reset the fault latch every switching cycle. Incorrect RST makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the gate low state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before IN+ goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle.
### 10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

![Figure 49. DESAT Pin Protection with Series Resistor and Schottky Diode](image)

### 10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT diode’s function is to conduct forward current, allowing sensing of the IGBT’s saturated collector-to-emitter voltage, \( V_{(CESAT)} \), (when the IGBT is on) and to block high voltages (when the IGBT is off). During the short transition time when the IGBT is switching, there is commonly a high \( dV_{CE}/dt \) voltage ramp rate across the IGBT. This results in a charging current \( I_{(CHARGE)} = C_{(D-DESAT)} \times dV_{CE}/dt \), charging the blanking capacitor. \( C_{(D-DESAT)} \) is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with theblanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of \( 1 + C_{(BLANK)} / C_{(D-DESAT)} \).

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, \( V_F + V_{CE} = V_{(DESAT)} \), the \( V_{CE} \) level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: \( V_{CE-FAULT(TH)} = 9 \text{ V} - n \times V_F \) (where \( n \) is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.
10.2.2.9 Determining the Maximum Available, Dynamic Output Power, \( P_{\text{OD-max}} \)

The ISO5451-Q1 maximum allowed total power consumption of \( P_D = 251 \text{ mW} \) consists of the total input power, \( P_{\text{ID}} \), the total output power, \( P_{\text{OD}} \), and the output power under load, \( P_{\text{OL}} \):

\[
P_D = P_{\text{ID}} + P_{\text{OD}} + P_{\text{OL}}
\]  

(1)

With:

\[
P_{\text{ID}} = V_{\text{DC1-max}} \times I_{\text{CC1-max}} = 5.5 \text{ V} \times 4.5 \text{ mA} = 24.75 \text{ mW}
\]  

(2)

and:

\[
P_{\text{OD}} = (V_{\text{CC2}} - V_{\text{EE2}}) \times I_{\text{CC2-max}} = (15 \text{ V} - (-8 \text{ V})) \times 6 \text{ mA} = 138 \text{ mW}
\]  

(3)

then:

\[
P_{\text{OL}} = P_D - P_{\text{ID}} - P_{\text{OD}} = 251 \text{ mW} - 24.75 \text{ mW} - 138 \text{ mW} = 88.25 \text{ mW}
\]  

(4)

In comparison to \( P_{\text{OL}} \), the actual dynamic output power under worst case condition, \( P_{\text{OL-WC}} \), depends on a variety of parameters:

\[
P_{\text{OL-WC}} = 0.5 \times f_{\text{INP}} \times Q_G \times (V_{\text{CC2}} - V_{\text{EE2}}) \times \left( \frac{r_{\text{on-max}}}{r_{\text{on-max}} + R_G} + \frac{r_{\text{off-max}}}{r_{\text{off-max}} + R_G} \right)
\]

(5)

where

- \( f_{\text{INP}} \) = signal frequency at the control input \( \text{IN}^+ \)
- \( Q_G \) = power device gate charge
- \( V_{\text{CC2}} \) = positive output supply with respect to \( \text{GND2} \)
- \( V_{\text{EE2}} \) = negative output supply with respect to \( \text{GND2} \)
- \( r_{\text{on-max}} \) = worst case output resistance in the on-state: 4 \( \Omega \)
- \( r_{\text{off-max}} \) = worst case output resistance in the off-state: 2.5 \( \Omega \)
- \( R_G \) = gate resistor

Once \( R_G \) is determined, Equation 5 is to be used to verify whether \( P_{\text{OL-WC}} < P_{\text{OL}} \). Figure 50 shows a simplified output stage model for calculating \( P_{\text{OL-WC}} \):

Figure 50. Simplified Output Model for Calculating \( P_{\text{OL-WC}} \)

10.2.2.10 Example

This example considers an IGBT drive with the following parameters:

\[
I_{\text{ON-PK}} = 2 \text{ A}, Q_G = 650 \text{ nC}, f_{\text{INP}} = 20 \text{ kHz}, V_{\text{CC2}} = 15 \text{ V}, V_{\text{EE2}} = -8 \text{ V}
\]  

(6)

Apply the value of the gate resistor \( R_G = 10 \text{ \( \Omega \))} \).
Then, calculating the worst-case output power consumption as a function of $R_G$, using Equation 5 $r_{on-max}$ = worst case output resistance in the on-state: $4\Omega$, $r_{off-max}$ = worst case output resistance in the off-state: $2.5\Omega$, $R_G$ = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20 \text{ kHz} \times 650 \text{ nC} \times (15 \text{ V} - (-8 \text{ V})) \times \left(\frac{4 \Omega}{4 \Omega + 10 \Omega} + \frac{2.5 \Omega}{2.5 \Omega + 10 \Omega}\right) = 72.61 \text{ mW}$$

(7)

Because $P_{OL-WC} = 72.61 \text{ mW}$ is below the calculated maximum of $P_{OL} = 88.25 \text{ mW}$, the resistor value of $R_G = 10 \Omega$ is suitable for this application.

10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 51) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/D45VH10 pair for up to 15 A maximum.

![Figure 51. Current Buffer for Increased Drive Current](image)

10.2.3 Application Curves

![Figure 52. Normal Operation - Bipolar Supply](image)

![Figure 53. Normal Operation - Unipolar Supply](image)
11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input supply pin \( V_{CC1} \) and 1-μF bypass capacitor is recommended at output supply pin \( V_{CC2} \). The capacitors should be placed as close to the supply pins as possible. The recommended placement of capacitors is 2-mm maximum from input and output power supply pin \( (V_{CC1} \text{ and } V_{CC2}) \).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 54). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUT and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch². On the gate-driver \( V_{EE2} \) and \( V_{CC2} \) can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For detailed layout recommendations, see the Digital Isolator Design Guide (SLLA284).

12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.3 Layout Example

![Figure 54. Recommended Layer Stack](image-url)
13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation
For related documentation see the following:
• Isolation Glossary (SLLA353)
• ISO5851 Evaluation Module (EVM) User’s Guide (SLLU218)
• Digital Isolator Design Guide (SLLA284)

13.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™ Online Community TI’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.
EXAMPLE BOARD LAYOUT

DW0016B
SOIC - 2.65 mm max height

SOIC

SOLDER MASK DETAILS

METAL
SOLDER MASK OPENING
0.07 MAX
ALL AROUND
NON SOLDER MASK DEFINED

SOLDER MASK OPENING
METAL
0.07 MIN
ALL AROUND
SOLDER MASK DEFINED

NOTES: (continued)
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO5451QDWQ1</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>ISO5451Q</td>
<td>Samples</td>
</tr>
<tr>
<td>ISO5451QDWRQ1</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>ISO5451Q</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO5451-Q1 :

- Catalog: ISO5451

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO5451DWRQ1</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>10.75</td>
<td>10.7</td>
<td>2.7</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

---

*Dimensions designed to accommodate the component width*

*Dimension designed to accommodate the component length*

*Dimension designed to accommodate the component thickness*

*Overall width of the carrier tape*

*Pitch between successive cavity centers*
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO5451QDWRQ1</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING Datasheets), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated