JFE2140 Ultra-Low Noise, Matched, Dual, Low-Gate Current, Discrete, Audio, N-Channel JFET

1 Features

- Ultra-low noise:
  - Voltage noise:
    - 0.9 nV/√Hz at 1 kHz, $I_{DS} = 5$ mA
    - 1.1 nV/√Hz at 1 kHz, $I_{DS} = 2$ mA
  - Current noise: 1.6 fA/√Hz at 1 kHz
- Low $V_{GS}$ mismatch: 4 mV (max)
- Low gate current: 10 pA (max)
- Low input capacitance: 13 pF at $V_{DS} = 5$ V
- High gate-to-drain and gate-to-source breakdown voltage: –40 V
- High transconductance: 30 mS
- Packages: SOIC, 2-mm × 2-mm WSON (Preview)

2 Applications

- Microphone inputs
- Hydrophones and marine equipment
- DJ controllers, mixers, and other DJ equipment
- Professional audio mixer or control surface
- Guitar amplifier and other music instrument amplifier
- Condition monitoring sensor

3 Description

The JFE2140 is a Burr-Brown™ matched-pair discrete JFET built using Texas Instruments' modern, high-performance, analog bipolar process. The JFE2140 features performance not previously available in older discrete JFET technologies. The JFE2140 offers excellent noise performance across all current ranges, where the quiescent current can be set by the user from 50 μA to 20 mA. When biased at 5 mA, the device yields 0.9 nV/√Hz of input-referred noise, giving ultra-low noise performance with extremely high input impedance (> 1 TΩ). In addition, the matching between JFETs is tested to ±4 mV, ensuring low offset and high CMRR performance for differential pair configurations. The JFE2140 also features integrated diodes connected to separate clamp nodes to provide protection without the addition of high leakage, nonlinear external diodes.

The JFE2140 can withstand a high drain-to-source voltage of 40-V, as well as gate-to-source and gate-to-drain voltages down to –40 V. The temperature range is specified from –40°C to +125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFE2140</td>
<td>WSON (8) - Preview</td>
<td>2.00 mm × 2.00 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.90 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.

Device Summary

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GSS}$ (Gate-to-source voltage)</td>
<td>–40 V</td>
</tr>
<tr>
<td>$V_{DSS}$ (Drain-to-source voltage)</td>
<td>±40 V</td>
</tr>
<tr>
<td>$C_{GS}$ (Input capacitance)</td>
<td>13 pF</td>
</tr>
<tr>
<td>$V_{GSS1} - V_{GSS2}$ (Differential gate-to-source voltage matching)</td>
<td>±4 mV</td>
</tr>
<tr>
<td>$T_J$ (Junction temperature)</td>
<td>–40°C to +125°C</td>
</tr>
<tr>
<td>$I_{DSS}$ (Drain-to-source saturation current)</td>
<td>18 mA</td>
</tr>
</tbody>
</table>

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
Table of Contents

1 Features ......................................................... 1
2 Applications .................................................. 1
3 Description .................................................... 1
4 Revision History .............................................. 2
5 Pin Configuration and Functions ......................... 3
6 Specifications .................................................. 4
   6.1 Absolute Maximum Ratings ......................... 4
   6.2 ESD Ratings ............................................. 4
   6.3 Recommended Operating Conditions ............... 4
   6.4 Thermal Information .................................. 4
   6.5 Electrical Characteristics ......................... 5
   6.6 Typical Characteristics .............................. 6
7 Parameter Measurement Information ................... 9
   7.1 AC Measurement Configurations .................... 9
8 Detailed Description ....................................... 10
   8.1 Overview ............................................... 10
   8.2 Functional Block Diagram ......................... 10
   8.3 Feature Description ................................. 10
8.4 Device Functional Modes .............................. 11
9 Application and Implementation ....................... 12
   9.1 Application Information ............................. 12
   9.2 Typical Applications ............................... 16
10 Power Supply Recommendations ..................... 19
11 Layout ....................................................... 19
   11.1 Layout Guidelines .................................. 19
   11.2 Layout Example ..................................... 19
12 Device and Documentation Support .................... 20
   12.1 Device Support ....................................... 20
   12.2 Documentation Support ............................ 21
   12.3 Receiving Notification of Documentation Updates .. 21
   12.4 Support Resources .................................. 21
   12.5 Trademarks .......................................... 21
   12.6 Electrostatic Discharge Caution ................... 21
   12.7 Glossary ............................................. 21
13 Mechanical, Packaging, and Orderable Information .... 21

4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>August 2021</td>
<td>*</td>
<td>Initial release</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

Figure 5-1. D (8-Pin SOIC) Package, Top View

Figure 5-2. DSG (8-Pin WSON, Preview) Package, Top View

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>D1</td>
<td>2</td>
<td>2 O Drain, channel 1</td>
</tr>
<tr>
<td>D2</td>
<td>6</td>
<td>6 O Drain, channel 2</td>
</tr>
<tr>
<td>G1</td>
<td>4</td>
<td>4 I Gate, channel 1</td>
</tr>
<tr>
<td>G2</td>
<td>8</td>
<td>8 I Gate, channel 2</td>
</tr>
<tr>
<td>S1</td>
<td>1</td>
<td>1 O Source, channel 1</td>
</tr>
<tr>
<td>S2</td>
<td>5</td>
<td>5 O Source, channel 2</td>
</tr>
<tr>
<td>VCH</td>
<td>3</td>
<td>3 — Positive diode clamp voltage. Float this pin if clamp diodes are not used.</td>
</tr>
<tr>
<td>VCL</td>
<td>7</td>
<td>7 — Negative diode clamp voltage. Float this pin if clamp diodes are not used.</td>
</tr>
<tr>
<td>Thermal Pad</td>
<td>Thermal Pad</td>
<td>— Exposed thermal pad. This pad is internally connected to the V_CL node. Connect this pad to the same node as V_CL or leave floating.</td>
</tr>
</tbody>
</table>
6 Specifications
6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)(1) (2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DS}</td>
<td>Drain-to-source voltage</td>
<td>–40</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>V_{GS}, V_{GD}</td>
<td>Gate-to-source voltage, gate-to-drain voltage</td>
<td>–40</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td>V_{VCH}</td>
<td>Voltage between VCH to D, G, or S</td>
<td>–40</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>V_{VCL}</td>
<td>Voltage between VCL to D, G, or S</td>
<td>–40</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>I_{VCH}, I_{VCL}</td>
<td>Clamp diode current</td>
<td>DC</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50-ms pulse(3)</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>I_{DS}</td>
<td>Drain-to-source current</td>
<td>–50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>I_{GS}, I_{GD}</td>
<td>Gate-to-source, gate-to-drain current</td>
<td>–20</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>T_A</td>
<td>Ambient temperature</td>
<td>–55</td>
<td>150</td>
<td>ºC</td>
</tr>
<tr>
<td>T_J</td>
<td>Junction temperature</td>
<td>–55</td>
<td>150</td>
<td>ºC</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage temperature</td>
<td>–55</td>
<td>175</td>
<td>ºC</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All gate, drain and source voltages are referred to the same-channel JFET (that is, V_{GS} applies to both V_{G1S1} and V_{G2S2}).

(3) Maximum diode current pulse specified for 50 ms at 1% duty cycle.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{(ESD)}</td>
<td>Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101(2)</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{DS}</td>
<td>Drain-to-source current</td>
<td>0.02</td>
<td>I_{DSS}</td>
<td>mA</td>
</tr>
<tr>
<td>V_{GS}</td>
<td>Gate-to-source voltage</td>
<td>–1.2</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>T_J</td>
<td>Specified temperature</td>
<td>–40</td>
<td>+125</td>
<td>ºC</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>JFE2140</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JJA}</td>
<td>Junction-to-ambient thermal resistance</td>
<td>139.8</td>
</tr>
<tr>
<td>R_{JJA(top)}</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>80.0</td>
</tr>
<tr>
<td>R_{JJB}</td>
<td>Junction-to-board thermal resistance</td>
<td>83.2</td>
</tr>
<tr>
<td>\psi_{JT}</td>
<td>Junction-to-top characterization parameter</td>
<td>29.1</td>
</tr>
<tr>
<td>\psi_{JB}</td>
<td>Junction-to-board characterization parameter</td>
<td>82.4</td>
</tr>
<tr>
<td>R_{JJA(bot)}</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

at $T_A = 25°C$, $I_{DS} = 2 mA$, $V_{DS} = 10 V$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$e_n$</td>
<td>Input-referred noise</td>
<td>$I_{DS} = 100 \mu A$</td>
<td>$f = 1 kHz$</td>
<td>2.5</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{DS} = 2 mA$</td>
<td>$f = 0.1 Hz$ to 10 Hz</td>
<td>0.26</td>
<td>µVpp</td>
</tr>
<tr>
<td>$e_i$</td>
<td>Input current noise, each input</td>
<td>$I_{DS} = 2 mA$, $V_{DS} = 5 V$</td>
<td>$f = 1 kHz$</td>
<td>1.6</td>
<td>fA/√Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.12</td>
<td></td>
</tr>
</tbody>
</table>

| INPUT CURRENT | $V_{DS} = 2 V$, $V_{VCH} = 5 V$, $V_{VCL} = -5 V$ | 1 | ±10 | pA |
|              | $V_{DS} = 0 V$, $V_{GS} = -30 V$ | 0.2 | ±60 | pA |
|              | $T_A = -40°C$ to $+85°C$ | 0.85 | nA |

| INPUT VOLTAGE | $V_{GS} = 0 V$, $I_{D} = -100 \mu A$ | $-40$ | V |
|              | $V_{GS} = 10 V$, $I_{D} = 0.1 \mu A$ | $-1.5$ | $-1.15$ | $-0.9$ | V |
|              | $I_{DS} = 100 \mu A$ | $-1.2$ | $-0.85$ | $-0.7$ | V |
|              | $I_{DS} = 2 mA$ | $-0.9$ | $-0.6$ | $-0.5$ | V |
|              | $T_A = -40°C$ to $+125°C$ | 1.1 | 4.2 | mV |

| INPUT IMPEDANCE | $V_{GS} = -30 V$ to $-1 V$, $V_{DS} = 0 V$ | 1 | TΩ |
|                 | $V_{DS} = 0 V$ | 17 | pF |
|                 | $V_{DS} = 5 V$ | 13 |      |

| OUTPUT | $V_{GS} = 0 V$ | 12 | 18 | 23 | mA |
|        | $T_A = -40°C$ to $+125°C$ | 10 | 28 |    |
|        | $V_{GS} = 0 V$, $I_{DSS1} / I_{DSS2}$ | 0.95 | 1 | 1.05 | 
|        | $I_{D} = 100 \mu A$ | 2.1 | mS |
|        | $I_{D} = 2 mA$ | 10 |      |
|        | $V_{GS} = 0 V$ | 24 | 30 | mS |
| $G_{FS}$ | Full conduction transconductance | $I_D = 100 \mu A$ | 40 | 43 | V |
| $C_{DSS}$ | Output capacitance | $I_D = 2 mA$ | 4.5 | pF |
6.6 Typical Characteristics

at $T_A = 25^\circ$C, $I_{DS} = 2$ mA, common-source configuration, and $V_{DS} = 10$ V (unless otherwise noted)

![Figure 6-1. Drain-to-Source Current vs Gate-to-Source Voltage](image1)

![Figure 6-2. Drain-to-Source Current vs Drain-to-Source Voltage](image2)

![Figure 6-3. Drain-to-Source Current vs Drain-to-Source Voltage](image3)

![Figure 6-4. Common Source Transconductance vs Drain-to-Source Current](image4)

![Figure 6-5. Common Source Transconductance vs Drain-to-Source Voltage](image5)

![Figure 6-6. Gate Current vs Drain-to-Source Voltage](image6)
6.6 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $I_{DS} = 2$ mA, common-source configuration, and $V_{DS} = 10$ V (unless otherwise noted)

Figure 6-7. Gate Current vs Gate-to-Source Voltage

Figure 6-8. Gate-to-Source Voltage vs Temperature

Figure 6-9. $I_{DS}$ vs Drain-to-Source Voltage

Figure 6-10. $V_{GS}$ Mismatch Histogram

Figure 6-11. $V_{GS}$ Mismatch vs Drain-to-Source Current

Figure 6-12. $V_{GS}$ Mismatch vs Temperature
6.6 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $I_{DS} = 2 \ mA$, common-source configuration, and $V_{DS} = 10 \ V$ (unless otherwise noted)

---

**Figure 6-13.** $V_{GS}$ Mismatch vs $V_{DS}$

**Figure 6-14.** Input-Referred Noise Density vs Frequency

**Figure 6-15.** Noise Density Contributors vs Input Gate Resistance

**Figure 6-16.** Input-Referred Noise Spectral Density vs Drain-to-Source Current

**Figure 6-17.** Input, Output, and Reverse Transfer Capacitance vs Drain-to-Source Voltage
7 Parameter Measurement Information

7.1 AC Measurement Configurations

The circuit configuration used for noise measurements is seen in Figure 7-1. The nominal $I_{DS}$ current is configured in the schematic by calibrating $V^-$. After $I_{DS}$ is fixed, the $V_{DS}$ voltage is set by calibrating $V^+$. For input-referred noise data, the gain of the circuit is calibrated from $V_{IN}$ to $V_{OUT}$ and used for the input-referred gain calculation.

![Figure 7-1. AC Measurement Reference Schematic](image-url)
8 Detailed Description

8.1 Overview

The JFE2140 is a ultra-low noise, matched-input pair N-type JFET designed to create low-noise gain stages for very high output impedance sensors or microphones. Advanced, high precision processing technology gives the JFE2140 tight channel-to-channel matching, extremely low-noise performance, a high gm/Ciss ratio, and ultra-low gate-current performance. The integrated Input-protection diodes clamp high-voltage spurious input signals without the need for additional input diodes that can add leakage current or distortion-creating nonlinear capacitance. The JFE2140 provides a next-generation device to implement low-noise amplifiers for piezoelectric sensors, transducers, large-area condenser microphones, and hydrophones in small-package options.

8.2 Functional Block Diagram

![Functional Block Diagram](image)

8.3 Feature Description

8.3.1 Precision Matching

The JFE2140 features matched-pair, n-type JFET transistors fabricated on a high-precision analog process. Precision matching between opposite JFETs is required in differential-pair configurations, where any mismatch between input devices results in gain and common-mode rejection degradation. Precision matching also minimizes offset voltages that produce excessive error voltages in high-gain, dc-coupled composite amplifiers. Matching distribution for a production lot of units can be seen in Figure 6-10.

8.3.2 Ultra-Low Noise

Junction field effect transistors (JFETs) are commonly used as an input stage in high-input-impedance, low-noise designs in audio, SONAR, vibration analysis, and other technologies. The JFE2140 is a new generation JFET device that offers very low noise performance at the lowest possible current consumption in high-input-impedance amplifier designs. The JFE2140 is manufactured on a high-performance analog process technology, giving tighter process parameter control than a standard JFET.

Designs that feature operational amplifiers (op amps) as the primary gain stage are common, but these designs are not able to achieve the lowest possible noise as a result of the inherent challenges and tradeoffs required from a full operational amplifier design. Noise in JFET designs can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less than 100 Hz. The JFE2140 achieves extremely low 1/f noise in this range. Thermal noise is noise in the region greater than 1 kHz and depends on the gain, or gm, of the circuit. The gm is a function of the drain-to-source bias current; therefore, thermal noise is also a function of drain-to-source bias current. Figure 6-14 shows both 1/f and thermal noise with multiple bias conditions measured using the circuit shown in Figure 7-1.

Noise is typically modeled as a voltage source (voltage noise) and current source (current noise) on the input. The 1/f and thermal noise can be represented as voltage noise. Current noise is dominated by current flow into the gate, and is called shot noise. The JFE2140 features extremely low gate current, and therefore, extremely low current noise. Figure 6-15 shows how source impedance on the input is the dominant noise source. In nearly all cases, noise created as a result of current noise is negligible.
8.3.3 Low Gate Current

The JFE2140 features a maximum gate current of 10 pA at room temperature, making the device an excellent choice for maximizing the gain and dynamic range from extremely high impedance sensors. Additionally, any noise contributions as a result of gate current are minimized because of the negligible shot noise at low current levels. As with all JFET devices, when the drain-to-source voltage increases, the gate current also increases. Keep the drain-to-source voltage to less than 5 V for the lowest gate input current operation.

8.3.4 Input Protection

The JFE2140 features input protection diodes that are used for surge clamping and ESD events. The diodes are rated to withstand high current surges for short times, steering current from the gate (G) pin to the VCH and VCL pins. The diodes also feature very low leakage, removing the need for external protection devices that may have high leakage currents or nonlinear capacitance that degrade the distortion performance.

8.4 Device Functional Modes

The JFE2140 functionality is identical to standard N-channel depletion JFET devices. The gate-to-source (\(V_{GS}\)) voltage, drain-to-source voltage (\(V_{DS}\)) and drain-to-source current (\(I_{DS}\)) determine the region of operation.

- For \(V_{GS} < V_{GSC}\): JFE2140 conduction channel is closed; \(I_{DS}\) is only determined by junction leakage current.
- For \(V_{GS} > V_{GSC}\): Two modes of operation can exist depending on \(V_{DS}\). When \(V_{DS}\) is less than the linear (saturation) region threshold (see Figure 8-1), the device operates in the linear region, meaning that the device behaves as a resistor connected from drain-to-source with minimal variation from any changes in \(V_{GS}\). When \(V_{DS}\) is greater than the linear (saturation) region threshold, \(I_{DS}\) has a strong dependence on \(V_{GS}\), where the relationship is described by the parameter \(g_m\).

---

**Figure 8-1.** \(V_{DS} vs I_{DS}\)
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Protection Diodes

The JFE2140 features diodes that are used to help clamp voltage surges that can occur on the input sensor to the gate. The diodes are connected between the gates, sources, and drains of each JFET to two separate pins, VCL and VCH. The clamping mechanism works by steering current from the gate into the VCL or VCH nodes when the voltage at the gate, source or drain is less than VCL or greater than VCH. Figure 9-1 shows an example of a microphone input circuit where a dc blocking capacitor operates with a large dc voltage. When the microphone input is dropped or shorted, the dc blocking capacitor discharges into the VCL or VCH nodes, thus helping eliminate large signal transient voltages on the gate. There are also clamping diodes from the drain and source to VCL and VCH, respectively. The clamping diodes can withstand high surge currents up to 200 mA for 50 ms; however, limit dc current to less than 20 mA.

![Figure 9-1. JFE2140 Clamping Diode Example](image-url)

The example in Figure 9-1 shows the diode clamp used to protect the JFET against overvoltage in a phantom-powered microphone circuit. Phantom power typically delivers 48 V through a 6.8-kΩ pullup resistor to a microphone or dynamic load. If the microphone is disconnected, dc blocking capacitor $C_{DC}$ can be biased up to 48 V. If the input to the capacitor is then shorted to ground (shown by the switch in Figure 9-1), the gate voltage can exceed the absolute maximum rating for $V_{GS}$. In this case, the blocking diode is used, along with current limiting resistors $R_G$ and $R_L$, to clamp the gate voltage to a safe level. Be aware that the thermal noise of $R_G$ couples directly into the gate input; therefore, make sure to minimize the resistance of $R_G$.

The clamping diodes are not required for operation. The $V_{GS}$ voltage can withstand $-40$ V, so clamping is not required if the $V_{GS}$ voltage is kept greater than this limit. If the diodes are not needed, leave the VCL and VCH nodes floating.
9.1.2 Cascode Configuration

The JFE2140 can be configured as a cascoded JFET front end. Cascode refers to using a second transistor in-series with the input transistor; see Figure 9-2 for an example.

![Figure 9-2. JFE2140 connected in Cascode Configuration](image)

Using a cascode configuration, as shown in Figure 9-2, increases the output impedance of the stage, resulting in higher gain, as well as buffers the input node from gate current that flows when the $V_{DS}$ voltages are higher. The $V_{BIAS}$ node must be forced to a voltage greater than what is required to allow both JFETs to remain in the saturated region. A JFET is not required to be used as the cascode device; the benefits of cascoding can be realized with other transistor types, while still maintaining the low-noise, high-impedance benefits of the JFE2140.

9.1.3 Common-Source Amplifier

The common-source amplifier is a commonly used open-loop gain stage for JFET amplifiers, the basic circuit is shown in Figure 9-3.

![Figure 9-3. Common-Source Amplifier](image)

The equation for gain of the circuit in Figure 9-3 is shown in Equation 1.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{g_{m}R_{D}}{1 + g_{m}R_{S}}$$

(1)

Generally, higher gain results in improved noise performance. Gain increases as the bias current is increased as a result of increasing $g_{m}$ (see Figure 6-4). As a result, the input-referred noise decreases as bias current is increased (see Figure 6-14). Any JFET design must make a tradeoff between current consumption and noise performance. The JFE2140, however, delivers significantly lower noise performance than most operational...
amplifiers at the same current consumption. The bias current (I_{DS}) is set by the value of the source resistor, R_S, and the threshold voltage, V_T, of the JFE2140. A graph showing nominal I_{DS} vs R_S is shown in Figure 9-4.

![Graph showing nominal I_{DS} vs R_S, V_{DS} = 5 V](image)

**Figure 9-4. Drain-to-Source Current vs R_S, V_{DS} = 5 V**

The bias current varies according to the resistor and threshold voltage tolerances. Additionally, thermal noise associated with R_S couples directly into the gain of the circuit, degrading the overall noise performance. To improve the circuit in Figure 9-5, use a current-source biasing scheme. Current-source biasing removes the JFET threshold variation from the biasing scheme, and allows for lower-value filtering capacitance (C_S) for equivalent filtering due to the high output impedance of current sources.

![Common-Source Amplifier With Current-Source Biasing](image)

**Figure 9-5. Common-Source Amplifier With Current-Source Biasing**
9.1.4 Composite Amplifiers

The JFE2140 can be configured to provide a low-noise, high-input impedance front-end stage for a typical op amp. Open-loop transistor gain stages shown previously suffer from wide gain variations that are dependent on the forward transconductance of the JFE2140. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results by allowing for a fixed gain determined by external resistors, and improving the noise and bandwidth of the operational amplifier. The JFE2140 gain stage provides a boost to the open-loop performance of the system, extending the bandwidth beyond what the operational amplifier alone can provide, and gives a high-input impedance, ultra-low noise input stage to interface with high source impedance microphones.

Figure 9-6 shows a generic schematic representation of a voltage-feedback composite amplifier. The component requirements and tradeoffs are listed in Table 9-1.

The gain of Figure 9-6 can be calculated using the equation below.

\[ A = 1 + \frac{R_{F1}}{R_{F2}} \]  

\[ (2) \]

**Table 9-1. Composite Amplifier Component List and Function**

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{S1}</td>
<td>Degeneration resistors. These resistors reduce the overall gain of the JFET stage, however, improve the linearity performance. Also, when used in differential configurations (see OPA1637 reference design) they will reduce CMRR errors that occur as a result of input mismatch voltages.</td>
</tr>
<tr>
<td>R_{S2}</td>
<td>Bias-current setting resistor. This resistor, along with R_{S1}, determine the bias current when using resistive biasing (see Figure 9-4). Note both R_{S1} and R_{S2} resistance will directly impact noise performance.</td>
</tr>
<tr>
<td>R_{G}</td>
<td>Gate resistor. Can be used to help limit current flow into gate in overvoltage cases. For improved DC precision, match R_{G} to the equivalent parallel resistance of R_{S1}</td>
</tr>
<tr>
<td>R_{D}</td>
<td>Drain resistor. Sets gain of JFET stage in common source biasing, along with gm and R_{S1} + R_{S2}. Higher resistance will increase gain, however will lower the nominal V_{DS} voltage.</td>
</tr>
<tr>
<td>R_{F1}</td>
<td>Feedback resistor 1. Along with R_{F2}, sets the gain of the composite amplifier.</td>
</tr>
<tr>
<td>R_{F2}</td>
<td>Feedback resistor 2. Along with R_{F1}, sets the gain of the composite amplifier.</td>
</tr>
<tr>
<td>R_{S2}</td>
<td>Source resistor 2. Along with R_{S1}, sets the DC bias current where the JFET is nominally operated.</td>
</tr>
<tr>
<td>C_{S}</td>
<td>Source capacitor. Reduces the noise coupling from R_{S2}.</td>
</tr>
</tbody>
</table>
9.2 Typical Applications

9.2.1 Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

The JFE2140 can be configured to provide a low-noise, high-input impedance single-ended amplifier stage that can be optimized for ultra-low noise performance at low power levels. This configuration is designed for battery-powered audio applications such as guitar pedals, amplifiers and handheld recorders. The OPA1692, a low-power, dual audio amplifier, is used for the composite voltage-feedback amplifier, as well as a rail-splitting amplifier that centers the ground voltage between the battery positive and negative voltage.

![Diagram of Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier]

Figure 9-7. Low-Noise, Low-Power, High-Input-Impedance Composite Amplifier

9.2.1.1 Design Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN GOAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>15 dB to 40 dB nominal with low-frequency boost</td>
</tr>
<tr>
<td>Frequency response</td>
<td>1 Hz to 20 kHz</td>
</tr>
<tr>
<td>Noise</td>
<td>&lt; 3 nV/√Hz at 1 kHz</td>
</tr>
<tr>
<td>Total current consumption</td>
<td>&lt; 4 mA</td>
</tr>
<tr>
<td>Input current</td>
<td>&lt; 100 pA</td>
</tr>
</tbody>
</table>
9.2.1.2 Detailed Design Procedure

This design provides single-ended, adjustable gain from 15 dB to 40 dB with extremely high input impedance at a very low frequency response. The power consumption is optimized for battery-powered audio applications.

- The JFE2140 is configured as a differential pair in a voltage-feedback composite amplifier. This configuration allows for low-frequency gain without large dc-blocking capacitors.
- The bias current is set by selecting the desired bias current and noise tradeoff (see Figure 6-16). To set the bias current point, adjust the source resistance according to Figure 9-4.
- After the bias current is selected, set the JFET stage gain as high as possible. To avoid pushing the device into the linear region of operation, use the largest drain resistor (RD1,2) possible while maintaining a minimum of 1 V across the drain-to-source nodes.
- The overall gain can be configured with the feedback resistors RF1, RF2 and RF3. Capacitor CF3 may be required depending on the gain configuration for amplifier stability; use amplifier stability best practices to maintain stability at both maximum and minimum gain configurations.

9.2.1.3 Application Curves

| Figure 9-8. Gain/Phase | Figure 9-9. Input-Referred Noise Density |
9.2.2 Differential Front-End Design

Differential pair architectures are useful for differential small signal amplification where high common-mode voltage rejection (CMRR) is required. In typical differential amplifiers or fully-differential amplifiers (FDA), the tolerance of the resistors alone dominates the CMRR performance. In addition, these amplifiers cannot be configured with high input impedance because of the requirement of input resistors. When used on the front-end of an FDA, the precision-matching on the JFE2140 removes the requirement of extremely low resistor matching (< 1%) by creating a matched-input gain stage. In addition, high input impedance significantly reduces the effects of source impedance mismatch on CMRR performance, creating a differential input designed for noisy environments that are common in professional audio.

Figure 9-10. The JFE2140 as a High Input Impedance Front End for the OPA1637

9.2.2.1 Application Curves

Figure 9-11. Gain and Phase vs Frequency

Figure 9-12. CMRR vs Frequency
10 Power Supply Recommendations

The JFE2140 is a dual, matched JFET transistor pair with clamping diodes. There are no specific power-supply connections; however, take care not to exceed any absolute maximum voltages on any of the pins if system supply voltages greater than or equal to 40 V are used.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Keep high impedance input signals away from noisy traces.
- Make sure supply voltages are adequately filtered.
- Minimize distance between source-connected and drain-connected components to the JFE2140.
- Consider a driven, low-impedance guard ring around the critical gate traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

![JFE2140 Layout Example: Differential Pair Configuration](image-url)

Figure 11-1. JFE2140 Layout Example: Differential Pair Configuration
12 Device and Documentation Support
12.1 Device Support
12.1.1 Development Support

12.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully functional version of the TINA software, preloaded with a library of macro models, in addition to a range of both passive and active models. TINA-TI software provides all the conventional dc, transient, and frequency domain analyses of SPICE, as well as additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.
12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers data sheet
- Texas Instruments, OPAx210 2.2-nV/√Hz Precision, Low-Power, 36-V Operational Amplifiers data sheet
- Texas Instruments, OPA1692 Low-Power, Low-Noise and Low-Distortion SoundPlus™ Audio Operational Amplifiers data sheet
- Texas Instruments, OPAx197 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage Operational Amplifiers data sheet

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

Burr-Brown™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments. TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc. WEBENCH® is a registered trademark of Texas Instruments. All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFE2140DR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>JF2140</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Addendum-Page 1
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**: 
- **Reel Width (W1)**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFE2140DR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFE2140DR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https://www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated