

# LF412QML Low Offset, Low Drift Dual JFET Input Operational Amplifier

Check for Samples: [LF412QML](#)

## FEATURES

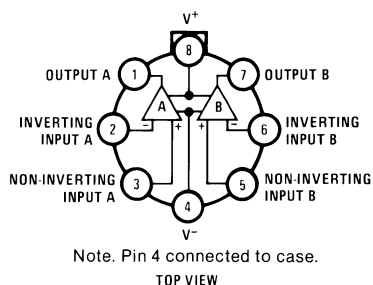
- **Input Offset Voltage Drift:** 20  $\mu\text{V}/^\circ\text{C}$  (Max)
- **Low Input Bias Current:** 50 pA (Typ)
- **Low Input Noise Current:** 0.01 pA/ $\sqrt{\text{Hz}}$  (Typ)
- **Wide Gain Bandwidth:** 2.7 MHz (Min)
- **High Slew Rate:** 8V/ $\mu\text{s}$  (Min)
- **High Input Impedance:**  $10^{12}\Omega$
- **Low Total Harmonic Distortion** <0.02%
- **Low 1/f Noise Corner:** 50 Hz
- **Fast Settling Time to 0.01%:** 2  $\mu\text{s}$

## DESCRIPTION

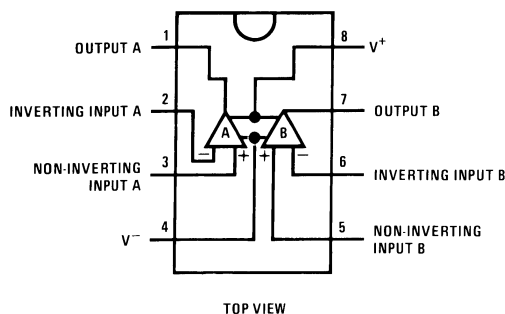
This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and ensured input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

## Connection Diagram



**Figure 1. TO-99 Package**



**Figure 2. CDIP Package**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## Simplified Schematic

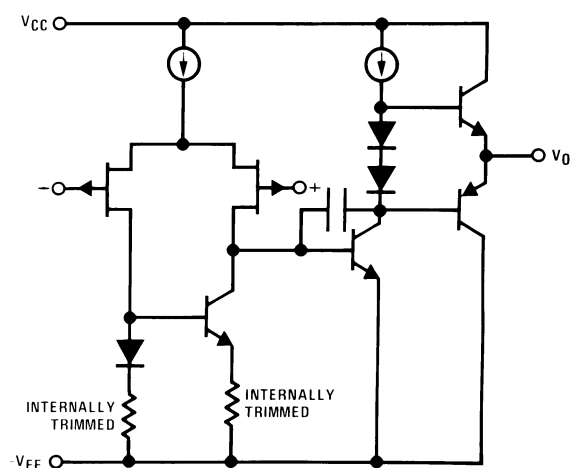
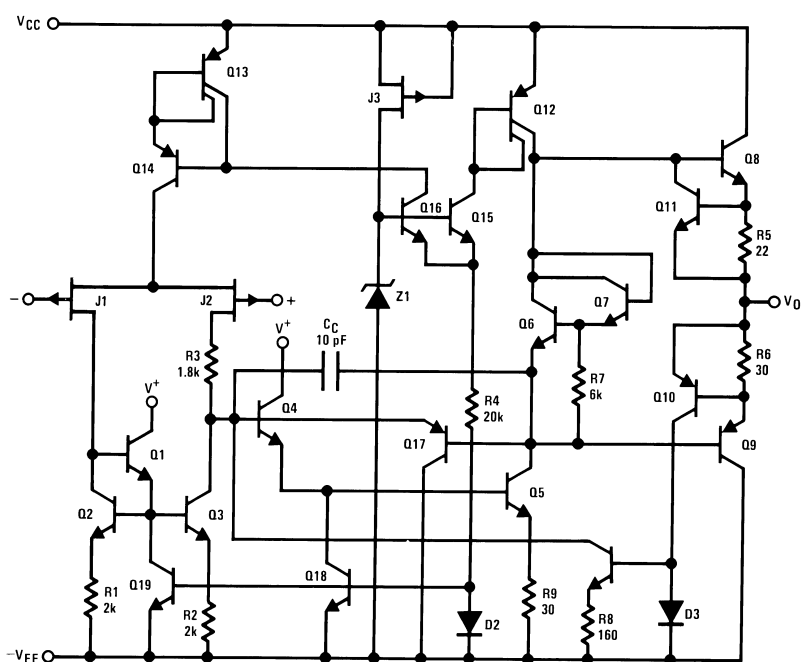


Figure 3. 1/2 Dual

## Detailed Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage			±18V
Differential Input Voltage			±30V
Input voltage Range <sup>(2)</sup>			±15V
Output Short Circuit Duration <sup>(3)</sup>			Continuous
Power Dissipation <sup>(4)</sup>		TO-99 Package	800mW
		CDIP Package	800mW
T <sub>Jmax</sub>			150°C
Thermal Resistance	θ <sub>JA</sub>	TO-99 Package (Still Air)	160°C/W
		TO-99 Package (500 LF/Min Air Flow)	83°C/W
		CDIP Package (Still Air)	122°C/W
		CDIP Package (500 LF/Min Air Flow)	66°C/W
	θ <sub>JC</sub>	TO-99 Package	38°C/W
		CDIP Package	15°C/W
Supply voltage Range			±5V to ±15V
Operating Temperature Range			-55°C ≤ T <sub>A</sub> ≤ 125°C
Storage Temperature Range			-65°C ≤ T <sub>A</sub> ≤ 150°C
Lead Temperature Soldering (10 Sec)			260°C
ESD Tolerance <sup>(5)</sup>			1,700V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- (3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>Jmax</sub> (maximum junction temperature), θ<sub>JA</sub> (package junction to ambient thermal resistance), and T<sub>A</sub> (ambient temperature). The maximum allowable power dissipation at any temperature is P<sub>Dmax</sub> = (T<sub>Jmax</sub> - T<sub>A</sub>)/θ<sub>JA</sub> or the number given in the Absolute Maximum Ratings, whichever is lower.
- (5) Human body model, 1.5 kΩ in series with 100 pF.

## Quality Conformance Inspection

**Table 1. Mil-Std-883, Method 5005 - Group A**

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

## Electrical Characteristics DC parameters

The following conditions apply, unless otherwise specified.  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
$V_{IO}$	Input offset Voltage	$R_S = 10K\Omega$		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient of Input Offset Voltage	$R_S = 10K\Omega$ , $25^\circ C \leq T_A \leq 125^\circ C$	See <sup>(1)</sup>	-20	20	$\mu V/^\circ C$	2
		$R_S = 10K\Omega$ , $-55^\circ C \leq T_A \leq 25^\circ C$	See <sup>(1)</sup>	-20	20	$\mu V/^\circ C$	3
$I_{IO}$	Input Offset Current		See <sup>(2)</sup>	-0.1	0.1	nA	1
				-25	25	nA	2
$\pm I_{IB}$	Input Bias Current		See <sup>(2)</sup>		0.2	nA	1
					50	nA	2
CMRR	Common Mode Rejection Ratio	$R_S \leq 10K\Omega$ , $V_{CM} = \pm 11V$		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	$6V \leq +V_{CC} \leq 15V$ , $-V_{CC} = -15V$		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	$+V_{CC} = 15V$ , $-15V \leq -V_{CC} \leq -6V$		70		dB	1, 2, 3
$I_S$	Supply Current				6.5	mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current			13	45	mA	1
				6.0	45	mA	2, 3
$+I_{OS}$	Output Short Circuit Current			-45	-13	mA	1
				-45	-6.0	mA	2, 3
$+A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $10V$ , $R_L = 2K\Omega$	See <sup>(3)</sup>	25		V/mV	4
				15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $-10V$ , $R_L = 2K\Omega$	See <sup>(3)</sup>	25		V/mV	4
				15		V/mV	5, 6
$+V_O$	Output Voltage Swing	$R_L = 10K\Omega$ , $+V_I = 11V$ , $-V_I = -11V$		12		V	4, 5, 6
$-V_O$	Output Voltage Swing	$R_L = 10K\Omega$ , $+V_I = -11V$ , $-V_I = 11V$			-12	V	4, 5, 6
$V_{CM}$	Input Common Mode Voltage Range		See <sup>(4)</sup>	-11	11	V	1, 2, 3

(1) Specified parameter, not tested.

(2)  $R_S = 10K\Omega$  @  $+125^\circ C$

(3) Datalog reading in K = V/mV.

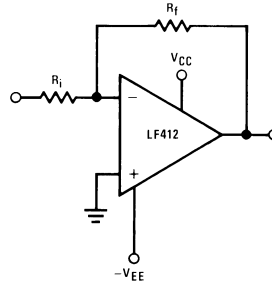
(4) Specified by CMRR.

## Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
SR+	Slew Rate	$V_O = -5V$ to $5V$		8.0		V/ $\mu$ s	7
SR-	Slew Rate	$V_O = 5V$ to $-5V$		8.0		V/ $\mu$ s	7
GBW	Gain Bandwidth Product			2.7		MHz	7

## Typical Connection



## Typical Performance Characteristics

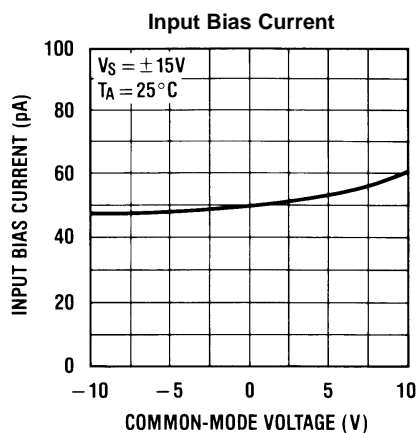


Figure 4.

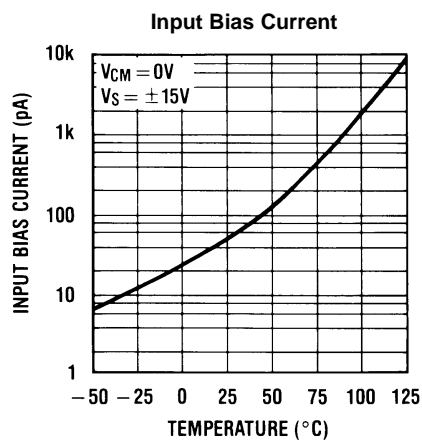


Figure 5.

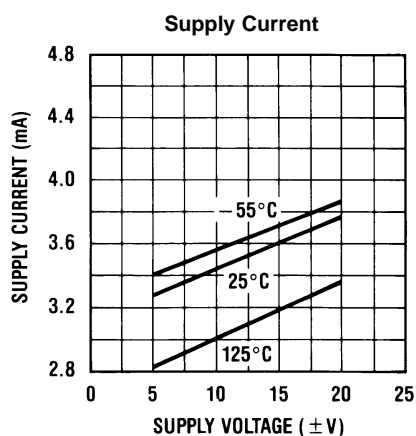


Figure 6.

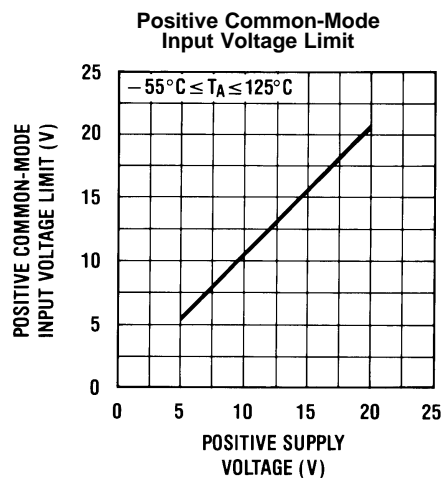


Figure 7.

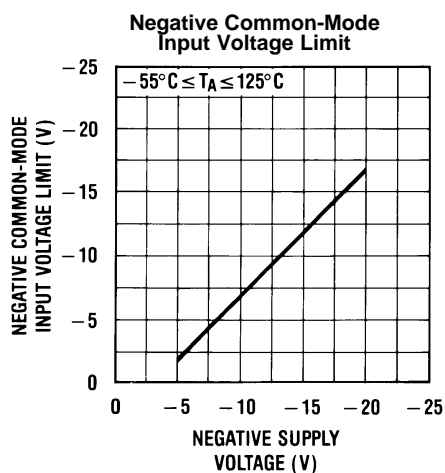


Figure 8.

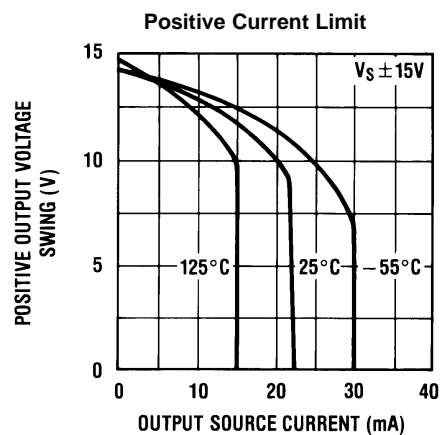


Figure 9.

## Typical Performance Characteristics (continued)

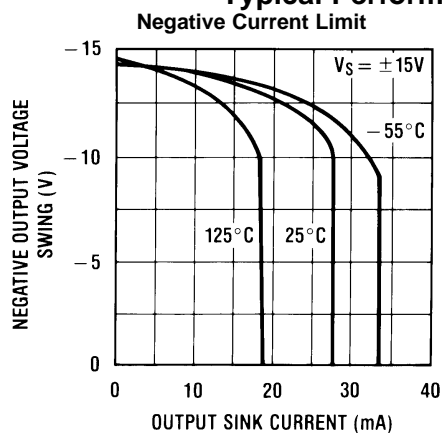


Figure 10.

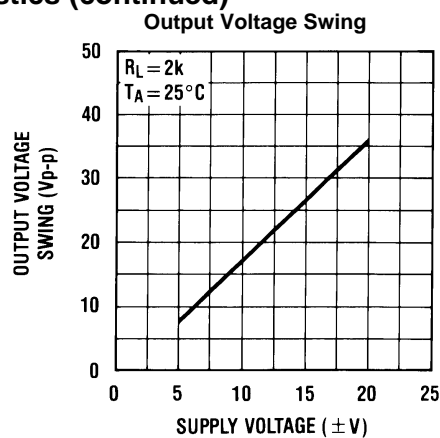


Figure 11.

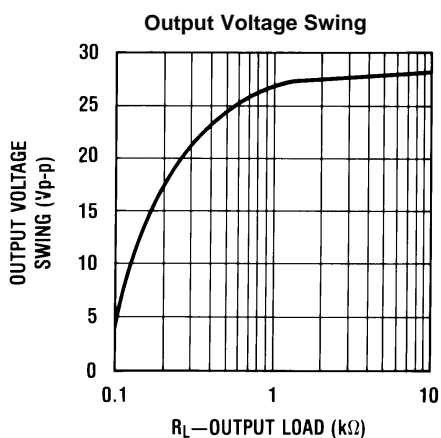


Figure 12.

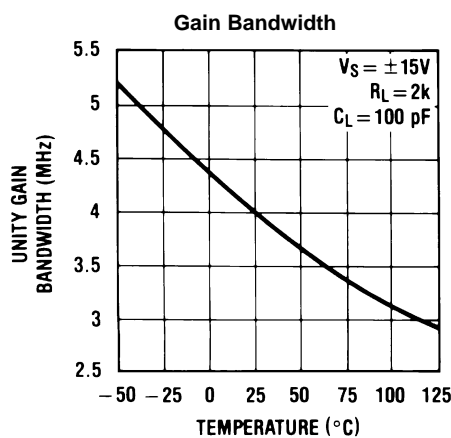


Figure 13.

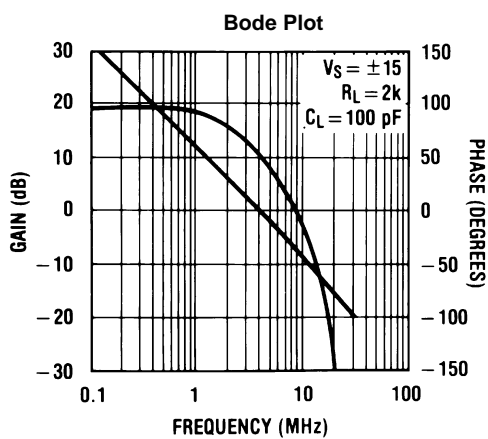


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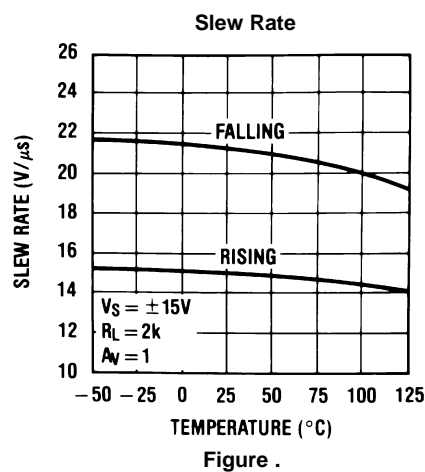
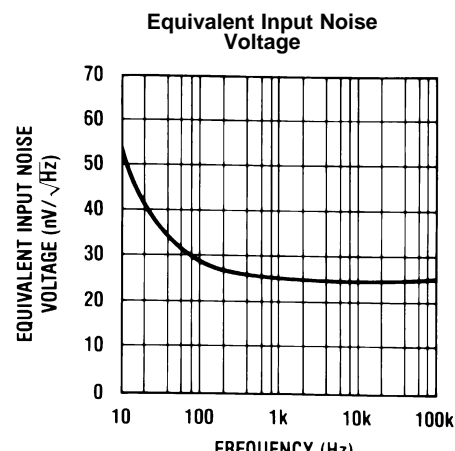
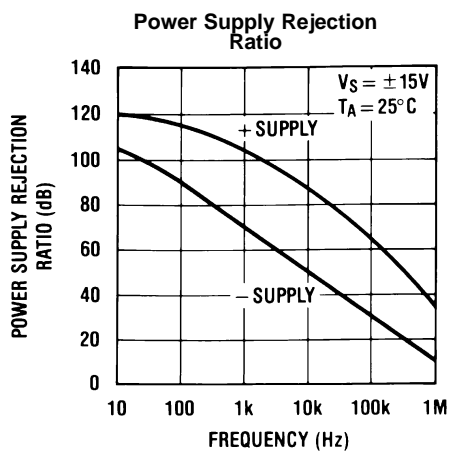
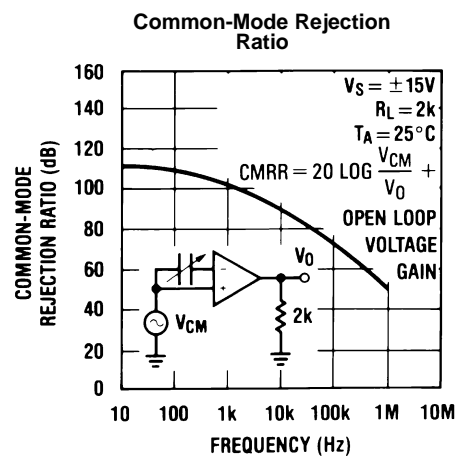
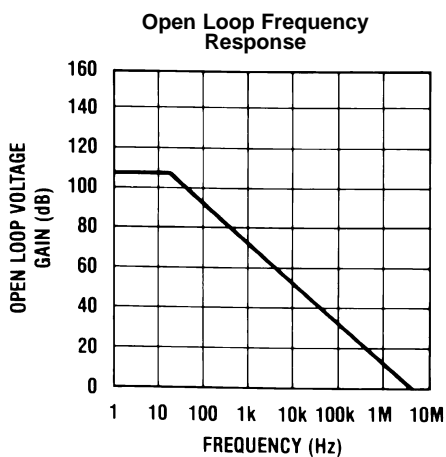
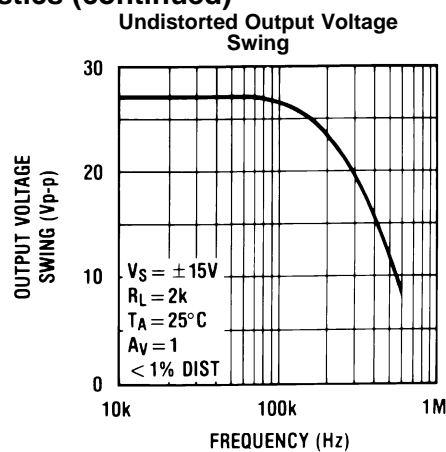
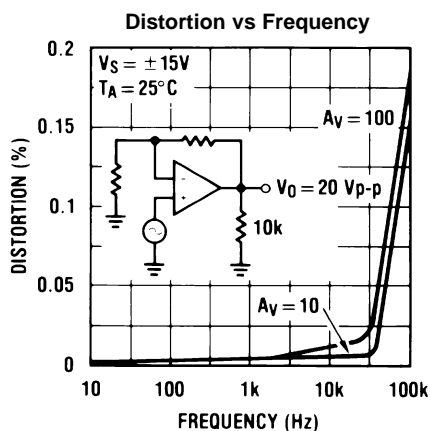


Figure .

## Typical Performance Characteristics (continued)





## Typical Performance Characteristics (continued)

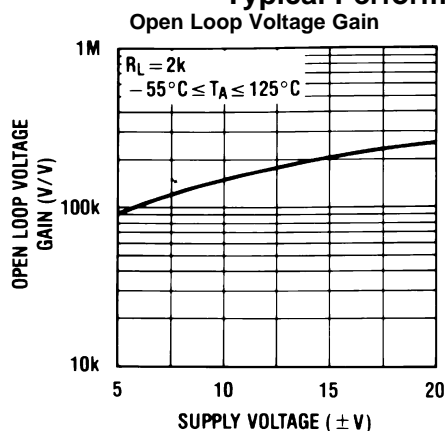


Figure 21.

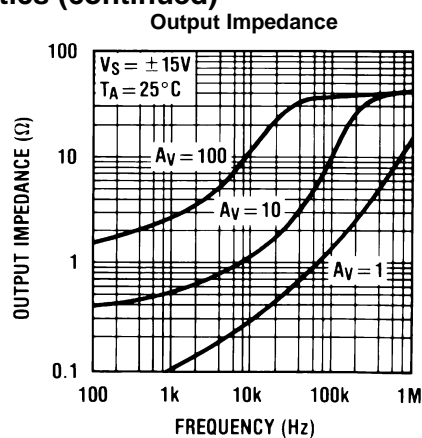


Figure 22.

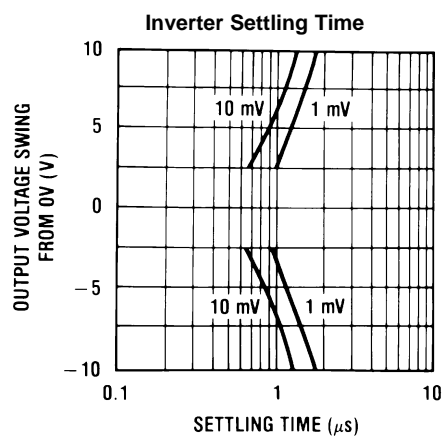


Figure 23.

## Pulse Response

$R_L = 2\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$

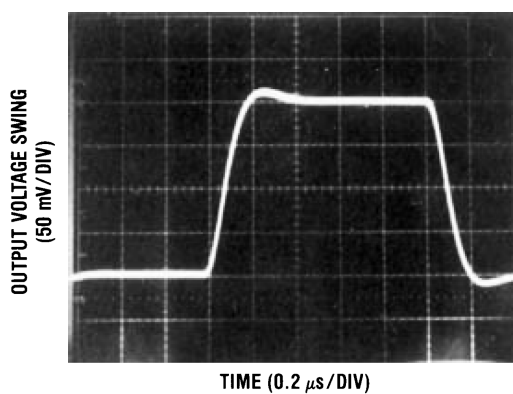


Figure 24. Small Signal Inverting

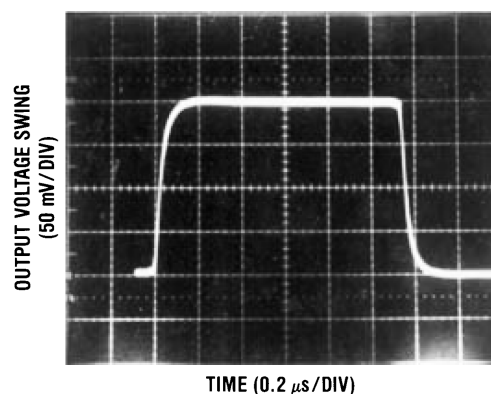


Figure 25. Small Signal Non-Inverting

## Pulse Response (continued)

$R_L=2\text{ k}\Omega$ ,  $C_L=10\text{ pF}$

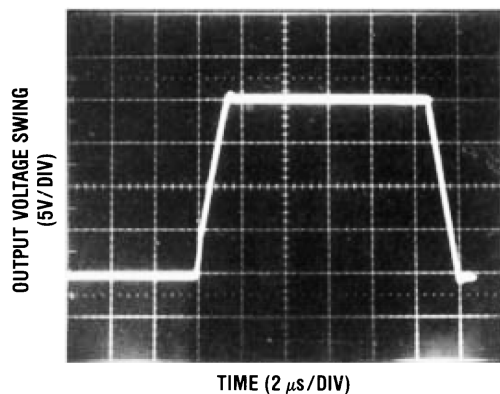


Figure 26. Large Signal Inverting

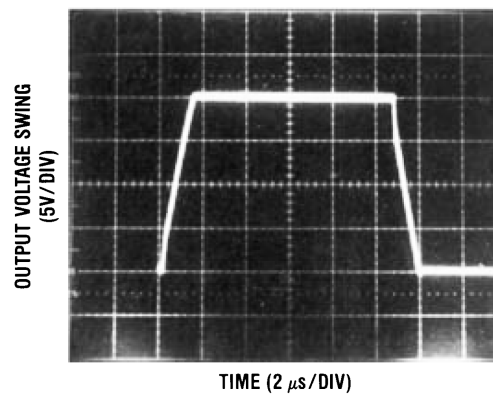


Figure 27. Large Signal Non-Inverting

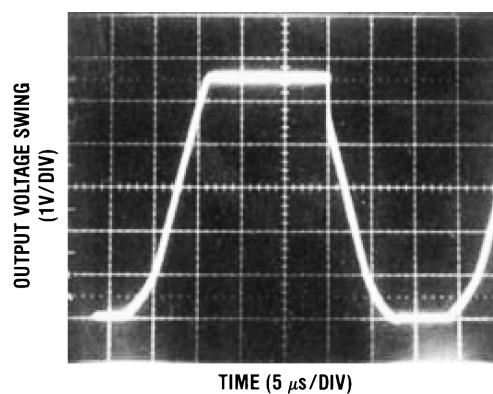


Figure 28. Current Limit ( $R_L=100\Omega$ )

## APPLICATION HINTS

The LF412 JFET input dual op amp is internally trimmed (BI-FET II™) providing very low input offset voltages and ensured input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on  $\pm 6.0\text{V}$  power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

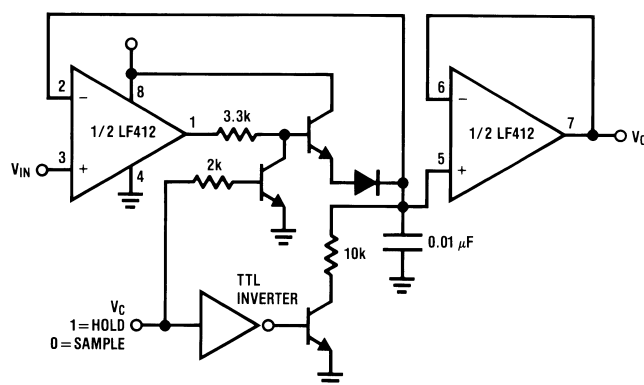
The amplifiers will drive a 2 k $\Omega$  load resistance to  $\pm 10\text{V}$  over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Application



**Figure 29. Single Supply Sample and Hold**

**Table 2. Revision History**

<b>Date Released</b>	<b>Revision</b>	<b>Section</b>	<b>Changes</b>
12/08/2010	A	New Release to Corporate format	1 MDS datasheet converted into Corporate datasheet format. MNLF412-X Rev 0C1 will be archived.
03/26/2013	A	All Sections	Changed layout of National Data Sheet to TI format

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF412 MD8	Active	Production	DIESALE (Y)   0	154   JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
<a href="#">LF412MH/883</a>	Active	Production	TO-99 (LMC)   8	20   JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LF412MH/883 Q ACO LF412MH/883 Q >T
<a href="#">LF412MJ/883</a>	Active	Production	CDIP (NAB)   8	40   TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LF412MJ /883 Q ACO /883 Q >T

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LF412MJ/883	NAB	CDIP	8	40	506.98	15.24	13440	NA

## TRAY



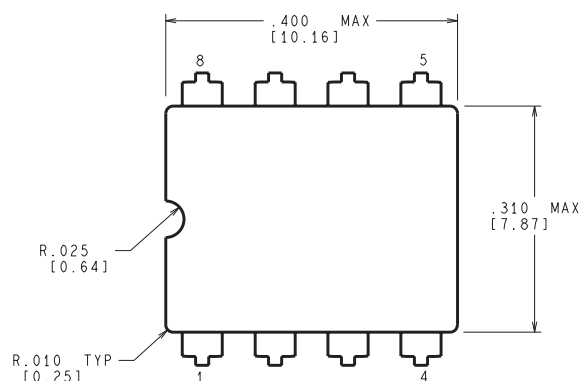
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

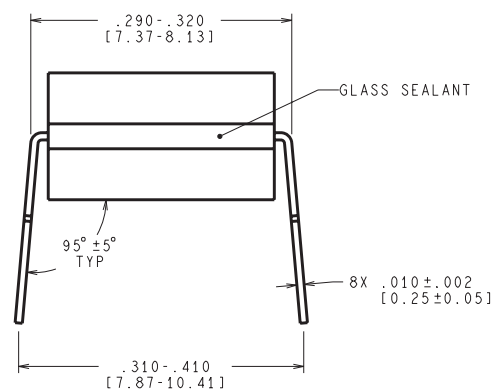
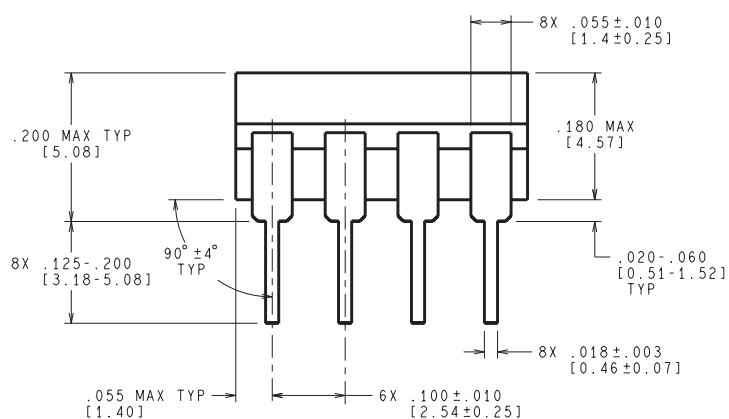
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
LF412MH/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54



NAB0008A



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS



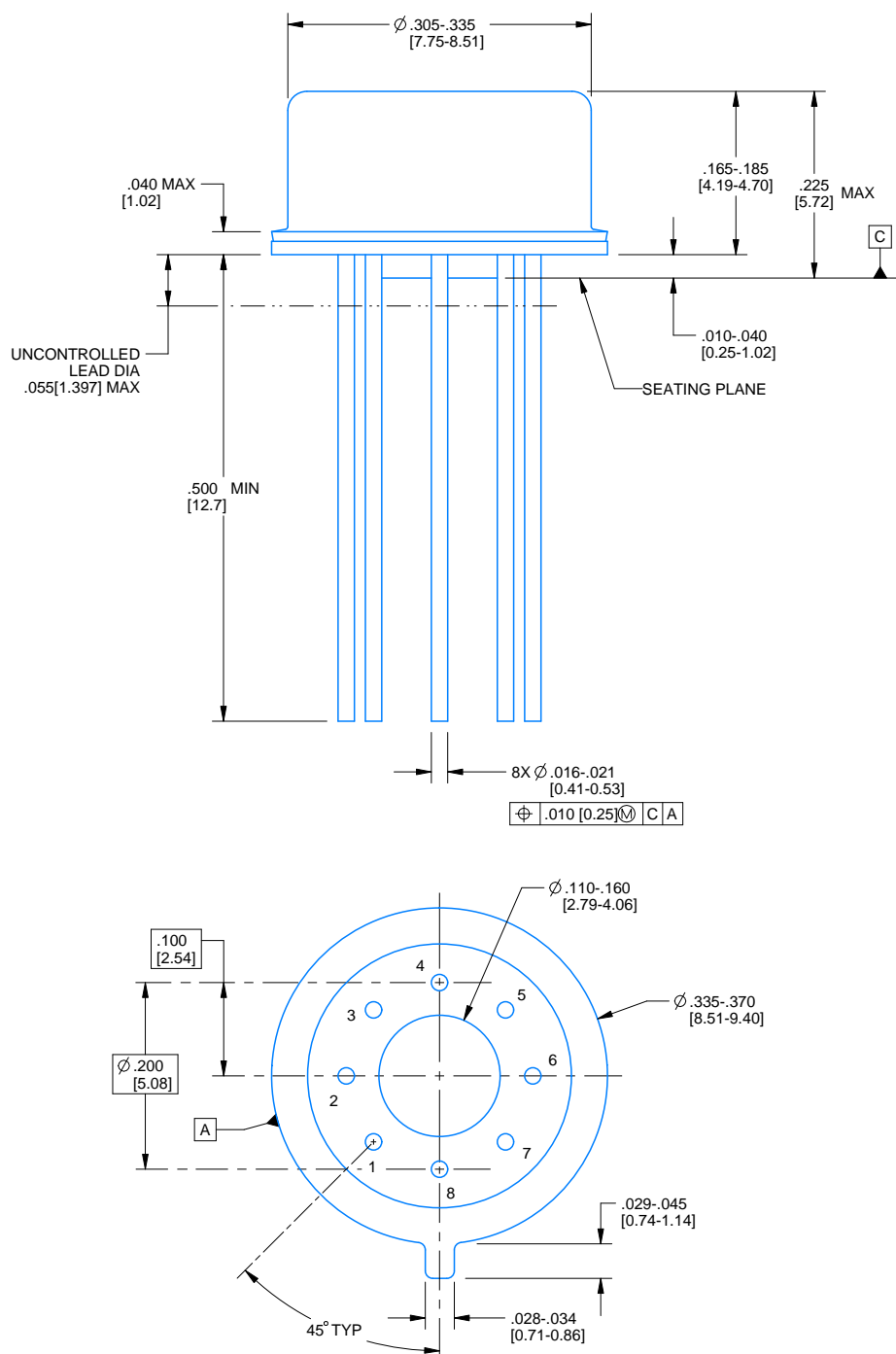
J08A (Rev M)

# PACKAGE OUTLINE

LMC0008A

TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



4220610/B 09/2024

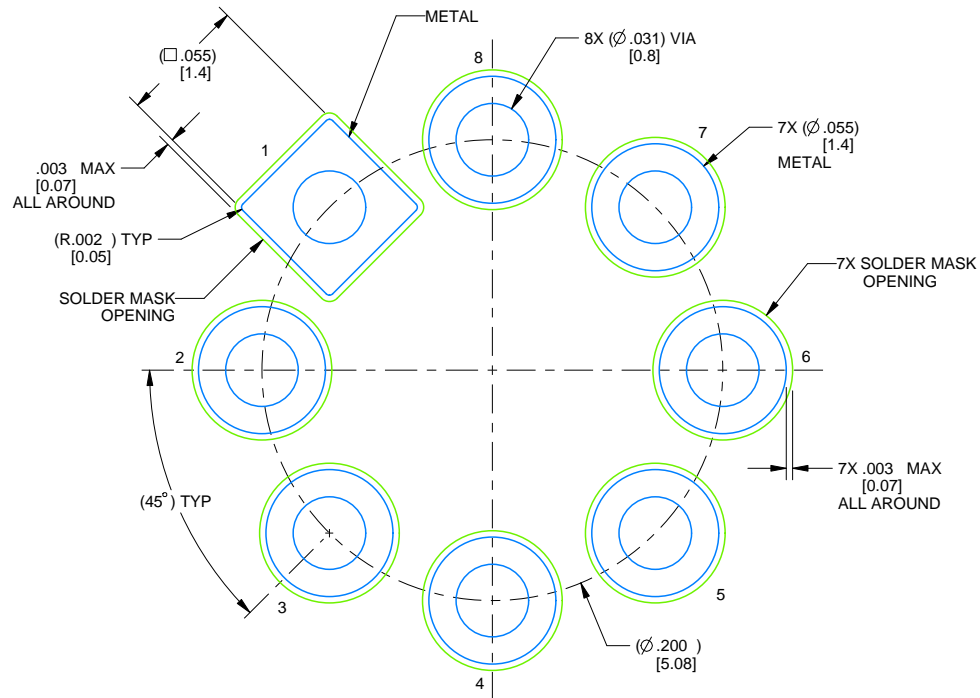
## NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.

# LMC0008A

**TO-CAN - 5.72 mm max height**

## TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 12X

4220610/B 09/2024

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