LM2704 Micropower Step-up DC/DC Converter with 550mA Peak Current Limit
Check for Samples: LM2704

FEATURES
- 550mA, 0.7Ω, Internal Switch
- Uses Small Surface Mount Components
- Adjustable Output Voltage up to 20V
- 2.2V to 7V Input Range
- Input Undervoltage Lockout
- 0.01μA Shutdown Current
- Small 5-Lead SOT-23 Package

DESCRIPTION
The LM2704 is a micropower step-up DC/DC in a small 5-lead SOT-23 package. A current limited, fixed off-time control scheme conserves operating current resulting in high efficiency over a wide range of load conditions. The 21V switch allows for output voltages as high as 20V. The low 400ns off-time permits the use of tiny, low profile inductors and capacitors to minimize footprint and cost in space-conscious portable applications. The LM2704 is ideal for LCD panels requiring low current and high efficiency as well as white LED applications for cellular phone back-lighting. The LM2704 can drive up to 8 white LEDs from a single Li-Ion battery.

APPLICATIONS
- LCD Bias Supplies
- White LED Back-Lighting
- Handheld Devices
- Digital Cameras
- Portable Applications

Typical Application Circuit

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The maximum allowable power dissipation is a function of the maximum junction temperature, \( T_{J\text{MAX}} \), the junction-to-ambient thermal resistance, \( \theta_{JA} \), and the ambient temperature, \( T_A \). See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using:

\[
P_{D\text{MAX}} = \frac{T_{J\text{MAX}} - T_A}{\theta_{JA}}
\]

Exceeding the maximum allowable power dissipation will cause excessive die temperature.

**PIN DESCRIPTIONS**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW</td>
<td>Power Switch input.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Output voltage feedback input.</td>
</tr>
<tr>
<td>4</td>
<td>SHDN</td>
<td>Shutdown control input, active low.</td>
</tr>
<tr>
<td>5</td>
<td>( V_{IN} )</td>
<td>Analog and Power input.</td>
</tr>
</tbody>
</table>

**SW(Pin 1):** Switch Pin. This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

**GND(Pin 2):** Ground Pin. Tie directly to ground plane.

**FB(Pin 3):** Feedback Pin. Set the output voltage by selecting values for \( R_1 \) and \( R_2 \) using:

\[
R_1 = R_2 \left( \frac{V_{\text{OUT}}}{1.237V} - 1 \right)
\]

**SHDN(Pin 4):** Shutdown Pin. The shutdown pin is an active low control. Tie this pin above 1.1V to enable the device. Tie this pin below 0.3V to turn off the device.

**\( V_{IN} \)(Pin 5):** Input Supply Pin. Bypass this pin with a capacitor as close to the device as possible.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min (°C)</th>
<th>Typ (°C)</th>
<th>Max (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW Voltage</td>
<td>7.5V</td>
<td>21V</td>
<td>2V</td>
<td></td>
</tr>
<tr>
<td>SHDN Voltage</td>
<td>7.5V</td>
<td>2V</td>
<td>2V</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>150 °C</td>
<td>300 °C</td>
<td>215 °C</td>
<td></td>
</tr>
<tr>
<td>Vapor Phase</td>
<td>220 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Infrared</td>
<td>215 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Ratings</td>
<td>2kV</td>
<td>200V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_j(MAX), the junction-to-ambient thermal resistance, θJA, and the ambient temperature, TA. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D(MAX) = (T_j(MAX) - T_A)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min (°C)</th>
<th>Typ (°C)</th>
<th>Max (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature</td>
<td>−40°C to +125°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.2V</td>
<td>7V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW Voltage Max.</td>
<td>20.5V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) All limits ensured at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

Specifications in standard type face for T_J = 25°C and those in bold face apply over the full Operating Temperature Range (T_J = −40°C to +125°C). Unless otherwise specified, V_IN = 2.2V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (°C)</th>
<th>Typ (°C)</th>
<th>Max (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IQ</td>
<td>Device Disabled</td>
<td>FB = 1.3V</td>
<td>40</td>
<td>70</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Device Enabled</td>
<td>FB = 1.2V</td>
<td>235</td>
<td>300</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Shutdown</td>
<td>SHDN = 0V</td>
<td>0.01</td>
<td>2.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>V_FB</td>
<td>Feedback Trip Point</td>
<td></td>
<td>1.189</td>
<td>1.237</td>
<td>1.269</td>
<td>V</td>
</tr>
<tr>
<td>I_CL</td>
<td>Switch Current Limit</td>
<td></td>
<td>490</td>
<td>550</td>
<td>610</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>420</td>
<td></td>
<td>620</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_B</td>
<td>FB Pin Bias Current</td>
<td>FB = 1.23V</td>
<td>30</td>
<td>120</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>V_IN</td>
<td>Input Voltage Range</td>
<td></td>
<td>2.2</td>
<td></td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>R_DSON</td>
<td>Switch R_DSON</td>
<td></td>
<td>0.7</td>
<td>1.6</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>T_OFF</td>
<td>Switch Off Time</td>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All limits ensured at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) Typical numbers are at 25°C and represent the most likely norm.

(3) Feedback current flows into the pin.
Electrical Characteristics\(^{(1)}\) (continued)
Specifications in standard type face are for \(T_J = 25^\circ C\) and those in **boldface type** apply over the full Operating Temperature Range \((T_J = -40^\circ C\) to \(+125^\circ C\)). Unless otherwise specified, \(V_{IN} = 2.2\) V.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (^{(1)})</th>
<th>Typ (^{(2)})</th>
<th>Max (^{(1)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{SD})</td>
<td>SHDN Pin Current</td>
<td>SHDN = (V_{IN}), (T_J = 25^\circ C)</td>
<td>0</td>
<td>80</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHDN = (V_{IN}), (T_J = 125^\circ C)</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHDN = GND</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_L)</td>
<td>Switch Leakage Current</td>
<td>(V_{SW} = 20) V</td>
<td>0.05</td>
<td>5</td>
<td></td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(UVP)</td>
<td>Input Undervoltage Lockout</td>
<td>ON/OFF Threshold</td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{FB}) Hysteresis</td>
<td>Feedback Hysteresis</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>SHDN Threshold</td>
<td>SHDN low</td>
<td></td>
<td>0.7</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SHDN High</td>
<td></td>
<td>1.1</td>
<td>0.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\theta_{JA})</td>
<td>Thermal Resistance</td>
<td></td>
<td>220</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics

Enable Current vs $V_{IN}$ (Part Switching)

Disable Current vs $V_{IN}$ (Part Not Switching)

Efficiency vs Load Current

Efficiency vs Load Current

SHDN Threshold vs $V_{IN}$
Typical Performance Characteristics (continued)

Switch Current Limit vs $V_{IN}$

Switch $R_{DS(on)}$ vs $V_{IN}$

FB Trip Point and FB Pin Current

Output Voltage vs Load Current

Temperature

FeedBack TRIP POINT (V)

Feedback Bias Current (mA)

Junction Temperature (°C)

Load Current (mA)

Voltage (V)

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Product Folder Links: LM2704
Typical Performance Characteristics (continued)

**Step Response**

\[ V_{OUT} = 20V, V_{IN} = 3.0V \]
1) Load, 1mA to 17mA to 1mA, DC
2) \( V_{OUT} \), 200mV/div, AC
3) \( I_L \), 500mA/div, DC
\[ T = 40 \mu s/\text{div} \]

**Start-Up/Shutdown**

\[ V_{OUT} = 20V, V_{IN} = 2.5V \]
1) SHDN, 1V/div, DC
2) \( I_L \), 250mA/div, DC
3) \( V_{OUT} \), 20V/div, DC
\[ T = 400 \mu s/\text{div} \]
\[ R_L = 1.3k\Omega \]
The LM2704 features a constant off-time control scheme. Operation can be best understood by referring to Figure 2 and Figure 3. Transistors Q1 and Q2 and resistors R3 and R4 of Figure 2 form a bandgap reference used to control the output voltage. When the voltage at the FB pin is less than 1.237V, the Enable Comp in Figure 2 enables the device and the NMOS switch is turned on pulling the SW pin to ground. When the NMOS switch is on, current begins to flow through inductor L while the load current is supplied by the output capacitor C_{OUT}. Once the current in the inductor reaches the peak current limit, the CL Comp trips and the 400ns One Shot
turns off the NMOS switch. The SW voltage will then rise to the output voltage plus a diode drop and the inductor current will begin to decrease as shown in Figure 3. During this time the energy stored in the inductor is transferred to \( C_{\text{OUT}} \) and the load. After the 400ns off-time the NMOS switch is turned on and energy is stored in the inductor again. This energy transfer from the inductor to the output causes a stepping effect in the output ripple as shown in Figure 3.

This cycle is continued until the voltage at FB reaches 1.237V. When FB reaches this voltage, the enable comparator then disables the device turning off the NMOS switch and reducing the \( I_q \) of the device to 40\( \mu \)A. The load current is then supplied solely by \( C_{\text{OUT}} \) indicated by the gradually decreasing slope at the output as shown in Figure 3. When the FB pin drops slightly below 1.237V, the enable comparator enables the device and begins the cycle described previously. The SHDN pin can be used to turn off the LM2704 and reduce the \( I_q \) to 0.01\( \mu \)A. In shutdown mode the output voltage will be a diode drop lower than the input voltage.

**APPLICATION INFORMATION**

**INDUCTOR SELECTION**

The appropriate inductor for a given application is calculated using the following equation:

\[
L = \left( \frac{V_{\text{D}} - V_{\text{IN(min)}} + V_D}{I_{\text{CL}}} \right) T_{\text{OFF}}
\]

(2)

where \( V_D \) is the schottky diode voltage, \( I_{\text{CL}} \) is the switch current limit found in the Typical Performance Characteristics section, and \( T_{\text{OFF}} \) is the switch off time. When using this equation be sure to use the minimum input voltage for the application, such as for battery powered applications. For the LM2704 constant-off time control scheme, the NMOS power switch is turned off when the current limit is reached. There is approximately a 200ns delay from the time the current limit is reached in the NMOS power switch and when the internal logic actually turns off the switch. During this 200ns delay, the peak inductor current will increase. This increase in inductor current demands a larger saturation current rating for the inductor. This saturation current can be approximated by the following equation:

\[
I_{\text{PK}} = I_{\text{CL}} + \left( \frac{V_{\text{IN(max)}}}{L} \right) 200\text{ns}
\]

(3)

Choosing inductors with low ESR decrease power losses and increase efficiency.

Care should be taken when choosing an inductor. For applications that require an input voltage that approaches the output voltage, such as when converting a Li-Ion battery voltage to 5V, the 400ns off time may not be enough time to discharge the energy in the inductor and transfer the energy to the output capacitor and load. This can cause a ramping effect in the inductor current waveform and an increased ripple on the output voltage. Using a smaller inductor will cause the \( I_{\text{PK}} \) to increase and will increase the output voltage ripple further. This can be solved by adding a 4.7pF capacitor across the \( R_{\text{F1}} \) feedback resistor (Figure 2) and slightly increasing the output capacitor. A smaller inductor can then be used to ensure proper discharge in the 400ns off time.

**DIODE SELECTION**

To maintain high efficiency, the average current rating of the schottky diode should be larger than the peak inductor current, \( I_{\text{PK}} \). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage.

**CAPACITOR SELECTION**

Choose low ESR capacitors for the output to minimize output voltage ripple. Multilayer ceramic capacitors are the best choice. For most applications, a 1\( \mu \)F ceramic capacitor is sufficient. For some applications a reduction in output voltage ripple can be achieved by increasing the output capacitor.

Local bypassing for the input is needed on the LM2704. Multilayer ceramic capacitors are a good choice for this as well. A 4.7\( \mu \)F capacitor is sufficient for most applications. For additional bypassing, a 100nF ceramic capacitor can be used to shunt high frequency ripple on the input.
LAYOUT CONSIDERATIONS

The input bypass capacitor $C_{\text{IN}}$, as shown in Typical Application Circuit, must be placed close to the IC. This will reduce copper trace resistance which affects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with $C_{\text{IN}}$ to shunt any high frequency noise to ground. The output capacitor, $C_{\text{OUT}}$, should also be placed close to the IC. Any copper trace connections for the Cout capacitor can increase the series resistance, which directly affects output voltage ripple. The feedback network, resistors R1 and R2, should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to an analog ground plane. The analog ground plane should tie directly to the GND pin. If no analog ground plane is available, the ground connection for the feedback network should tie directly to the GND pin. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.

Figure 4. White LED Application

Figure 5. Li-Ion 5V Application

Figure 6. Li-Ion 12V Application
Figure 7. 5V to 12V Application
# REVISION HISTORY

Changes from Revision C (May 2013) to Revision D | Page
--- | ---
• Changed layout of National Data Sheet to TI format | 11
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2704MF-ADJ/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>S28B</td>
<td>Samples</td>
</tr>
</tbody>
</table>

1. The marketing status values are defined as follows:
   - **ACTIVE**: Product device recommended for new designs.
   - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE**: TI has discontinued the production of the device.

2. **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

   **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

   **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

3. **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

5. Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

6. **Lead finish/Ball material**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component thickness
- K0: Dimension designed to accommodate the component length
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**TAPE DIMENSIONS**

- **Pocket Quadrants**
  - Q1
  - Q2
  - Q3
  - Q4

- **Sprocket Holes**

- **User Direction of Feed**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2704MF-ADJ/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

---

Pack Materials-Page 1
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2704MF-ADJ/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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