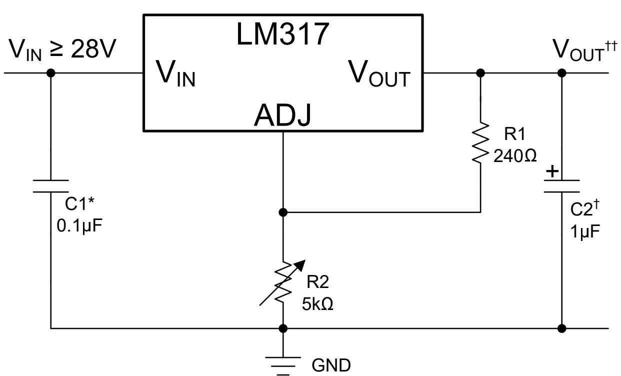
LM317 3-Pin Adjustable Regulator

1 Features

- Output voltage range:
  - Adjustable: 1.25V to 37V
- Output current: 1.5A
- Line regulation: 0.01%/V (typ)
- Load regulation: 0.1% (typ)
- Internal short-circuit current limiting
- Thermal overload protection
- Output safe-area compensation (new chip)
- PSRR: 80dB at 120Hz for C_{ADJ} = 10µF (new chip)
- Packages:
  - 4-pin, SOT-223 (DCY)
  - 3-pin, TO-263 (KTT)
  - 3-pin, TO-220 (KCS, KCT), legacy chip

2 Applications

- Multifunction printers
- AC drive power stage modules
- Electricity meters
- Servo drive control modules
- Merchant network and server PSU



*Needed if the device is more than 6 inches from filter capacitors.

†Optional, improves transient response.

††See Equation 1.

$$V_{OUT} = 1.25V \times \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} \times (R_2) \quad (1)$$

Typical Application

3 Description

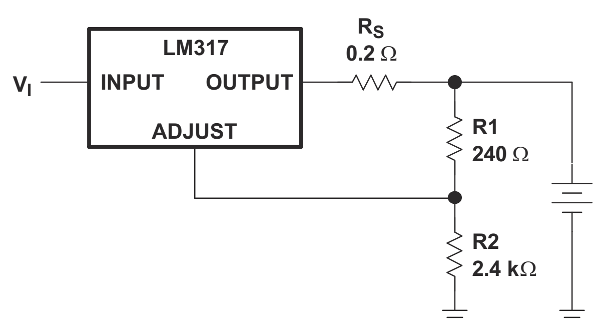
The LM317 is an adjustable three-pin, positive-voltage regulator capable of supplying more than 1.5A over an output voltage range of 1.25V to 37V. The device requires only two external resistors to set the output voltage. The device features a typical line regulation of 0.01% and typical load regulation of 0.1%. The LM317 includes current limiting, thermal overload protection, and safe operating area protection. Overload protection remains functional even if the ADJUST pin is disconnected.

Typically, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors. In that case, an input bypass is needed. Add an optional output capacitor to improve transient response. Bypass the adjustment pin to achieve very high ripple rejection ratios that are difficult to achieve with standard 3-pin regulators.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM317	DCY (SOT-223, 4)	6.5mm × 7mm
	KTT (TO-263, 3)	10.16mm × 15.24mm
	KCS, KCT (TO-220, 3) (3)	10.16mm × 4.55mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Legacy chip.



Battery-Charger Circuit

The regulator is *floating* and detects only the input-to-output differential voltage. Thus, supplies of several hundred volts are regulated as long as the maximum input-to-output differential is not exceeded. That is, avoid short-circuiting the output.

By connecting a fixed resistor between the adjustment pin and output, the LM317 is also able to be used as a precision current regulator. Supplies with electronic shutdown are achieved by clamping the adjustment terminal to ground, which programs the output to 1.25V where most loads draw little current.

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4 Device Comparison Table

I_{OUT}	PARAMETER	LM317 (Legacy Chip)	LM317 (New Chip)	LM317-N	LM317A	LM317HV	UNIT
1.5A	Input voltage range	4.25 to 40	4.25 to 40	4.25 to 40	4.25 to 40	4.25 - 60	V
	Load regulation accuracy	1.5	1.5	1.5	1	1.5	%
	PSRR (120Hz)	64	80	80	80	65	dB
	Recommended operating temperature	0 to 125	0 to 125	0 to 125	–40 to 125	0 to 125	°C
	TO-220 (NDE) T_{JA}	23.5		23.2	23.3	23	°C/W
	TO-200 (KCT) T_{JA}	37.9		N/A	N/A		°C/W
	TO-252 T_{JA}	N/A		54	54		°C/W
	TO-263 T_{JA}	38	41	41	N/A		°C/W
	SOT-223 T_{JA}	66.8	59.6	59.6	59.6		°C/W
	TO-92 T_{JA}	N/A		186	186		°C/W
0.5A		LM317M					
	Input voltage range	3.75 to 40					V
	Load regulation accuracy	1.5					%
	PSRR (120Hz)	80					dB
	Recommended operating temperature	−40 to 125					°C
	SOT-223 T_{JA}	60.2					°C/W
	TO-252 T_{JA}	56.9					°C/W
0.1A		LM317L		LM317L-N			
	Input voltage range	3.75 to 40		4.25 to 40			V
	Load regulation accuracy	1		1.5			%
	PSRR (120Hz)	62		80			dB
	Recommended operating temperature	–40 to 125		–40 to 125			°C
	SOT-23 T_{JA}	167.8		N/A			°C/W
	SO-8 T_{JA}	N/A		165			°C/W
	DSBGA T_{JA}	N/A		290			°C/W
	TO-92 T_{JA}	N/A		180			°C/W

5 Pin Configuration and Functions

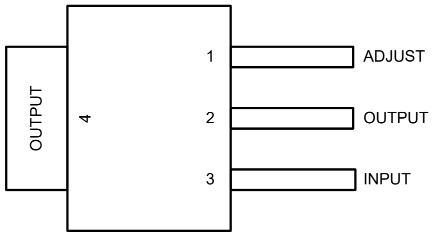


Figure 5-1. DCY Package, 4-Pin SOT-223 (Top View)

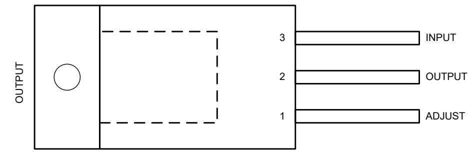


Figure 5-2. KCS or KCT Package, 3-Pin TO-220 (Top View), Legacy Chip

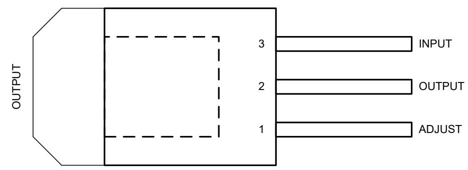


Figure 5-3. KTT Package, 3-Pin TO-263 (Top View)

Pin Functions, Metal Can Packages

PIN				I/O	DESCRIPTION
NAME	TO-220 (Legacy Chip)	TO-263	SOT-223		
ADJUST	1	1	1	—	Output voltage adjustment pin. Connect to a resistor divider to set V_{OUT}.
INPUT	3	3	3	I	Input voltage pin for the regulator.
OUTPUT	2, TAB	2, TAB	2, TAB	O	Output voltage pin for the regulator.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

	MIN	MAX	UNIT
Power dissipation	Internally limited		
Input-output voltage differential	−0.3	40	V
Storage temperature, T_{stg}	−65	150	°C
Operating virtual junction temperature, T_J (legacy chip)	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE		UNIT
			Legacy Chip	New Chip	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2500	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	NA	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_O	Output voltage	1.25	37	V
$V_I - V_O$	Input-to-output differential voltage	3	40	V
I_O	Output current	0.01	1.5	A
T_J	Operating virtual junction temperature	0	125	°C

6.4 Thermal Information (Legacy Chip)

THERMAL METRIC[1]		LM317				UNIT
		DCY (SOT-223)	KCS (TO-220)	KCT (TO-220)	KTT (TO-263)	
		4 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta(JA)}$	Junction-to-ambient thermal resistance	66.8	23.5	37.9	38.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.2	15.9	51.1	36.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	7.9	23.2	18.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.6	3.0	13.0	6.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.8	7.8	22.8	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	0.1	4.2	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

6.5 Thermal Information (New Chip)

THERMAL METRIC [1] [2]		LM317		UNIT
		DCY (SOT-223)	KTT (TO-263)	
		4 PINS	3 PINS	
$R_{\theta(JA)}$	Junction-to-ambient thermal resistance	59.6	41.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	43.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	23.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	10.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.3	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.
(2) When surface-mount packages are used (SOT-223), the junction to ambient thermal resistance is reduced by increasing the PCB copper area that is thermally connected to the package. See the *Heat Sink Requirements* section for heat sink techniques.

6.6 Electrical Characteristics

some specifications apply over the full operating temperature range as noted; unless otherwise specified, T_J = 25°C, V_{IN} − V_{OUT} = 5V, and I_{OUT} = 10mA[(1)]

PARAMETER	TEST CONDITIONS[(1)]			MIN	TYP	MAX	UNIT
Reference voltage	T_J = 25°C				1.25		V
	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V, 10mA ≤ I_{OUT} ≤ 1500mA, P_D ≤ 20W			1.2	1.25	1.3	
Line regulation[(2)]	3V ≤ (V_{IN} − V_{OUT}) ≤ 40V[(4)]		T_J = 25°C		0.01	0.04	%/V
			(over full operating temperature range)		0.02	0.07	
Load regulation	Legacy chip	I_O = 10mA to 1500mA, C_{ADJ} = 10μF[(3)], T_J = 25°C	V_O ≤ 5V			25	mV
			V_O ≥ 5V		0.1	0.5	%V_O
		I_O = 10mA to 1500mA, T_J = 0°C to 125°C	V_O ≤ 5V		20	70	mV
			V_O ≥ 5V		0.3	1.5	%V_O
	New chip	10mA ≤ I_{OUT} ≤ I_{MAX} [(5)]	T_J = 25°C		0.1	0.5	
			(over full operating temperature range)		0.3	1.5	
Thermal regulation	20ms pulse				0.04	0.07	%/W
Adjustment pin current	Over full operating temperature range				50	100	μA
Adjustment pin current change	10mA ≤ I_{OUT} ≤ I_{MAX} [(4)] 3V ≤ (V_{IN} − V_{OUT}) ≤ 40V		Over full operating temperature range		0.2	5	μA
Temperature stability	Legacy chip	T_{MIN} ≤ T_J ≤ T_{MAX}	Over full operating temperature range		0.7		%V_O
	New chip				1%		
Minimum load current	(V_{IN} − V_{OUT}) = 40V		Over full operating temperature range		3.5	10	mA
Current limit	(V_{IN} − V_{OUT}) ≤ 15V		P_D < P_{MAX} [(3)]	1.5	2.2		A
	(V_{IN} − V_{OUT}) = 40V		P_D < P_{MAX} [(3)], T_J = 25°C	0.15	0.4		
RMS output noise, % of V_{OUT}	10Hz ≤ f ≤ 10kHz				0.003		%
Ripple rejection ratio	Legacy chip	V_{OUT} = 10V, f = 120Hz, C_{ADJ} = 0μF[(4)]			57		dB
		V_{OUT} = 10V, f = 120Hz, C_{ADJ} = 10μF[(4)]		62	64		
	New chip	V_{OUT} = 10V, f = 120Hz, C_{ADJ} = 0μF (over full operating temperature range)			65		
		V_{OUT} = 10V, f = 120Hz, C_{ADJ} = 10μF (over full operating temperature range)		66	80		
Long-term stability	T_J = 25°C				0.3	1	%/1k hr

(1) For the legacy chip (unless otherwise noted), the following test conditions apply: $|V_I – V_O|$ = 5V, I_{OMAX} = 1.5A, and T_J = 0°C to 125°C. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(2) For the legacy chip, line regulation is expressed as the percentage change in output voltage per 1V change at the input.
(3) For the legacy chip, maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C potentially affects reliability.
(4) For the legacy chip, C_{ADJ} is connected between the ADJUST pin and GND.
(5) For the new chip, regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage resulting from heating effects are covered under the specifications for thermal regulation.

6.7 Typical Characteristics

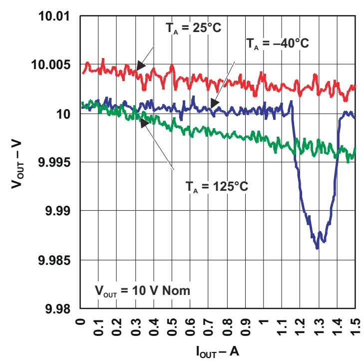


Figure 6-1. Load Regulation (Legacy Chip)

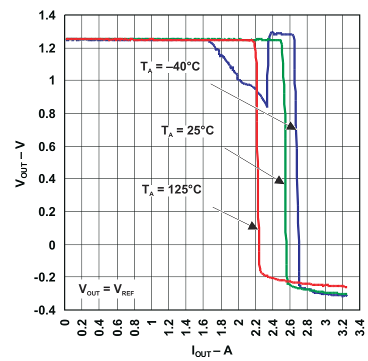


Figure 6-2. Load Regulation (Legacy Chip)

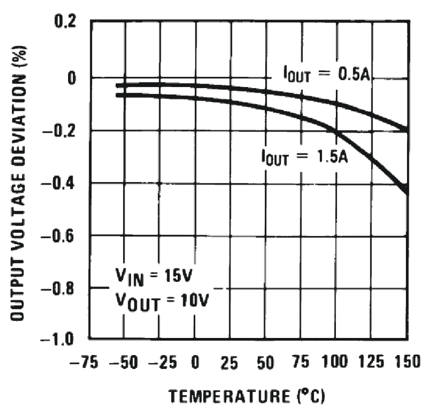


Figure 6-3. Load Regulation (New Chip)

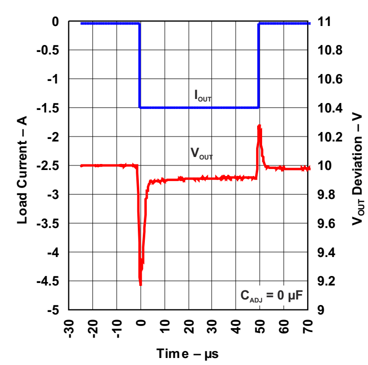


Figure 6-4. Load Transient Response (Legacy Chip)

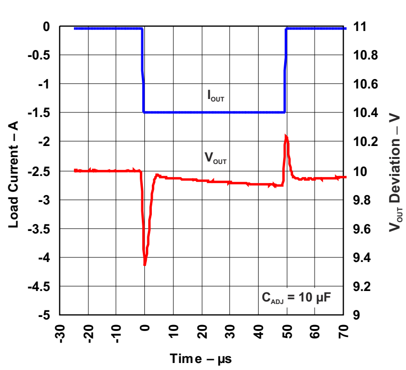


Figure 6-5. Load Transient Response (Legacy Chip)

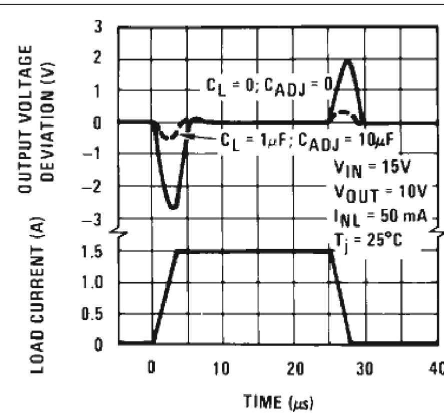


Figure 6-6. Load Transient Response (New Chip)

6.7 Typical Characteristics (continued)

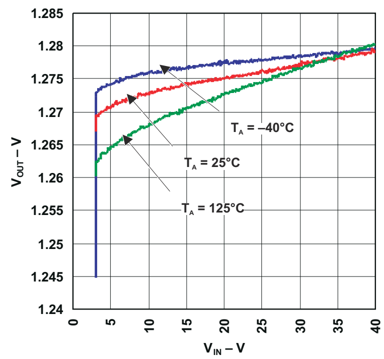


Figure 6-7. Line Regulation (Legacy Chip)

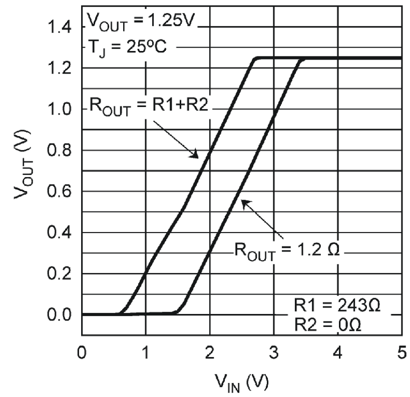


Figure 6-8. Output Voltage vs Input Voltage, V_{OUT} = V_{REF} (New Chip)

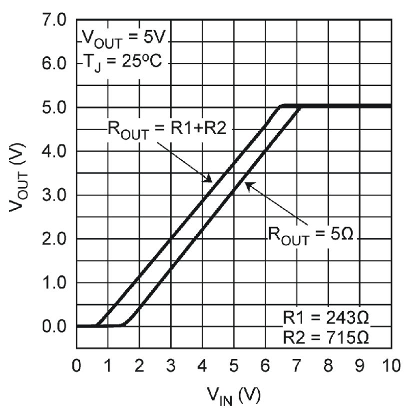


Figure 6-9. Output Voltage vs Input Voltage, V_{OUT} = 5V (New Chip)

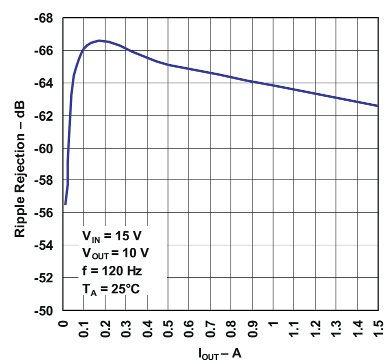


Figure 6-10. Ripple Rejection vs Output Current (Legacy Chip)

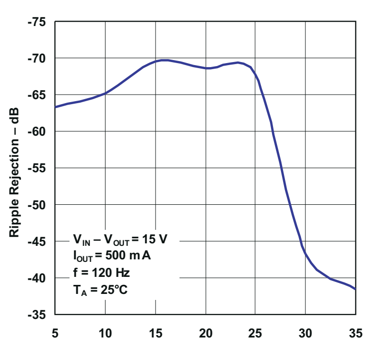


Figure 6-11. Ripple Rejection vs Output Voltage (Legacy Chip)

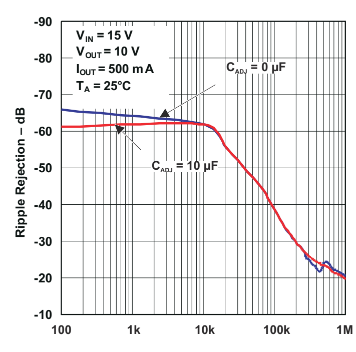


Figure 6-12. Ripple Rejection vs Frequency (Legacy Chip)

6.7 Typical Characteristics (continued)

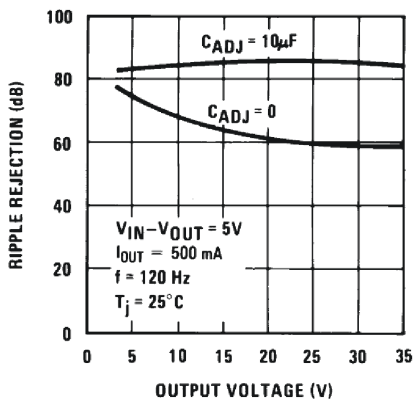


Figure 6-13. Ripple Rejection vs Output Voltage (New Chip)

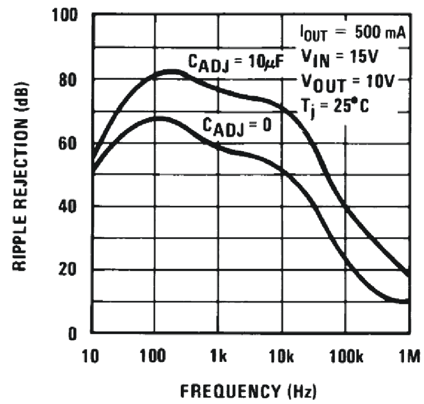


Figure 6-14. Ripple Rejection vs Frequency (New Chip)

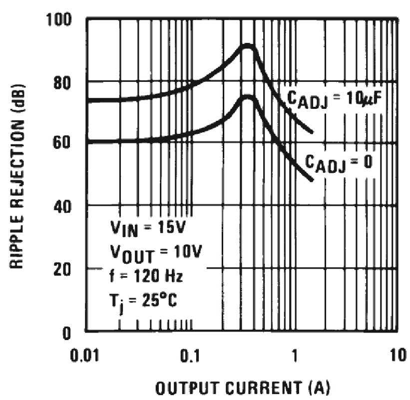


Figure 6-15. Ripple Rejection vs Output Current (New Chip)

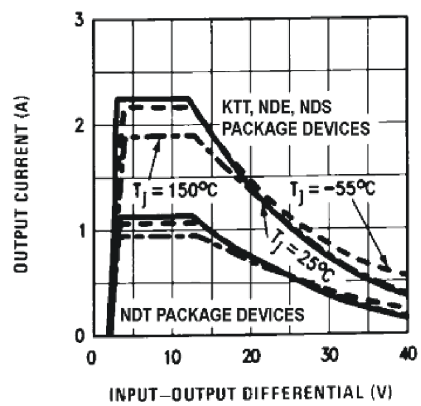


Figure 6-16. Current Limit Threshold (New Chip)

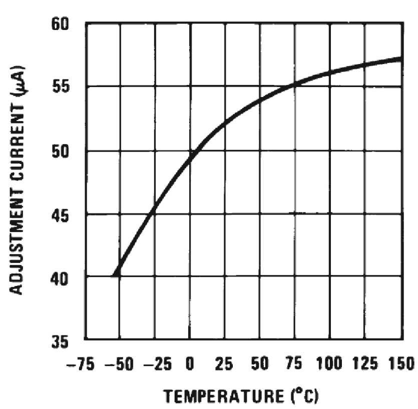


Figure 6-17. Adjustment Current vs Temperature (New Chip)

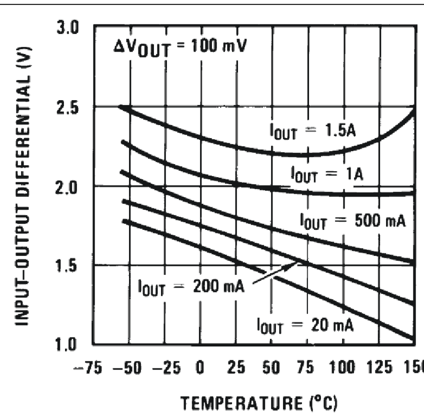


Figure 6-18. Dropout Voltage vs Temperature (New Chip)

6.7 Typical Characteristics (continued)

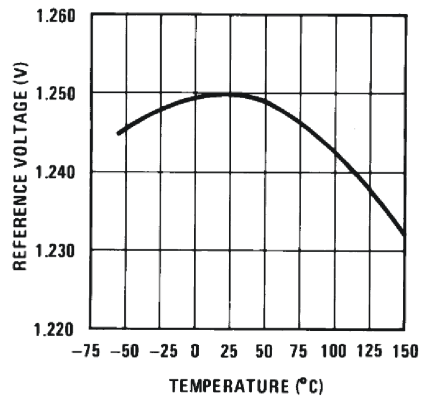


Figure 6-19. Temperature Stability (New Chip)

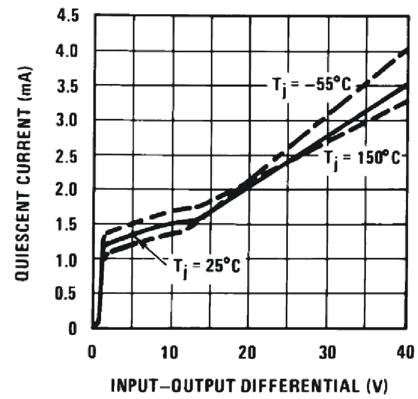


Figure 6-20. Minimum Operating Current (New Chip)

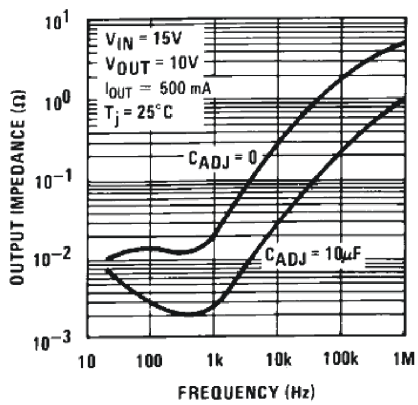


Figure 6-21. Output Impedance vs Frequency (New Chip)

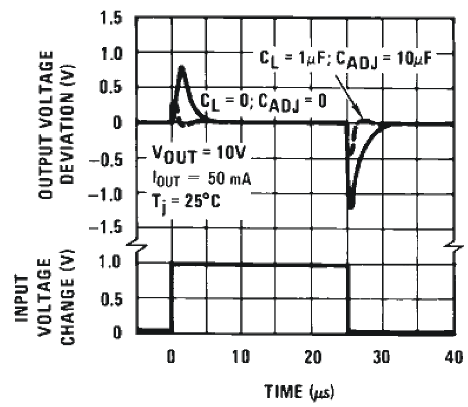


Figure 6-22. Line Transient Response (New Chip)

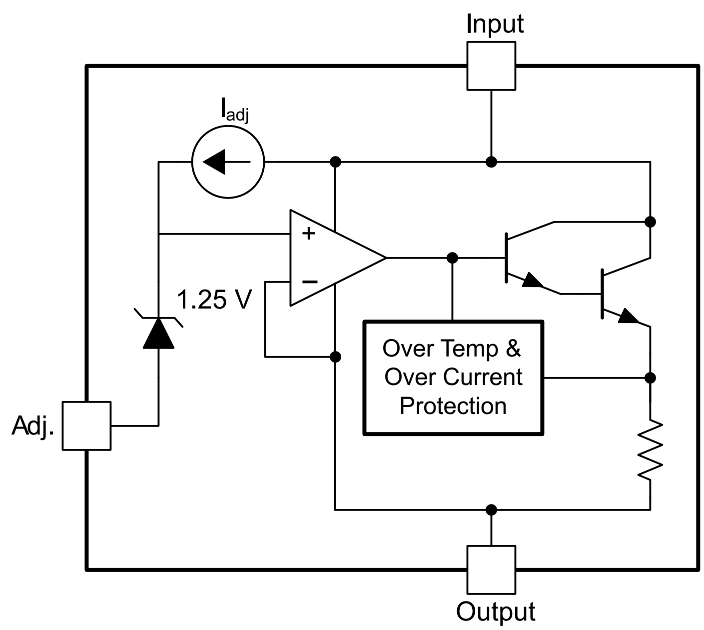
7 Detailed Description

7.1 Overview

The LM317 is an adjustable three-pin, positive-voltage regulator capable of supplying up to 1.5A over an output voltage range of 1.25V to 37V. The device requires only two external resistors to set the output voltage. The device features a typical line regulation of 0.01% and typical load regulation of 0.1%. The LM317 includes current limiting, thermal overload protection, and safe operating area protection. Overload protection remains functional even if the ADJUST pin is disconnected.

The LM317 is designed to minimize the I_{ADJUST} current and make this current constant with line and load changes. A 100µA current from the ADJUST pin represents an error term.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 NPN Darlington Output Drive

The NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. A 3V headroom is recommended (V_I – V_O) to support maximum current and lowest temperature.

7.3.2 Overload Block

Overcurrent and overtemperature shutdown protects the device against overload or damage from operating in excessive heat.

7.3.3 Programmable Feedback

An op amp with a 1.25V offset input at the ADJUST pin provides easy output voltage or current programming (but not both). For current regulation applications, use a single resistor whose resistance value is 1.25V / I_O and a power rating greater than $(1.25V)^2$ / R. For voltage regulation applications, two resistors set the output voltage.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25V greater than ADJUST pin to provide output regulation.

7.4.2 Operation With Low Input Voltage

The device requires up to 3V headroom (V_I – V_O) to operate in regulation. The device potentially drops out and OUTPUT voltage becomes the INPUT voltage minus the dropout voltage with less headroom.

7.4.3 Operation at Light Loads

The device passes the bias current to the OUTPUT pin. Make sure the load or feedback consumes this minimum current for regulation or the output is potentially too high. See the *Electrical Characteristics* table for the minimum load current needed to maintain regulation.

7.4.4 Operation In Self Protection

When an overload occurs, the device shuts down the Darlington NPN output stage or reduces the output current to prevent device damage. The device automatically resets from the overload. The output is either reduced or alternates between on and off until the overload is removed.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The flexibility of the LM317 allows the device to be configured to take on many different functions in DC power applications.

8.2 Typical Application

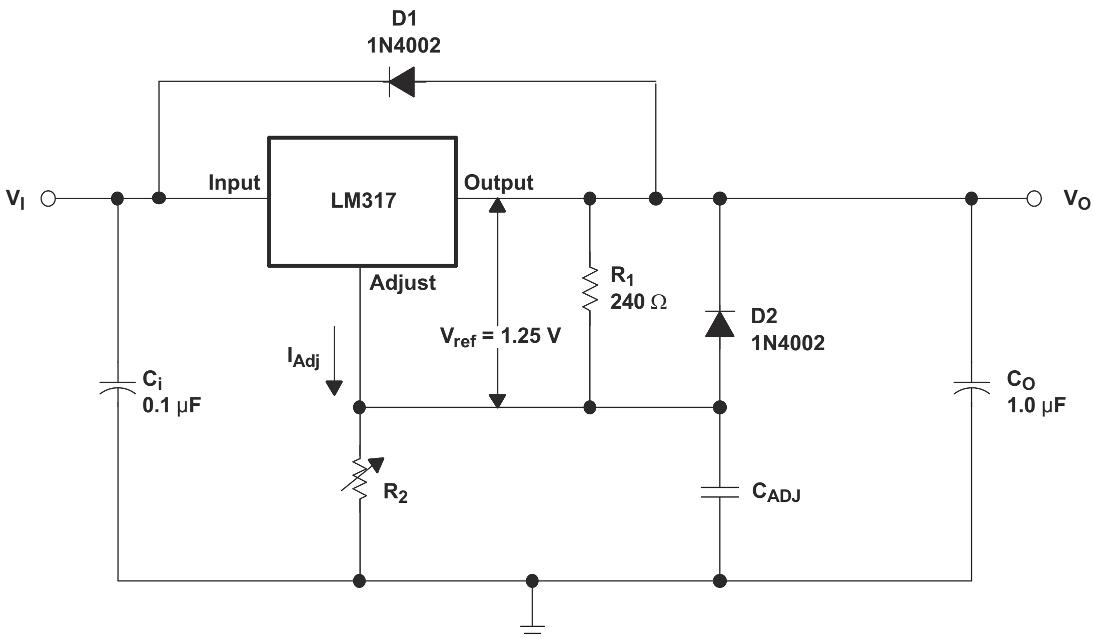


Figure 8-1. Adjustable Voltage Regulator

8.2.1 Design Requirements

- R1 and R2 are required to set the output voltage.
- Use C_{ADJ} to improve ripple rejection. C_{ADJ} prevents amplification of the ripple when the output voltage is adjusted higher. The impact of C_{ADJ} on the ripple rejection performance is captured in the *Electrical Characteristics* table.
- C_i is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1µF or 1µF ceramic or tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.
- C_O improves transient response, but is not needed for stability.
- Protection diode D2 is recommended if C_{ADJ} is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.
- Protection diode D1 is recommended if C_O is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.

8.2.2 Detailed Design Procedure

V_O is calculated as shown in Equation 2. I_{ADJ} is typically 50µA and negligible in most applications.

$$V_O = V_{REF} (1 + R2 / R1) + (I_{ADJ} \times R2) \quad (2)$$

8.2.3 Application Curves

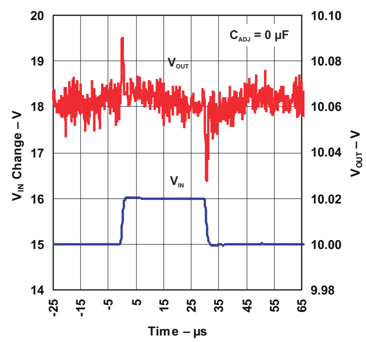


Figure 8-2. Line-Transient Response (Legacy Chip)

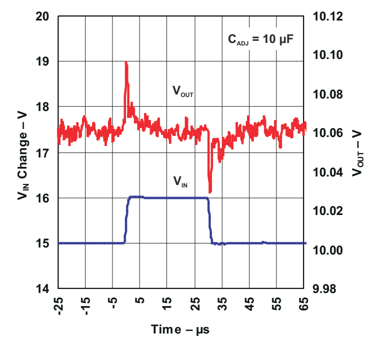


Figure 8-3. Line-Transient Response (Legacy Chip)

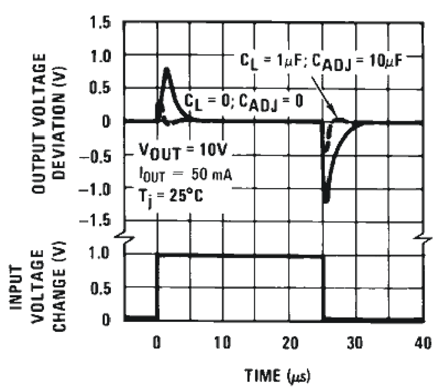


Figure 8-4. Line-Transient Response (New Chip)

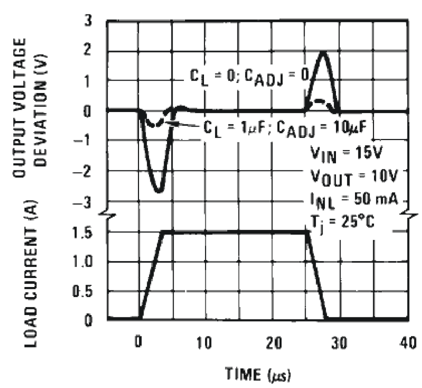


Figure 8-5. Load Transient Response (New Chip)

8.3 System Examples

8.3.1 0V to 30V Regulator Circuit

Here, the voltage is determined by:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V \tag{3}$$

By varying the voltage at the terminal of R3 (−10V in Figure 8-6), V_{OUT} is varied from 0V to 30V. In the absence of −10V, the V_{OUT} is only regulated to the lowest value of V_{REF} by making R_2 = 0Ω.

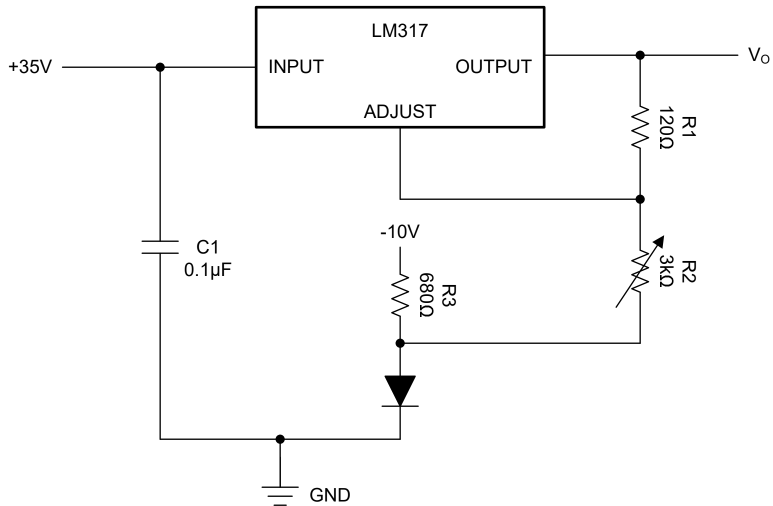


Figure 8-6. 0V to 30V Regulator Circuit

8.3.2 Adjustable Regulator Circuit With Improved Ripple Rejection

As shown in Figure 8-7, C2 helps stabilize the voltage at the ADJUST pin, which helps reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.

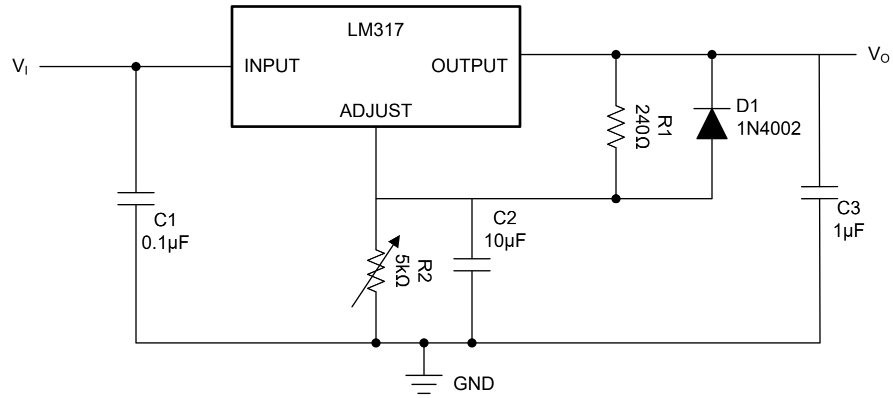


Figure 8-7. Adjustable Regulator Circuit with Improved Ripple Rejection

8.3.3 Precision Current-Limiter Circuit

This application limits the output current to I_{LIMIT} in Figure 8-8.

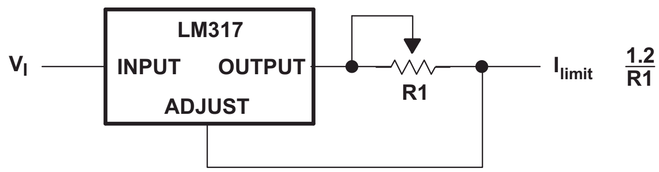


Figure 8-8. Precision Current-Limiter Circuit

8.3.4 Tracking Preregulator Circuit

This application keeps a constant voltage across the second LM317 in the circuit of Figure 8-9.

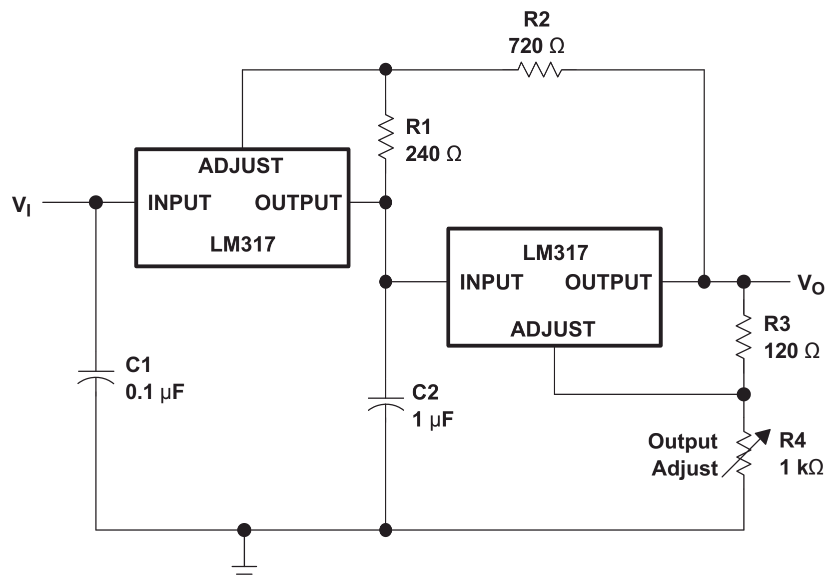


Figure 8-9. Tracking Preregulator Circuit

8.3.5 1.25V to 20V Regulator Circuit With Minimum Program Current

Because the value of V_{REF} is constant, the value of R_1 determines the amount of current that flows through R_1 and R_2. The size of R2 determines the IR drop from ADJUSTMENT to GND. Higher values of R2 translate to higher V_{OUT}. Equation 4, Equation 5, and Figure 8-10 illustrate this relationship.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \tag{4}$$

$$(R_1 + R_2)_{min} = Vol_{reg(min)} \tag{5}$$

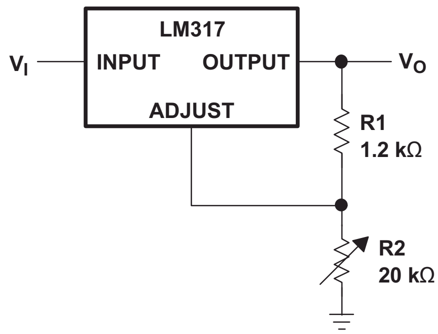


Figure 8-10. 1.25V to 20V Regulator Circuit With Minimum Program Current

8.3.6 Battery-Charger Circuit

The series resistor limits the current output of the LM317, minimizing damage to the battery cell.

$$V_{OUT} = 1.25\text{ V} \times \left(1 + \frac{R2}{R1}\right) \tag{6}$$

$$I_{OUT}(short) = \frac{1.25V}{RS} \tag{7}$$

$$\text{Output Impedance} = RS \times \left(1 + \frac{R2}{R1}\right) \tag{8}$$

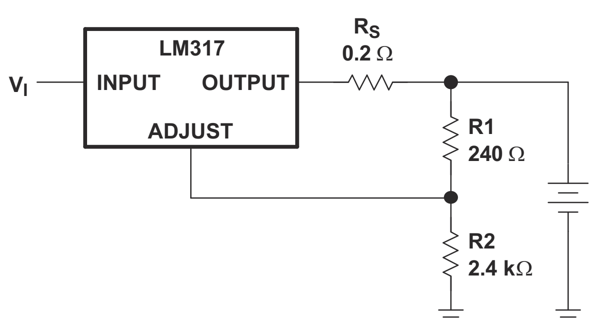


Figure 8-11. Battery-Charger Circuit

8.3.7 50mA, Constant-Current, Battery-Charger Circuit

Use the current-limit operation mode to trickle charge a battery at a fixed current. I_{CHG} = 1.25V ÷ 24Ω. Make sure V_I is greater than V_{BAT} + 4.25V. (1.25V [V_{REF}] + 3V [headroom]). Figure 8-12 shows a diagram of a battery-charger circuit.

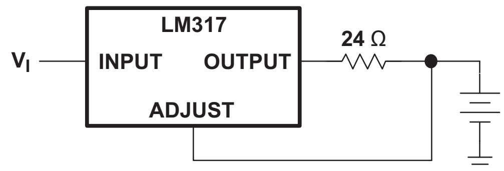


Figure 8-12. 50mA, Constant-Current, Battery-Charger Circuit

8.3.8 Slow Turn-On 15V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit (Figure 8-13) to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, the output voltage starts at V_{C1}+ V_{BE} + 1.25V = 0V + 0.65V + 1.25V = 1.9V. When the capacitor voltage rises, V_{OUT} rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

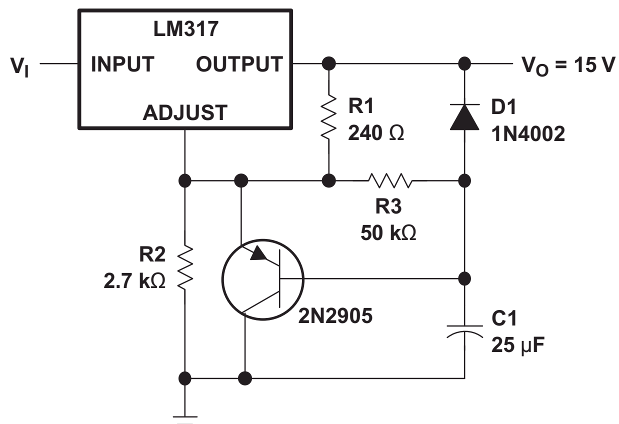


Figure 8-13. Slow Turn-On 15V Regulator Circuit

8.3.9 AC Voltage-Regulator Circuit

Figure 8-14 shows a circuit employing two LM317 devices. These two LM317 devices regulate both the positive and negative swings of a sinusoidal AC input.

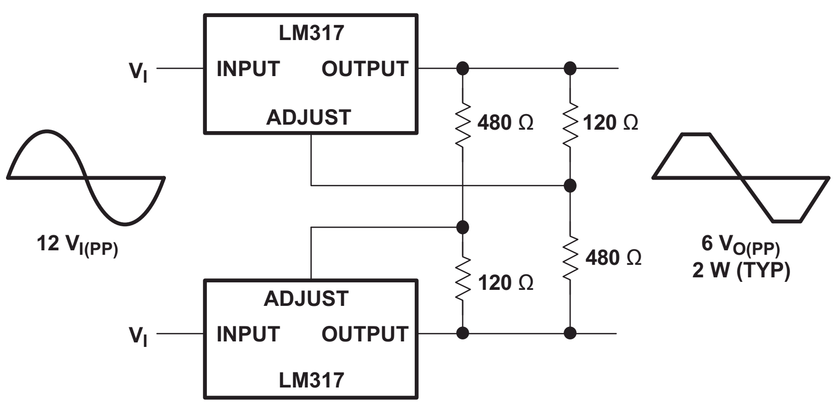


Figure 8-14. AC Voltage-Regulator Circuit

8.3.10 Current-Limited 6V Charger Circuit

When charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the ADJUST pin. The voltage at the ADJUST pin drops, and consequently the output voltage decreases until the NPN stops conducting. Figure 8-15 shows the current-limited circuit.

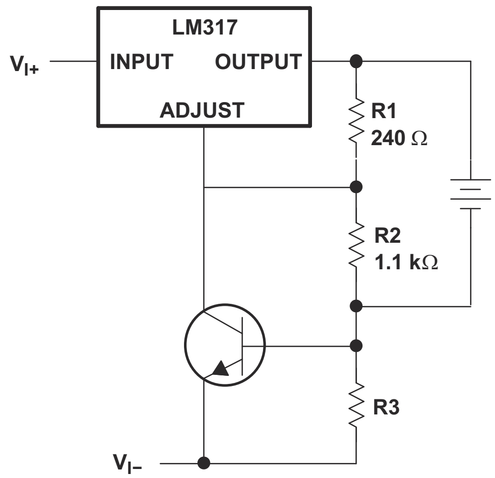


Figure 8-15. Current-Limited 6V Charger Circuit

8.3.11 Adjustable 4A Regulator Circuit

This application keeps the output current at 4A while having the ability to adjust the output voltage using the adjustable (1.5kΩ in Figure 8-16) resistor.

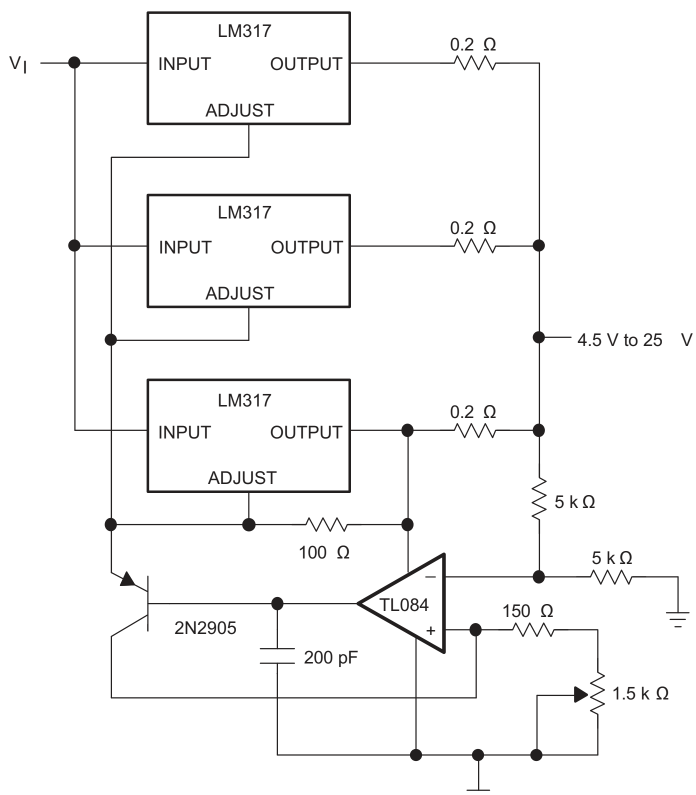


Figure 8-16. Adjustable 4A Regulator Circuit

8.3.12 High-Current Adjustable Regulator Circuit

The PNP (2N2905) and NPN (2N6486) at the top of Figure 8-17 allow higher currents at V_{OUT} than the LM317 provides. Meanwhile, the output voltage remains at levels determined by the ADJUST pin resistor divider of the LM317.

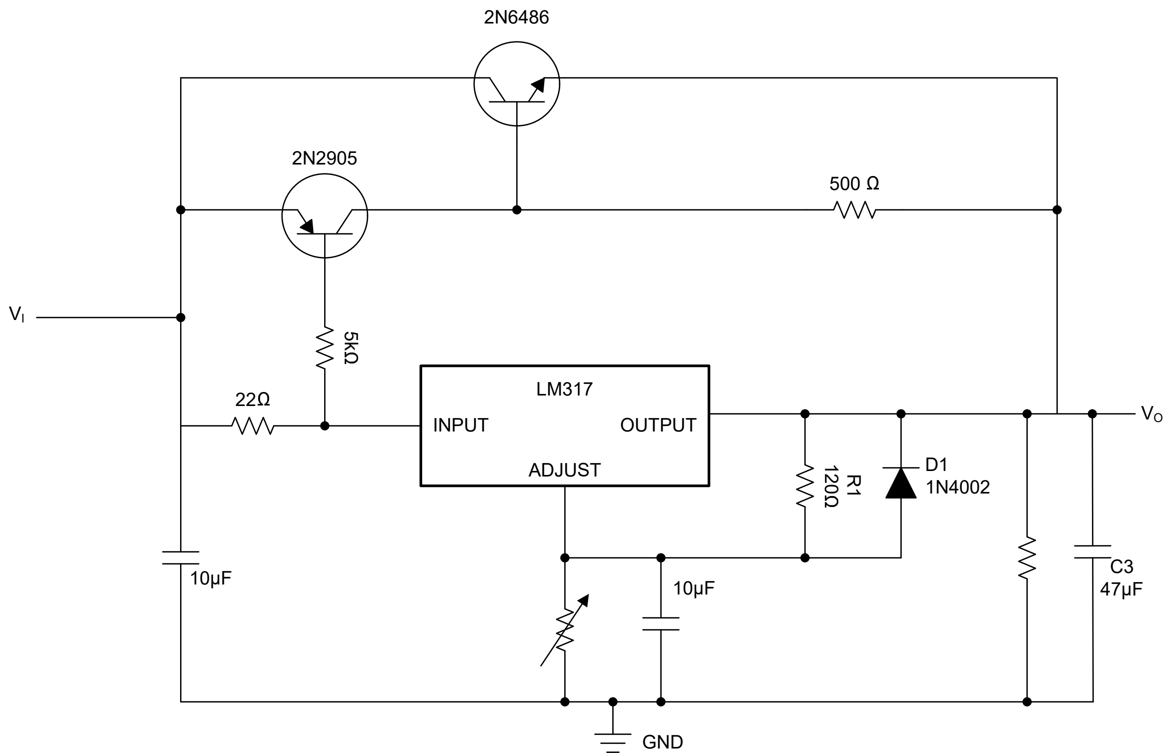


Figure 8-17. High-Current Adjustable Regulator Circuit

8.4 Power Supply Recommendations

The LM317 is designed to operate from an input voltage supply range between 1.25V to 37V greater than the output voltage. If the device is more than six inches from the input filter capacitors, use an input bypass capacitor of any type for stability. Make sure this capacitor is 0.1μF or greater.

8.5 Layout

8.5.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement is closest to the input pin of the device and the system GND. Take care to minimize the loop area formed by the bypass-capacitor connection, the input pin, and the system GND.
- For operation at full rated load, use wide trace lengths to eliminate I × R drop and heat dissipation.

8.5.1.1 Thermal Considerations

8.5.1.1.1 Heat Sink Requirements

The LM317 (new chip) regulators have internal thermal shutdown to protect the device from overheating. Under all operating conditions, make sure the device junction temperature does not exceed the rated maximum junction temperature (T_J) of 125°C for the LM317 (new chip). A heat sink is required depending on the maximum device power dissipation and the maximum ambient temperature of the application. To determine if a heat sink is needed, Equation 9 calculates the power dissipated by the regulator, P_D.

$$P_D = ((V_{IN} - V_{OUT}) \times I_L) + (V_{IN} \times I_G) \quad (9)$$

Figure 8-18 shows the voltage and currents that are present in the circuit.

Equation 10 calculates the next parameter, which is the maximum allowable temperature rise, $T_{R(MAX)}$.

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} \quad (10)$$

where:

- $T_{J(MAX)}$ is the maximum allowable junction temperature (125°C for the LM317, new chip)
- $T_{A(MAX)}$ is the maximum ambient temperature encountered in the application

Using the calculated values for $T_{R(MAX)}$ and P_D, Equation 11 calculates the maximum allowable value for the junction-to-ambient thermal resistance ($R_{\theta JA}$).

$$R_{\theta JA} = (T_{R(MAX)} / P_D) \quad (11)$$

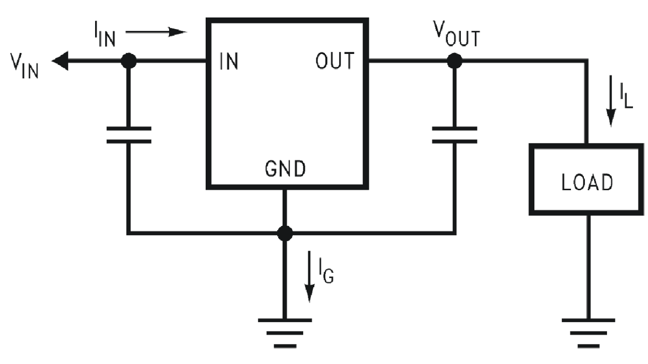


Figure 8-18. Power Dissipation Diagram

If the calculated maximum allowable thermal resistance is higher than the actual package rating, then no additional work is needed. If the calculated maximum allowable thermal resistance is lower than the actual package rating, correct this issue. Either reduce P_D or $T_{A(MAX)}$, or lower $R_{\theta JA}$ by adding a heat sink, or some combination thereof. P_D is the device power dissipation, $T_{A(MAX)}$ is the maximum ambient temperature, and $R_{\theta JA}$ is the device thermal resistance.

Equation 12 calculates the value if a heat sink is needed.

$$\theta_{HA} \leq (R_{\theta JA} - (\theta_{CH} + R_{\theta JC})) \quad (12)$$

where:

- θ_{CH} is the thermal resistance of the contact area between the device case and the heat sink surface
- $R_{\theta JC}$ is thermal resistance from the junction of the die to the surface of the package case

When a value for θ_{HA} is calculated, select a heat sink with a value that is less than, or equal to, this number.

The θ_{HA} rating is specified numerically by the heat sink manufacturer in the catalog, or given in a curve plotting temperature rise versus power dissipation for the heat sink.

8.5.1.1.2 Heat Sinking Surface-Mount Packages

The TO-263 (KTT), SOT-223 (DCY), and TO-220 (KCS, KCT) packages use a copper plane on the PCB and the PCB as a heat sink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

8.5.1.1.2.1 Heatsinking the SOT-223 (DCY) Package

Figure 8-19 and Figure 8-20 show information for the SOT-223 package. Figure 8-20 assumes a $R_{\theta JA}$ of 74°C/W for 1oz. copper and 59.6°C/W for 2oz. copper (further details are in Section 6.5) and a maximum junction temperature of 125°C. See the *AN-1028 Maximum Power Enhancement Techniques for Power Packages* application note for thermal enhancement techniques to be used with the SOT-223 and TO-252 packages.

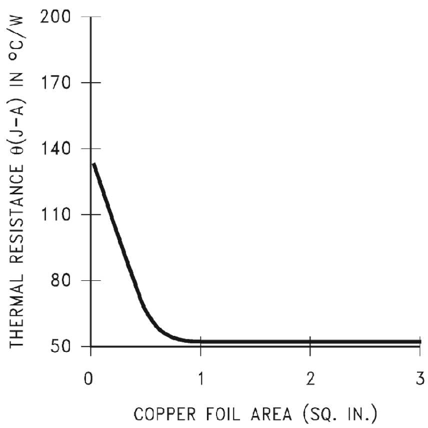


Figure 8-19. $R_{\theta JA}$ vs Copper (2oz.) Area for the SOT-223 Package

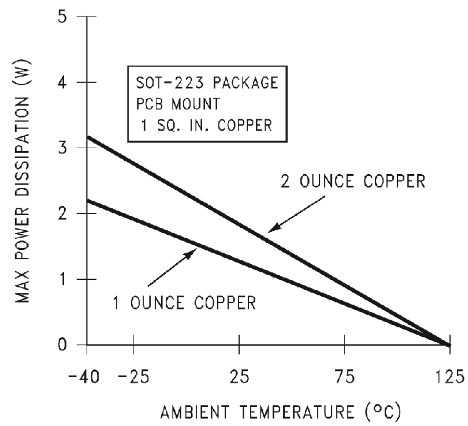


Figure 8-20. Maximum Power Dissipation vs T_{AMB} for the SOT-223 Package

8.5.1.1.2.2 Heat Sinking the TO-263 (KTT) Package

Figure 8-21 shows the TO-263 measured values of $R_{\theta JA}$ for different copper area sizes using a typical PCB with 1oz. copper. This figure also shows no solder mask over the copper area used for heat sinking.

As shown in Figure 8-21, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value of $R_{\theta JA}$ for the TO-263 package mounted to a PCB is 32°C/W.

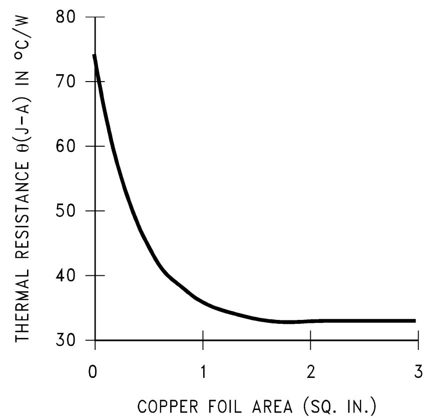


Figure 8-21. $R_{\theta JA}$ vs Copper (1-oz.) Area for the TO-263 Package

As a design aid, Figure 8-22 shows the maximum allowable power dissipation compared to ambient temperature for the TO-263 device. This figure assumes $R_{\theta JA}$ is 35°C/W and the maximum junction temperature is 125°C.

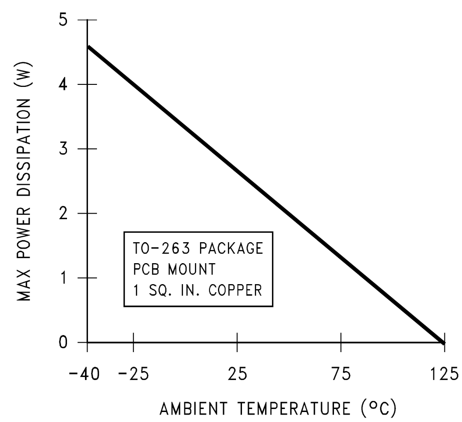


Figure 8-22. Maximum Power Dissipation vs T_{AMB} for the TO-263 Package

8.5.2 Layout Examples

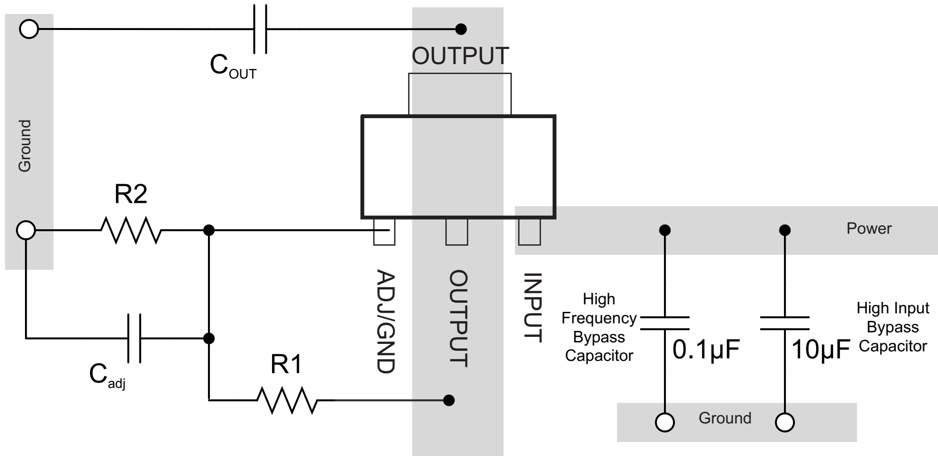


Figure 8-23. Layout Example (Legacy Chip)

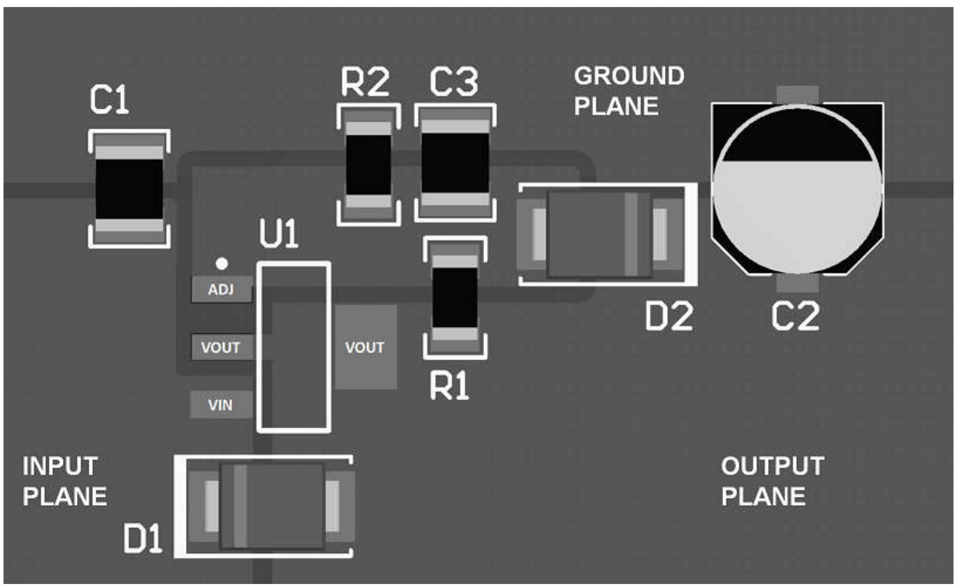


Figure 8-24. SOT-223 Layout Example (New Chip)

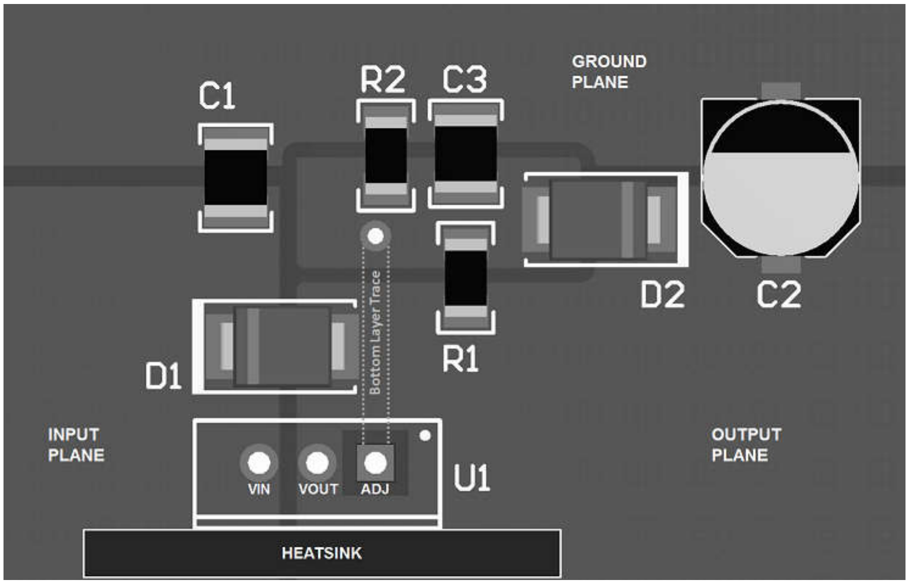


Figure 8-25. TO-220 Layout Example (New Chip)

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Device Nomenclature

PRODUCT[(1)]	V_{OUT}
LM317**yyyz**	**yyy** is the package designator. **z** is the package quantity designator. Devices ship with either the legacy chip (CSO: SHE) or the new chip (CSO: FFAB). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the data sheet.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Y (April 2020) to Revision Z (April 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added new silicon devices to document	1
• Added new silicon curves to *Typical Characteristics* section	1
• Changed *Features*, *Applications*, and *Description* sections	1
• Added *LM317 (New Chip)* column to *Device Comparison Table*	4
• Changed DCY pinout drawing and INPUT and OUTPUT description in *Pin Functions* table	5
• Added *Power dissipation* row to *Absolute Maximum Ratings* table	6
• Added new chip information to *ESD Ratings* table	6
• Added *Thermal Information (New Chip)* table	7
• Changed *Electrical Characteristics* table	8
• Changed ADJUST pin current discussion in second paragraph of *Overview* section	13
• Added effect of C_{ADJ} on ripple rejection discussion to second bullet of *Design Requirements*	15
• Added new silicon curves to *Application Curves*	16
• Deleted *−10V* from Equation 2	19
• Changed *The NPNs* to *The PNP (2N2905) and NPN (2N6486)* in *High-Current Adjustable Regulator Circuit* section	22
• Added *Thermal Considerations* section and subsections	23

Changes from Revision X (September 2016) to Revision Y (April 2020)	Page
• Added *Device Comparison Table*	4
• Changed V_{IN} to I_{OUT} in *Load Transient Response* figures	9
• Added missing caption to second y-axis in second *Load Transient Response* figure	9
• Changed V_{OUT} and output impedance equations in *Battery-Charger Circuit* section	19

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM317DCY	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCY.A	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCY.B	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCYG3	Active	Production	SOT-223 (DCY) | 4	80 | TUBE	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCYR	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCYR.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCYR.B	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317DCYRG3	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	L3
LM317KCS	NRND	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	LM317
LM317KCS.A	NRND	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	LM317
LM317KCSE3	NRND	Production	TO-220 (KCS) | 3	50 | TUBE	Yes	SN	N/A for Pkg Type	0 to 125	LM317
LM317KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTR	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTR.A	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTR.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTR.B	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	0 to 125	LM317
LM317KTTRG3	Active	Production	DDPAK/ TO-263 (KTT) | 3	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	0 to 125	LM317

(1) **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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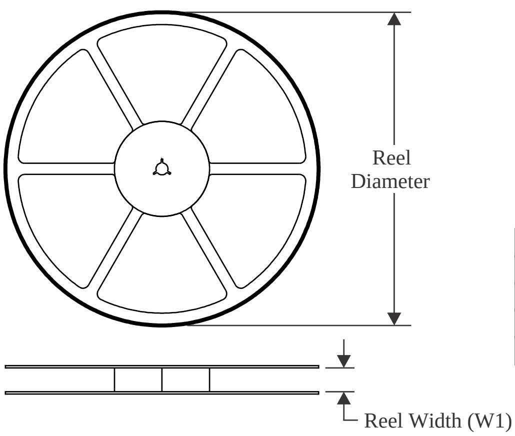
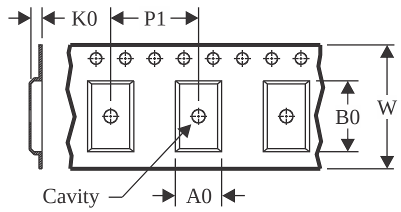
TAPE AND REEL INFORMATION

REEL DIMENSIONS

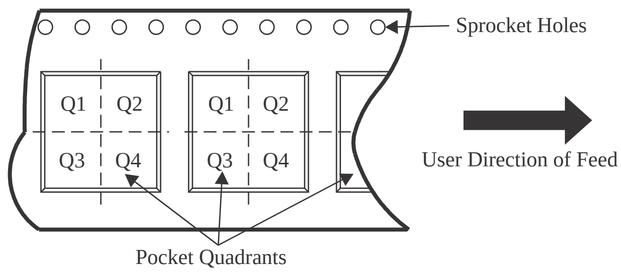


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

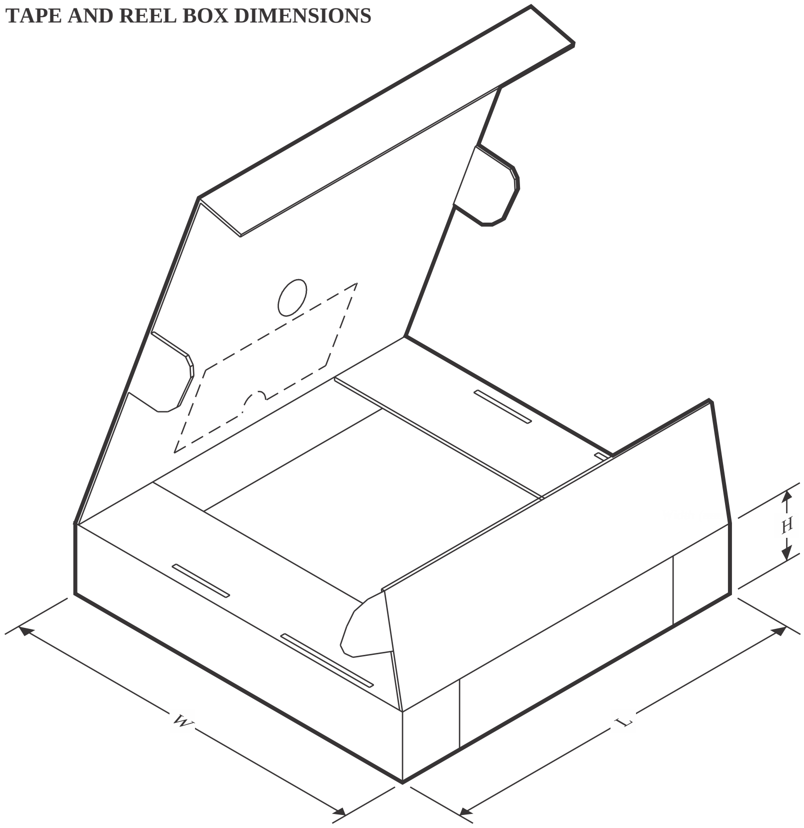
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
LM317KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM317KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

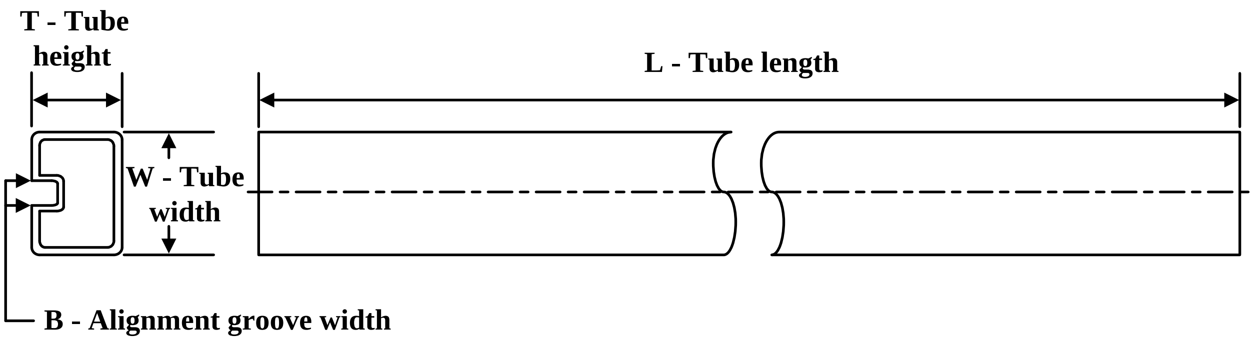
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317DCYR	SOT-223	DCY	4	2500	367.0	367.0	35.0
LM317DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
LM317DCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
LM317KTTR	DDPAK/TO-263	KTT	3	500	356.0	356.0	45.0
LM317KTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

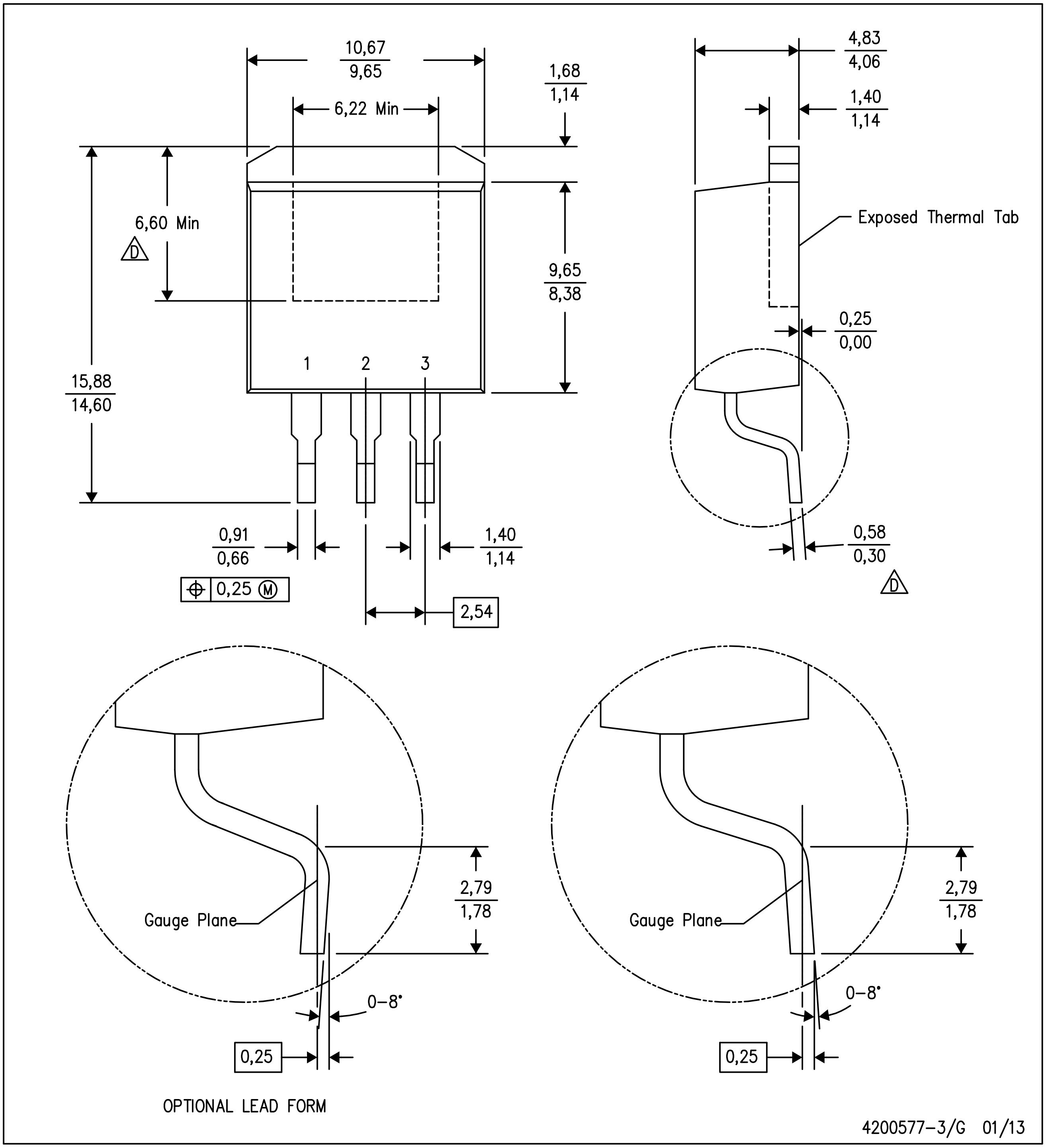
TUBE



*All dimensions are nominal

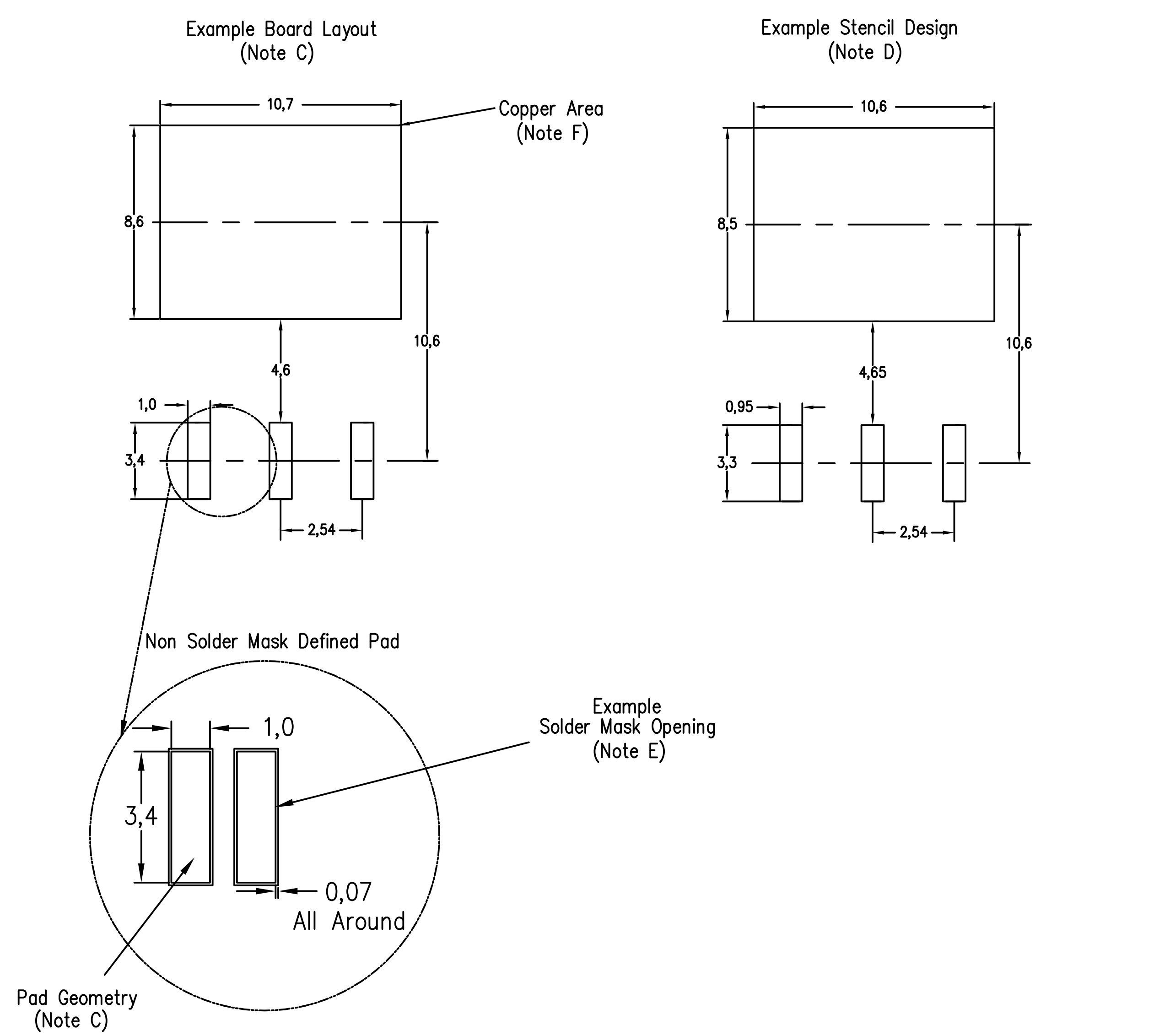
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM317DCY	DCY	SOT-223	4	80	559	8.6	500	3.6
LM317DCY	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
LM317DCY.A	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
LM317DCY.A	DCY	SOT-223	4	80	559	8.6	500	3.6
LM317DCY.B	DCY	SOT-223	4	80	559	8.6	500	3.6
LM317DCY.B	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
LM317DCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
LM317DCYG3	DCY	SOT-223	4	80	542.9	8.6	3606	2.67
LM317KCS	KCS	TO-220	3	50	532	34.1	700	9.6
LM317KCS.A	KCS	TO-220	3	50	532	34.1	700	9.6
LM317KCSE3	KCS	TO-220	3	50	532	34.1	700	9.6

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



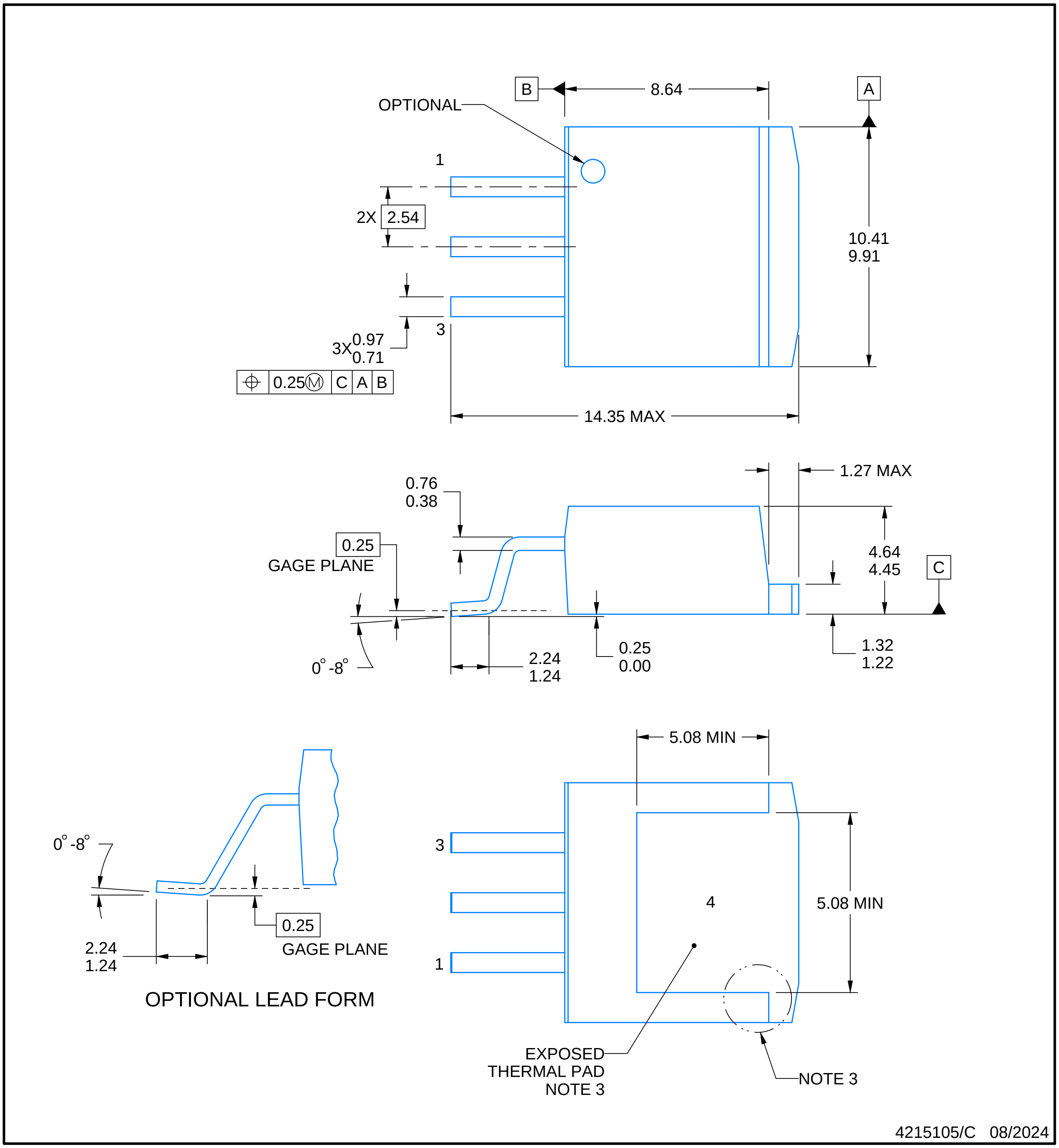
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



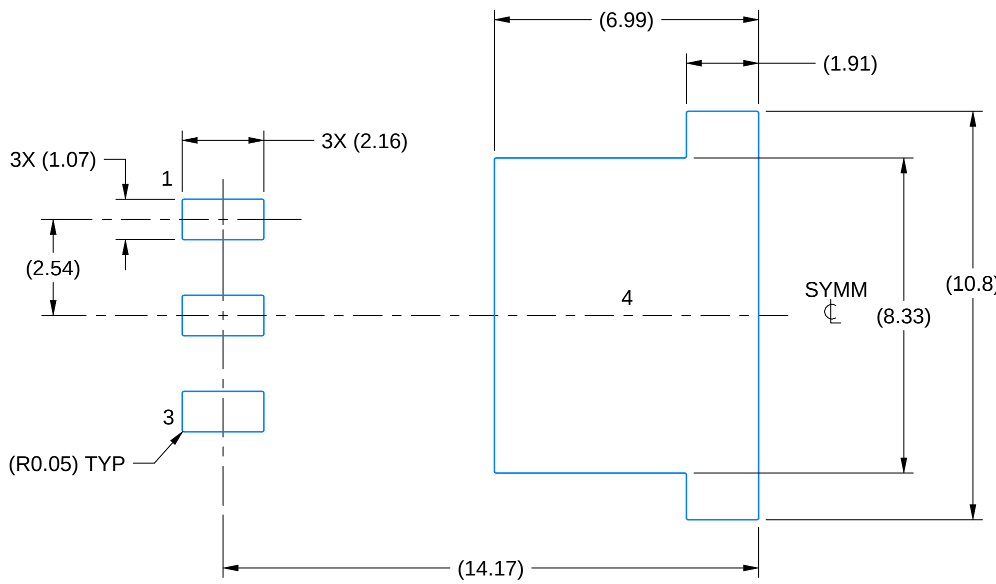
4208208–2/C 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

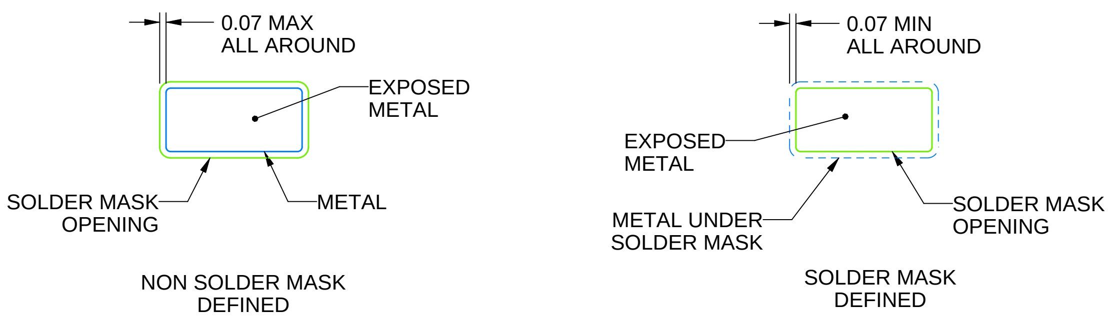


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263, except minimum lead thickness and minimum exposed pad length.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

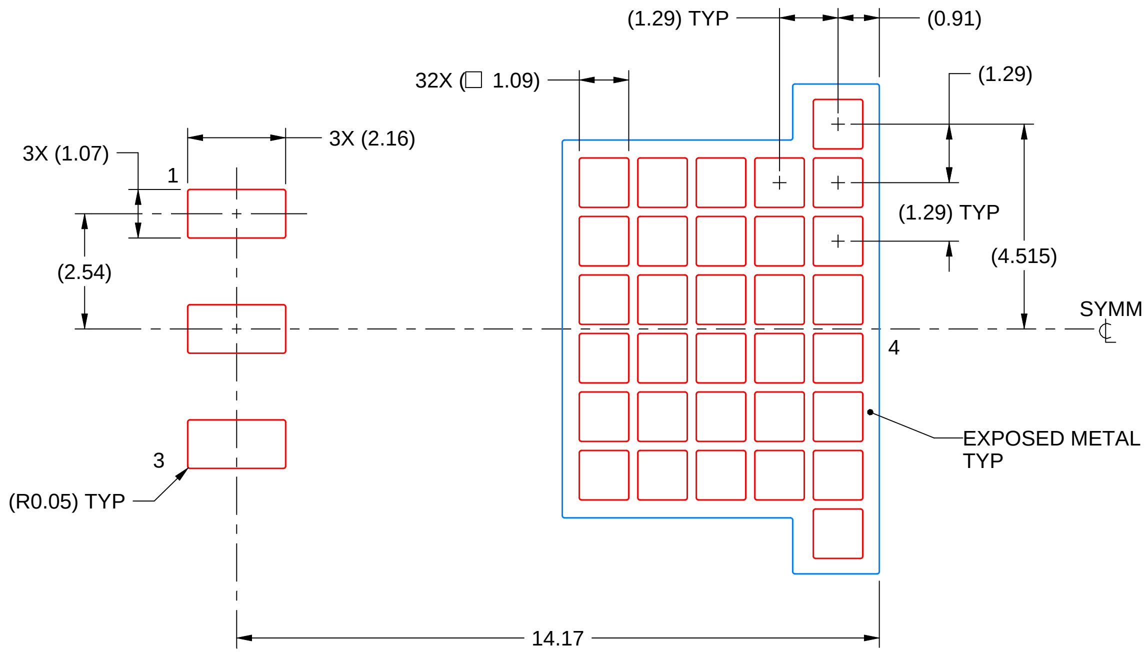


SOLDER MASK DETAILS

4215105/C 08/2024

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

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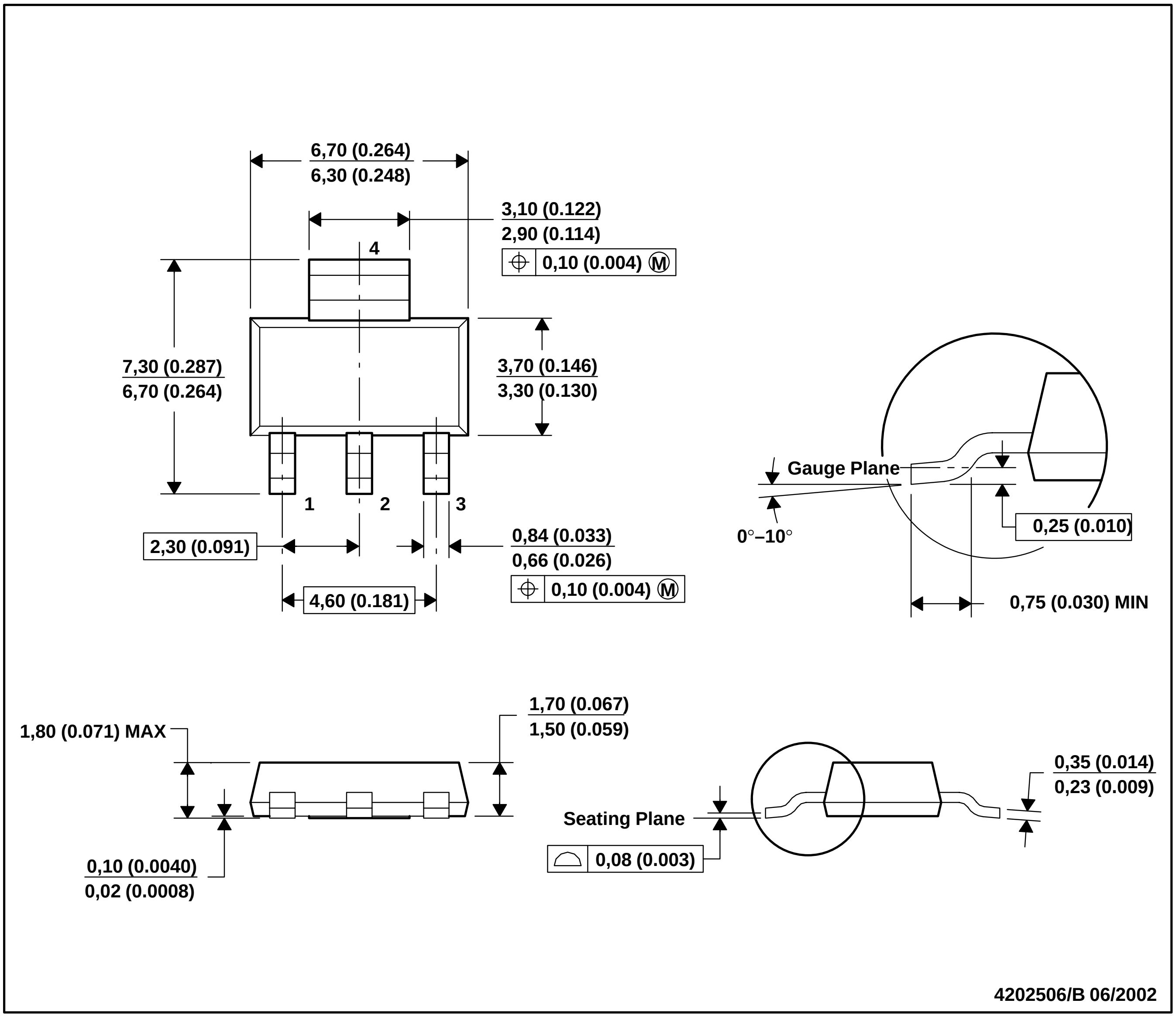
NOTES: (continued)

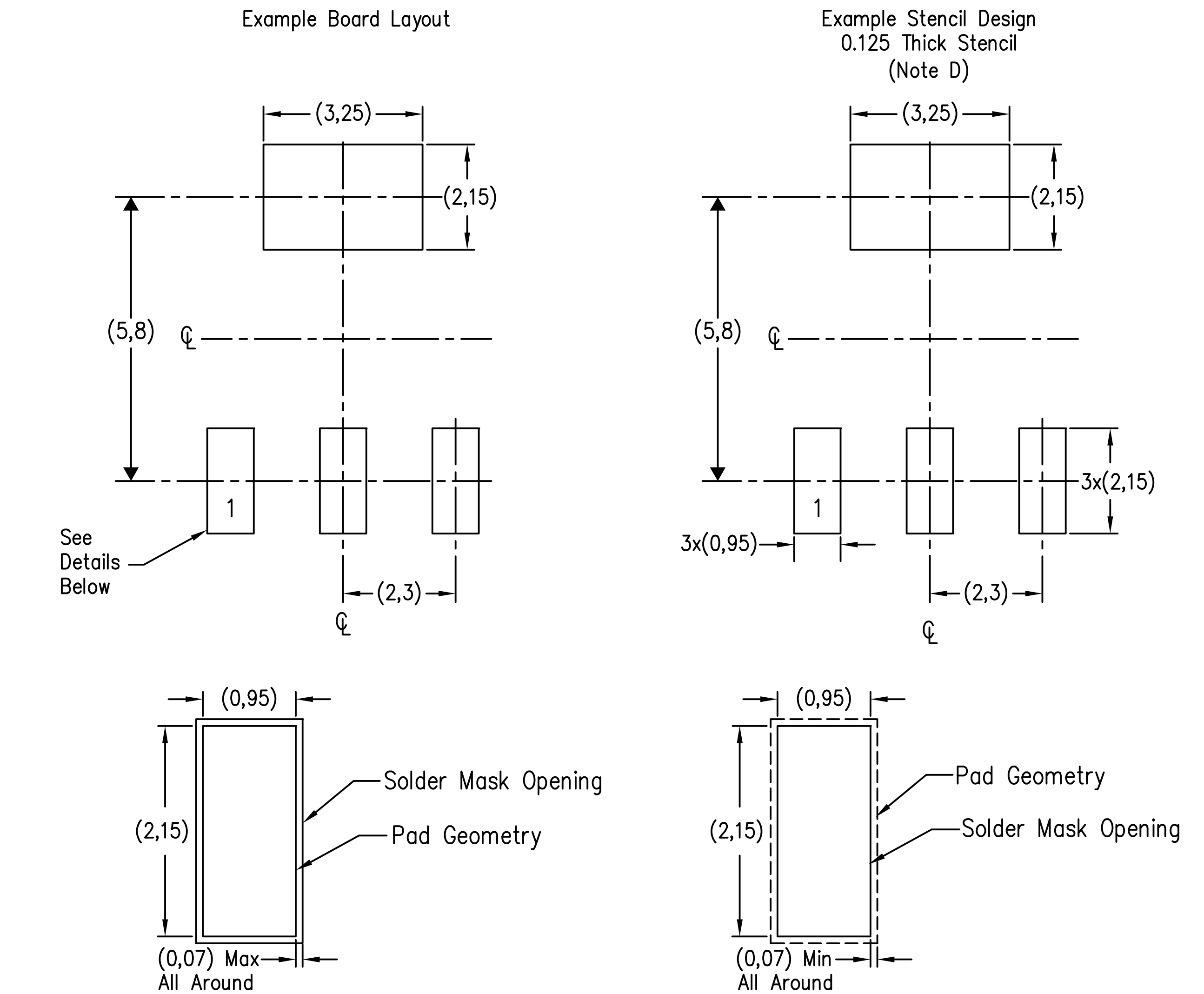
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE

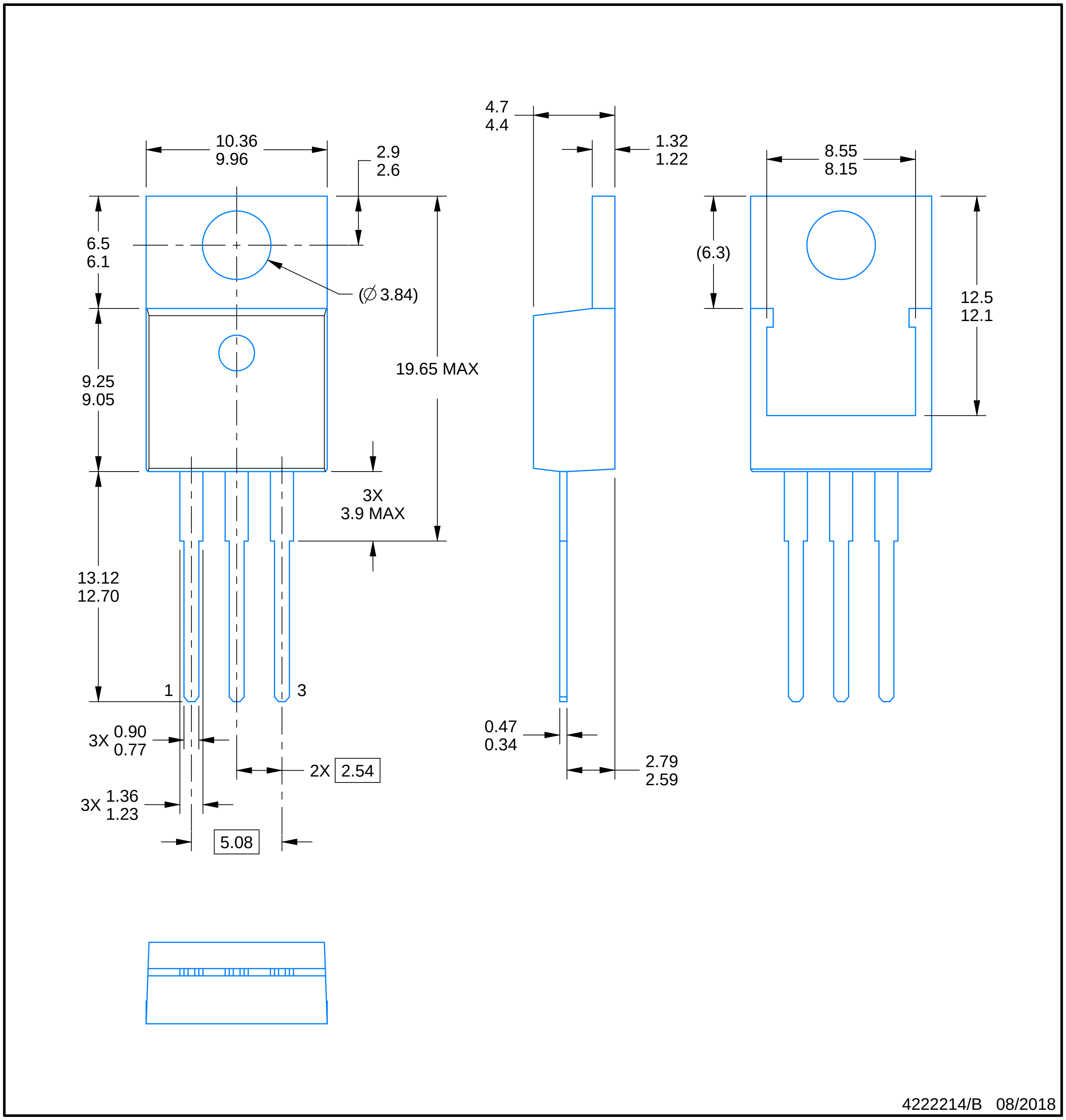


Example, non–solder mask defined pad.
(Preferred)

Example, solder mask defined pad.

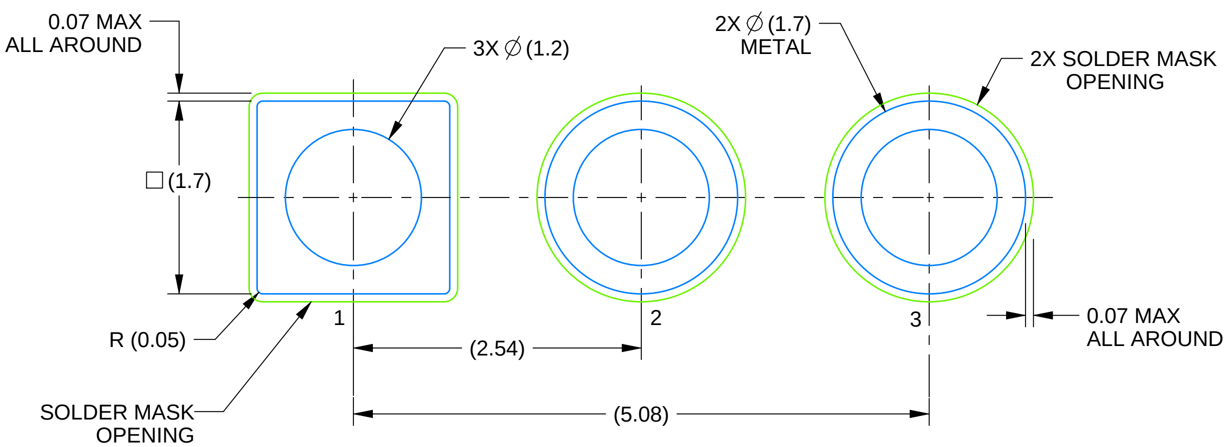
4210278/C 07/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.



NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X