LM36923 Highly Efficient Triple-String White LED Driver

1 Features

- 1% Matched Current Sinks Across (Process, Voltage, Temp)
- 3% Current Sink Accuracy Across (Process, Voltage, Temp)
- 11-Bit Dimming Resolution
- Up to 91.6% Solution Efficiency
- Drives from One to Three Parallel LED Strings at up to 28 V
- PWM Dimming Input
- I^2C Programmable
- Selectable 500-kHz and 1-MHz Switching Frequency with Optional –12% shift
- Auto Switch Frequency Mode (250 kHz, 500 kHz, 1 MHz)
- Four Configurable Overvoltage Protection Thresholds (17 V, 21 V, 25 V, 29 V)
- Four Configurable Overcurrent Protection Thresholds (750 mA, 1000 mA, 1250 mA, 1500 mA)
- Thermal Shutdown Protection

2 Applications

Power Source for Smart Phone and Tablet Backlighting

3 Description

The LM36923 is an ultra-compact, highly efficient, threestring white-LED driver designed for LCD display backlighting. The device can power up to 8 series LEDs at up to 25 mA per string. An adaptive current regulation method allows for different LED voltages in each string while maintaining current regulation.

The LED current is adjusted via an I^2C interface or through a logic level PWM input. The PWM duty cycle is internally sensed and mapped to an 11-bit current thus allowing for a wide range of PWM frequencies and noise-free operation.

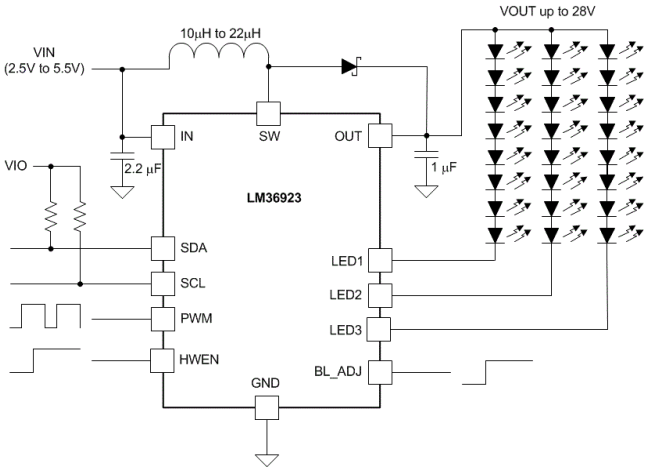
The device operates over the 2.5-V to 5.5-V input voltage range and -40°C to 85°C temperature range.

Device Information(1)

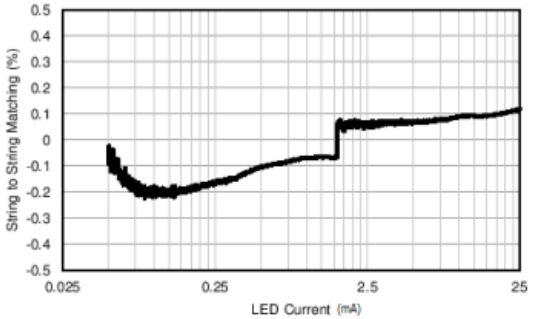
PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM36923	DSBGA (12)	1.755 mm × 1.355 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Typical String-to-String Matching vs LED Current



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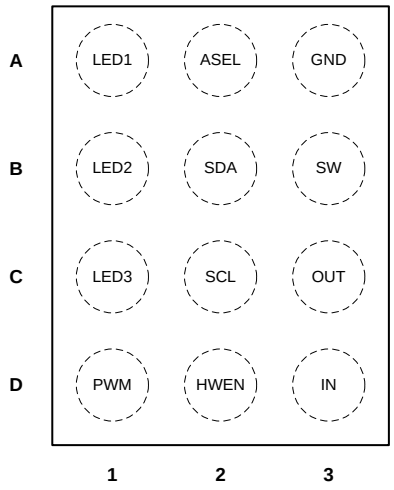
4 Revision History

Changes from Original (March 2015) to Revision A **Page**

- Changed pin name "VOUT" to "OUT" ... 3
- Changed pin name in Layout Example from 'VOUT' to 'OUT' ... 39

5 Pin Configuration and Functions

YFF Package
12-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	LED1	Input	Input to current sink 1. The boost converter regulates the minimum voltage between LED1, LED2, LED3 to VHR.
A2	BL_ADJ	Input	LED current adjust input. When BL_ADJ is driven to a logic high voltage the LED current steps down to the programmed low current value.
A3	GND	Input	Ground
B1	LED2	Input	Input pin to current sink 2. The boost converter regulates the minimum voltage between LED1, LED2 ,LED3 to VHR.
B2	SDA	I/O	Data I/O for I^2C-Compatible Interface.
B3	SW	Output	Drain Connection for internal low side NFET, and anode connection for external Schottky diode.
C1	LED3	Input	Input pin to current sink 3. The boost converter regulates the minimum voltage between LED1, LED2, LED3 to VHR.
C2	SCL	Input	Clock Input for I^2C-compatible interface.
C3	OUT	Input	OUT serves as the sense point for overvoltage protection. Connect OUT to the positive pin of the output capacitor.
D1	PWM	Input	Logic level input for PWM current control.
D2	HWEN	Input	Hardware enable input. Drive HWEN high to bring the device out of shutdown and allow I^2C writes or PWM control.
D3	IN	Input	Input voltage connection. Bypass IN to GND with a minimum 2.2-µF ceramic capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN	Input voltage	–0.3	6	V
OUT	Output overvoltage sense input	–0.3	30	V
SW	Inductor connection	–0.3	30	V
LED1, LED2, LED3	LED string cathode connection	–0.3	30	V
HWEN, PWM, SDA, SCL, BL_ADJ	Logic I/Os	–0.3	6	V
Maximum junction temperature, T_{J_MAX}			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
IN	Input voltage	2.5	5.5	V
OUT	Overvoltage sense input	0	29.5	V
SW	Inductor connection	0	29.5	V
LED1, LED2, LED3	LED string cathode connection	0	29.5	V
HWEN, PWM, SDA, SCL, BL_ADJ	Logic I/Os	0	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		YFQ (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	
$\Psi_{\theta JT}$	Junction-to-top characterization parameter	2.9	
$\Psi_{\theta JB}$	Junction-to-board characterization parameter	43.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6 V, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BOOST							
I_{MATCH} (1)	LED current matching I_{LED1} to I_{LED2} to I_{LED3}	50 µA ≤ I_{LED} ≤ 25 mA, 2.7 V ≤ V_{IN} ≤ 5 V (linear or exponential mode)		–1%	0.1%	1%	
Accuracy	Absolute Accuracy (I_{LED1}, I_{LED2}, I_{LED3})	50 µA ≤ I_{LED} ≤ 25 mA, 2.7 V ≤ V_{IN} ≤ 5 V (linear or exponential mode)		–3%	0.1%	3%	
I_{LED_MIN}	Minimum LED current (per string)	PWM or I^2C current control (linear or exponential mode)			50		µA
I_{LED_MAX}	Maximum LED current (per string)				25		mA
R_{DNL}	IDAC ratio-metric DNL	exponential mode only			1/3 (0.3%)		LSB
V_{HR}	Regulated current sink headroom voltage	I_{LED} = 25 mA			210		mV
		I_{LED} = 5 mA			100		
V_{HR_MIN}	Current sink minimum headroom voltage	I_{LED} = 95% of nominal, I_{LED} = 5 mA			35	50	mV
Efficiency	Typical efficiency	V_{IN} = 3.7 V, I_{LED} = 5 mA/string, Typical Application circuit (3x7 LEDs), (P_{OUT}/P_{IN})			87%		
R_{NMOS}	NMOS switch on resistance	I_{SW} = 250 mA			0.25		Ω
I_{CL}	NMOS switch current limit	2.7 V ≤ V_{IN} ≤ 5 V	OCP = 00	575	750	875	mA
			OCP = 01	860	1000	1110	
			OCP = 10	1100	1250	1400	
			OCP = 11	1350	1500	1650	
V_{OVP}	Output overvoltage protection	ON threshold, 2.7 V ≤ V_{IN} ≤ 5 V	OVP = 00	16	17	17.5	V
			OVP = 01	20	21	21.5	
			OVP = 10	24	25	25.5	
			OVP = 11	28	29	29.5	
OVP Hysteresis					0.5		V
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5 V, boost frequency shift = 0	Boost frequency select = 0	475	500	525	kHz
			Boost frequency select = 1	950	1000	1050	
D_{MAX}	Maximum boost duty cycle			92%	94%		
I_{SHDN}	Shutdown current	Chip enable bit = 0, SDA = SCL = IN or GND, 2.7 V ≤ V_{IN} ≤ 5 V			1.2	5	µA
T_{SD}	Thermal shutdown				135		°C
	Hysteresis				15		
PWM INPUT							
Min f_{PWM}						50	Hz
Max f_{PWM}		Sample rate = 24 MHz		50			kHz
t_{MIN_ON}	Minimum pulse ON time	Sample rate = 24 MHz				183.3	ns
		Sample rate = 4 MHz				1100	
		Sample rate = 800 kHz				5500	
t_{MIN_OFF}	Minimum pulse OFF time	Sample rate = 24 MHz				183.3	ns
		Sample rate = 4 MHz				1100	
		Sample rate = 800 kHz				5500	

(1) LED Current Matching between strings is given as the worst case matching between any two strings. Matching is calculated as ((I_{LEDX} – I_{LEDY})/(I_{LEDX} + I_{LEDY}) × 100.

Electrical Characteristics (continued)

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6 V, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{START-UP}$	Turn-on delay from shutdown to backlight on	PWM input active, PWM = logic high,HWEN input from low to high, f_{PWM} = 10 kHz (50% duty cycle)		3.5	5	ms
PWM_{RES}	PWM input resolution	1.6 kHz ≤ f_{PWM} ≤ 12 kHz, PWM hysteresis = 00, PWM sample rate = 11			11	bits
V_{IH}	Input logic high	HWEN, BL_ADJ, SCL, SDA, PWM inputs	1.25		V_{IN}	V
V_{IL}	Input logic low	HWEN, BL_ADJ, SCL, SDA, PWM inputs	0		0.4	
t_{GLITCH}	PWM input glitch rejection	PWM pulse filter = 00		0	15	ns
		PWM pulse filter = 01	60	100	140	
		PWM pulse filter = 10	90	150	210	
		PWM pulse filter = 11	120	200	280	
t_{PWM_STBY}	PWM shutdown period	Sample rate = 24 MHz	0.54	0.6	0.66	ms
		Sample rate = 4 MHz	2.7	3	3.3	
		Sample rate = 800 kHz	22.5	25	27.5	

6.6 I²C Timing Requirements

		MIN	TYP	MAX	UNIT
t1	SCL clock period	2.5			µs
t2	Data in setup time to SCL high	100			ns
t3	Data out stable after SCL low	0			ns
t4	SDA low Setup Time to SCL low (start)	100			ns
t5	SDA high hold time after SCL high (stop)	100			ns

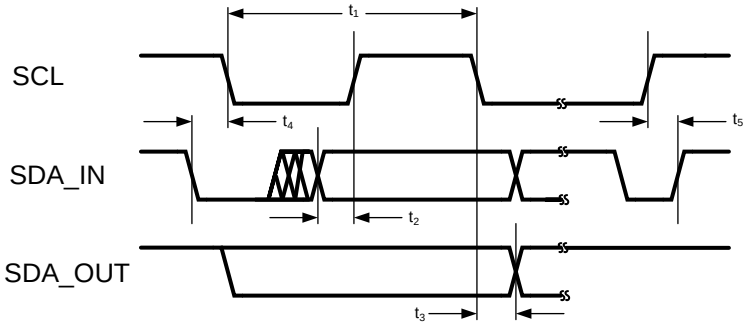


Figure 1. I²C Timing

6.7 Typical Characteristics

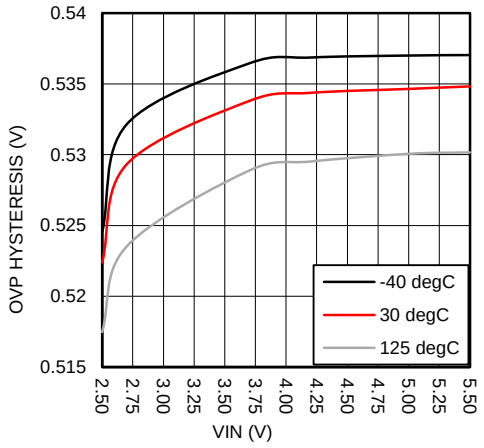


Figure 2. OVP Hysteresis

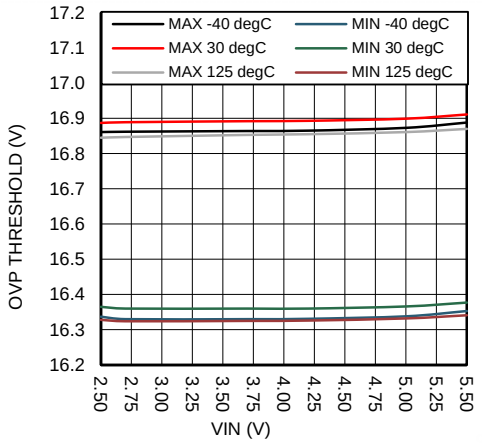


Figure 3. 17-V OVP Threshold

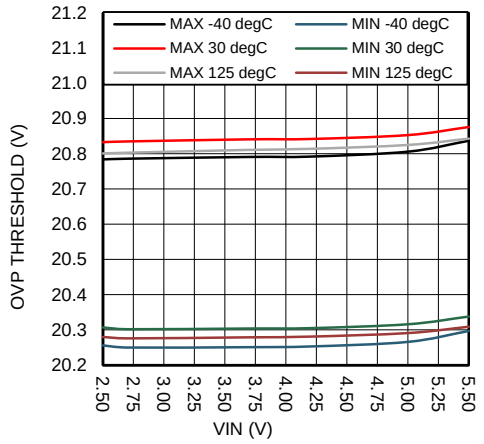


Figure 4. 21-V OVP Threshold

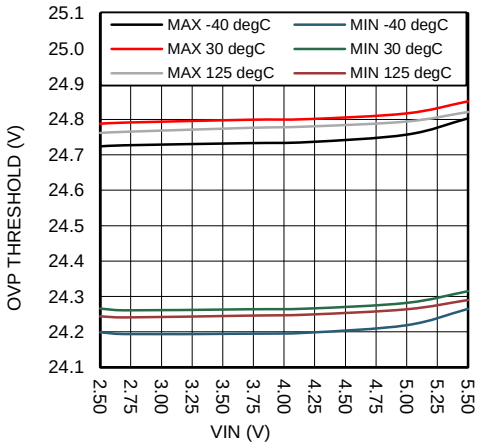


Figure 5. 25-V OVP Threshold

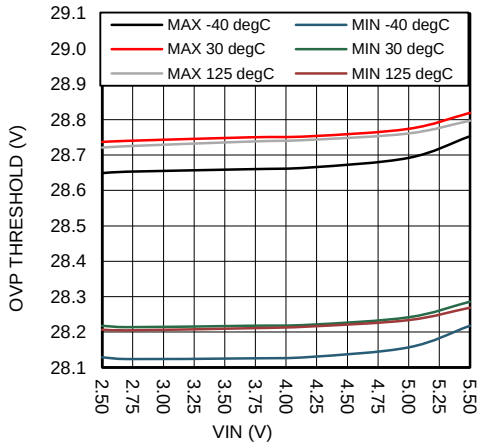


Figure 6. 29-V OVP Threshold

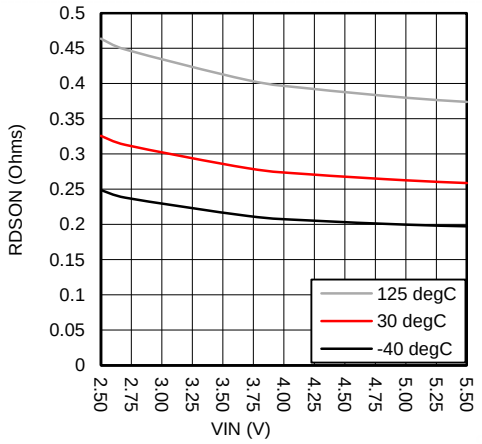
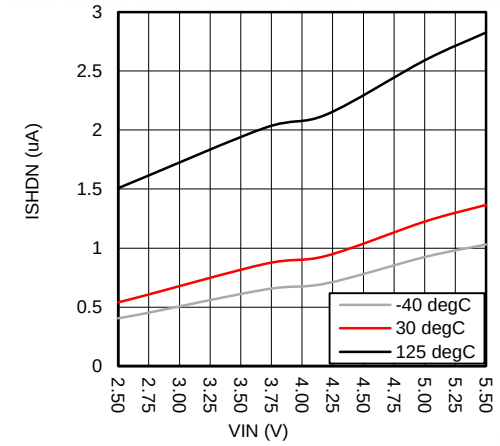


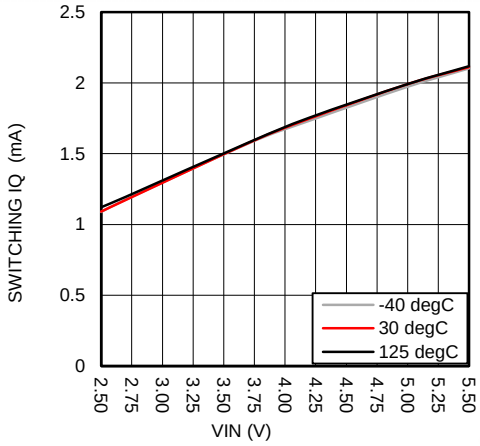
Figure 7. R_{DSON}

Typical Characteristics (continued)



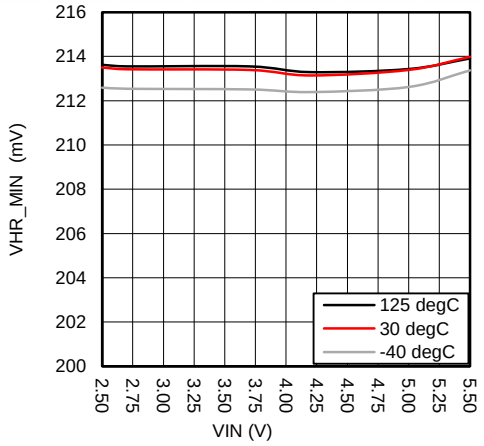
HWEN = GND

Figure 8. Shutdown Current



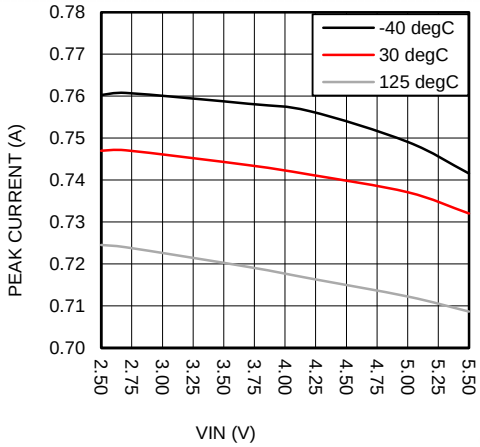
f_{SW}= 1 Mhz No Load

Figure 9. I_Q Current (Switching)



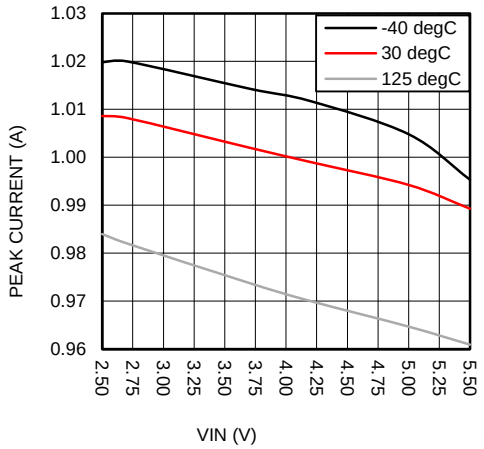
I_{LED} = 25 mA

Figure 10. VHR MIN



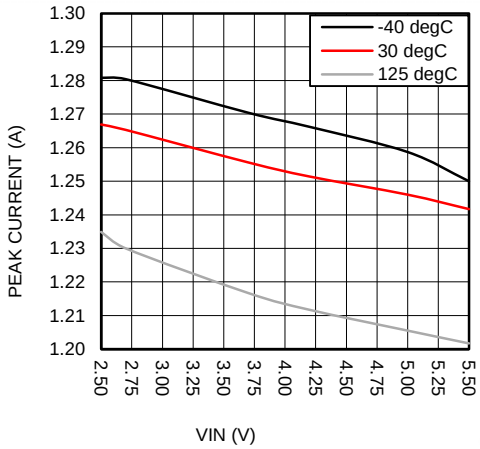
Open Loop

Figure 11. 750-mA OCP Current



Open Loop

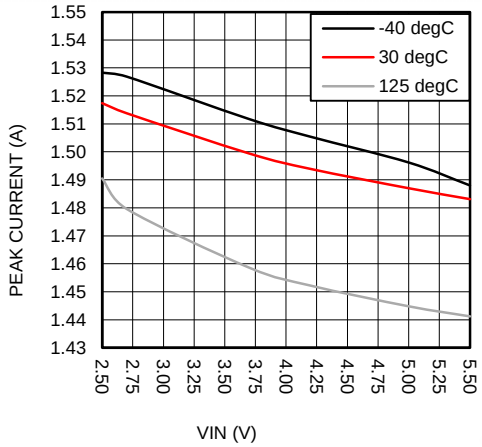
Figure 12. 1000-mA OCP Current



Open Loop

Figure 13. 1250-mA OCP Current

Typical Characteristics (continued)



Open Loop

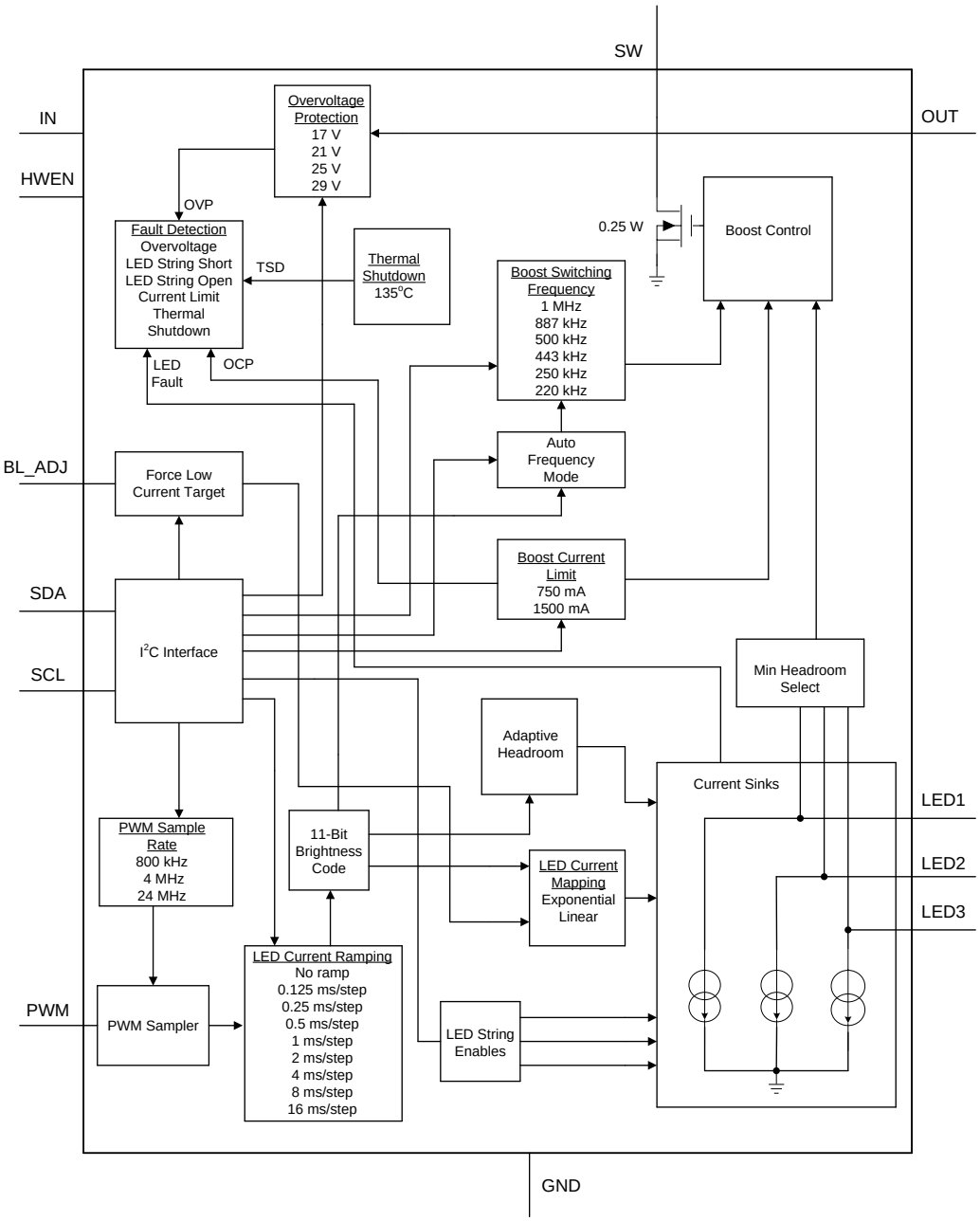
Figure 14. 1500-mA OCP Current

7 Detailed Description

7.1 Overview

The LM36923 is an inductive boost plus 3 current sink white-LED driver designed for powering from one to three strings of white LEDs used in display backlighting. The device operates over the 2.5-V to 5.5-V input voltage range. The 11-bit LED current is set via an I^2C interface, via a logic level PWM input, or a combination of both.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enabling the LM36923

The LM36923 has a logic level input HWEN which serves as the master enable/disable for the device. When HWEN is low the device is disabled, the registers are reset to their default state, the I^2C bus is inactive, and the device is placed in a low-power shutdown mode. When HWEN is forced high the device is enabled, and I^2C writes are allowed to the device.

7.3.1.1 Current Sink Enable

Each current sink in the device has a separate enable input. This allows for a 1-string, 2-string, or 3-string application. The default is with three strings enabled. Once the correct LED string configuration is programmed, the device can be enabled by writing the chip enable bit high (register 0x10 bit[0]), and then either enabling PWM and driving PWM high, or writing a non-zero code to the brightness registers.

The default setting for the device is with the chip enable bit set to 1, PWM input enabled, and the device in linear mapped mode. Therefore, on power up once HWEN is driven high, the device enters the standby state and actively monitors the PWM input. After a non-zero PWM duty cycle is detected the LM36923 converts the duty cycle information to the linearly weighted 11-bit brightness code. This allows for operation of the device in a stand-alone configuration without the need for any I^2C writes. Figure 15 and Figure 16 describe the start-up timing for operation with both PWM controlled current and with I^2C controlled current.

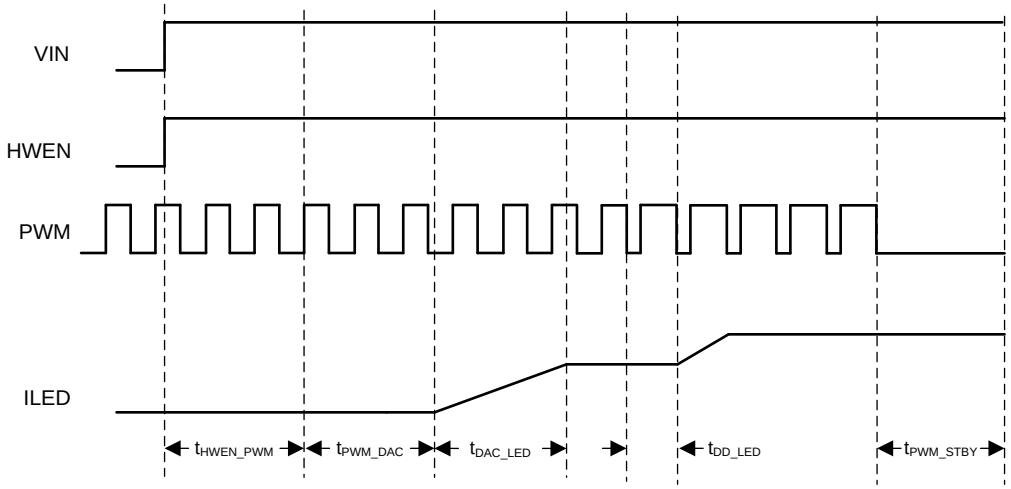


Figure 15. Enabling the LM36923 via PWM

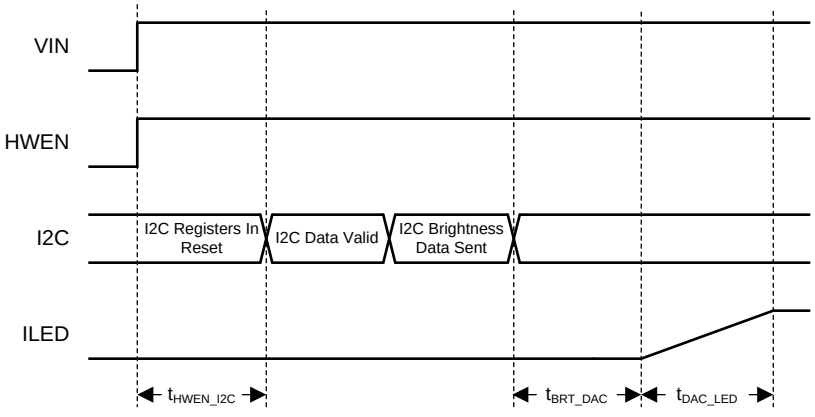


Figure 16. Enabling the LM36923 via I^2C

Feature Description (continued)

7.3.2 LM36923 Start-Up

The LM36923 can be enabled or disabled in various ways. When disabled, the device is considered shutdown, and the quiescent current drops to I_{SHDN}. When the device is in standby, it returns to the I_{SHDN} current level retaining all programmed register values. Table 1 describes the different operating states for the LM36923.

Table 1. LM36923 Operating Modes

LED STRING ENABLES 0x10 bits[3:1]	PWM INPUT	I²C BRIGHTNESS REGISTERS 0x18 bits[2:0] 0x19 bits[7:0]	BRIGHTNESS MODE 0x11 bits[6:5]	DEVICE ENABLE 0x10 bit[0]	LED CURRENT	
					(EXP MAPPING) 0x11 bit[7] = 1	(LIN MAPPING) 0x11 bit[7] = 0
XXX	X	XXX	XX	0	Off, device disabled	
0	X	XXX	XX	1	Off, device standby	
At least one enabled	X	0	00	1	Off, device in standby	
At least one enabled	X	Code > 000	00	1	$I_{LED} = 50\mu A \times 1.003040572^{Code}$ See (1)	$I_{LED} = 37.806\mu A + 12.195\mu A \times Code$ See (1)
At least one enabled	0	XXX	01	1	Off, device in standby	
At least one enabled	PWM Signal	XXX	01	1	$I_{LED} = 50\mu A \times 1.003040572^{Code}$ See (1)	$I_{LED} = 37.806\mu A + 12.195\mu A \times Code$ See (1)
At least one enabled	0	XXX	10 or 11	1	Off, device in standby	
At least one enabled	X	0	10 or 11	1	Off, device in standby	
At least one enabled	PWM Signal	Code > 000	10 or 11	1	$I_{LED} = 50\mu A \times 1.003040572^{Code}$ See (1)	$I_{LED} = 37.806\mu A + 12.195\mu A \times Code$ See (1)

(1) Code is the 11-bit code output from the ramper (see Figure 21, Figure 23, Figure 25, Figure 27). This can be the I²C brightness code, the converted PWM duty cycle or the 11-bit product of both.

7.3.3 Brightness Mapping

There are two different ways to map the brightness code (or PWM duty cycle) to the LED current: linear and exponential mapping.

7.3.3.1 Linear Mapping

For linear mapped mode the LED current increases proportionally to the 11-bit brightness code and follows the relationship:

$$I_{LED} = 37.806\mu A + 12.195\mu A \times Code \quad (1)$$

This is valid from codes 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the I²C brightness code, the digitized PWM duty cycle, or the product of the two.

7.3.3.2 Exponential Mapping

In exponential mapped mode the LED current follows the relationship:

$$I_{LED} = 50\mu A \times 1.003040572^{Code} \quad (2)$$

This results in an LED current step size of approximately 0.304% per code. This is valid for codes from 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the I²C brightness code, the digitized PWM duty cycle, or the product of the two. Figure 17 details the LED current exponential response.

The 11-bit (0.304%) per code step is small enough such that the transition from one code to the next in terms of LED brightness is not distinguishable to the eye. This therefore gives a perfectly smooth brightness increase between adjacent codes.

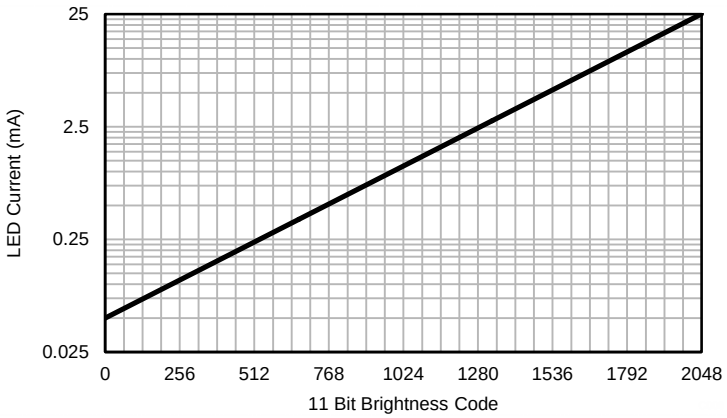


Figure 17. LED Current vs Brightness Code (Exponential Mapping)

7.3.4 PWM Input

The PWM input is a sampled input which converts the input duty cycle information into an 11-bit brightness code. The use of a sampled input eliminates any noise and current ripple that traditional PWM controlled LED drivers are susceptible to.

The PWM input uses logic level thresholds with V_{IH_MIN} = 1.25 V and V_{IL_MAX} = 0.4 V. Since this is a sampled input, there are limits on the max PWM input frequency as well as the resolution that can be achieved.

7.3.4.1 PWM Sample Frequency

There are four selectable sample rates for the PWM input. The choice of sample rate depends on three factors:

1. Required PWM Resolution (input duty cycle to brightness code, with 11 bits max)
2. PWM Input Frequency
3. Efficiency

7.3.4.1.1 PWM Resolution and Input Frequency Range

The PWM input frequency range is 50 Hz to 50 kHz. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code (BRT), the input PWM duty cycle must be ≥ 11 bits, and the PWM sample period ($1/f_{SAMPLE}$) must be smaller than the minimum PWM input pulse width. Figure 18 shows the possible brightness code resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is described in *PWM Timeout*.

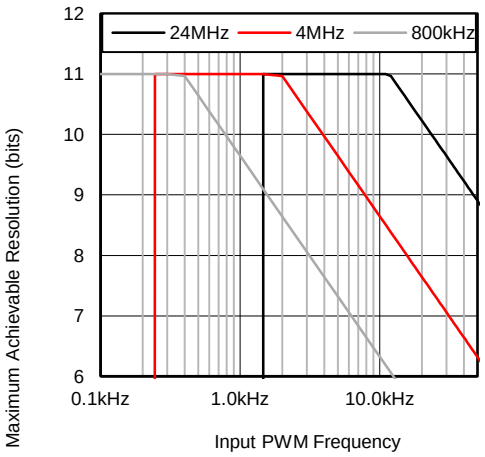


Figure 18. PWM Sample Rate, Resolution, and PWM Input Frequency

7.3.4.1.2 PWM Sample Rate and Efficiency

Efficiency is maximized when the lowest f_{SAMPLE} is chosen since this lowers the quiescent operating current of the device. Table 2 describes the typical efficiency tradeoffs for the different sample clock settings.

Table 2. PWM Sample Rate Trade-Offs

PWM SAMPLE RATE (f_{SAMPLE})	TYPICAL INPUT CURRENT, DEVICE ENABLED I_{LED} = 10 mA/string, 2 x 7 LEDs	TYPICAL EFFICIENCY
(0x12 Bits[7:6])	f_{SW} = 1 MHz	V_{IN} = 3.7 V
0	1.03 mA	90.7%
1	1.05 mA	90.6%
1X	1.35 mA	90.4%

7.3.4.1.2.1 PWM Sample Rate Example

The number of bits of resolution on the PWM input varies according to the PWM Sample rate and PWM input frequency.

Table 3. PWM Resolution vs PWM Sample Rate

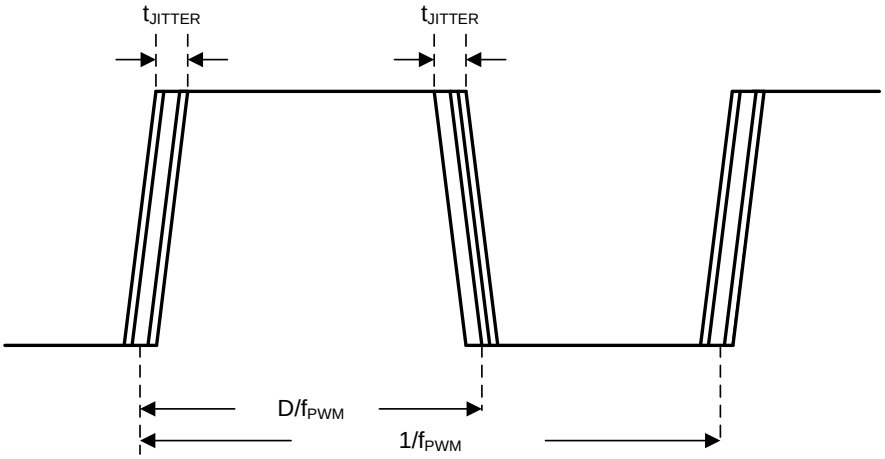
PWM FREQUENCY (kHz)	RESOLUTION (PWM SAMPLE RATE = 800 kHz)	RESOLUTION (PWM SAMPLE RATE = 4 MHz)	RESOLUTION (PWM SAMPLE RATE = 24 MHz)
0.4	11	11	11
2	8.6	11	11
12	6.1	8.4	11

7.3.4.2 PWM Hysteresis

To prevent jitter at the input PWM signal from feeding through the PWM path and causing oscillations in the LED current, the LM36923 offers 7 selectable hysteresis settings. The hysteresis works by forcing a specific number of 11-bit LSB code transitions to occur in the input duty cycle before the LED current changes. Table 4 describes the hysteresis. The hysteresis only applies during the change in direction of brightness currents. Once the change in direction has taken place, the PWM input must over come the required LSB(s) of the hysteresis setting before the brightness change takes effect. Once the initial hysteresis has been overcome and the direction in brightness change remains the same, the PWM to current response changes with no hysteresis.

Table 4. PWM Input Hysteresis

HYSTERESIS SETTING (0x12 Bits[4:2])	MIN CHANGE IN PWM PULSE WIDTH (Δt) REQUIRED TO CHANGE LED CURRENT, AFTER DIRECTION CHANGE (for f_{PWM} < 11.7 kHz)	MIN CHANGE IN PWM DUTY CYCLE (ΔD) REQUIRED TO CHANGE LED CURRENT AFTER DIRECTION CHANGE	MIN (ΔI_{LED}), INCREASE FOR INITIAL CODE CHANGE	
			EXPONENTIAL MODE	LINEAR MODE
000 (0 LSB)	$1/(f_{PWM} \times 2047)$	0.05%	0.30%	0.05%
001 (1 LSB)	$1/(f_{PWM} \times 1023)$	0.10%	0.61%	0.10%
010 (2 LSBs)	$1/(f_{PWM} \times 511)$	0.20%	1.21%	0.20%
011 (3 LSBs)	$1/(f_{PWM} \times 255)$	0.39%	2.40%	0.39%
100 (4 LSBs)	$1/(f_{PWM} \times 127)$	0.78%	4.74%	0.78%
101 (5 LSBs)	$1/(f_{PWM} \times 63)$	1.56%	9.26%	1.56%
110 (6 LSBs)	$1/(f_{PWM} \times 31)$	3.12%	17.66%	3.12%



- D is t_{JITTER} x f_{PWM} or equal to #LSB's = ΔD x 2048 codes.
- For 11-bit resolution, #LSBs is equal to a hysteresis setting of LN(#LSB's)/LN(2).
- For example, with a t_{JITTER} of 1 µs and a f_{PWM} of 5 kHz, the hysteresis setting should be: LN(1 µ s x 5 kHz x 2048)/LN(2) = 3.35 (4 LSBs).

Figure 19. PWM Hysteresis Example

7.3.4.3 PWM Step Response

The LED current response due to a step change in the PWM input is approximately 2 ms to go from minimum LED current to maximum LED current.

7.3.4.4 PWM Timeout

The LM36923 PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected. The timeout duration changes based on the PWM Sample Rate selected which results in a minimum supported PWM input frequency. The sample rate, timeout, and minimum supported PWM frequency are summarized in Table 5.

Table 5. PWM Timeout and Minimum Supported PWM Frequency vs PWM Sample Rate

SAMPLE RATE	TIMEOUT	MINIMUM SUPPORTED PWM FREQUENCY
0.8 MHz	25 msec	48 Hz
4 MHz	3 msec	400 Hz
24 MHz	0.6 msec	2000 Hz

7.3.5 LED Current Ramping

There are 8 programmable ramp rates available in the LM36923. These ramp rates are programmable as a time per step. Therefore, the ramp time from one current set-point to the next, depends on the number of code steps between currents and the programmed time per step. This ramp time to change from one brightness set-point (Code A) to the next brightness set-point (Code B) is given by:

$$\Delta t = Ramp\_rate \times (Code\ B - CodeA - 1) \quad (3)$$

For example, assume the ramp is enabled and set to 1 ms per step. Additionally, the brightness code is set to 0x444 (1092d). Then the brightness code is adjusted to 0x7FF (2047d). The time the current takes to ramp from the initial set-point to max brightness is:

(4)

$$\Delta t = \frac{1ms}{step} \times (0x7FF - 0x444 - 1) = 954ms \quad (5)$$

7.3.6 Regulated Headroom Voltage

In order to optimize efficiency, current accuracy, and string-to-string matching the LED current sink regulated headroom voltage (VHR) varies with the target LED current. Figure 20 details the typical variation of VHR with LED current. This allows for increased solution efficiency as the dropout voltage of the LED driver changes. Furthermore, in order to ensure that both current sinks remain in regulation whenever there is a mismatch in string voltages, the minimum headroom voltage between VLED1, VLED2, VLED3 becomes the regulation point for the boost converter. For example, if the LEDs connected to LED1 require 12 V, the LEDs connected to LED2 require 12.5 V , and the LEDs connected to LED3 require 13 V at the programmed current, then the voltage at LED1 is VHR + 1 V, the voltage at LED2 is VHR + 0.5 V, and the voltage at LED3 is regulated at VHR. In other words, the boost makes the cathode of the highest voltage LED string the regulation point.

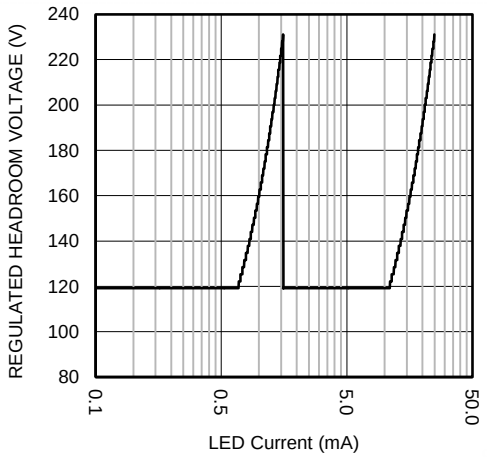


Figure 20. LM36923 Typical Exponential Regulated Headroom Voltage vs Programmed LED Current

7.4 Device Functional Modes

Device Functional Modes describes the different operating modes and features available within the LM36923.

7.4.1 Brightness Control Modes

The LM36923 has 4 brightness control modes:

1. I^2C Only (brightness mode 00)
2. PWM Only (brightness mode 01)
3. I^2C × PWM with ramping only between I^2C codes (brightness mode 10)
4. I^2C × PWM with ramping between I^2C × PWM changes (brightness mode 11)

7.4.1.1 I^2C Only (Brightness Mode 00)

In brightness control mode 00 the I^2C Brightness registers are in control of the LED current, and the PWM input is disabled. The brightness data (BRT) is the concatenation of the two brightness registers (3 LSBs) and (8 MSBs) (registers 0x18 and 0x19, respectively). The LED current only changes when the MSBs are written, meaning that to do a full 11-bit current change via I^2C, first the 3 LSBs are written and then the 8 MSBs are written. In this mode the ramper only controls the time from one I^2C brightness set-point to the next Figure 21.

Device Functional Modes (continued)

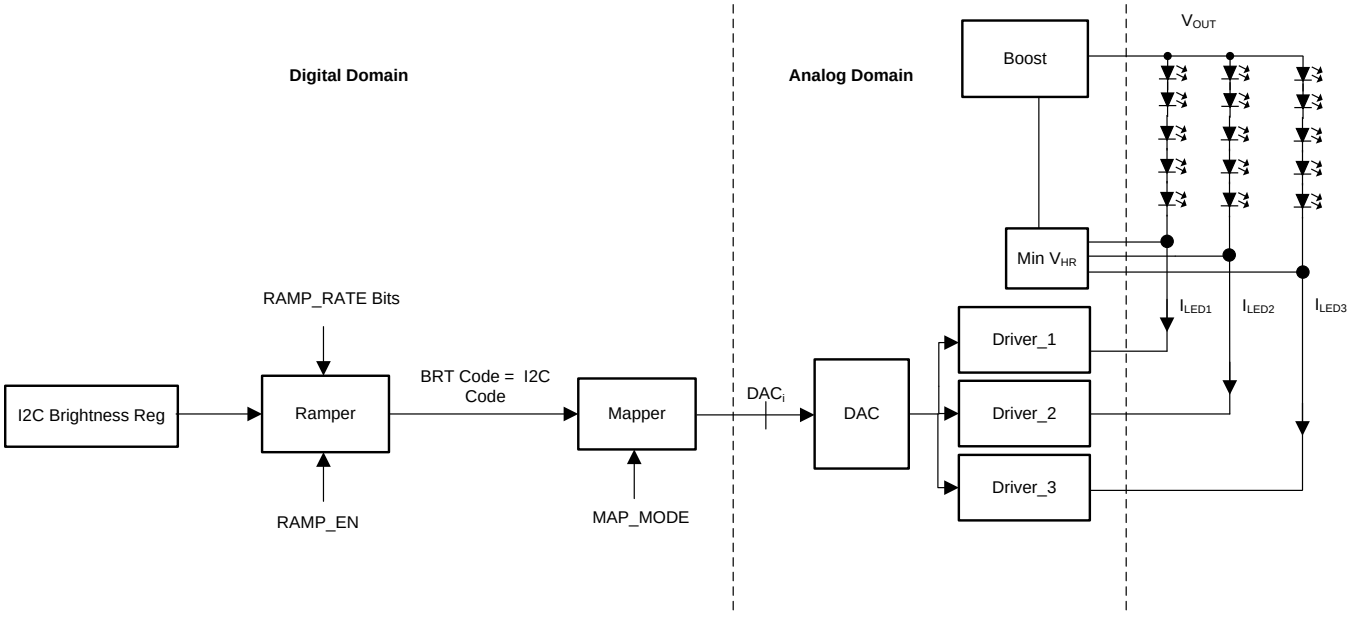
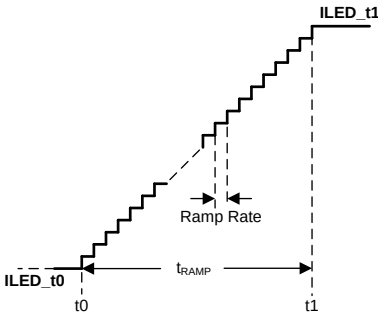


Figure 21. Brightness Control 00 (I²C Only)



1. At time t0 the I²C Brightness Code is changed from 0x444 (1092d) to 0x7FF (2047d)
2. Ramp Rate programmed to 1ms/step
3. Mapping Mode set to Linear
4. ILED_t0 = 1092 × 12.213 µA = 13.337 mA
5. ILED_t1 = 2047 × 12.213 µA = 25 mA
6. t_{RAMP} = (t1 – t0) = 1ms/step × (2047 – 1092 – 1) = 954 ms

Figure 22. I²C Brightness Mode 00 Example (Ramp Between I²C Code Changes)

7.4.1.2 PWM Only (Brightness Mode 01)

In brightness mode 01, only the PWM input sets the brightness. The I²C code is ignored. The LM36923 samples the PWM input, determines the duty cycle and this measured duty cycle is translated into an 11-bit digital code. The resultant code is then applied to the internal ramper (see Figure 23).

Device Functional Modes (continued)

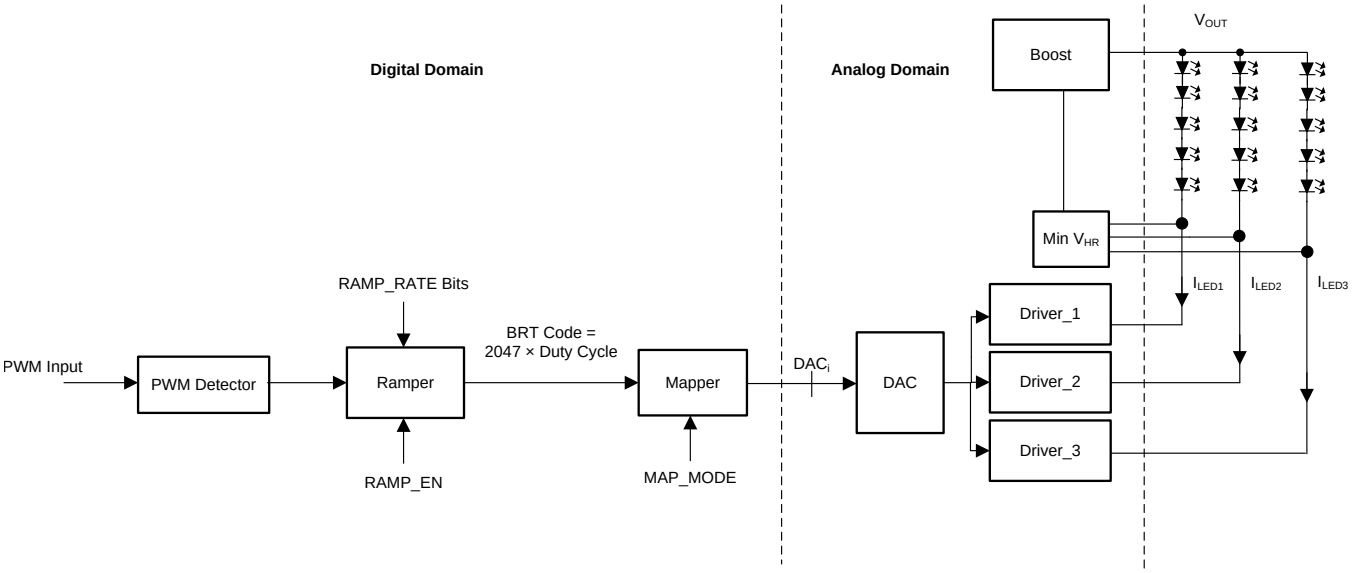
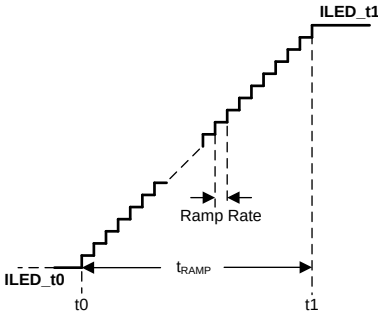


Figure 23. Brightness Control 01 (PWM Only)



1. At time t0 the PWM duty cycle changed from 25% to 100%
2. Ramp Rate programmed to 1 ms/step
3. Mapping Mode set to Linear
4. ILED_t0 = 25 mA × 0.25 = 6.25 mA
5. ILED_t1 = 25 mA × 1 = 25 mA
6. t_{RAMP} = (t1 – t0) = 1ms/step × (2047 × 1 – 2047 × 0.25 – 1) = 1534 ms

Figure 24. Brightness Control Mode 01 Example (Ramp Between Duty Cycle Changes)

7.4.1.3 I²C + PWM Brightness Control (Multiply Then Ramp) Brightness Mode 10

In brightness control mode 10 the I²C Brightness register and the PWM input are both in control of the LED current. In this case the I²C brightness code is multiplied with the PWM duty cycle to produce an 11-bit code which is then sent to the ramper. In this mode ramping is achieved between I²C x PWM currents (see Figure 25).

Device Functional Modes (continued)

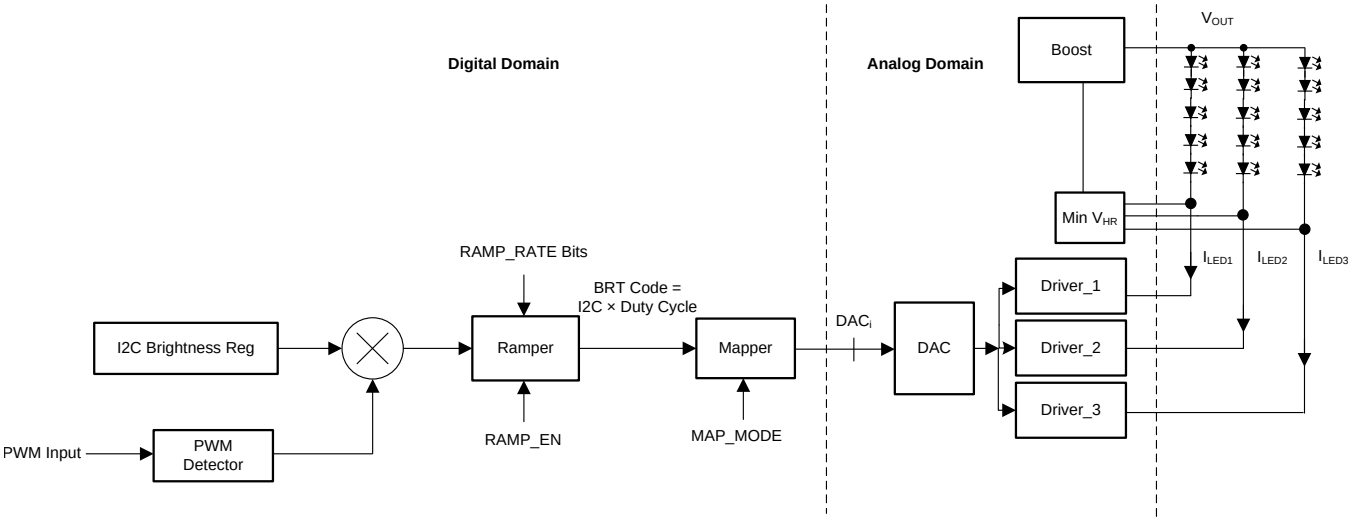
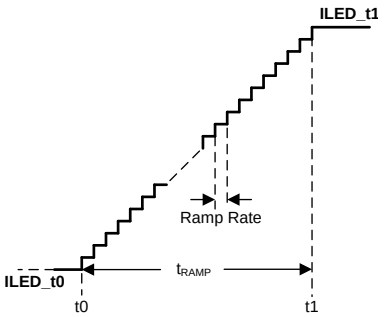


Figure 25. Brightness Control 10 (I^2C + PWM)



1. At time t0 the I^2C Brightness code changed from 0x444 (1092d) to 0x7FF (2047d)
2. At time t0 the PWM duty cycle changed from 50% to 75%
3. Ramp Rate programmed to 1ms/step
4. Mapping Mode set to Linear
5. ILED_t0 = 1092 × 12.213 µA × 0.5 = 6.668 mA
6. ILED_t1 = 2047 × 12.213 µA × 0.75 = 18.75 mA
7. t_{RAMP} = (t1 – t0) = 1ms/step × (2047 × 0.75 – 1092 × 0.5 – 1) = 988 ms

Figure 26. Brightness Control Mode 10 Example (Multiply Duty Cycle then Ramp)

7.4.1.4 I^2C + PWM Brightness Control (Ramp Then Multiply) Brightness Mode 11

In brightness control mode 11 both the I^2C brightness code and the PWM duty cycle control the LED current. In this case the ramper only changes the time from one I^2C brightness code to the next. The PWM duty cycle is multiplied with the I^2C brightness code at the output of the ramper (see Figure 27).

Device Functional Modes (continued)

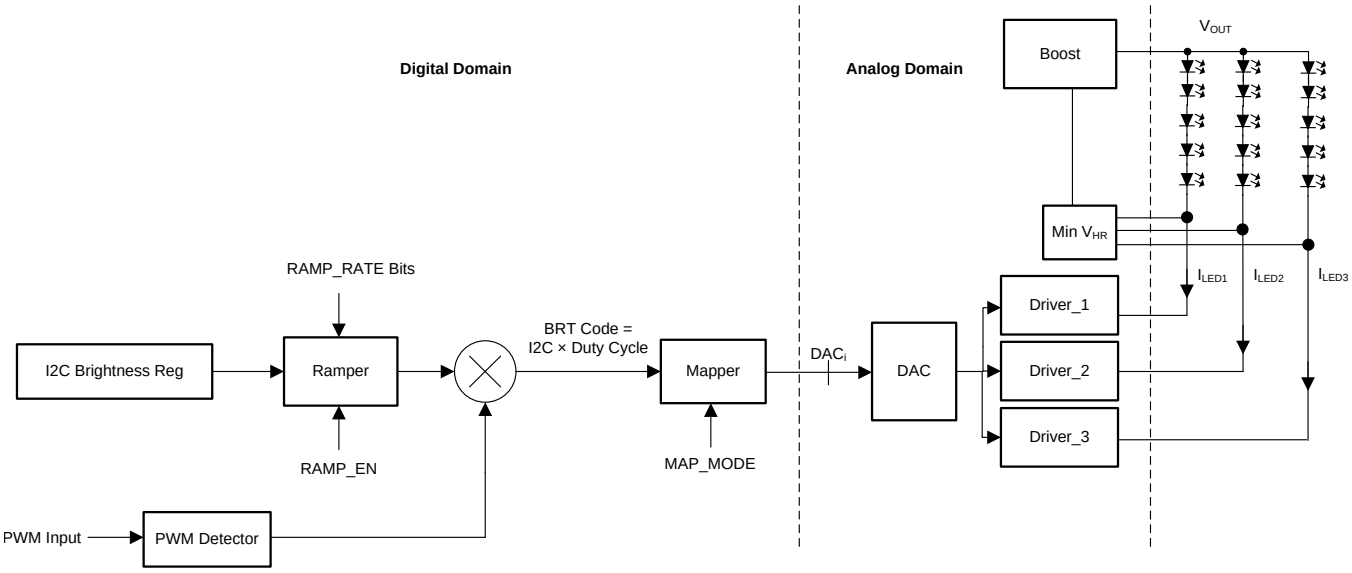
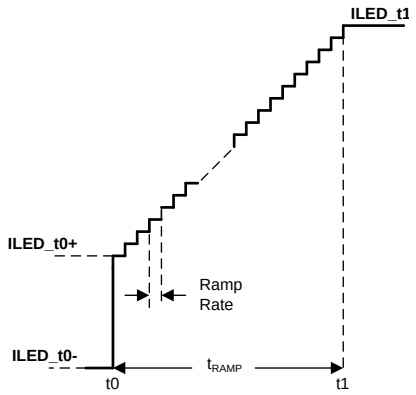


Figure 27. Brightness Control 11 (I^2C + PWM)



1. At time t0 the I^2C Brightness code changed from 0x444 (1092d) to 0x7FF (2047d)
2. At time t0 the PWM duty cycle changed from 50% to 75%
3. Ramp Rate programmed to 1 ms/step
4. Mapping Mode set to Linear
5. ILED_t0– = 1092 × 12.213 µA × 0.5 = 6.668 mA
6. ILED_t0+ = 1092 × 12.213 µA × 0.75 = 10.002 mA
7. t_{RAMP} = (t1 – t0) = 1 ms/step × (2047 – 1092 – 1) = 954 ms

Figure 28. Brightness Control Mode 11 Example (Ramp Current Then Multiply Duty Cycle)

7.4.2 Boost Switching Frequency

The LM36923 has two programmable switching frequencies: 500 kHz and 1 MHz. These are set via the Boost Control 1 register 0x13 bit [5]. Once the switching frequency is set, this nominal value can be shifted down by 12% via the boost switching frequency shift bit (register 0x13 bit[6]). Operation at 500 kHz is better suited for configurations which use a 22-µH inductor. Operation at 1 MHz is primarily beneficial when using a 10-µH inductor and where efficiency at maximum load current is more important. For maximum efficiency across the entire load current range the device incorporates an automatic frequency shift mode (see *Auto Switching Frequency*).

Device Functional Modes (continued)

7.4.2.1 Minimum Inductor Select

The LM36923 can use inductors in the range of 10 µH to 22 µH. In order to optimize the converter response to changes in V_{IN} and load, the Min Inductor Select bit (register 0x13 bit[4]) should be selected depending on which value of inductance is chosen. For 22-µH inductors this bit should be set to 1. For less than 22 µH, this bit should be set to 0.

7.4.3 Auto Switching Frequency

To take advantage of frequency vs load dependent losses, the LM36923 has the ability to automatically change the boost switching frequency based on the magnitude of the load current. In addition to the register programmable switching frequencies of 500 kHz and 1 MHz, the auto-frequency mode also incorporates a low frequency selection of 250 kHz. It is important to note that the 250-kHz frequency is only accessible in auto-frequency mode and has a maximum boost duty cycle (D_{MAX}) of 50%.

Auto-frequency mode operates by using 2 programmable registers (Auto Frequency High Threshold (register 0x15) and Auto Frequency Low Threshold (0x16)). The high threshold determines the switchover from 1 MHz to 500 kHz. The low threshold determines the switchover from 500 kHz to 250 kHz. Both the High and Low Threshold registers take an 8-bit code which is compared against the 8 MSB of the brightness register (register 0x19). Table 6 details the boundaries for this mode.

Table 6. Auto Switching Frequency Operation

BRIGHTNESS CODE MSBs (Register 0x19 bits[7:0])	BOOST SWITCHING FREQUENCY
< Auto Frequency Low Threshold (register 15 Bits[7:0])	250 kHz (D_{MAX} = 50%)
> Auto Frequency Low Threshold (Register 15 Bits[7:0]) or < Auto Frequency High Threshold (Register 14 Bits[7:0])	500 kHz
≥ Auto Frequency High Threshold (register 14 Bits[7:0])	1 MHz

Automatic-frequency mode is enabled whenever there is a non-zero code in either the Auto-Frequency High or Auto-Frequency Low registers. To disable the auto-frequency shift mode, set both registers to 0x00. When automatic-frequency select mode is disabled, the switching frequency operates at the programmed frequency (Register 0x13 bit[5]) across the entire LED current range. Table 7 provides a guideline for selecting the auto frequency 250-kHz threshold setting, the actual setting needs to be verified in the application.

Table 7. Auto Frequency 250-kHz Threshold Settings

CONDITION (V_f=3.2 V, I_{LED}=25 mA)	INDUCTOR (µH)	RECOMMENDED AUTO FREQUENCY LOW THRESHOLD MAXIMUM VALUE (NO SHIFT)	OUTPUT POWER AT AUTO FREQUENCY SWITCHOVER (W)
3 × 4 LEDs	10	0x17	0.079
3 × 5 LEDs	10	0x15	0.089
3 × 6 LEDs	10	0x13	0.097
3 × 7 LEDs	10	0x11	0.101
3 × 8 LEDs	10	0x0f	0.102

7.4.4 Backlight Adjust Input (BL_ADJ)

Driving BL_ADJ to a logic high voltage provides a way to quickly reduce the LED current during system high-power conditions such as camera flash, PA transmit, or other high battery-current conditions. The adjusted current target is programmable via register 0x17 bits[7:0]. Only the MSBs of the brightness code are adjustable. Additionally, the BL_ADJ input only decreases the current from the initial target. If the initial target is > the adjusted current then nothing happens — the LED current remains at its current value. Figure 30 details the BL_ADJ operation.

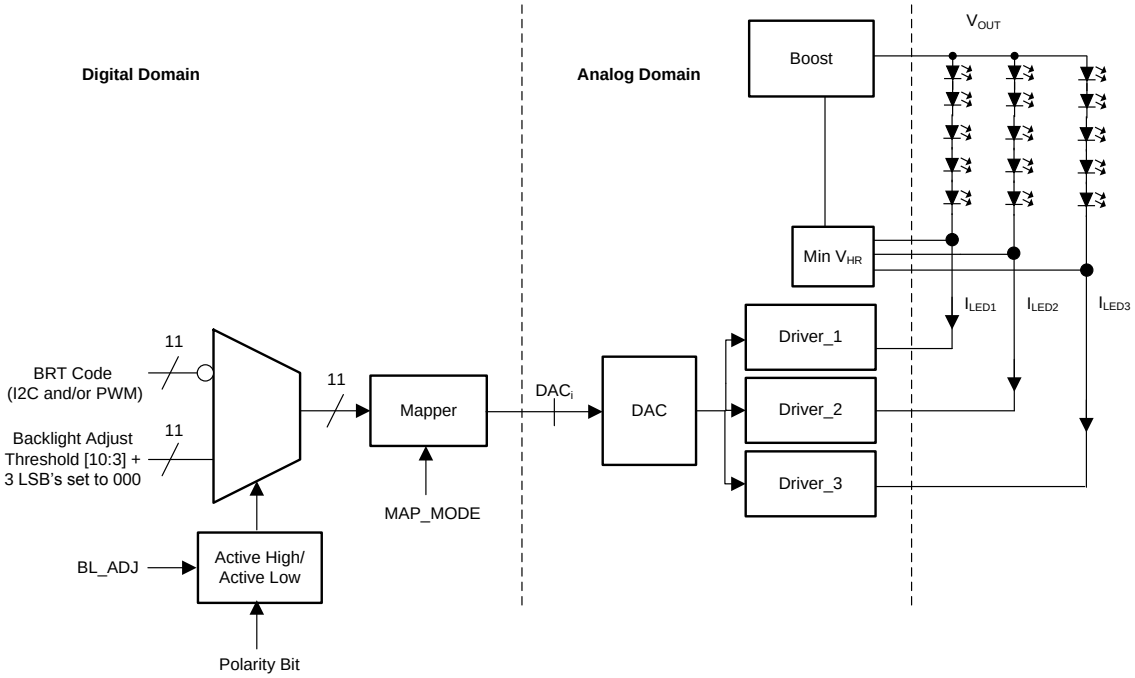
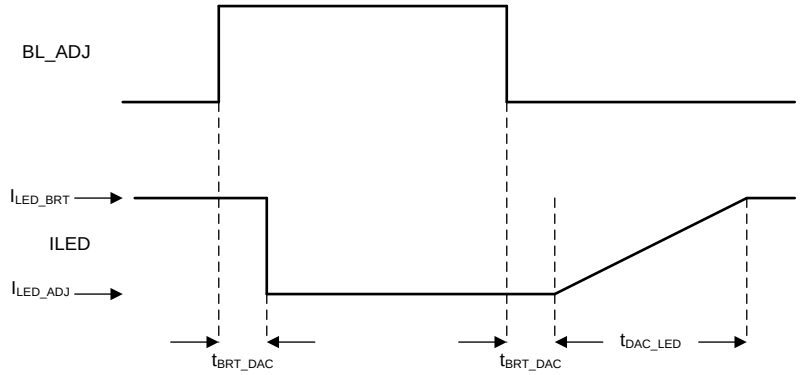


Figure 29. Backlight Adjust Operation



LED Current operates at an initial target ILED_BRT which is set by either I^2C or PWM (or both).

When the BL_ADJ input is driven to a logic high the LM36923's brightness code at the Mapper input has the MSBs set to the BL_ADJ Threshold and the LSBs set to 000.

ILED steps down to the new target current in < 50 µs.

When BL_ADJ is forced low the LED current returns to the initial brightness target.

Figure 30. Backlight Adjust Timing

7.4.4.1 Back-Light Adjust Input Polarity

The BL_ADJ input can have either active high or active low polarity. With active high polarity (default), driving the BL_ADJ input high forces the LED current to the BL_ADJ low target current. With active low polarity, driving the BL_ADJ input low forces the LED current to the BL_ADJ low target current. The polarity is set via bit 0 in register 11.

7.4.5 Fault Protection/Detection

7.4.5.1 Overvoltage Protection (OVP)

The LM36923 provides four OVP thresholds (17 V, 21 V, 25 V, and 29 V). The OVP circuitry monitors the boost output voltage (V_{OUT}) and protects OUT and SW from exceeding safe operating voltages in case of open load conditions or in the event the LED string voltage requires more voltage than the programmed OVP setting. The OVP thresholds are programmed in register 13 bits[3:2]. The operation of OVP differentiates between two overvoltage conditions and responds differently as outlined below:

7.4.5.1.1 Case 1 OVP Fault Only (OVP Threshold Hit and All Enabled Current Sink Inputs > 40 mV)

In steady-state operation with V_{OUT} near the OVP threshold a rapid change in V_{IN} or brightness code can result in a momentary transient excursion of V_{OUT} above the OVP threshold. In this case the boost circuitry is disabled until V_{OUT} drops below OVP – hysteresis (1 V). Once this happens the boost is re-enabled and steady state regulation continues. If V_{OUT} remains above the OVP threshold for > 1 ms the OVP Flag is set (register 0x1F bit[0]).

7.4.5.1.2 Case 2a OVP Fault and Open LED String Fault (OVP Threshold Occurrence and Any Enabled Current Sink Input ≤ 40 mV)

When any of the enabled LED strings is open the boost converter tries to drive V_{OUT} above OVP and at the same time the open string(s) current sink headroom voltage(s) (LED1, LED2, LED3) drop to 0. When the LM36923 detects three occurrences of V_{OUT} > OVP and any enabled current sink input (V_{LED1} or V_{LED2}, V_{LED3}) ≤ 40 mV, the OVP Fault flag is set (register 0x1F bit[0]), and the LED Open Fault flag is set (register 0x1F bit[4]).

7.4.5.1.3 Case 2b OVP Fault and Open LED String Fault (OVP Threshold Duration and Any Enabled Current Sink Input ≤ 40 mV)

When any of the enabled LED strings is open the boost converter tries to drive V_{OUT} above OVP and at the same time the open string(s) current sink headroom voltage(s) (LED1, LED2, LED3) drop to 0. When the LM36923 detects V_{OUT} > OVP for > 1 msec and any enabled current sink input (V_{LED1} or V_{LED2}, V_{LED3}) ≤ 40 mV, the OVP Fault flag is set (register 0x1F bit[0]), and the LED Open Fault flag is set (register 0x1F bit[4]).

7.4.5.1.4 OVP/LED Open Fault Shutdown

The LM36923 has the option of shutting down the device when the OVP flag is set. This option can be enabled or disabled via register 0x1E bit[0]. When the shutdown option is disabled the fault flag is a report only. When the device is shut down due to an OVP/LED String Open fault, the fault flags register must be read back before the LM36923 can be re-enabled.

7.4.5.1.5 Testing for LED String Open

The procedure for detecting an open in a LED string is:

- Apply power the the LM36923.
- Enable all LED strings (Register 0x10 = 0x0F).
- Set maximum brightness (Register 0x18 = 0x07 and Register 0x19 = 0xFF).
- Set the brightness control (Register 0x11 = 0x00).
- Open LED1 string.
- Wait 4 msec.
- Read LED open fault (Register 0x1F).
- If bit[4] = 1, then a LED open fault condition has been detected.
- Connect LED1 string.
- Repeat the procedure for the other LED strings.

7.4.5.2 LED String Short Fault

The LM36923 can detect an LED string short fault. This happens when the voltage between V_{IN} and any enabled current sink input has dropped below (1.5 V). This test can only be performed on one LED string at a time. Performing this test with more than one LED string enabled can result in a faulty reading. The procedure for detecting a short in a LED string is:

- Apply power the the LM36923.
- Enable only LED1 string (Register 0x10 = 0x03).
- Enable short fault (Register 0x1E = 0x01.
- Set maximum brightness (Register 0x18 = 0x07 and Register 0x19 = 0xFF).
- Set the brightness control (Register 0x11 = 0x00).
- Wait 4 msec.
- Read LED short fault (Register 0x1F).
- If bit[3] = 1, then a LED short fault condition has been detected.
- Set chip enable and LED string enable low (Register 0x10 = 0x00).
- Repeat the procedure for the other LED strings.

7.4.5.3 Overcurrent Protection (OCP)

The LM36923 has 4 selectable OCP thresholds (750 mA, 1000 mA, 1250 mA, and 1500 mA). These are programmable in register 0x13 bits[1:0]. The OCP threshold is a cycle-by-cycle current limit and is detected in the internal low-side NFET. Once the threshold is hit the NFET turns off for the remainder of the switching period.

7.4.5.3.1 OCP Fault

If enough overcurrent threshold events occur, the OCP Flag (register 0x1F bit[1]) is set. To avoid transient conditions from inadvertently setting the OCP Flag, a pulse density counter monitors OCP threshold events over a 128-µs period. If 8 consecutive 128-µs periods occur where the pulse density count has found 2 or more OCP events,then the OCP Flag is set.

During device start-up and during brightness code changes, there is a 4-ms blank time where OCP events are ignored. As a result, if the device starts up in an overcurrent condition there is an approximate 5-ms delay before the OCP Flag is set.

7.4.5.3.2 OCP Shutdown

The LM36923 has the option of shutting down the device when the OCP flag is set. This option can be enabled or disabled via register 0x1E bit[1]. When the shutdown option is disabled, the fault flag is a report only. When the device is shut down due to an OCP fault, the fault flags register must be read back before the LM36923 can be re-enabled.

7.4.5.4 Device Overtemperature (TSD)

Thermal shutdown (TSD) is triggered when the device die temperature reaches 135˚C. When this happens the boost stops switching, and the TSD Flag (register 0x1F bit[2]) is set. The boost automatically starts up again when the die temperature cools down to 120˚C.

7.4.5.4.1 Overtemperature Shutdown

The LM36923 has the option of shutting down the device when the TSD flag is set. This option can be enabled or disabled via register 0x1E bit[2]. When the shutdown option is disabled the fault flag is a report only. When the device is shutdown due to a TSD fault, the Fault Flags register must be read back before the LM36923 can be re-enabled.

7.5 Programming

7.5.1 I²C Interface

7.5.1.1 Start and Stop Conditions

The LM36923 is configured via an I²C interface. START (S) and STOP (P) conditions classify the beginning and the end of the I²C session Figure 31. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During the data transmission the I²C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

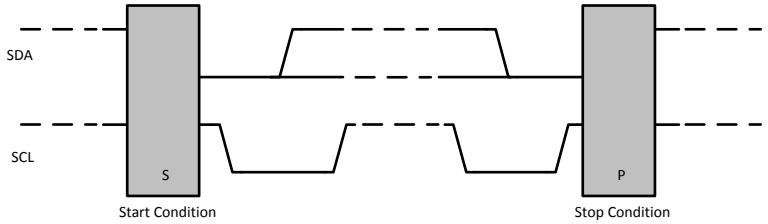


Figure 31. I²C Start and Stop Conditions

7.5.1.2 I²C Address

The 7-bit chip address for the LM36923 is (0x36). After the START condition the I²C master sends the 7-bit chip address followed by an eighth bit read or write (R/W). R/W = 0 indicates a WRITE, and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

7.5.1.3 Transferring Data

Every byte on the SDA line must be eight bits long with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse, (9th clock pulse), is generated by the master. The master then releases SDA (HIGH) during the 9th clock pulse. The LM36923 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

7.5.1.4 Register Programming

For glitch free operation, the following bits and/or registers should only be programmed while the LED Enable bits are 0 (Register 0x10, Bit [3:1] = 0) and Device Enable bit is 1 (Register 0x10, Bit[0] = 1) :

1. Register 0x11 Bit[7] (Mapping Mode)
2. Register 0x11 Bits[6:5] (Brightness Mode)
3. Register 0x11 Bit[4] (Ramp Enable)
4. Register 0x11 Bit[3:1] (Ramp Rate)
5. Register 0x12 Bits[7:6] (PWM Sample Rate)
6. Register 0x12 Bits[5] (PWM Polarity)
7. Register 0x12 Bit[3:2] (PWM Hysteresis)
8. Register 0x12 Bit[3:2] (PWM Pulse Filter)
9. Register 0x15 (auto frequency high threshold)
10. Register 0x16 (auto frequency low threshold)
11. Register 0x17 (back-light adjust threshold)

7.6 Register Maps

Note: Read of Reserved (R) or Write Only register returns 0

Table 8. Revision (0x00)

Bits [7:4]	Bits [3:0]
R	Revision Code

Table 9. Software Reset (0x01)

Bits [7:1]	Software Reset Bit [0]
R	0 = Normal Operation 1 = Device Reset (automatically resets back to 0)

Table 10. Enable (0x10)

Bits [7:4]	LED3 Enable Bit [3]	LED2 Enable Bit [2]	LED1 Enable Bit [1]	Device Enable Bit [0]
R	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)	0 = Disabled 1 = Enabled (Default)
NOTE: When the Device Enable (Bit [0]) is set high the following registers/bits are set to the default value: Register 0x11 Bit[0], Register 0x12 Bits[7:0].				

Table 11. Brightness Control (0x11)

Mapping Mode Bit [7]	Brightness Mode Bits [6:5]	Ramp Enable Bits [4]	Ramp Rate Bit [3:1]	BL_ADJ Polarity Bits [0]
0 = Linear (default) 1 = Exponential	00 = Brightness Register Only 01 = PWM Duty Cycle Only 10 = Multiply Then Ramp (Brightness Register × PWM) 11 = Ramp Then Multiply (Brightness Register × PWM) (default)	0 = Ramp Disabled (default) 1 = Ramp Enabled	000 = 0.125 ms/step (default) 001 = 0.250 ms/step 010 = 0.5 ms/step 011 = 1 ms/step 100 = 2 ms/step 101 = 4 ms/step 110 = 8 ms/step 111 = 16 ms/step	0 = Active Low 1 = Active High (default)

Table 12. PWM Control (0x12)

PWM Sample Rate Bit [7:6]	PWM Input Polarity Bit [5]	PWM Hysteresis Bits [4:2]	PWM Pulse Filter Bit [1:0]
00 = 800 kHz 01 = 4 MHz (default) 1X = 24 MHz	0 = Active Low 1 = Active High (default)	000 = None 001 = 1 LSB 010 = 2 LSBs 011 = 3 LSBs 100 = 4 LSBs (default) 101 = 5 LSBs 110 = 6 LSBs 111 = N/A	00 = No Filter 01 = 100 ns 10 = 150 ns 11 = 200 ns (default)

Table 13. Boost Control 1 (0x13)

Reserved Bit [7]	Boost Switching Frequency Shift Bit [6]	Boost Switching Frequency Select Bit [5]	Minimum Inductor Select Bit [4]	Overvoltage Protection (OVP) Bits [3:2]	Current Limit (OCP) Bits [1:0]
N/A	0 = –12% Shift 1 =No Shift (default)	0 = 500 kHz 1 = 1 MHz (default)	0 = 10 µH (default) 1 = 22 µH	00 = 17 V 01 = 21 V 10 = 25 V 11 = 29 V (default)	00 = 750 mA 01 = 1000 mA 10 = 1250 mA 11 = 1500 mA (default)

Table 14. Auto Frequency High Threshold (0x15)

Auto Frequency High Threshold (500 kHz to 1000 kHz) Bits [7:0]
Compared against the 8 MSBs of 11-bit brightness code (default = 00000000).

Table 15. Auto Frequency Low Threshold (0x16)

Auto Frequency High Threshold (250 kHz to 500 kHz) Bits [7:0]
Compared against the 8 MSBs of 11-bit brightness code (default = 00000000).

Table 16. Back Light Adjust Threshold (0x17)

Back Light Adjust Threshold (Brightness Ceiling) Bits [7:0]
When BL_ADJ Input is driven high the MSBs of the brightness code are forced to the code in this register (default = 00000000).

Table 17. Brightness Register LSBs (0x18)

Bits [7:3]	I^2C Brightness Code (LSB) Bits [2:0]
R	This is the lower 3 bits of the 11-bit brightness code (default = 111).

Table 18. Brightness Register MSBs (0x19)

I2C Brightness Code (MSB) Bits [7:0]
This is the upper 8 bits of the 11-bit brightness code (default = 11111111).

Table 19. Fault Control (0x1E)

Reserved Bits [7:4]	LED Short Fault Enable Bit [3]	TSD Shutdown Disable Bit [2]	OCP Shutdown Disable Bit [1]	OVP/LED Open Shutdown Disable Bit [0]
R	0 = LED Short Fault Detection is disabled (default) 1 = LED Short Fault Detection is enabled	0 = When the TSD Flag is set, the device is forced into shutdown. 1 = No shutdown (default)	0 = When the OCP Flag is set, the device is forced into shutdown. 1 = No shutdown (default)	0 = When the OVP Flag is set, the device is forced into shutdown. 1 = No shutdown (default)

Table 20. Fault Flags (0x1F)

Reserved Bits [7:5]	LED Open Fault Bit [4]	LED Short Fault Bit [3]	TSD Fault Bit [2]	OCP Fault Bit [1]	OVP Fault Bit [0]
R	1 = LED String Open Fault	1 = LED Short Fault	1 = Thermal Shutdown Fault	1 = Current Limit Fault	1 = Output Overvoltage Fault

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM36923 provides a complete high-performance LED lighting solution for mobile handsets. The LM36923 is highly configurable and can support multiple LED configurations.

8.2 Typical Application

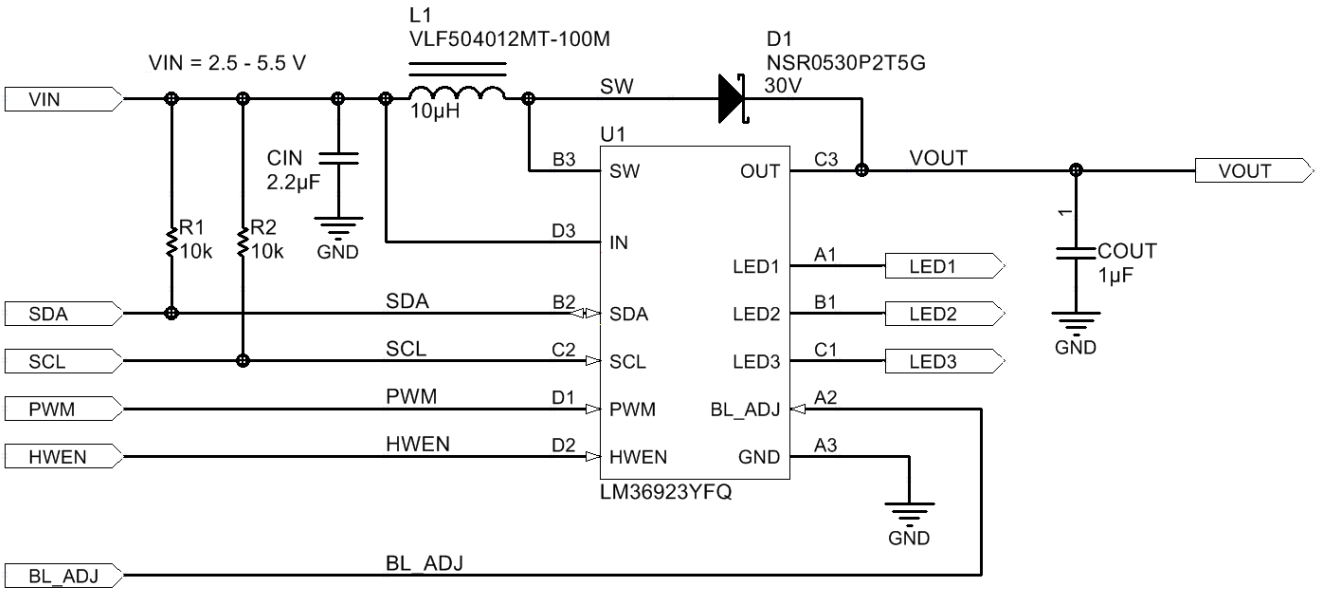


Figure 32. LM36923 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage (V_{IN})	2.7 V
LED parallel/series configuration	3 × 5
LED maximum forward voltage (V_f)	3.2 V
Efficiency	82%

The number of LED strings, number of series LEDs, and minimum input voltage are needed in order to calculate the peak input current. This information guides the designer to make the appropriate inductor selection for the application. The LM36923 boost converter output voltage (V_{OUT}) is calculated as follows: number of series LEDs × Vf + 0.23 V. The LM36923 boost converter output current (I_{OUT}) is calculated as follows: number of parallel LED strings × 25 mA. The LM36923 peak input current is calculated using Equation 6.

8.2.2 Detailed Design Procedure

Table 21. Typical Application Component List

CONFIGURATION	L1	D1	C_{OUT}
3p7s, 3p8s	VLF504012MT-100M VLF504012MT-150M	NSR0530P2T5G	C2012X7R1H105K085AC
3p6s	VLF504012MT-220M	NSR0530P2T5G	C2012X7R1H105K085AC
3p5s	VLF403210MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC
3p4s	VLF302510MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC

8.2.2.1 Component Selection

8.2.2.1.1 Inductor

The LM36923 requires a typical inductance in the range of 10 µH to 22 µH. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current of the application (I_{PEAK}) given in the inductor datasheet. The peak inductor current occurs at the maximum load current, the maximum output voltage, the minimum input voltage, and the minimum switching frequency setting. Also, the peak current requirement increases with decreasing efficiency. I_{PEAK} can be estimated using Equation 6:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{V_{IN}}{2 \times f_{SW} \times L} \times \left(1 + \frac{V_{IN} \times \eta}{V_{OUT}}\right) \quad (6)$$

Also, the peak current calculated above is different from the peak inductor current setting (I_{SAT}). The NMOS switch current limit setting (I_{CL_MIN}) must be greater than I_{PEAK} from Equation 6 above.

8.2.2.1.2 Output Capacitor

The LM36923 requires a ceramic capacitor with a minimum of 0.4 µF of capacitance at the output, specified over the entire range of operation. This ensures that the device remains stable and oscillation free. The 0.4 µF of capacitance is the minimum amount of capacitance, which is different than the value of capacitor. Capacitance would take into account tolerance, temperature, and DC voltage shift.

Table 22 lists possible output capacitors that can be used with the LM36923. Figure 33 shows the DC bias of the four TDK capacitors. The useful voltage range is determined from the effective output voltage range for a given capacitor as determined by Equation 7:

$$DC\ Voltage\ Derating \geq \frac{0.38\mu F}{(1 - Tol) \times (1 - Temp\_co)} \quad (7)$$

Table 22. Recommended Output Capacitors

PART NUMBER	MANUFACTURER	CASE SIZE	VOLTAGE RATING (V)	NOMINAL CAPACITANCE (µF)	TOLERANCE (%)	TEMPERATURE COEFFICIENT (%)	RECOMMENDED MAX OUTPUT VOLTAGE (FOR SINGLE CAPACITOR)
C2012X5R1H105K085AB	TDK	0805	50	1	±10	±15	22
C2012X5R1H225K085AB	TDK	0805	50	2.2	±10	±15	24
C1608X5R1V225K080AC	TDK	0603	35	2.2	±10	±15	12
C1608X5R1H105K080AB	TDK	0603	50	1	±10	±15	15

For example, with a 10% tolerance, and a 15% temperature coefficient, the DC voltage derating must be ≥ 0.38/(0.9 × 0.85) = 0.5 µF. For the C1608X5R1H225K080AB (0603, 50-V) device, the useful voltage range occurs up to the point where the DC bias derating falls below 0.523 µF, or around 12 V. For configurations where V_{OUT} is > 15 V, two of these capacitors can be paralleled, or a larger capacitor such as the C2012X5R1H105K085AB must be used.

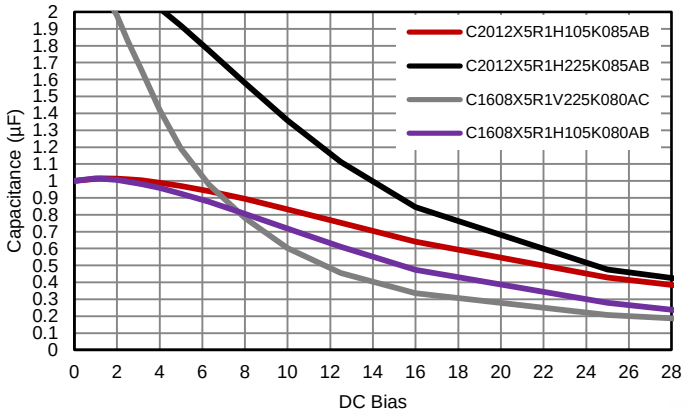


Figure 33. DC Bias Derating for 0805 Case Size and 0603 Case Size 35-V and 50-V Ceramic Capacitors

8.2.2.1.3 Input Capacitor

The input capacitor in a boost is not as critical as the output capacitor. The input capacitor primary function is to filter the switching supply currents at the device input and to filter the inductor current ripple at the input of the inductor. The recommended input capacitor is a 2.2-µF ceramic (0402, 10-V device) or equivalent.

8.2.3 Application Curves

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

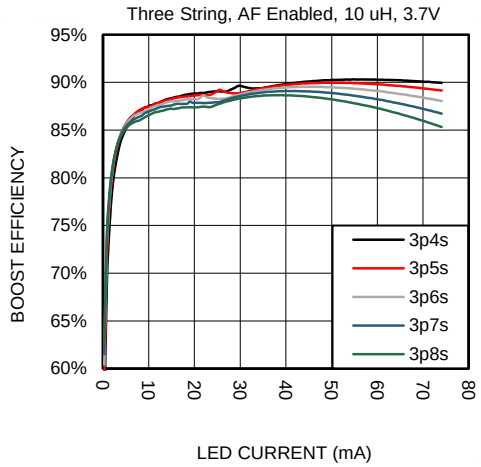


Figure 34. Boost Efficiency vs Series LEDs

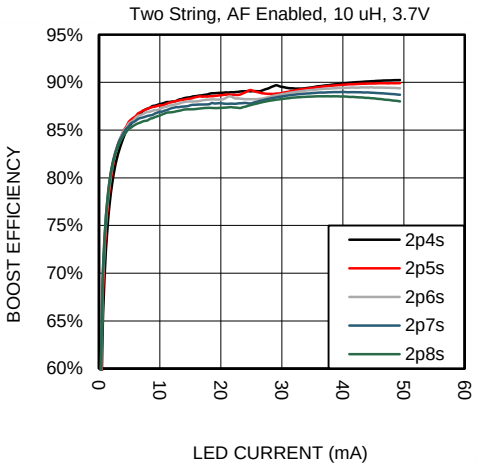


Figure 35. Boost Efficiency vs Series LEDs

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

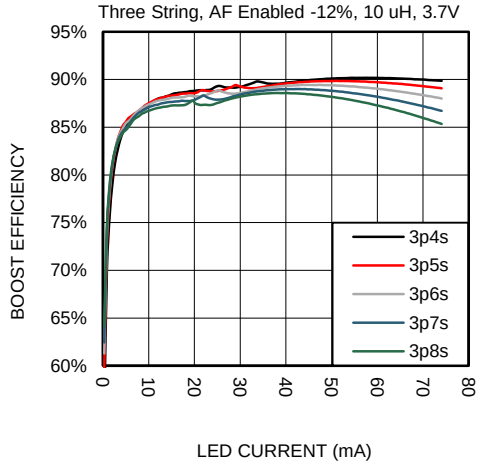


Figure 36. Boost Efficiency vs Series LEDs

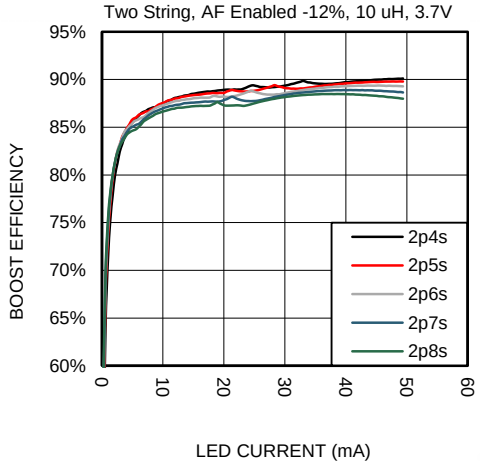


Figure 37. Boost Efficiency vs Series LEDs

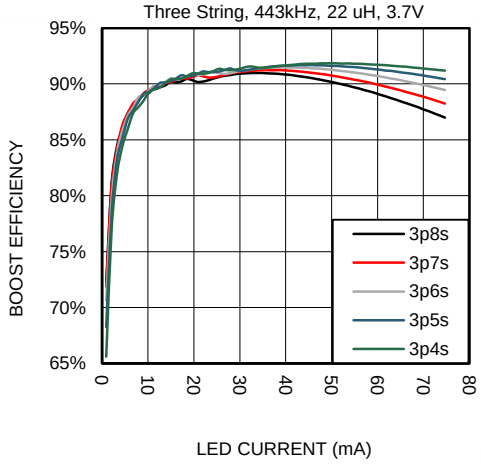


Figure 38. Boost Efficiency vs Series LEDs

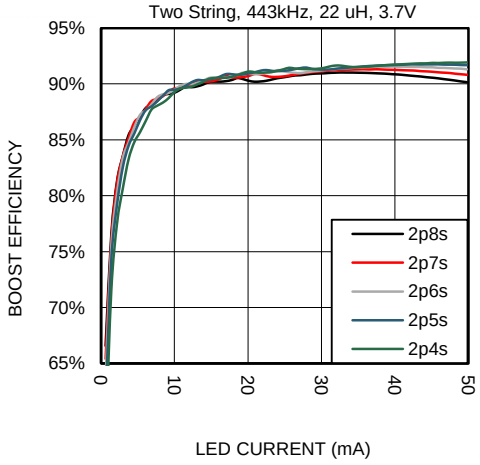


Figure 39. Boost Efficiency vs Series LEDs

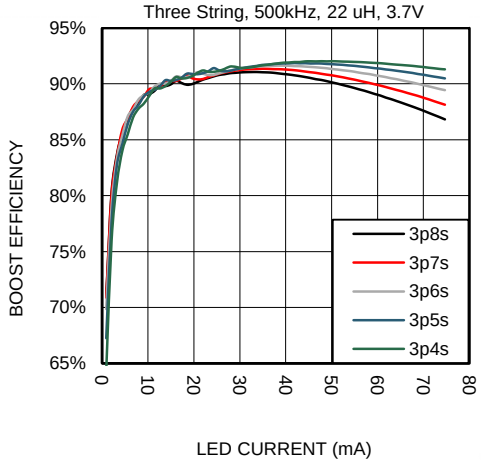


Figure 40. Boost Efficiency vs Series LEDs

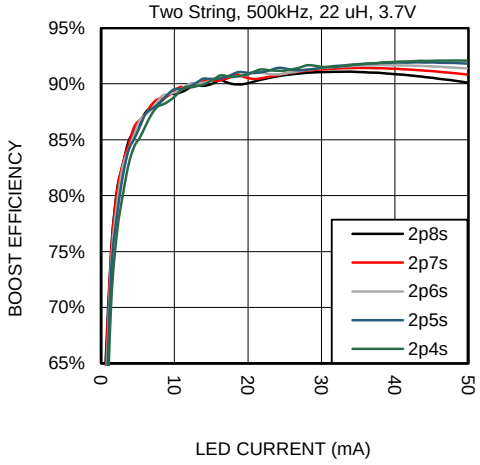


Figure 41. Boost Efficiency vs Series LEDs

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

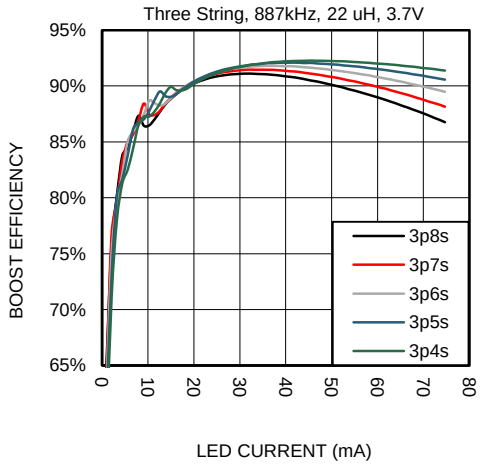


Figure 42. Boost Efficiency vs Series LEDs

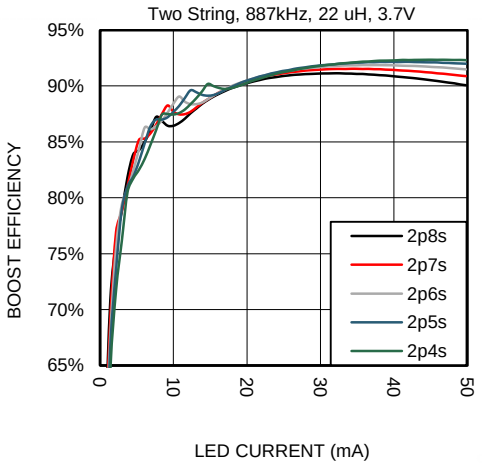


Figure 43. Boost Efficiency vs Series LEDs

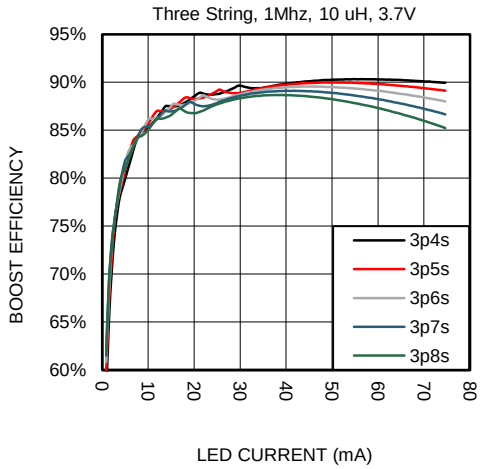


Figure 44. Boost Efficiency vs Series LEDs

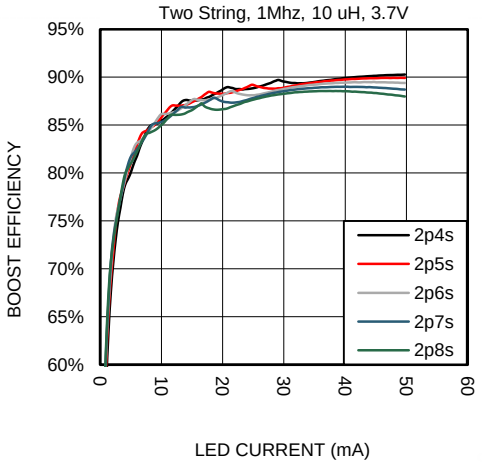


Figure 45. Boost Efficiency vs Series LEDs

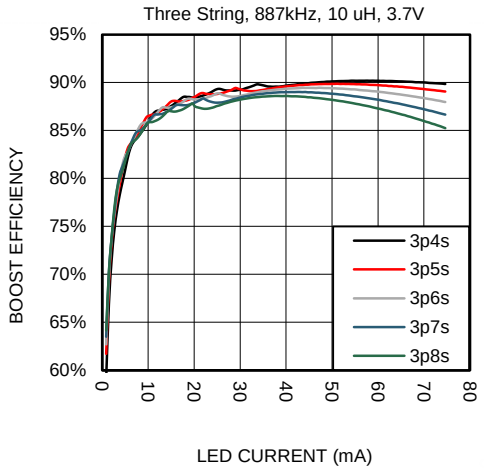


Figure 46. Boost Efficiency vs Series LEDs

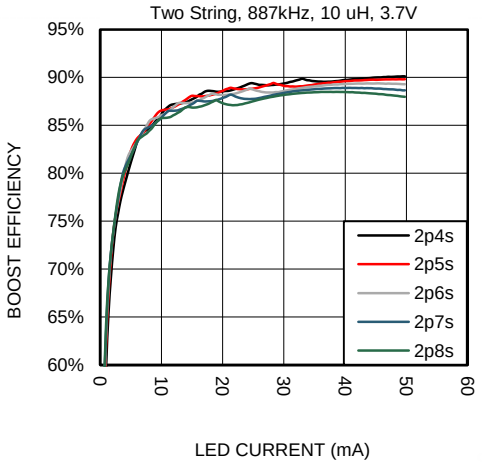


Figure 47. Boost Efficiency vs Series LEDs

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

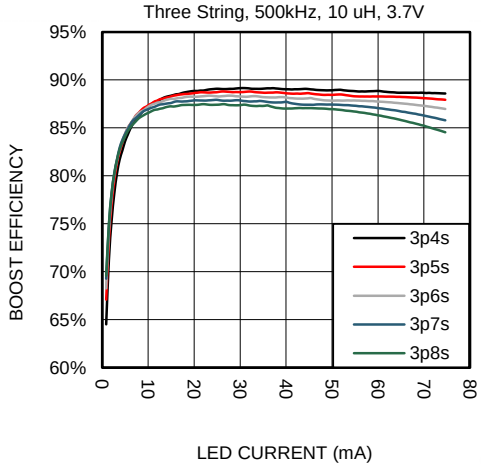


Figure 48. Boost Efficiency vs Series LEDs

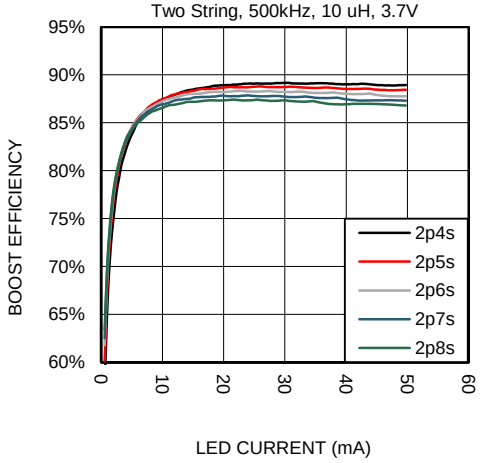


Figure 49. Boost Efficiency vs Series LEDs

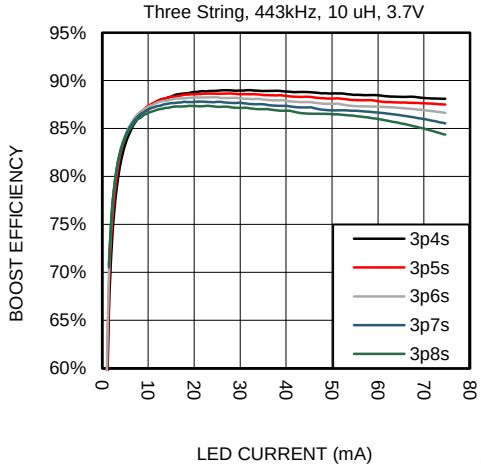


Figure 50. Boost Efficiency vs Series LEDs

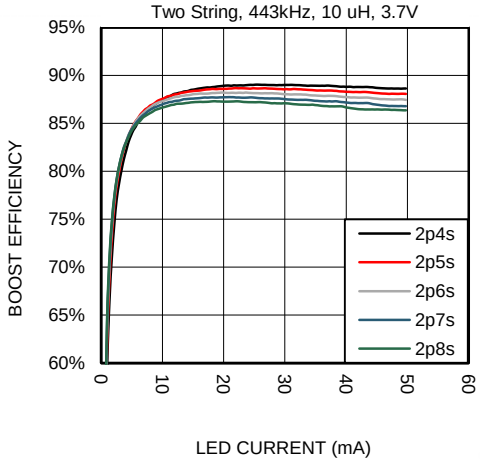


Figure 51. Boost Efficiency vs Series LEDs

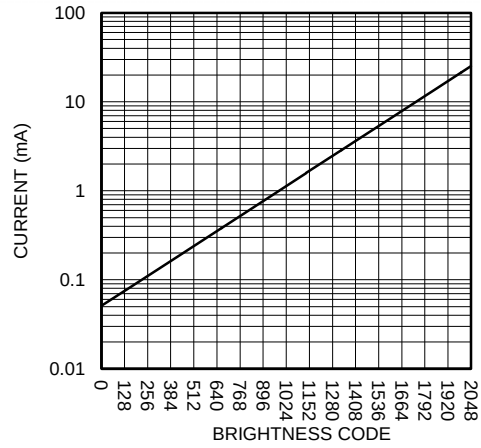


Figure 52. LED Current vs Brightness Code (Exponential Mapping)

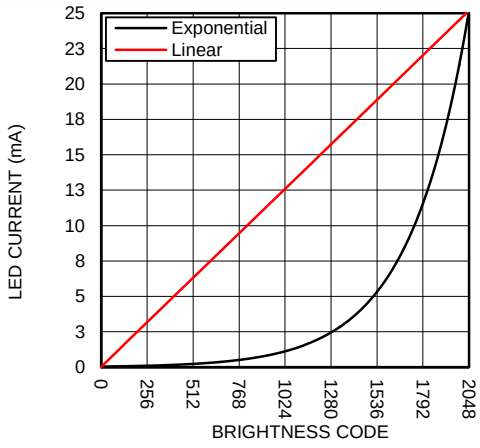


Figure 53. LED Current vs Brightness Code

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

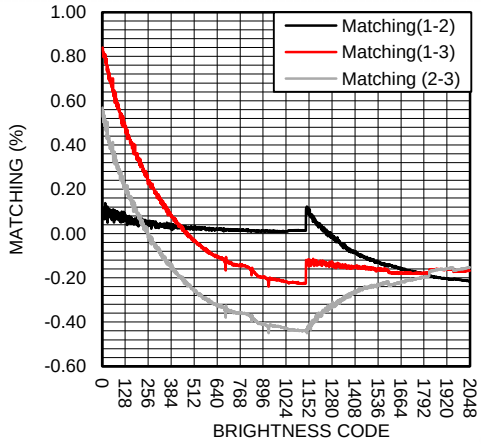


Figure 54. LED Matching (Exponential Mapping)

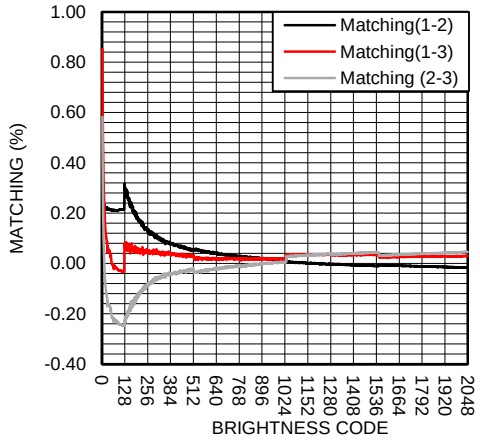


Figure 55. LED Matching (Linear Mapping)

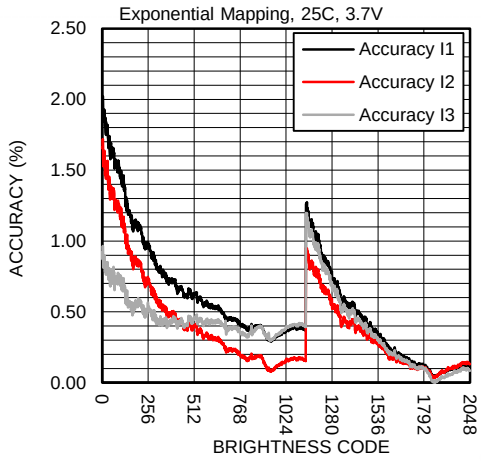


Figure 56. LED Current Accuracy

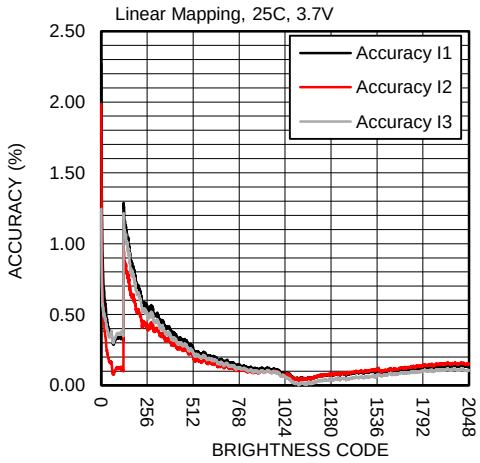


Figure 57. LED Current Accuracy

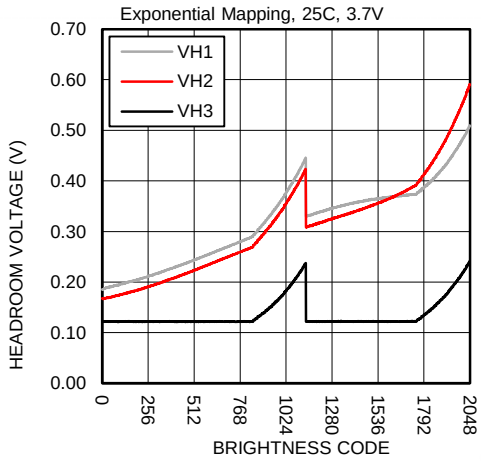


Figure 58. LED Headroom Voltage (Mis-Matched Strings)

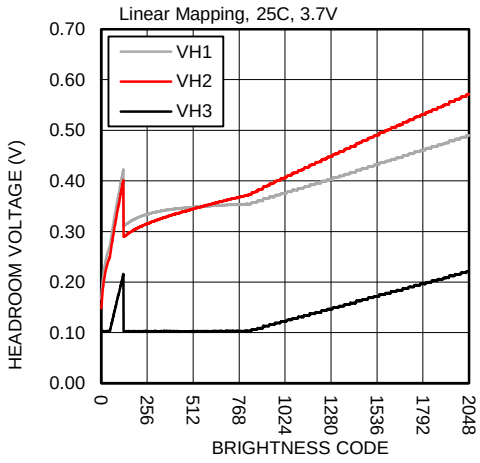


Figure 59. LED Headroom Voltage (Mis-Matched Strings)

L1 = 10 µH (VLF403212-100M) or 22 µH (VLF504015-220M) as noted in graphs, D1 = NSR530P2T5G, LEDs are Rohm SML312WBCW1, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.

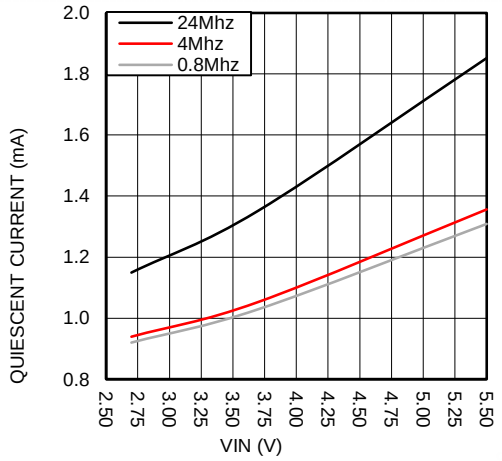


Figure 60. Current vs PWM Sample Frequency

9 Power Supply Recommendations

9.1 Input Supply Bypassing

The LM36923 is designed to operate from an input supply range of 2.5 V to 5.5 V. This input supply should be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). The resistance of the input supply rail should be low enough such that the input current transient does not cause the LM36923 supply voltage to droop more than 5%. Additional bulk decoupling located close to the input capacitor (C_{IN}) may be required to minimize the impact of the input supply rail resistance.

10 Layout

10.1 Layout Guidelines

The LM36923's inductive boost converter sees a high switched voltage (up to V_{OVP}) at the SW pin, and a step current (up to I_{CL}) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OUT pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 61 highlights these two noise-generating components.

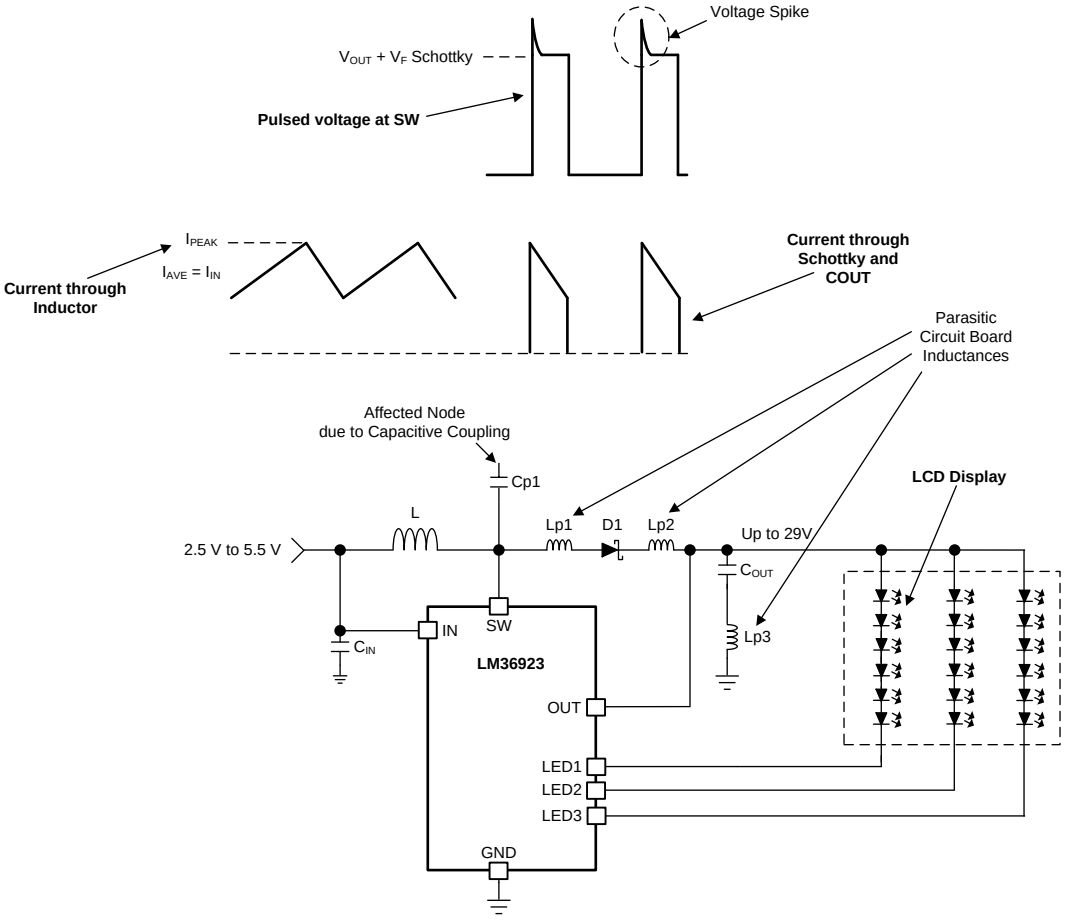


Figure 61. SW Pin Voltage (High Dv/Dt) and Current Through Schottky Diode and COUT (High Di/Dt)

Layout Guidelines (continued)

The following list details the main (layout sensitive) areas of the LM36923's inductive boost converter in order of decreasing importance:

- Output Capacitor
  - Schottky Cathode to COUT+
  - COUT– to GND
- Schottky Diode
  - SW pin to Schottky Anode
  - Schottky Cathode to COUT+
- Inductor
  - SW Node PCB capacitance to other traces
- Input Capacitor
  - CIN+ to IN pin

10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path it detects a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the LM36923's GND pin contributes to voltage spikes ($V_{SPIKE} = L_{P\_} \times di/dt$) at SW and OUT. These spikes can potentially overvoltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close as possible to the cathode of the Schottky diode, and COUT− must be connected as close as possible to the LM36923's GND pin. The best placement for COUT is on the same layer as the LM36923 in order to avoid any vias that can add excessive series inductance.

10.1.2 Schottky Diode Placement

In the LM36923's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike ($V_{SPIKE} = L_{P\_} \times di/dt$) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to C_{OUT} and reduces the inductance ($L_{P\_}$) and minimize these voltage spikes.

10.1.3 Inductor Placement

The node where the inductor connects to the LM36923's SW pin has 2 issues. First, a large switched voltage (0 to $V_{OUT} + V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range. To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, BL_ADJ, and PWM. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces. Lastly, limit the trace resistance of the V_{IN} to inductor connection and from the inductor to SW connection, by use of short, wide traces.

10.1.4 Boost Input Capacitor Placement

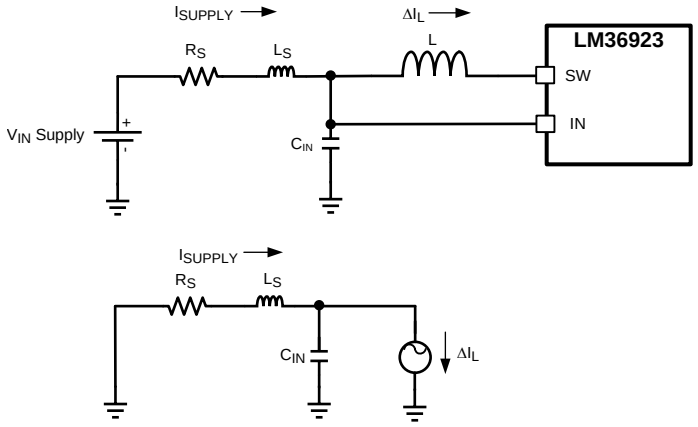
For the LM36923 boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn on of the internal power switch. The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane. Close

Layout Guidelines (continued)

placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM36923, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the LM36923 switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM36923 switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.

Figure 62 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is redrawn for the AC case where the V_{IN} supply is replaced with a short to GND, and the LM36923 + Inductor is replaced with a current source (ΔI_L). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_{IN}. As an example, consider a 3.6-V supply with 0.1 Ω of series resistance connected to C_{IN} through 50 nH of connecting traces. This results in an underdamped input-filter circuit with a resonant frequency of 712 kHz. Since both the 1-MHz and 500-kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500-kHz switching frequency) and 0.86 times the inductor current ripple using a 1-MHz switching frequency. Increasing the series inductance (LS) to 500 nH causes the resonant frequency to move to around 225 kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500-kHz switching frequency) and 0.053 times for a 1-MHz switching frequency.



1. $\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$

2. $f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$

3. $I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\frac{1}{2\pi \times 500\ kHz \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\ kHz \times L_S - \frac{1}{2\pi \times 500\ kHz \times C_{IN}}\right)^2}}$

Figure 62. Input RLC Network

10.2 Layout Example

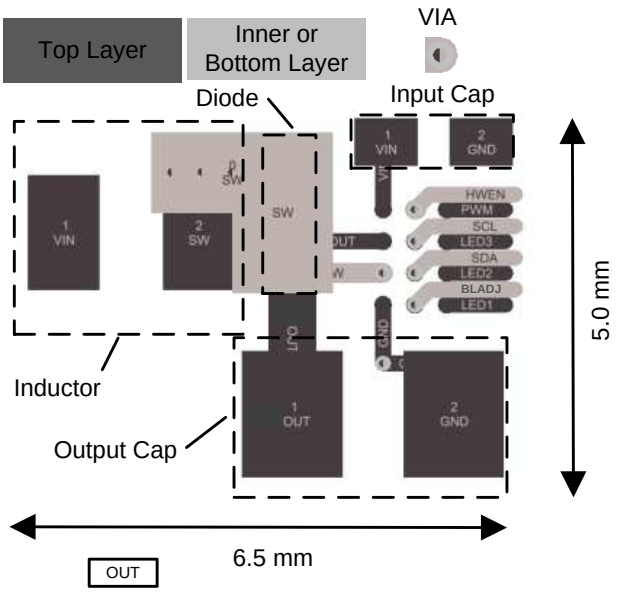


Figure 63. LM36923 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM36923YFFR	Active	Production	DSBGA (YFF) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	36923

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

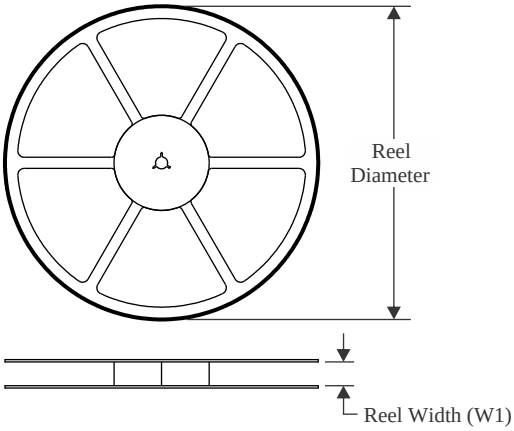
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

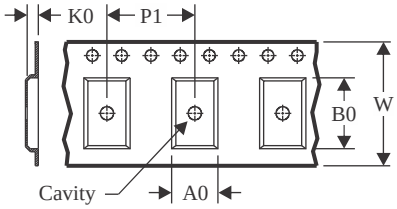
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

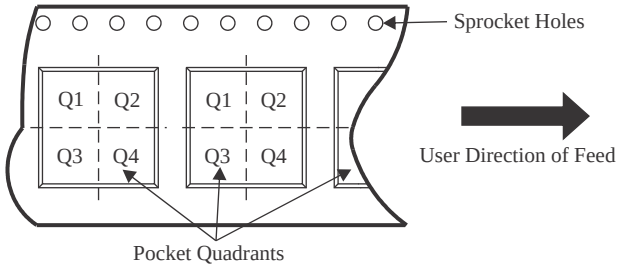


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

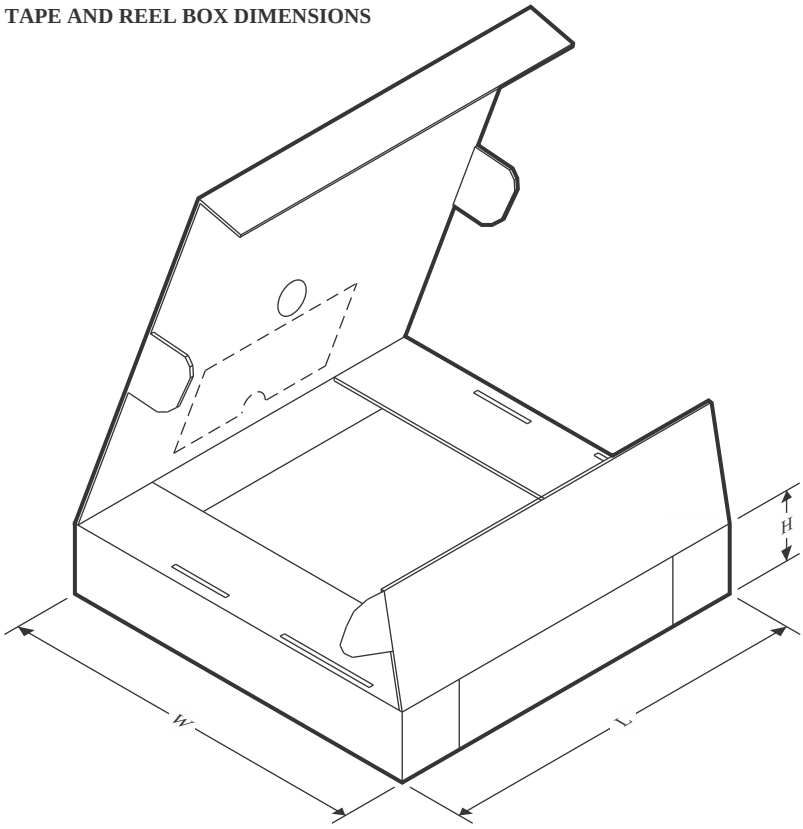
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

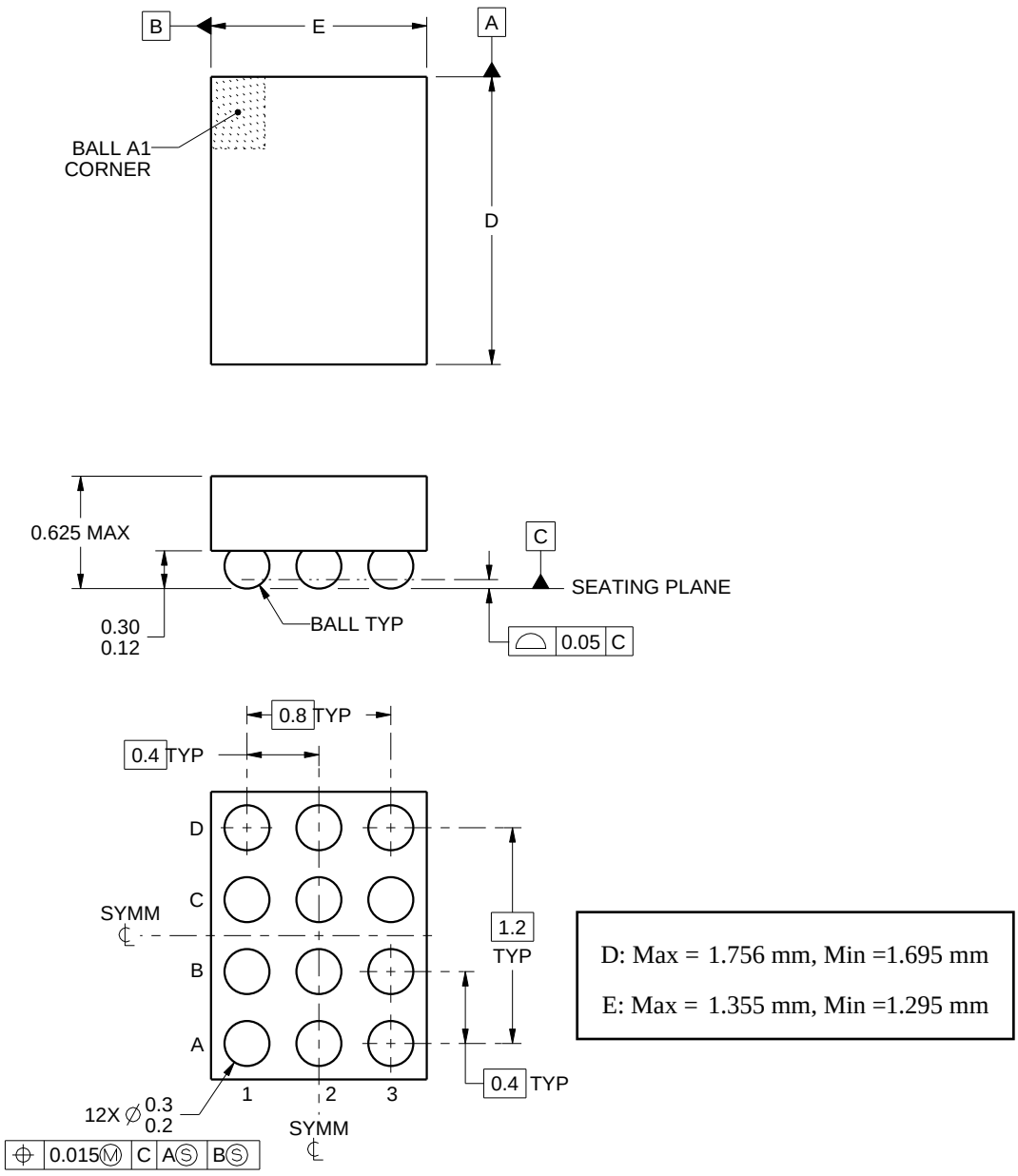
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM36923YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.5	1.99	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



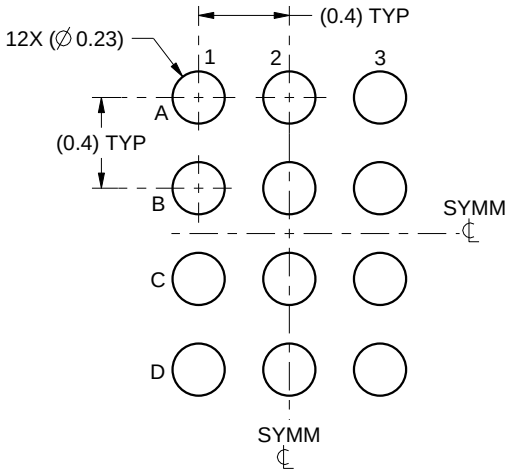
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM36923YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0

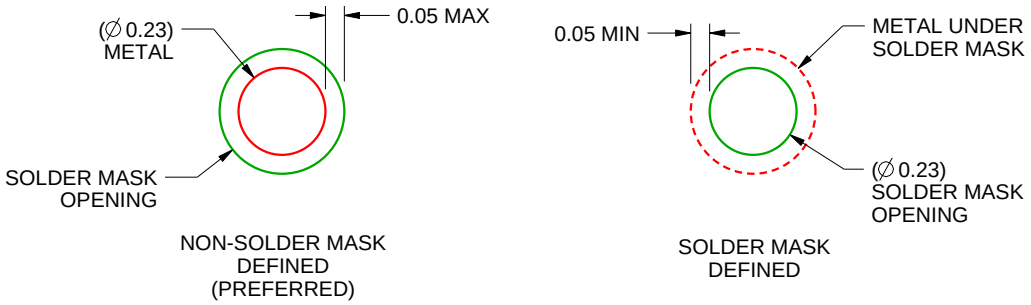


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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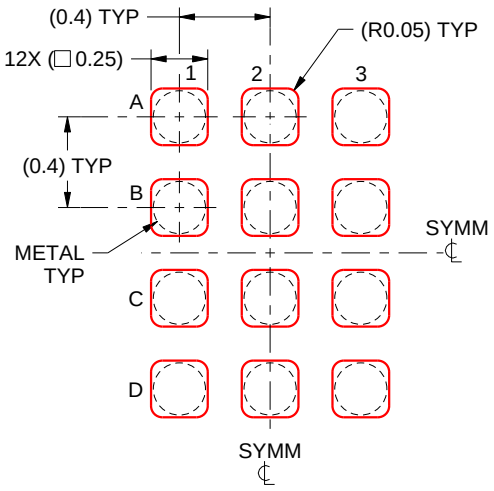
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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