LM36923H Highly Efficient Triple-String White LED Driver

1 Features
- 1% Matched Current Sinks Across Process, Voltage, Temperature
- 3% Current-Sink Accuracy Across Process, Voltage, Temperature
- 11-Bit Dimming Resolution
- Up to 90% Solution Efficiency
- Drives from One to Three Parallel LED Strings at up to 38 V at 25 mA per String
- PWM Dimming Input
- I2C Programmable
- Selectable 500-kHz and 1-MHz Switching Frequency With Optional –12% shift
- Auto Switch Frequency Mode (250 kHz, 500 kHz, 1 MHz)
- Four Configurable Overvoltage Protection Thresholds (17 V, 24 V, 31 V, 38 V)
- Four Configurable Overcurrent Protection Thresholds (750 mA, 1000 mA, 1250 mA, 1500 mA)
- Thermal Shutdown Protection
- Externally Selectable I2C Address Options via ASEI Input

2 Applications
- Power Source for Smart Phone and Tablet Backlighting
- LCD Panels With up to 24 LEDs

3 Description
The LM36923H is an ultra-compact, highly efficient, three-string white-LED driver designed for LCD display backlighting. The device can power up to 12 series LEDs at up to 25 mA per string. An adaptive current regulation method allows for different LED voltages in each string while maintaining current regulation.

The LED current is adjusted via an I2C interface or through a logic level PWM input. The PWM duty cycle is internally sensed and mapped to an 11-bit current thus allowing for a wide range of PWM frequencies with noise-free operation from 50 µA to 25 mA.

Other features include an auto-frequency mode, which can automatically change the frequency based on load current in order to optimize efficiency.

The device operates over the 2.5-V to 5.5-V input voltage range and a –40°C to +85°C temperature range.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (MAX)</th>
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</thead>
<tbody>
<tr>
<td>LM36923H</td>
<td>DSBGA (12)</td>
<td>1.756 mm × 1.355 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2016) to Revision B 

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<tr>
<th>Changes from Revision A (February 2016) to Revision B</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed pin name &quot;OVP&quot; to &quot;OUT&quot; in page 1 Typ App</td>
<td>1</td>
</tr>
<tr>
<td>• Changed from &quot;VOUT&quot; to &quot;OUT&quot; on page 3 connection diagram</td>
<td>3</td>
</tr>
<tr>
<td>• Changed pin name on FBD from &quot;OVP&quot; to &quot;OUT&quot;</td>
<td>10</td>
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Changes from Original (February 2016) to Revision A

<table>
<thead>
<tr>
<th>Changes from Original (February 2016) to Revision A</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed device from product preview to production</td>
<td>1</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

YFF Package
12-Pin DSBGA
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>LED1</td>
<td>Input to current sink 1. The boost converter regulates the minimum voltage between LED1, LED2, LED3 to VHR.</td>
</tr>
<tr>
<td>A2</td>
<td>ASEL</td>
<td>Input ASEL is a logic input which selects between two I2C address options. This pin is read on power up (Vin going above 1.8 V, and HWEN going above a logic high voltage). GND = address 0x36, logic high = address 0x37.</td>
</tr>
<tr>
<td>A3</td>
<td>GND</td>
<td>Input Ground</td>
</tr>
<tr>
<td>B1</td>
<td>LED2</td>
<td>Input pin to current sink 2. The boost converter regulates the minimum voltage between LED1, LED2, LED3 to VHR.</td>
</tr>
<tr>
<td>B2</td>
<td>SDA</td>
<td>I/O Data I/O for I^C-Compatible Interface.</td>
</tr>
<tr>
<td>B3</td>
<td>SW</td>
<td>Output Drain connection for internal low side NFET, and anode connection for external Schottky diode.</td>
</tr>
<tr>
<td>C1</td>
<td>LED3</td>
<td>Input Input pin to current sink 3. The boost converter regulates the minimum voltage between LED1, LED2, LED3 to VHR.</td>
</tr>
<tr>
<td>C2</td>
<td>SCL</td>
<td>Input Clock input for I^C-compatible interface.</td>
</tr>
<tr>
<td>C3</td>
<td>OUT</td>
<td>Input OUT serves as the sense point for overvoltage protection. Connect OUT to the positive pin of the output capacitor.</td>
</tr>
<tr>
<td>D1</td>
<td>PWM</td>
<td>Input Logic level input for PWM current control.</td>
</tr>
<tr>
<td>D2</td>
<td>HWEN</td>
<td>Input Hardware enable input. Drive HWEN high to bring the device out of shutdown and allow I^C writes or PWM control.</td>
</tr>
<tr>
<td>D3</td>
<td>IN</td>
<td>Input Input voltage connection. Bypass IN to GND with a minimum 2.2-µF ceramic capacitor.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN Input voltage</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>OUT Output overvoltage sense input</td>
<td>–0.3</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>SW Inductor connection</td>
<td>–0.3</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>LED1, LED2, LED3 LED string cathode connection</td>
<td>–0.3</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>HWEN, PWM, SDA, SCL, ASEL Logic I/Os</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Maximum junction temperature, T(_{\text{J_MAX}})</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, T(_{\text{stg}})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>V(_{\text{(ESD)}}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN Input voltage</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>OUT Overvoltage sense input</td>
<td>0</td>
<td>38</td>
<td>V</td>
</tr>
<tr>
<td>SW Inductor connection</td>
<td>0</td>
<td>38</td>
<td>V</td>
</tr>
<tr>
<td>LED1, LED2, LED3 LED string cathode connection</td>
<td>0</td>
<td>29.5</td>
<td>V</td>
</tr>
<tr>
<td>HWEN, PWM, SDA, SCL, ASEL Logic I/Os</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM36923H</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{UA}}) Junction-to-ambient thermal resistance</td>
<td>88.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{UJC(top)}}) Junction-to-case (top) thermal resistance</td>
<td>0.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{UB}}) Junction-to-board thermal resistance</td>
<td>43.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{\text{UT}}) Junction-to-top characterization parameter</td>
<td>2.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{\text{UB}}) Junction-to-board characterization parameter</td>
<td>43.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*. 
6.5 Electrical Characteristics

Minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), typical values are at T_A = 25°C, and V_IN = 3.6 V (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BOOST</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{MATCH}^{(1)}</td>
<td>LED current matching I_{LED1} to I_{LED2} to I_{LED3}</td>
<td>50 µA ≤ I_{LED} ≤ 25 mA, 2.7 V ≤ V_IN ≤ 5 V (linear or exponential mode)</td>
<td>−1%</td>
<td>0.1%</td>
<td>1%</td>
</tr>
<tr>
<td>Accuracy</td>
<td>Absolute accuracy (I_{LED1}, I_{LED2}, I_{LED3})</td>
<td>50 µA ≤ I_{LED} ≤ 25 mA, 2.7 V ≤ V_IN ≤ 5 V (linear or exponential mode)</td>
<td>−3%</td>
<td>0.1%</td>
<td>3%</td>
</tr>
<tr>
<td>I_{LED_MIN}</td>
<td>Minimum LED current (per string)</td>
<td>PWM or I2C current control (linear or exponential mode)</td>
<td>50</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>I_{LED_MAX}</td>
<td>Maximum LED current (per string)</td>
<td>25</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{DNL}</td>
<td>IDAC ratio-metric DNL</td>
<td>exponential mode only</td>
<td>1/3 (0.3%)</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>V_{HR}</td>
<td>Regulated current sink headroom voltage</td>
<td>I_{LED} = 25 mA</td>
<td>210</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>V_{HR_MIN}</td>
<td>Current sink minimum headroom voltage</td>
<td>I_{LED} = 95% of nominal, I_{LED} = 5 mA</td>
<td>35</td>
<td>50 mV</td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>Typical efficiency</td>
<td>V_IN = 3.7 V, I_{LED} = 5 mA/string, Typical Application circuit (3x7 LEDs), (P_{OUT}/P_{IN})</td>
<td>87%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{NMOS}</td>
<td>NMOS switch on resistance</td>
<td>I_SW = 250 mA</td>
<td>0.29</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>I_{CL}</td>
<td>NMOS switch current limit</td>
<td>2.7 V ≤ V_IN ≤ 5 V</td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OVP}</td>
<td>Output overvoltage protection</td>
<td>ON threshold, 2.7 V ≤ V_IN ≤ 5 V</td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVP Hysteresis</td>
<td></td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f_{SW}</td>
<td>Switching frequency</td>
<td>2.7 V ≤ V_IN ≤ 5 V, boost frequency shift = 0</td>
<td>92%</td>
<td>94%</td>
<td></td>
</tr>
<tr>
<td>D_{MAX}</td>
<td>Maximum boost duty cycle</td>
<td></td>
<td>92%</td>
<td>94%</td>
<td></td>
</tr>
<tr>
<td>I_{SHDN}</td>
<td>Shutdown current</td>
<td>Chip enable bit = 0, SDA = SCL = IN or GND, 2.7 V ≤ V_IN ≤ 5 V</td>
<td>1.2</td>
<td>5 µA</td>
<td></td>
</tr>
<tr>
<td>T_{SD}</td>
<td>Thermal shutdown</td>
<td></td>
<td>135</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

| **PWM INPUT**                    |                 |     |      |      |      |
| Min f_{PWM}                      |                  |     |      |      |      |
| Max f_{PWM}                      |                  |     |      |      |      |
| I_{MIN_ON}                       | Minimum pulse ON time |                  | 92% | 94% |
| I_{MIN_OFF}                      | Minimum pulse OFF time |                  | 92% | 94% |

(1) LED Current Matching between strings is given as the worst case matching between any two strings. Matching is calculated as ((I_{LEDX} - I_{LEDY})/(I_{LEDX} + I_{LEDY})) × 100.
## Electrical Characteristics (continued)

Minimum and maximum limits apply over the full operating ambient temperature range (-40°C ≤ $T_A$ ≤ 85°C), typical values are at $T_A = 25°C$, and $V_IN = 3.6$ V (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{START-UP}$</td>
<td>Turnon delay from shutdown to backlight on</td>
<td>PWM input active, PWM = logic high, HWEN input from low to high, $f_{PWM} = 10$ kHz (50% duty cycle)</td>
<td>3.5</td>
<td>5</td>
<td>ms</td>
</tr>
<tr>
<td>$PWM_{RES}$</td>
<td>PWM input resolution</td>
<td>$1.6$ kHz ≤ $f_{PWM}$ ≤ $12$ kHz, PWM hysteresis = 00, PWM sample rate = 11</td>
<td>11</td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input logic high</td>
<td>HWEN, ASEL, SCL, SDA, PWM inputs</td>
<td>1.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input logic low</td>
<td>HWEN, ASEL, SCL, SDA, PWM inputs</td>
<td>0</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>$t_{GLITCH}$</td>
<td>PWM input glitch rejection</td>
<td>PWM pulse filter = 00</td>
<td>0</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PWM pulse filter = 01</td>
<td>60</td>
<td>100</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PWM pulse filter = 10</td>
<td>90</td>
<td>150</td>
<td>210</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PWM pulse filter = 11</td>
<td>120</td>
<td>200</td>
<td>280</td>
</tr>
<tr>
<td>$t_{PWM,STBY}$</td>
<td>PWM shutdown period</td>
<td>Sample rate = 24 MHz</td>
<td>0.54</td>
<td>0.6</td>
<td>0.66</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sample rate = 4 MHz</td>
<td>2.7</td>
<td>3</td>
<td>3.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sample rate = 800 kHz</td>
<td>22.5</td>
<td>25</td>
<td>27.5</td>
</tr>
</tbody>
</table>

### 6.6 I2C Timing Requirements

See Figure 1

| $t_1$ | SCL clock period | 2.5 | | µs |
| $t_2$ | Data in setup time to SCL high | 100 | | ns |
| $t_3$ | Data out stable after SCL low | 0 | | ns |
| $t_4$ | SDA low Setup Time to SCL low (start) | 100 | | ns |
| $t_5$ | SDA high hold time after SCL high (stop) | 100 | | ns |

Figure 1. I2C Timing
6.7 Typical Characteristics

![Figure 2. OVP Hysteresis](image)

![Figure 3. 17-V OVP Threshold](image)

![Figure 4. 24-V OVP Threshold](image)

![Figure 5. 31-V OVP Threshold](image)

![Figure 6. 38-V OVP Threshold](image)

![Figure 7. RDSON](image)
Typical Characteristics (continued)

**Figure 8. Shutdown Current**

- $I_{ISHDN}$ in mA vs. $V_{IN}$
- HWEN = GND

**Figure 9. $I_Q$ Current (Switching)**

- $I_Q$ in mA vs. $V_{IN}$
- $f_{SW} = 1$ Mhz
- No Load

**Figure 10. VHR MIN**

- $V_{HR\_MIN}$ in mV vs. $V_{IN}$
- $I_{LED} = 5$ mA

**Figure 11. 750-mA OCP Current**

- Peak Current in A vs. $V_{IN}$
- Open Loop

**Figure 12. 1000-mA OCP Current**

- Peak Current in A vs. $V_{IN}$
- Open Loop

**Figure 13. 1250-mA OCP Current**

- Peak Current in A vs. $V_{IN}$
- Open Loop
Typical Characteristics (continued)

![Typical Characteristics Graph](image)

Figure 14. 1500-mA OCP Current
7 Detailed Description

7.1 Overview
The LM36923H is an inductive boost plus three current sinks white-LED driver designed for powering from one to three strings of white LEDs used in display backlighting. The device operates over the 2.5-V to 5.5-V input voltage range. The 11-bit LED current is set via an I²C interface, via a logic level PWM input, or a combination of both.

7.2 Functional Block Diagram
### 7.3 Feature Description

#### 7.3.1 Enabling the LM36923H

The LM36923H has a logic level input HWEN which serves as the master enable/disable for the device. When HWEN is low the device is disabled, the registers are reset to their default state, the \( \text{I}^2\text{C} \) bus is inactive, and the device is placed in a low-power shutdown mode. When HWEN is forced high the device is enabled, and \( \text{I}^2\text{C} \) writes are allowed to the device.

#### 7.3.1.1 Current Sink Enable

Each current sink in the device has a separate enable input. This allows for a 1-string, 2-string, or 3-string application. The default is with three strings enabled. Once the correct LED string configuration is programmed, the device can be enabled by writing the chip enable bit high (register 0x10 bit[0]), and then either enabling PWM and driving PWM high, or writing a non-zero code to the brightness registers.

The default setting for the device is with the chip enable bit set to 1, PWM input enabled, and the device in linear mapped mode. Therefore, on power up once HWEN is driven high, the device enters the standby state and actively monitors the PWM input. After a non-zero PWM duty cycle is detected the LM36923H converts the duty cycle information to the linearly weighted 11-bit brightness code. This allows for operation of the device in a stand-alone configuration without the need for any \( \text{I}^2\text{C} \) writes. Figure 15 and Figure 16 describe the start-up timing for operation with both PWM controlled current and with \( \text{I}^2\text{C} \) controlled current.

![Figure 15. Enabling the LM36923H via PWM](image1.png)

![Figure 16. Enabling the LM36923H via \( \text{I}^2\text{C} \)](image2.png)
Feature Description (continued)

7.3.2 LM36923H Start-Up

The LM36923H can be enabled or disabled in various ways. When disabled, the device is considered shutdown, and the quiescent current drops to \( I_{\text{SHDN}} \). When the device is in standby, it returns to the \( I_{\text{SHDN}} \) current level retaining all programmed register values. Table 1 describes the different operating states for the LM36923H.

### Table 1. LM36923H Operating Modes

<table>
<thead>
<tr>
<th>LED STRING ENABLES</th>
<th>PWM INPUT</th>
<th>( \text{I}^2 \text{C BRIGHTNESS REGISTERS} )</th>
<th>( \text{BRIGHTNESS MODE} )</th>
<th>DEVICE ENABLE</th>
<th>LED CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>0x10 bits[3:1]</td>
<td>0x18 bits[2:0]</td>
<td>0x11 bits[6:5]</td>
<td></td>
</tr>
<tr>
<td>XXX</td>
<td>XXX</td>
<td>XX</td>
<td>0</td>
<td>Off, device disabled</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>XXX</td>
<td>XX</td>
<td>0x11 bit[0] = 0</td>
<td>Off, device standby</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>X</td>
<td>0</td>
<td>00</td>
<td>1</td>
<td>Off, device in standby</td>
</tr>
<tr>
<td>At least one enabled</td>
<td></td>
<td>Code &gt; 000</td>
<td>00</td>
<td>1</td>
<td>( I_{\text{LED}} = 50 \mu A \times 1.003040572 \text{Code} )</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>0</td>
<td>XXX</td>
<td>01</td>
<td>1</td>
<td>LED = 37.806 \mu A + 12.195 \mu A \times \text{Code} See(1)</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>PWM Signal</td>
<td>XXX</td>
<td>01</td>
<td>1</td>
<td>( I_{\text{LED}} = 50 \mu A \times 1.003040572 \text{Code} ) See(1)</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>0</td>
<td>XXX</td>
<td>10 or 11</td>
<td>1</td>
<td>Off, device in standby</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>X</td>
<td>0</td>
<td>10 or 11</td>
<td>1</td>
<td>Off, device in standby</td>
</tr>
<tr>
<td>At least one enabled</td>
<td>PWM Signal</td>
<td>Code &gt; 000</td>
<td>10 or 11</td>
<td>1</td>
<td>( I_{\text{LED}} = 50 \mu A \times 1.003040572 \text{Code} ) See(1)</td>
</tr>
</tbody>
</table>

(1) Code is the 11-bit code output from the ramp (see Figure 21, Figure 23, Figure 25, Figure 27). This can be the \( I^2 \text{C} \) brightness code, the converted PWM duty cycle or the 11-bit product of both.

7.3.3 Brightness Mapping

There are two different ways to map the brightness code (or PWM duty cycle) to the LED current: linear and exponential mapping.

#### 7.3.3.1 Linear Mapping

For linear mapped mode the LED current increases proportionally to the 11-bit brightness code and follows the relationship:

\[
I_{\text{LED}} = 37.806 \mu A + 12.195 \mu A \times \text{Code} \quad (1)
\]

This is valid from codes 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the \( I^2 \text{C} \) brightness code, the digitized PWM duty cycle, or the product of the two.

#### 7.3.3.2 Exponential Mapping

In exponential mapped mode the LED current follows the relationship:

\[
I_{\text{LED}} = 50 \mu A \times 1.003040572 \text{Code} \quad (2)
\]

This results in an LED current step size of approximately 0.304% per code. This is valid for codes from 1 to 2047. Code 0 programs 0 current. Code is an 11-bit code that can be the \( I^2 \text{C} \) brightness code, the digitized PWM duty cycle, or the product of the two. Figure 17 details the LED current exponential response. The 11-bit (0.304%) per code step is small enough such that the transition from one code to the next in terms of LED brightness is not distinguishable to the eye. This therefore gives a perfectly smooth brightness increase between adjacent codes.
7.3.4 PWM Input

The PWM input is a sampled input which converts the input duty cycle information into an 11-bit brightness code. The use of a sampled input eliminates any noise and current ripple that traditional PWM controlled LED drivers are susceptible to.

The PWM input uses logic level thresholds with $V_{IH_{\text{MIN}}} = 1.25 \, \text{V}$ and $V_{IL_{\text{MAX}}} = 0.4 \, \text{V}$. Because this is a sampled input, there are limits on the max PWM input frequency as well as the resolution that can be achieved.

### 7.3.4.1 PWM Sample Frequency

There are four selectable sample rates for the PWM input. The choice of sample rate depends on three factors:

1. Required PWM Resolution (input duty cycle to brightness code, with 11 bits max)
2. PWM Input Frequency
3. Efficiency

#### 7.3.4.1.1 PWM Resolution and Input Frequency Range

The PWM input frequency range is 50 Hz to 50 kHz. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code (BRT), the input PWM duty cycle must be $\geq 11$ bits, and the PWM sample period ($1/f_{\text{SAMPLE}}$) must be smaller than the minimum PWM input pulse width. Figure 18 shows the possible brightness code resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is described in PWM Timeout.

![Figure 17. LED Current vs Brightness Code (Exponential Mapping)](image)

**Figure 17. LED Current vs Brightness Code (Exponential Mapping)**

---

![Figure 18. PWM Sample Rate, Resolution, and PWM Input Frequency](image)

**Figure 18. PWM Sample Rate, Resolution, and PWM Input Frequency**

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7.3.4.1.2 PWM Sample Rate and Efficiency

Efficiency is maximized when the lowest $f_{\text{SAMPLE}}$ is chosen as this lowers the quiescent operating current of the device. Table 2 describes the typical efficiency tradeoffs for the different sample clock settings.

Table 2. PWM Sample Rate Trade-Offs

<table>
<thead>
<tr>
<th>PWM SAMPLE RATE ($f_{\text{SAMPLE}}$)</th>
<th>TYPICAL INPUT CURRENT, DEVICE ENABLED $I_{\text{LED}} = 10 \text{ mA/string, } 2 \times 7 \text{ LEDs}$</th>
<th>TYPICAL EFFICIENCY $V_{\text{IN}} = 3.7 \text{ V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0x12 Bits[7:6])</td>
<td>$f_{\text{SW}} = 1 \text{ MHz}$</td>
<td>89.7%</td>
</tr>
<tr>
<td>0</td>
<td>1.03 mA</td>
<td>89.6%</td>
</tr>
<tr>
<td>1</td>
<td>1.05 mA</td>
<td>89.4%</td>
</tr>
<tr>
<td>1X</td>
<td>1.35 mA</td>
<td></td>
</tr>
</tbody>
</table>

7.3.4.1.2.1 PWM Sample Rate Example

The number of bits of resolution on the PWM input varies according to the PWM Sample rate and PWM input frequency.

Table 3. PWM Resolution vs PWM Sample Rate

<table>
<thead>
<tr>
<th>PWM FREQUENCY (kHz)</th>
<th>RESOLUTION (PWM SAMPLE RATE = 800 kHz)</th>
<th>RESOLUTION (PWM SAMPLE RATE = 4 MHz)</th>
<th>RESOLUTION (PWM SAMPLE RATE = 24 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>11</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>2</td>
<td>8.6</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>12</td>
<td>6.1</td>
<td>8.4</td>
<td>11</td>
</tr>
</tbody>
</table>

7.3.4.2 PWM Hysteresis

To prevent jitter at the input PWM signal from feeding through the PWM path and causing oscillations in the LED current, the LM36923H offers seven selectable hysteresis settings. The hysteresis works by forcing a specific number of 11-bit LSB code transitions to occur in the input duty cycle before the LED current changes. Table 4 describes the hysteresis. The hysteresis only applies during the change in direction of brightness currents. Once the change in direction has taken place, the PWM input must overcome the required LSB(s) of the hysteresis setting before the brightness change takes effect. Once the initial hysteresis has been overcome and the direction in brightness change remains the same, the PWM to current response changes with no hysteresis.

Table 4. PWM Input Hysteresis

<table>
<thead>
<tr>
<th>HYSTERESIS SETTING (0x12 Bits[4:2])</th>
<th>MIN CHANGE IN PWM PULSE WIDTH ($\Delta t$) REQUIRED TO CHANGE LED CURRENT, AFTER DIRECTION CHANGE (for $f_{\text{PWM}} &lt; 11.7 \text{ kHz}$)</th>
<th>MIN CHANGE IN PWM DUTY CYCLE ($\Delta D$) REQUIRED TO CHANGE LED CURRENT AFTER DIRECTION CHANGE</th>
<th>MIN ($I_{\text{LED}}$), INCREASE FOR INITIAL CODE CHANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>000 (0 LSB)</td>
<td>$1/(f_{\text{PWM}} \times 2047)$</td>
<td>0.05%</td>
<td>0.30%</td>
</tr>
<tr>
<td>001 (1 LSB)</td>
<td>$1/(f_{\text{PWM}} \times 1023)$</td>
<td>0.10%</td>
<td>0.61%</td>
</tr>
<tr>
<td>010 (2 LSBs)</td>
<td>$1/(f_{\text{PWM}} \times 511)$</td>
<td>0.20%</td>
<td>1.21%</td>
</tr>
<tr>
<td>011 (3 LSBs)</td>
<td>$1/(f_{\text{PWM}} \times 255)$</td>
<td>0.39%</td>
<td>2.40%</td>
</tr>
<tr>
<td>100 (4 LSBs)</td>
<td>$1/(f_{\text{PWM}} \times 127)$</td>
<td>0.78%</td>
<td>4.74%</td>
</tr>
<tr>
<td>101 (5 LSBs)</td>
<td>$1/(f_{\text{PWM}} \times 63)$</td>
<td>1.56%</td>
<td>9.26%</td>
</tr>
<tr>
<td>110 (6 LSBs)</td>
<td>$1/(f_{\text{PWM}} \times 31)$</td>
<td>3.12%</td>
<td>17.66%</td>
</tr>
</tbody>
</table>
7.3.4.3 PWM Step Response

The LED current response due to a step change in the PWM input is approximately 2 ms to go from minimum LED current to maximum LED current.

7.3.4.4 PWM Timeout

The LM36923H PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected. The timeout duration changes based on the PWM Sample Rate selected which results in a minimum supported PWM input frequency. The sample rate, timeout, and minimum supported PWM frequency are summarized in Table 5.

Table 5. PWM Timeout and Minimum Supported PWM Frequency vs PWM Sample Rate

<table>
<thead>
<tr>
<th>SAMPLE RATE</th>
<th>TIMEOUT</th>
<th>MINIMUM SUPPORTED PWM FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8 MHz</td>
<td>25 msec</td>
<td>48 Hz</td>
</tr>
<tr>
<td>4 MHz</td>
<td>3 msec</td>
<td>400 Hz</td>
</tr>
<tr>
<td>24 MHz</td>
<td>0.6 msec</td>
<td>2000 Hz</td>
</tr>
</tbody>
</table>

7.3.5 LED Current Ramping

There are 8 programmable ramp rates available in the LM36923H. These ramp rates are programmable as a time per step. Therefore, the ramp time from one current set-point to the next, depends on the number of code steps between currents and the programmed time per step. This ramp time to change from one brightness set-point (Code A) to the next brightness set-point (Code B) is given by:

\[ \Delta t = \text{Ramp rate} \times (\text{Code B} - \text{Code A} - 1) \]  
(3)

For example, assume the ramp is enabled and set to 1 ms per step. Additionally, the brightness code is set to 0x444 (1092d). Then the brightness code is adjusted to 0x7FF (2047d). The time the current takes to ramp from the initial set-point to max brightness is:

\[ \Delta t = \frac{1 \text{ms}}{\text{step}} \times (0x7FF - 0x444 - 1) = 954 \text{ms} \]  
(4)
7.3.6 Regulated Headroom Voltage

In order to optimize efficiency, current accuracy, and string-to-string matching the LED current sink regulated headroom voltage (VHR) varies with the target LED current. Figure 20 details the typical variation of VHR with LED current. This allows for increased solution efficiency as the dropout voltage of the LED driver changes. Furthermore, in order to ensure that both current sinks remain in regulation whenever there is a mismatch in string voltages, the minimum headroom voltage between VLED1, VLED2, VLED3 becomes the regulation point for the boost converter. For example, if the LEDs connected to LED1 require 12 V, the LEDs connected to LED2 require 12.5 V, and the LEDs connected to LED3 require 13 V at the programmed current, then the voltage at LED1 is VHR + 1 V, the voltage at LED2 is VHR + 0.5 V, and the voltage at LED3 is regulated at VHR. In other words, the boost makes the cathode of the highest voltage LED string the regulation point.

Figure 20. LM36923H Typical Exponential Regulated Headroom Voltage vs Programmed LED Current

7.4 Device Functional Modes

7.4.1 Brightness Control Modes

The LM36923H has four brightness control modes:

1. **I₂C Only** (brightness mode 00)
2. **PWM Only** (brightness mode 01)
3. **I₂C x PWM** with ramping only between I₂C codes (brightness mode 10)
4. **I₂C x PWM** with ramping between I₂C x PWM changes (brightness mode 11)
Device Functional Modes (continued)

7.4.1.1 I2C Only (Brightness Mode 00)

In brightness control mode 00 the I2C Brightness registers are in control of the LED current, and the PWM input is disabled. The brightness data (BRT) is the concatenation of the two brightness registers (3 LSBs) and (8 MSBs) (registers 0x18 and 0x19, respectively). The LED current only changes when the MSBs are written, meaning that to do a full 11-bit current change via I2C, first the 3 LSBs are written and then the 8 MSBs are written. In this mode the ramper only controls the time from one I2C brightness set-point to the next (see Figure 21).

![Figure 21. Brightness Control 00 (I2C Only)](image)

1. At time t0 the I2C Brightness Code is changed from 0x444 (1092d) to 0x7FF (2047d)
2. Ramp Rate programmed to 1ms/step
3. Mapping Mode set to Linear
4. $I_{LED_t0} = 1092 \times 12.213 \mu A = 13.337 \, mA$
5. $I_{LED_t1} = 2047 \times 12.213 \mu A = 25 \, mA$
6. $t_{RAMP} = (t_1 - t_0) = 1\, ms/\text{step} \times (2047 - 1092 - 1) = 954 \, ms$

![Figure 22. I2C Brightness Mode 00 Example (Ramp Between I2C Code Changes)](image)

7.4.1.2 PWM Only (Brightness Mode 01)

In brightness mode 01, only the PWM input sets the brightness. The I2C code is ignored. The LM36923 samples the PWM input and determines the duty cycle; this measured duty cycle is translated into an 11-bit digital code. The resultant code is then applied to the internal ramper (see Figure 23).
Device Functional Modes (continued)

Figure 23. Brightness Control 01 (PWM Only)

1. At time $t_0$ the PWM duty cycle changed from 25% to 100%.
2. Ramp Rate programmed to 1 ms/step.
3. Mapping Mode set to Linear.
4. $I_{LED_{t0}} = 25 \text{ mA} \times 0.25 = 6.25 \text{ mA}$
5. $I_{LED_{t1}} = 25 \text{ mA} \times 1 = 25 \text{ mA}$
6. $t_{RAMP} = (t_1 - t_0) = 1 \text{ ms/step} \times (2047 \times 1 - 2047 \times 0.25 - 1) = 1534 \text{ ms}$

Figure 24. Brightness Control Mode 01 Example (Ramp Between Duty Cycle Changes)

7.4.1.3 $I^2C$ + PWM Brightness Control (Multiply Then Ramp) Brightness Mode 10

In brightness control mode 10 the $I^2C$ Brightness register and the PWM input are both in control of the LED current. In this case the $I^2C$ brightness code is multiplied with the PWM duty cycle to produce an 11-bit code which is then sent to the ramper. In this mode ramping is achieved between $I^2C$ and PWM currents (see Figure 25).
Device Functional Modes (continued)

1. At time t0 the I2C Brightness code changed from 0x444 (1092d) to 0x7FF (2047d)
2. At time t0 the PWM duty cycle changed from 50% to 75%
3. Ramp Rate programmed to 1ms/step
4. Mapping Mode set to Linear
5. I_{LED_0} = 1092 \times 12.213 \mu A \times 0.5 = 6.668 mA
6. I_{LED_1} = 2047 \times 12.213 \mu A \times 0.75 = 18.75 mA
7. t_{RAMP} = (t_1 - t_0) = 1 \text{ms/step} \times (2047 \times 0.75 - 1092 \times 0.5 - 1) = 988 ms

**Figure 26. Brightness Control Mode 10 Example (Multiply Duty Cycle then Ramp)**

### 7.4.1.4 I2C + PWM Brightness Control (Ramp Then Multiply) Brightness Mode 11

In brightness control mode 11 both the I2C brightness code and the PWM duty cycle control the LED current. In this case the ramper only changes the time from one I2C brightness code to the next. The PWM duty cycle is multiplied with the I2C brightness code at the output of the ramper (see **Figure 27**).
Device Functional Modes (continued)

Figure 27. Brightness Control 11 (I$^2$C + PWM)

1. At time t0 the I$^2$C Brightness code changed from 0x444 (1092d) to 0x7FF (2047d)
2. At time t0 the PWM duty cycle changed from 50% to 75%
3. Ramp Rate programmed to 1 ms/step
4. Mapping Mode set to Linear
5. $I_{LED, t0-} = 1092 \times 12.213 \mu A \times 0.5 = 6.668 mA$
6. $I_{LED, t0+} = 1092 \times 12.213 \mu A \times 0.75 = 10.002 mA$
7. $t_{RAMP} = (t_1 - t_0) = 1 \text{ ms/step} \times (2047 - 1092 - 1) = 954 \text{ ms}$

Figure 28. Brightness Control Mode 11 Example (Ramp Current Then Multiply Duty Cycle)

7.4.2 Boost Switching Frequency

The LM36923H has two programmable switching frequencies: 500 kHz and 1 MHz. These are set via the Boost Control 1 register 0x13 bit [5]. Once the switching frequency is set, this nominal value can be shifted down by 12% via the boost switching frequency shift bit (register 0x13 bit[6]). Operation at 500 kHz is better suited for configurations which use a 10-µH inductor or use the auto-frequency mode and switch over to 500 kHz at lighter loads. Operation at 1 MHz is primarily beneficial at higher output currents, where the average inductor current is much larger than the inductor current ripple. For maximum efficiency across the entire load current range the device incorporates an automatic frequency shift mode (see Auto-Switching Frequency).
Device Functional Modes (continued)

7.4.2.1 Minimum Inductor Select

The LM36923H can use inductors in the range of 4.7 µH to 10 µH. In order to optimize the converter response to changes in \( V_{IN} \) and load, the Min Inductor Select bit (register 0x13 bit[4]) should be selected depending on which value of inductance is chosen. For 10-µH inductors this bit should be set to 1. For less than 10 µH, this bit should be set to 0.

7.4.3 Auto-Switching Frequency

To take advantage of frequency vs load dependent losses, the LM36923H has the ability to automatically change the boost switching frequency based on the magnitude of the load current. In addition to the register programmable switching frequencies of 500 kHz and 1 MHz, the auto-frequency mode also incorporates a low frequency selection of 250 kHz. It is important to note that the 250-kHz frequency is only accessible in auto-frequency mode and has a maximum boost duty cycle (\( D_{MAX} \)) of 50%.

Auto-frequency mode operates by using 2 programmable registers (Auto Frequency High Threshold (register 0x15) and Auto Frequency Low Threshold (0x16)). The high threshold determines the switchover from 1 MHz to 500 kHz. The low threshold determines the switchover from 500 kHz to 250 kHz. Both the High and Low Threshold registers take an 8-bit code which is compared against the 8 MSB of the brightness register (register 0x19). Table 6 details the boundaries for this mode.

<table>
<thead>
<tr>
<th>BRIGHTNESS CODE MSBs (Register 0x19 bits[7:0])</th>
<th>BOOST SWITCHING FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; Auto Frequency Low Threshold (register 15 Bits[7:0])</td>
<td>250 kHz (( D_{MAX} = 50% ))</td>
</tr>
<tr>
<td>&gt; Auto Frequency Low Threshold (Register 15 Bits[7:0]) or &lt; Auto Frequency High Threshold (Register 14 Bits[7:0])</td>
<td>500 kHz</td>
</tr>
<tr>
<td>≥ Auto Frequency High Threshold (register 14 Bits[7:0])</td>
<td>1 MHz</td>
</tr>
</tbody>
</table>

Automatic-frequency mode is enabled whenever there is a non-zero code in either the Auto-Frequency High or Auto-Frequency Low registers. To disable the auto-frequency shift mode, set both registers to 0x00. When automatic-frequency select mode is disabled, the switching frequency operates at the programmed frequency (Register 0x13 bit[5]) across the entire LED current range. Table 7 provides a guideline for selecting the auto-frequency 250-kHz threshold setting; the actual setting needs to be verified in the application.

<table>
<thead>
<tr>
<th>CONDITION ( (V_F = 3.2 \text{ V}, I_{LED} = 25 \text{ mA}) )</th>
<th>INDUCTOR (µH)</th>
<th>RECOMMENDED AUTO FREQUENCY LOW THRESHOLD MAXIMUM VALUE (NO SHIFT)</th>
<th>OUTPUT POWER AT AUTO FREQUENCY SWITCHOVER ( (W) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 × 4 LEDs</td>
<td>10</td>
<td>0x17</td>
<td>0.079</td>
</tr>
<tr>
<td>3 × 5 LEDs</td>
<td>10</td>
<td>0x15</td>
<td>0.089</td>
</tr>
<tr>
<td>3 × 6 LEDs</td>
<td>10</td>
<td>0x13</td>
<td>0.097</td>
</tr>
<tr>
<td>3 × 7 LEDs</td>
<td>10</td>
<td>0x11</td>
<td>0.101</td>
</tr>
<tr>
<td>3 × 8 LEDs</td>
<td>10</td>
<td>0x0f</td>
<td>0.102</td>
</tr>
</tbody>
</table>

7.4.4 I\(^2\)C Address Select (ASEL)

The LM36923H provides two I\(^2\)C slave address options. When ASEL = GND the slave address is set to 0x36. When ASEL = VIN the slave address is set to 0x37. This static input pin is read on power up (VIN > 1.8 V and HWEN > VIH) and must not be changed after power up.
7.4.5 Fault Protection/Detection

7.4.5.1 Overvoltage Protection (OVP)

The LM36923H provides four OVP thresholds (17 V, 24 V, 32 V, and 38 V). The OVP circuitry monitors the boost output voltage ($V_{OUT}$) and protects OUT and SW from exceeding safe operating voltages in case of open load conditions or in the event the LED string voltage requires more voltage than the programmed OVP setting. The OVP thresholds are programmed in register 13 bits[3:2]. The operation of OVP differentiates between two overvoltage conditions (see Case 1 OVP Fault Only (OVP Threshold Hit and All Enabled Current Sink Inputs > 40 mV), Case 2b OVP Fault and Open LED String Fault (OVP Threshold Duration and Any Enabled Current Sink Input ≤ 40 mV)).

7.4.5.1.1 Case 1 OVP Fault Only (OVP Threshold Hit and All Enabled Current Sink Inputs > 40 mV)

In steady-state operation with $V_{OUT}$ near the OVP threshold a rapid change in $V_{IN}$ or brightness code can result in a momentary transient excursion of $V_{OUT}$ above the OVP threshold. In this case the boost circuitry is disabled until $V_{OUT}$ drops below OVP – hysteresis (1 V). Once this happens the boost is re-enabled and steady state regulation continues. If $V_{OUT}$ remains above the OVP threshold for > 1 ms the OVP Flag is set (register 0x1F bit[0]).

7.4.5.1.2 Case 2a OVP Fault and Open LED String Fault (OVP Threshold Occurrence and Any Enabled Current Sink Input ≤ 40 mV)

When any of the enabled LED strings is open the boost converter tries to drive $V_{OUT}$ above OVP and at the same time the open string(s) current sink headroom voltage(s) (LED1, LED2, LED3) drop to 0. When the LM36923H detects three occurrences of $V_{OUT} > OVP$ and any enabled current sink input ($V_{LED1}$ or $V_{LED2}$, $V_{LED3}$) ≤ 40 mV, the OVP Fault flag is set (register 0x1F bit[0]), and the LED Open Fault flag is set (register 0x1F bit[4]).

7.4.5.1.3 Case 2b OVP Fault and Open LED String Fault (OVP Threshold Duration and Any Enabled Current Sink Input ≤ 40 mV)

When any of the enabled LED strings is open the boost converter tries to drive $V_{OUT}$ above OVP and at the same time the open string(s) current sink headroom voltage(s) (LED1, LED2, LED3) drop to 0. When the LM36923H detects $V_{OUT} > OVP$ for > 1 msec and any enabled current sink input ($V_{LED1}$ or $V_{LED2}$, $V_{LED3}$) ≤ 40 mV, the OVP Fault flag is set (register 0x1F bit[0]), and the LED Open Fault flag is set (register 0x1F bit[4]).

7.4.5.1.4 OVP/LED Open Fault Shutdown

The LM36923H has the option of shutting down the device when the OVP flag is set. This option can be enabled or disabled via register 0x1E bit[0]. When the shutdown option is disabled the fault flag is a report only. When the device is shut down due to an OVP/LED String Open fault, the fault flags register must be read back before the LM36923H can be re-enabled.

7.4.5.1.5 Testing for LED String Open

The procedure for detecting an open in a LED string is:

- Apply power the the LM36923H.
- Enable all LED strings (Register 0x10 = 0x0F).
- Set maximum brightness (Register 0x18 = 0x07 and Register 0x19 = 0xFF).
- Set the brightness control (Register 0x11 = 0x00).
- Open LED1 string.
- Wait 4 msec.
- Read LED open fault (Register 0x1F).
- If bit[4] = 1, then a LED open fault condition has been detected.
- Connect LED1 string.
- Repeat the procedure for the other LED strings.
7.4.5.2 Voltage Limitations on LED1, LED2, and LED3
The inputs to current sinks LED1, LED2, and LED3 are rated for 30 V (absolute maximum voltage). This is lower than the boost output capability as set by the OVP threshold (maximum specification) of 39 V. To ensure that the current sink inputs remain below their absolute maximum rating, the LED configuration between LED1 or LED2 or LED3 must not have a voltage difference between strings so that VLED1/2/3 have a voltage greater than 30 V.

7.4.5.3 LED String Short Fault
The LM36923H can detect an LED string short fault. This happens when the voltage between V\text{IN} and any enabled current sink input has dropped below (1.5 V). This test can only be performed on one LED string at a time. Performing this test with more than one LED string enabled can result in a faulty reading. The procedure for detecting a short in a LED string is:

- Apply power the LM36923H.
- Enable only LED1 string (Register 0x10 = 0x03).
- Enable short fault (Register 0x1E = 0x01).
- Set maximum brightness (Register 0x18 = 0x07 and Register 0x19 = 0xFF).
- Set the brightness control (Register 0x11 = 0x00).
- Wait 4 msec.
- Read LED short fault (Register 0x1F).
- If bit[3] = 1, then a LED short fault condition has been detected.
- Set chip enable and LED string enable low (Register 0x10 = 0x00).
- Repeat the procedure for the other LED strings.

7.4.5.4 Overcurrent Protection (OCP)
The LM36923H has four selectable OCP thresholds (750 mA, 1000 mA, 1250 mA, and 1500 mA). These are programmable in register 0x13 bits[1:0]. The OCP threshold is a cycle-by-cycle current limit and is detected in the internal low-side NFET. Once the threshold is hit the NFET turns off for the remainder of the switching period.

7.4.5.4.1 OCP Fault
If enough overcurrent threshold events occur, the OCP Flag (register 0x1F bit[1]) is set. To avoid transient conditions from inadvertently setting the OCP Flag, a pulse density counter monitors OCP threshold events over a 128-µs period. If 8 consecutive 128-µs periods occur where the pulse density count has found two or more OCP events, then the OCP Flag is set.

During device start-up and during brightness code changes, there is a 4-ms blank time where OCP events are ignored. As a result, if the device starts up in an overcurrent condition there is an approximate 5-ms delay before the OCP Flag is set.

7.4.5.4.2 OCP Shutdown
The LM36923H has the option of shutting down the device when the OCP flag is set. This option can be enabled or disabled via register 0x1E bit[2]. When the shutdown option is disabled, the fault flag is a report only. When the device is shut down due to an OCP fault, the fault flags register must be read back before the LM36923H can be re-enabled.

7.4.5.5 Device Overtemperature
Thermal shutdown (TSD) is triggered when the device die temperature reaches 135°C. When this happens the boost stops switching, and the TSD Flag (register 0x1F bit[2]) is set. The boost automatically starts up again when the die temperature cools down to 120°C.

7.4.5.5.1 Overtemperature Shutdown
The LM36923H has the option of shutting down the device when the TSD flag is set. This option can be enabled or disabled via register 0x1E bit[2]. When the shutdown option is disabled the fault flag is a report only. When the device is shut down due to a TSD fault, the Fault Flags register must be read back before the LM36923H can be re-enabled.
7.5 Programming

7.5.1 I2C Interface

7.5.1.1 Start and Stop Conditions

The LM36923H is configured via an I2C interface. START (S) and STOP (P) conditions classify the beginning and the end of the I2C session Figure 29. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I2C master always generates the START and STOP conditions. The I2C bus is considered busy after a START condition and free after a STOP condition. During the data transmission the I2C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

![Figure 29. I2C Start and Stop Conditions](image)

7.5.1.2 I2C Address

The 7-bit chip address for the LM36923 is 0x36 with ASEL connected to GND and 0x37 with ASEL connected to a logic high voltage. After the START condition the I2C master sends the 7-bit chip address followed by an eighth bit read or write (R/W). R/W = 0 indicates a WRITE, and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

7.5.1.3 Transferring Data

Every byte on the SDA line must be eight bits long with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse, (9th clock pulse), is generated by the master. The master then releases SDA (HIGH) during the 9th clock pulse. The LM36923H pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

7.5.1.4 Register Programming

For glitch free operation, the following bits and/or registers should only be programmed while the LED Enable bits are 0 (Register 0x10, Bit [3:1] = 0) and Device Enable bit is 1 (Register 0x10, Bit[0] = 1) :

1. Register 0x11 Bit[7] (Mapping Mode)
2. Register 0x11 Bits[6:5] (Brightness Mode)
3. Register 0x11 Bit[4] (Ramp Enable)
4. Register 0x11 Bit[3:1] (Ramp Rate)
5. Register 0x12 Bits[7:6] (PWM Sample Rate)
6. Register 0x12 Bits[5] (PWM Polarity)
7. Register 0x12 Bit[3:2] (PWM Hysteresis)
8. Register 0x12 Bit[3:2] (PWM Pulse Filter)
9. Register 0x15 (auto frequency high threshold)
10. Register 0x16 (auto frequency low threshold)
7.6 Register Maps

Note: Read of reserved (R) or write-only register returns 0.

Table 8. Revision (0x00)

<table>
<thead>
<tr>
<th>Bits [7:4]</th>
<th>Bits [3:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Revision Code</td>
</tr>
</tbody>
</table>

Table 9. Software Reset (0x01)

<table>
<thead>
<tr>
<th>Bits [7:1]</th>
<th>Software Reset Bit [0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0 = Normal Operation</td>
</tr>
<tr>
<td></td>
<td>1 = Device Reset (automatically resets back to 0)</td>
</tr>
</tbody>
</table>

Table 10. Enable (0x10)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0 = Disabled</td>
<td>0 = Disabled</td>
<td>0 = Disabled</td>
<td>0 = Disabled</td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td>1 = Enabled</td>
<td>1 = Enabled</td>
<td>1 = Enabled</td>
</tr>
</tbody>
</table>

Table 11. Brightness Control (0x11)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0 = Linear (default)</td>
<td>00 = Brightness Register Only</td>
<td>0 = Ramp Disabled (default)</td>
<td>000 = 0.125 ms/step</td>
<td>R</td>
</tr>
<tr>
<td>1 = Exponential</td>
<td>01 = PWM Duty Cycle Only</td>
<td>1 = Ramp Enabled</td>
<td>(default)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = Multiply Then Ramp</td>
<td>000 = 0.250 ms/step</td>
<td>010 = 0.5 ms/step</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Brightness Register × PWM)</td>
<td>011 = 1 ms/step</td>
<td>100 = 2 ms/step</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 = Ramp Then Multiply</td>
<td>101 = 4 ms/step</td>
<td>110 = 8 ms/step</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Brightness Register × PWM)</td>
<td>111 = 16 ms/step</td>
<td>(default)</td>
<td></td>
</tr>
</tbody>
</table>

Table 12. PWM Control (0x12)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00 = 800 kHz</td>
<td>0 = Active Low</td>
<td>000 = None</td>
<td>00 = No Filter</td>
</tr>
<tr>
<td>01 = 4 MHz</td>
<td>1 = Active High (default)</td>
<td>001 = 1 LSB</td>
<td>01 = 100 ns</td>
</tr>
<tr>
<td>1X = 24 MHz (default)</td>
<td></td>
<td>010 = 2 LSBs</td>
<td>10 = 150 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011 = 3 LSBs</td>
<td>11 = 200 ns (default)</td>
</tr>
</tbody>
</table>
Table 13. Boost Control 1 (0x13)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>N/A</td>
<td>0 = –12% Shift</td>
<td>0 = 500 kHz</td>
<td>0 = 4.7 µH (default)</td>
<td>00 = 17 V</td>
<td>00 = 750 mA</td>
</tr>
<tr>
<td></td>
<td>1 = No Shift (default)</td>
<td>1 = 1 MHz (default)</td>
<td>1 = 10 µH (default)</td>
<td>01 = 24 V</td>
<td>01 = 1000 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 = 31 V</td>
<td>11 = 38 V (default)</td>
<td>10 = 1250 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 = 1500 mA (default)</td>
</tr>
</tbody>
</table>

Table 14. Auto Frequency High Threshold (0x15)

Auto Frequency High Threshold (500 kHz to 1000 kHz) Bits [7:0]

Compared against the 8 MSBs of 11-bit brightness code (default = 00000000).

Table 15. Auto Frequency Low Threshold (0x16)

Auto Frequency High Threshold (250 kHz to 500 kHz) Bits [7:0]

Compared against the 8 MSBs of 11-bit brightness code (default = 00000000).

Table 16. Brightness Register LSBs (0x18)

<table>
<thead>
<tr>
<th>Bits [7:3]</th>
<th>I2C Brightness Code (LSB) Bits [2:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>This is the lower 3 bits of the 11-bit brightness code (default = 111).</td>
</tr>
</tbody>
</table>

Table 17. Brightness Register MSBs (0x19)

<table>
<thead>
<tr>
<th>I2C Brightness Code (MSB) Bits [7:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>This is the upper 8 bits of the 11-bit brightness code (default = 11111111).</td>
</tr>
</tbody>
</table>

Table 18. Fault Control (0x1E)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0 = LED Short Fault Detection is disabled (default).</td>
<td>0 = When the TSD Flag is set, the device is forced into shutdown.</td>
<td>0 = When the OCP Flag is set, the device is forced into shutdown.</td>
<td>0 = When the OVP Flag is set, the device is forced into shutdown.</td>
</tr>
<tr>
<td></td>
<td>1 = LED Short Fault Detection is enabled</td>
<td>1 = No shutdown (default)</td>
<td>1 = No shutdown (default)</td>
<td>1 = No shutdown (default)</td>
</tr>
</tbody>
</table>

Table 19. Fault Flags (0x1F)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>1 = LED String Open Fault</td>
<td>1 = LED Short Fault</td>
<td>1 = Thermal Shutdown Fault</td>
<td>1 = Current Limit Fault</td>
<td>1 = Output Overvoltage Fault</td>
</tr>
</tbody>
</table>
8 Applications and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LM36923H provides a complete high-performance LED lighting solution for mobile handsets. The LM36923H is highly configurable and can support multiple LED configurations.

8.2 Typical Application

8.2.1 Design Requirements

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input voltage ($V_{IN}$)</td>
<td>2.7 V</td>
</tr>
<tr>
<td>LED parallel/series configuration</td>
<td>3 × 5</td>
</tr>
<tr>
<td>LED maximum forward voltage ($V_f$)</td>
<td>3.2 V</td>
</tr>
<tr>
<td>Efficiency</td>
<td>82%</td>
</tr>
</tbody>
</table>

The number of LED strings, number of series LEDs, and minimum input voltage are needed in order to calculate the peak input current. This information guides the designer to make the appropriate inductor selection for the application. The LM36923H boost converter output voltage ($V_{OUT}$) is calculated: number of series LEDs × $V_f$ + 0.23 V. The LM36923H boost converter output current ($I_{OUT}$) is calculated: number of parallel LED strings × 25 mA. The LM36923H peak input current is calculated using Equation 5.

Figure 30. LM36923H Typical Application
8.2.2 Detailed Design Procedure

### Table 20. Typical Application Component List

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>L1</th>
<th>D1</th>
<th>COUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>3p7s, 3p8s</td>
<td>VLF504012MT-100M</td>
<td>NSR0530P2T5G</td>
<td>C2012X7R1H105K085AC</td>
</tr>
<tr>
<td></td>
<td>VLF504012MT-150M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3p6s</td>
<td>VLF504012MT-220M</td>
<td>NSR0530P2T5G</td>
<td>C2012X7R1H105K085AC</td>
</tr>
<tr>
<td>3p5s</td>
<td>VLF403210MT-100M</td>
<td>NSR0530P2T5G</td>
<td>C2012X7R1H105K085AC</td>
</tr>
<tr>
<td>3p4s</td>
<td>VLF302510MT-100M</td>
<td>NSR0530P2T5G</td>
<td>C2012X7R1H105K085AC</td>
</tr>
</tbody>
</table>

#### 8.2.2.1 Component Selection

##### 8.2.2.1.1 Inductor

The LM36923H requires a typical inductance in the range of 4.7 µH to 10 µH. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current of the application (I_{PEAK}) given in the inductor datasheet. The peak inductor current occurs at the maximum load current, the maximum output voltage, the minimum input voltage, and the minimum switching frequency setting. Also, the peak current requirement increases with decreasing efficiency. I_{PEAK} can be estimated using Equation 5:

\[
I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{V_{IN}}{2 \times f_{SW} \times L} \times \left(1 + \frac{V_{IN} \times \eta}{V_{OUT}}\right)
\]

Also, the peak current calculated above is different from the peak inductor current setting (I_{SAT}). The NMOS switch current limit setting (I_{CL_MIN}) must be greater than I_{PEAK} from Equation 5 above.

##### 8.2.2.1.2 Output Capacitor

The LM36923H requires a ceramic capacitor with a minimum of 0.4 µF of capacitance at the output, specified over the entire range of operation. This ensures that the device remains stable and oscillation free. The 0.4 µF of capacitance is the minimum amount of capacitance, which is different than the value of capacitor. Capacitance would take into account tolerance, temperature, and DC voltage shift.

Table 21 lists possible output capacitors that can be used with the LM36923H. Figure 31 shows the DC bias of the four TDK capacitors. The useful voltage range is determined from the effective output voltage range for a given capacitor as determined by Equation 6:

\[
DC \text{ Voltage Derating} \geq \frac{0.38\mu F}{(1 - Tol) \times (1 - Temp_co)}
\]

For example, with a 10% tolerance, and a 15% temperature coefficient, the DC voltage derating must be ≥ 0.38 / (0.9 × 0.85) = 0.5 µF. For the C1608X5R1H225K080AC (0603, 50-V) device, the useful voltage range occurs up to the point where the DC bias derating falls below 0.523 µF, or around 12 V. For configurations where V_{OUT} is > 15 V, two of these capacitors can be paralleled, or a larger capacitor such as the C2012X5R1H105K085AB must be used.
8.2.2.1.3 Input Capacitor

The input capacitor in a boost is not as critical as the output capacitor. The input capacitor primary function is to filter the switching supply currents at the device input and to filter the inductor current ripple at the input of the inductor. The recommended input capacitor is a 2.2-µF ceramic (0402, 10-V device) or equivalent.
8.2.3 Application Curves

L1 = 4.7 µH (VLF504012-4R7M) or 10 µH (VLF504015-100M) as noted in graphs, D1 = NSR240P2T5G, LEDs are Samsung SPMWHT325AD5YBTMS0, temperature = 25°C, $V_{IN}= 3.7 \text{ V}$, unless otherwise noted.
L1 = 4.7 µH (VLF504012-4R7M) or 10 µH (VLF504015-100M) as noted in graphs, D1 = NSR240P2T5G, LEDs are Samsung SPMWHT325AD5YBTMS0, temperature = 25°C, $V_{IN}$ = 3.7 V, unless otherwise noted.
L1 = 4.7 µH (VLF504012-4R7M) or 10 µH (VLF504015-100M) as noted in graphs, D1 = NSR240P2T5G, LEDs are Samsung SPMWHT325AD5YBTMS0, temperature = 25°C, V_{IN} = 3.7 V, unless otherwise noted.
L1 = 4.7 µH (VLF504012-4R7M) or 10 µH (VLF504015-100M) as noted in graphs, D1 = NSR240P2T5G, LEDs are Samsung SPMWHT325AD5YBTMS0, temperature = 25°C, V\textsubscript{IN} = 3.7 V, unless otherwise noted.
L1 = 4.7 µH (VLF504012-4R7M) or 10 µH (VLF504015-100M) as noted in graphs, D1 = NSR240P2T5G, LEDs are Samsung SPMWHT325AD5YBTMS0, temperature = 25°C, $V_{IN} = 3.7$ V, unless otherwise noted.

---

**Figure 56. LED Current Accuracy**

**Figure 57. LED Current Accuracy**

**Figure 58. LED Headroom Voltage (Mis-Matched Strings)**

**Figure 59. LED Headroom Voltage (Mis-Matched Strings)**

**Figure 60. Current vs PWM Sample Frequency**
9 Power Supply Recommendations

9.1 Input Supply Bypassing

The LM36923H is designed to operate from an input supply range of 2.5 V to 5.5 V. This input supply should be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). The resistance of the input supply rail should be low enough such that the input current transient does not cause the LM36923H supply voltage to droop more than 5%. Additional bulk decoupling located close to the input capacitor (C_IN) may be required to minimize the impact of the input supply rail resistance.

10 Layout

10.1 Layout Guidelines

The inductive boost converter of the LM36923H device detects a high switched voltage (up to V_OVP) at the SW pin, and a step current (up to I_CL) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OUT pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 61 highlights these two noise-generating components.

![Diagram of SW Pin Voltage (High Dv/Dt) and Current Through Schottky Diode and COUT (High Di/Dt)](image.png)

Figure 61. SW Pin Voltage (High Dv/Dt) and Current Through Schottky Diode and COUT (High Di/Dt)
Layout Guidelines (continued)

The following list details the main (layout sensitive) areas of the inductive boost converter of the LM36923 device in order of decreasing importance:

- **Output Capacitor**
  - Schottky Cathode to COUT+
  - COUT− to GND
- **Schottky Diode**
  - SW pin to Schottky Anode
  - Schottky Cathode to COUT+
- **Inductor**
  - SW Node PCB capacitance to other traces
- **Input Capacitor**
  - CIN+ to IN pin

### 10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path it detects a high-current step from 0 to \(V_{PEAK}\) each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through \(C_{OUT}\) and back into the GND pin of the LM36923H device GND pin contributes to voltage spikes \((V_{SPIKE} = L_p \times \frac{di}{dt})\) at SW and OUT. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close to the cathode of the Schottky diode as possible, and COUT− must be connected as close to the GND pin of the device as possible. The best placement for COUT is on the same layer as the LM36923H in order to avoid any vias that can add excessive series inductance.

### 10.1.2 Schottky Diode Placement

In the boost circuit of the LM36923H device the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to \(I_{PEAK}\) each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike \((V_{SPIKE} = L_p \times \frac{di}{dt})\) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to GND. Connecting the anode of the diode as close to the SW pin as possible and the cathode of the diode as close to \(C_{OUT}\) as possible reduces the inductance \((L_p)\) and minimize these voltage spikes.

### 10.1.3 Inductor Placement

The node where the inductor connects to the LM36923H device SW pin has 2 issues. First, a large switched voltage \((0 \text{ to } V_{OUT} + V_{F\_SCHOTTKY})\) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high impedance nodes that are more susceptible to electric field coupling must be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, ASEL, and PWM. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the \(V_{IN}\) to inductor connection and from the inductor to SW connection by use of short, wide traces.

### 10.1.4 Boost Input Capacitor Placement

For the LM36923H boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turnon of the internal power switch. The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical because any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND.
Layout Guidelines (continued)

plane. Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM36923H, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the LM36923H switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM36923H switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.

Figure 62 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is redrawn for the AC case where the V_IN supply is replaced with a short to GND, and the LM36923H + Inductor is replaced with a current source (ΔI_L). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_IN. As an example, consider a 3.6-V supply with 0.1 Ω of series resistance connected to C_IN through 50 nH of connecting traces. This results in an underdamped input-filter circuit with a resonant frequency of 712 kHz. Because both the 1-MHz and 500-kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500-kHz switching frequency) and 0.86 times the inductor current ripple using a 1-MHz switching frequency.

Increasing the series inductance (L_S) to 500 nH causes the resonant frequency to move to around 225 kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500-kHz switching frequency) and 0.053 times for a 1-MHz switching frequency.

Figure 62. Input RLC Network
10.2 Layout Example

Figure 63. LM36923H Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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11.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper
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changed. For change details, review the revision history included in any revised document.

11.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
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TI E2E™ Online Community  Ti’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration
among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support  Ti’s Design Support Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

11.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with
appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more
susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status(1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM36923HYFFR</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YFF</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>36923H</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM36923HYFR</td>
<td>DSBGA</td>
<td>YFF</td>
<td>12</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>1.5</td>
<td>1.99</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM36923HYFFR</td>
<td>DSBGA</td>
<td>YFF</td>
<td>12</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.
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