LM4510 Synchronous Step-Up DC/DC Converter with True Shutdown Isolation

1 Features

- 18 V@ 80 mA from 3.2 V Input
- 5 V @ 280 mA from 3.2 V Input
- No External Schottky Diode Required
- 85% Peak Efficiency
- Soft Start
- True Shutdown Isolation
- Stable with Small Ceramic or Tantalum Output Capacitors
- Output Short-Circuit Protection
- Feedback Fault Protection
- Input Undervoltage Lock Out
- Thermal Shutdown
- 0.002-µA Shutdown Current
- Wide Input Voltage Range: 2.7 V to 5.5 V
- 1-MHz Fixed Frequency Operation
- Low-profile 10-pin WSON Package (3 mm x 3 mm x 0.8 mm)

2 Applications

- Organic LED Panel Power Supply
- Charging Holster
- White LED Backlight
- USB Power Supply
- Class D Audio Amplifier
- Camera Flash LED Driver

3 Description

The LM4510 is a current mode step-up DC/DC converter with a 1.2-A internal NMOS switch designed to deliver up to 120 mA at 16 V from a Li-Ion battery.

The device’s synchronous switching operation (no external Schottky diode) at heavy-load, and non-synchronous switching operation at light-load, maximizes power efficiency.

True shutdown function by synchronous FET and related circuitry ensures input and output isolation.

A programmable soft-start circuit allows the user to limit the amount of inrush current during start-up. The output voltage can be adjusted by external resistors.

The LM4510 features advanced short-circuit protection to maximize safety during output to ground short condition. During shutdown the feedback resistors and the load are disconnected from the input to prevent leakage current paths to ground.

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM4510</td>
<td>WSON (10)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Efficiency at VOUT = 16 V

<table>
<thead>
<tr>
<th>V IN</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.7V</td>
<td></td>
</tr>
<tr>
<td>3.6V</td>
<td></td>
</tr>
<tr>
<td>4.5V</td>
<td></td>
</tr>
<tr>
<td>5.5V</td>
<td></td>
</tr>
</tbody>
</table>

Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D Page

• Added Device Information and Handling Rating tables, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections; moved some curves to Application Curves section .......... 1

Changes from Revision B (May 2013) to Revision C Page

• Changed layout of National Data Sheet to TI format ................................................................. 19
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW</td>
<td>A</td>
<td>Switch pin. Drain connections of both internal NMOS and PMOS devices.</td>
</tr>
<tr>
<td>2</td>
<td>PGND</td>
<td>G</td>
<td>Power ground</td>
</tr>
<tr>
<td>3</td>
<td>VIN</td>
<td>P</td>
<td>Analog and Power supply input. Input range: 2.7 V to 5.5 V.</td>
</tr>
<tr>
<td>4</td>
<td>EN</td>
<td>I</td>
<td>Enable logic input. HIGH= Enabled, LOW=Shutdown.</td>
</tr>
<tr>
<td>5</td>
<td>SS</td>
<td>A</td>
<td>Soft-start pin</td>
</tr>
<tr>
<td>6</td>
<td>AGND</td>
<td>G</td>
<td>Analog ground</td>
</tr>
<tr>
<td>7</td>
<td>COMP</td>
<td>A</td>
<td>Compensation network connection.</td>
</tr>
<tr>
<td>8</td>
<td>FB</td>
<td>A</td>
<td>Output voltage feedback connection.</td>
</tr>
<tr>
<td>9</td>
<td>N/C</td>
<td></td>
<td>No internal connection.</td>
</tr>
<tr>
<td>10</td>
<td>VOUT</td>
<td>A</td>
<td>Internal PMOS source connection for synchronous rectification.</td>
</tr>
<tr>
<td>DAP</td>
<td>DAP</td>
<td></td>
<td>Die Attach Pad thermal connection</td>
</tr>
</tbody>
</table>

### WSON Package (DSC) 10 Pins

- **Top View**
- **Bottom View**
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>−0.3</td>
<td>21</td>
<td>V</td>
</tr>
<tr>
<td>SW(4)</td>
<td>−0.3</td>
<td>VOUT + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>EN, SS, COMP FB</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>PGND to AGND</td>
<td>−0.2</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>Continuous power dissipation(5)</td>
<td>Internally Limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction temperature (TJ-MAX)</td>
<td>150</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead temperature (soldering, 10 sec)(6)</td>
<td>260</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Recommended Operating Conditions are conditions for which the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

(2) All voltages are with respect to the potential at the GND pin.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) This condition applies if VIN < VOUT. If VIN > VOUT, a voltage greater than VIN + 0.3 V should not be applied to the VOUT or SW pins.

(5) The absolute maximum specification applies to DC voltage. An extended negative voltage limit of –1 V applies for a pulse of up to 1 µs, and –2 V for a pulse of up to 40 ns. An extended positive voltage limit of 22 V applies for a pulse of up to 20 ns.

(6) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at TJ = 150°C (Typ.) and disengages at TJ = 140°C (Typ.).

For detailed soldering information and specifications, please refer to Application Note 1187: Leadless Leadframe Package (LLP) (SNOI401).

6.2 Handling Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tstg Storage temperature range</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>V(ESD) Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)</td>
<td>2</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Machine model</td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (VIN)</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Junction temperature (TJ)(1)</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Output voltage (VOUT)</td>
<td>18</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature (TJ-MAX-OP = 125°C), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to-ambient thermal resistance of the part/package in the application (RθJA), as given by the following equation: TA-MAX = TJ-MAX-OP – (RθJA × PD-MAX)
## 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM4510</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JJA}) Junction-to-ambient thermal resistance</td>
<td>36</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JJC(top)}) Junction-to-case (top) thermal resistance</td>
<td>48.3</td>
<td></td>
</tr>
<tr>
<td>(R_{JJB}) Junction-to-board thermal resistance</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>(\Psi_{JT}) Junction-to-top characterization parameter</td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td>(\Psi_{JB}) Junction-to-board characterization parameter</td>
<td>22.1</td>
<td></td>
</tr>
<tr>
<td>(R_{JJC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>3.8</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

Unless otherwise stated the following conditions apply: \(V_{IN} = 3.6\) V, \(EN = 3.6\) V, \(T_{J} = 25°C\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(^{(1)})</th>
<th>TYP(^{(2)})</th>
<th>MAX(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{FB}) FB Pin Voltage</td>
<td>(2.7) V (\leq V_{IN} \leq 5.5) V</td>
<td>2.7 V (\leq V_{IN} \leq 5.5) V, (-40°C \leq T_{J} \leq 125°C)</td>
<td>1.24</td>
<td>1.29</td>
<td>V</td>
</tr>
<tr>
<td>(I_{FB}) FB Pin Bias Current(^{(3)})</td>
<td>(-40°C \leq T_{J} \leq 125°C)</td>
<td>0.050</td>
<td>1.5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(R_{DS(on)}) NMOS Switch (R_{DS(on)})</td>
<td>(I_{SW} = 0.3) A</td>
<td>0.45</td>
<td>1.1</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>(R_{DS(on)}) PMOS Switch (R_{DS(on)})</td>
<td>(I_{SW} = 0.3) A, (V_{OUT} = 10) V</td>
<td>0.9</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CL}) NMOS Switch Current Limit</td>
<td></td>
<td>1</td>
<td>1.2</td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td>(I_{Q}) Device Switching</td>
<td>EN = 3.6 V, (FB = COMP)</td>
<td>1.7</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>EN = 3.6 V, (FB = COMP), (-40°C \leq T_{J} \leq 125°C)</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN = 3.6 V, (FB &gt; 1.29) V</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN = 3.6 V, (FB &gt; 1.29) V, (-40°C \leq T_{J} \leq 125°C)</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Shutdown Current</td>
<td>EN = 0 V</td>
<td>0.002</td>
<td>0.050</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{L}) SW Leakage Current(^{(3)})</td>
<td>SW = 20 V</td>
<td>0.01</td>
<td>0.150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(I_{VOUT}) VOUT Bias Current(^{(3)})</td>
<td>(V_{OUT} = 20) V</td>
<td></td>
<td>90</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>(V_{OUT} = 20) V, (-40°C \leq T_{J} \leq 125°C)</td>
<td>50</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{VL}) PMOS Switch Leakage Current</td>
<td>SW = 0 V, (V_{OUT} = 20) V</td>
<td>0.001</td>
<td>0.100</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(I_{SW}) Switching Frequency</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>(-40°C \leq T_{J} \leq 125°C)</td>
<td>0.85</td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(D_{MAX}) Maximum Duty Cycle</td>
<td>FB = 0 V</td>
<td></td>
<td>94%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FB = 0 V, (-40°C \leq T_{J} \leq 125°C)</td>
<td>88%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(D_{MIN}) Minimum Duty Cycle</td>
<td></td>
<td></td>
<td>15%</td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>(G_{m}) Error Amplifier Transconductance</td>
<td>(-40°C \leq T_{J} \leq 125°C)</td>
<td>130</td>
<td></td>
<td></td>
<td>µmho</td>
</tr>
<tr>
<td>(EN) Device Enable</td>
<td>HIGH</td>
<td>0.81</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>HIGH, (-40°C \leq T_{J} \leq 125°C)</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LOW</td>
<td>0.78</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LOW, (-40°C \leq T_{J} \leq 125°C)</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) All room temperature limits are production tested, specified through statistical analysis or by design. All limits at \(-40°C \leq T_{J} \leq 125°C\) are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

\(^{(2)}\) Typical numbers are at 25°C and represent the most likely norm.

\(^{(3)}\) Current flows into the pin.
## Electrical Characteristics (continued)

Unless otherwise stated the following conditions apply: \( \text{VIN} = 3.6 \text{ V}, \text{EN} = 3.6 \text{ V}, \text{T} \text{J} = 25^\circ \text{C}. \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(^{(1)})</th>
<th>TYP(^{(2)})</th>
<th>MAX(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{EN}} )</td>
<td>EN Pin Bias Current</td>
<td>( 0 &lt; \text{EN} &lt; 3.6 \text{ V} )</td>
<td>3.2</td>
<td>8</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0 &lt; \text{EN} &lt; 3.6 \text{ V}, \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{FB}} )</td>
<td>Feedback Fault Protection</td>
<td>( \text{ON Threshold} )</td>
<td>19.7</td>
<td></td>
<td>( \text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{ON Threshold, } \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td>18</td>
<td>20.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{OFF Threshold} )</td>
<td>18.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{OFF Threshold, } \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td>17</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{UVLO}} )</td>
<td>Input Undervoltage Lockout</td>
<td>( \text{ON Threshold} )</td>
<td>2.5</td>
<td></td>
<td>( \text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{ON Threshold, } \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td></td>
<td>2.65</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{OFF Threshold} )</td>
<td>2.35</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{OFF Threshold, } \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td>2.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SS}} )</td>
<td>Soft-Start Pin Current(^{(4)})</td>
<td>( \text{−40}^\circ \text{C} \leq \text{T} \text{J} \leq \text{125}^\circ \text{C} )</td>
<td>11.3</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
</tbody>
</table>

\(^{(4)}\) Current flows out of the pin.
### 6.6 Typical Characteristics

LM4510SD, Circuit of Figure 18, (L = 4.7 µH, COILCRAFT, DO3316-472ML; C\textsubscript{IN} = 4.7 µF, TDK, C2012X5R0J475K; C\textsubscript{OUT} = 10 µF, AVX, 12103D106KAT2A; C\textsubscript{S} = 10 nF, TDK, C1608C0G1E103J; C\textsubscript{CH} = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R\textsubscript{C} = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V\textsubscript{IN} = 3.6 V, V\textsubscript{OUT} = 16 V, T\textsubscript{A} = 25°C, unless otherwise noted.

#### Figure 1. Switching Quiescent Current vs V\textsubscript{IN}

#### Figure 2. R\textsubscript{DS(on)} vs Temperature at V\textsubscript{IN} = 3.6 V

#### Figure 3. Load Capability vs V\textsubscript{IN} (V\textsubscript{OUT} = 16 V)

#### Figure 4. Output Voltage vs Temperature (V\textsubscript{OUT} = 17 V)

#### Figure 5. Switching Frequency vs Temperature

#### Figure 6. Load Regulation (V\textsubscript{OUT} = 16 V)
Typical Characteristics (continued)

LM4510SD, Circuit of Figure 18, (L = 4.7 μH, COILCRAFT, DO3316-472ML; C\text{IN} = 4.7 μF, TDK, C2012X5R0J475K; C\text{OUT} = 10 μF, AVX, 12103D106KAT2A; C\text{S} = 10 nF, TDK, C1608C0G1E103J; C\text{C1} = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R\text{C} = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V\text{IN} = 3.6 V, V\text{OUT} = 16 V, T\text{A} = 25°C, unless otherwise noted.

Figure 7. Load Regulation (V\text{OUT} = 5 V)

Figure 8. Line Regulation (V\text{OUT} = 16 V)

Figure 9. Line Regulation (V\text{OUT} = 5 V)

Figure 10. Line Transient Response (V\text{OUT} = 16 V)

Figure 11. Load Transient Response (V\text{OUT} = 16 V)

Figure 12. Short Circuit Response (V\text{OUT} = 16 V)
Typical Characteristics (continued)

LM4510SD, Circuit of Figure 18, (L = 4.7 µH, COILCRAFT, DO3316-472ML; C_in = 4.7 µF, TDK, C2012X5R0J475K; C_out = 10 µF, AVX, 12103D106KAT2A; C_s = 10 nF, TDK, C1608C0G1E103J; C_C1 = 2.2 nF, Taiyo Yuden, TMK107SD222JA-T; R_C = 46.4 kΩ, Yageo, 9t06031A4642FBHFT), V_in = 3.6 V, V_out = 16 V, T_A = 25°C, unless otherwise noted.

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7 Detailed Description

7.1 Overview
LM4510 is a peak current-mode, fixed-frequency PWM boost regulator that employs both Synchronous and Non-Synchronous Switching.

The DC/DC regulator regulates the feedback output voltage providing excellent line and load transient response. The operation of the LM4510 can best be understood by referring to the Block Diagram.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Short Circuit Protection
When $V_{OUT}$ goes down to $V_{IN} - 0.7V$ (typ.), the device stops switching due to the short-circuit protection circuitry and the short-circuit output current is limited to $I_{INIT\_CHARGE}$.
Feature Description (continued)

7.3.2 Feedback Fault Protection

The LM4510 features unique Feedback Fault Protection to maximize safety when the feedback resistor is not properly connected to a circuit or the feedback node is shorted directly to ground.

Feedback fault triggers $V_{\text{OUT}}$ monitoring. During monitoring, if $V_{\text{OUT}}$ reaches a protection level, the device shuts down. When the feedback network is reconnected and $V_{\text{OUT}}$ is lower than the OFF threshold level of Feedback Fault Protection, $V_{\text{OUT}}$ monitoring stops. $V_{\text{OUT}}$ is then regulated by the control loop.

7.3.3 Input Undervoltage Lock-Out

The LM4510 has dedicated circuitry to protect the IC and the external components when the battery voltage is lower than the preset threshold. This undervoltage lock-out with hysteresis prevents malfunctions during start-up or abnormal power off.

7.3.4 Thermal Shutdown

If the die temperature exceeds 150°C (typ.), the thermal protection circuitry shuts down the device. The switches remain off until the die temperature is reduced to approximately 140°C (typ.).

7.4 Device Functional Modes

7.4.1 Non-Synchronous Operation

The device operates in Non-synchronous Mode at light load ($I_{\text{OUT}} < 10$ mA) or when output voltage is lower than 10 V (typ.). At light load, LM4510 automatically changes its switching operation from 'Synchronous' to 'Non-Synchronous' depending on $V_{\text{IN}}$ and $L$. Non-Synchronous operation at light load maximizes power efficiency by reducing PMOS driving loss.

7.4.2 Operation in Synchronous Continuous Conduction Mode (Cycle 1, Cycle 2)

Synchronous boost converter is shown in Figure 15. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device and turns off the PMOS power device.

7.4.2.1 Cycle 1 Description

Refer to Figure 16. NMOS switch turn-on → Inductor current increases and flows to GND.
PMOS switch turn-off → Isolate $V_{\text{OUT}}$ from SW → Output capacitor supplies load current.
Device Functional Modes (continued)

During operation, EAMP output voltage ($V_{COMP}$) increases for larger loads and decreases for smaller loads. When the sum of the ramp compensation and the sensed NMOS current reaches a level determined by the EAMP output voltage, the PWM COMP resets the logic, turning off the NMOS power device and turning on the PMOS power device.

7.4.2.2 Cycle 2 Description

Refer to Figure 17. NMOS Switch turn-off → PMOS Switch turn-on → Inductor current decreases and flows through PMOS → Inductor current recharges output capacitor and supplies load current.

![Figure 17. Equivalent Circuit During Cycle 2](image)

After the switching period the oscillator then sets the driver logic again repeating the process.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM4510 shuts down when the EN pin is low. In this mode the feedback resistors and the load are disconnected from the input in order to avoid leakage current flow and to allow the output voltage to drop to 0 V.

The LM4510 turns on when EN is high. There is an internal pull-down resistor on the EN pin so the device is in a normally off state.

8.2 Typical Applications

8.2.1 2.7 V to 5.5 V Input with a 16 V Output

8.2.1.1 Design Requirements

The LM4510 is designed to operate up to 75 mA at 2.7 V input and 350 mA at 5.5 V input to output 16 V. In any case, it is recommended to avoid starting up the device at minimum input voltage and maximum load. Special attention must be taken to avoid operating near thermal shutdown condition. A simple calculation can be used to determine the power dissipation at the operating condition. \( P_{D-MAX} = \frac{(T_{J-MAX-OP} - T_{A-MAX})}{R_{\theta JA}} \) (\( T_{J-MAX-OP} = 125°C \)).

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjusting Output Voltage

The output voltage is set using the feedback pin and a resistor voltage divider (\( R_{F1}, R_{F2} \)) connected to the output as shown in Figure 18.

The ratio of the feedback resistors sets the output voltage.

\( R_{F2} \) Selection First of all choose a value for \( R_{F2} \) generally between 10 kΩ and 25 kΩ.

\( R_{F1} \) Selection Calculate \( R_{F1} \) using Equation 1:
Typical Applications (continued)

\[ R_{F1} = \left( \frac{V_O}{V_{FB}} - 1 \right) \times R_{F2}[\Omega] \]  

(1)

Table 1 gives suggested component values for several typical output voltages.

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE (V)</th>
<th>( R_{F2} ) (kΩ)</th>
<th>( R_{F1} ) (kΩ)</th>
<th>( R_C ) (kΩ)</th>
<th>( C_{C1} ) (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>20.5</td>
<td>240</td>
<td>46.4</td>
<td>2.2</td>
</tr>
<tr>
<td>12</td>
<td>20.5</td>
<td>174</td>
<td>46.4</td>
<td>2.2</td>
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<td>5</td>
<td>20.5</td>
<td>60.4</td>
<td>46.4</td>
<td>2.2</td>
</tr>
<tr>
<td>3.3</td>
<td>20.5</td>
<td>33</td>
<td>46.4</td>
<td>2.2</td>
</tr>
</tbody>
</table>

8.2.1.2.2 Maximum Output Current

When the output voltage is set at different level, it is important to know the maximum load capability. By first order estimation, \( I_{OUT(MAX)} \) can be estimated by Equation 2:

\[ I_{OUT,\text{Max}} = \frac{1.32 \times V_{IN} - 2.79}{V_{OUT}} [A] \]  

(2)

8.2.1.2.3 Inductor Selection

The larger value inductor makes lower peak inductor current and reduces stress on internal power NMOS.

On the other hand, the smaller value inductor has smaller outline, lower DCR and a higher current capacity. Generally a 4.7-μH to 15-μH inductor is recommended.

8.2.1.2.4 \( I_{L_AVE} \) Check

The average inductor current is given by Equation 3:

\[ I_{L_AVE} = \frac{I_{OUT}}{\eta \times D'} [A], \ D' = \frac{V_{IN}}{V_{OUT}} \]  

(3)

Where \( I_{OUT} \) is output current, \( \eta \) is the converter efficiency of the total driven load and \( D' \) is the off duty cycle of the switching regulator.

Inductor DC current rating (40°C temperature rise) should be more than the average inductor current at worst case.

\( \Delta I \) Define

The inductor ripple current is given by Equation 4:

\[ \Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} [A], \ D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \]  

(4)

Where \( D \) is the on-duty cycle of the switching regulator. A common choice is to set \( \Delta I_L \) to about 30% of \( I_{L_AVE} \).

\( I_{L_PK} \leq I_{CL} \) Check & \( I_{MIN} \) Define

The peak inductor current is given by Equation 5:
\[ I_{L_{pk}} = I_{L_{ave}} + \frac{\Delta I_{L}}{2} [A] \]

\[ I_{L_{pk}} = \frac{I_{OUT}}{\eta \times D} + \frac{V_{IN} \times D}{2L \times f_{SW}} [A] \]

(5)

To prevent loss of regulation, ensure that the NMOS power switch current limit is greater than the worst-case peak inductor current in the target application.

Also make sure that the inductor saturation current is greater than the peak inductor current under the worst-case load transient, high ambient temperature and start-up conditions. Refer to Table 2 for suggested inductors.

### Table 2. Suggested Inductors and Their Suppliers

<table>
<thead>
<tr>
<th>MODEL</th>
<th>VENDOR</th>
<th>DIMENSIONS LxWxH (mm)</th>
<th>D.C.R (max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DO3314-472ML</td>
<td>COILCRAFT</td>
<td>3.3mm x 3.3mm x 1.4mm</td>
<td>320 mΩ</td>
</tr>
<tr>
<td>DO3316P-472ML</td>
<td>COILCRAFT</td>
<td>12.95mm x 9.4mm x 5.4mm</td>
<td>18 mΩ</td>
</tr>
</tbody>
</table>

#### 8.2.1.2.5 Input Capacitor Selection

Due to the presence of an inductor, the input current waveform is continuous and triangular. So the input capacitor is less critical than output capacitor in boost applications. Typically, a 4.7-μF to 10-μF ceramic input capacitor is recommended on the VIN pin of the IC.

**I\text{CIN\_RMS} Check**

The RMS current in the input capacitor is given by Equation 6:

\[ I_{\text{CIN\_RMS}} = \frac{\Delta I_{L}}{\sqrt{12}} [A] \]

(6)

The input capacitor should be capable of handling the RMS current.

#### 8.2.1.2.6 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the switch is closed and the inductor is charging. As a result, it sees very large ripple currents.

A ceramic capacitor of value 4.7 μF to 10 μF is recommended at the output. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used.

**I\text{COUT\_RMS} Check**

The RMS current in the output capacitor is given by Equation 7:

\[ I_{\text{COUT\_RMS}} = \sqrt{(1 - D) \left[ \frac{2}{D (1 - D)^2} \frac{\Delta I_{L}^2}{12} \right]} [A] \]

(7)

The output capacitor should be capable of handling the RMS current.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. The output capacitor also affects the soft-start time (See Soft-Start Function and Soft-Start Capacitor Selection). Table 3 shows suggested input and output capacitors.
Table 3. Suggested $C_{IN}$ and $C_{OUT}$ Capacitors and Their Suppliers

<table>
<thead>
<tr>
<th>MODEL</th>
<th>TYPE</th>
<th>VENDOR</th>
<th>VOLTAGE RATING</th>
<th>CASE SIZE INCH (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7 µF for $C_{IN}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2012X5R0J475</td>
<td>Ceramic, X5R</td>
<td>TDK</td>
<td>6.3 V</td>
<td>0805 (2012)</td>
</tr>
<tr>
<td>GRM21BR60J475</td>
<td>Ceramic, X5R</td>
<td>muRata</td>
<td>6.3 V</td>
<td>0805 (2012)</td>
</tr>
<tr>
<td>JMK212BJ475</td>
<td>Ceramic, X5R</td>
<td>Taiyo-Yuden</td>
<td>6.3 V</td>
<td>0805 (2012)</td>
</tr>
<tr>
<td>C2012X5R0J475K</td>
<td>Ceramic, X5R</td>
<td>TDK</td>
<td>6.3 V</td>
<td>0603 (1608)</td>
</tr>
<tr>
<td>10 µF for $C_{OUT}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMK316BJ106KL</td>
<td>Ceramic, X5R</td>
<td>Taiyo-Yuden</td>
<td>25 V</td>
<td>1206 (3216)</td>
</tr>
<tr>
<td>12103D106KAT2A</td>
<td>Ceramic, X5R</td>
<td>AVX</td>
<td>25 V</td>
<td>1210 (3225)</td>
</tr>
</tbody>
</table>

8.2.1.2.7 Soft-Start Function and Soft-Start Capacitor Selection

The LM4510 has a soft-start pin that can be used to limit the input inrush current. Connect a capacitor from SS pin to GND to set the soft-start period. Figure 19 describes the soft start process.

- Initial charging period: When the device is turned on, the control circuitry linearly regulating initial charge current charges $V_{OUT}$ by limiting the inrush current.
- Soft-start period: After $V_{OUT}$ reaches $V_{IN} - 0.7$ V (typ.), the device starts switching and the $C_S$ is charged at a constant current of $11 \mu A$, ramping up to $V_{IN}$. This period ends when $V_{SS}$ reaches $V_{FB}$. $C_S$ should be large enough to ensure soft-start period ends after $C_O$ is fully charged.

During the initial charging period, the required load current must be smaller than the initial charge current to ensure $V_{OUT}$ reaches $V_{IN} - 0.7$ V (typ.).

\[ I_{SS} = \frac{C_{OUT} \times (V_{IN} - 0.7)}{I_{INIT\_CHARGE}} + \frac{C_S \times V_{FB}}{I_{SS\_CHARGE}} [sec] \]  

(8)

Where the $I_{INIT\_CHARGE}$ is Initial Charging Current depending on $V_{IN}$ and $I_{SS\_CHARGE}$ (11 µA (typ.). Also, when selecting the fuse current rating, make sure the value is higher than the initial charging current.

Figure 19. Soft-Start Timing Diagram
8.2.1.2.8 Compensation Component Selection

The LM4510 provides a compensation pin COMP to customize the voltage loop feedback. It is recommended that a series combination of \( R_C \) and \( C_{C1} \) be used for the compensation network, as shown in the typical application circuit. In addition, \( C_{C2} \) is used for compensating high frequency zeros.

The series combination of \( R_C \) and \( C_{C1} \) introduces a pole-zero pair according to Equation 9:

\[
\begin{align*}
  f_{PC} &= \frac{1}{2\pi(R_C + R_C)C_{C1}} \text{ [Hz]} \\
  f_{ZC} &= \frac{1}{2\pi R_CC_{C1}} \text{ [Hz]}
\end{align*}
\]  

(9)

In addition, \( C_{C2} \) introduces a pole according to Equation 10:

\[
  f_{PC2} = \frac{1}{2\pi R_C/R_CC_{C2}} \text{ [Hz]}
\]  

(10)

Where \( R_O \) is the output impedance of the error amplifier, approximately 1 M\( \Omega \), and amplifier voltage gain is typically 200 V/V depending on temperature and \( V_{IN} \).

Refer to Table 4 for suggested soft start capacitor and compensation components.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>TYPE</th>
<th>VENDOR</th>
<th>VOLTAGE RATING</th>
<th>CASE SIZE INCH (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( (C_S) ) C1608CG1E103J</td>
<td>Ceramic, X5R</td>
<td>TDK</td>
<td>6.3 V</td>
<td>603 (1608)</td>
</tr>
<tr>
<td>( (C_1) ) TMK107SD222JA-T</td>
<td>Ceramic, X5R</td>
<td>Taiyo Yuden</td>
<td>25 V</td>
<td>603 (1608)</td>
</tr>
<tr>
<td>( (R_C) ) 906031A4642FBHFT</td>
<td>Resistor</td>
<td>Yageo Corporation</td>
<td>1/10 W</td>
<td>603 (1608)</td>
</tr>
</tbody>
</table>
8.2.1.3 Application Curves

Figure 20. Efficiency vs Output Current ($V_{OUT} = 16$ V)

Figure 21. Efficiency vs Output Current ($V_{OUT} = 12$ V)

Figure 22. Efficiency vs Output Current ($V_{OUT} = 5$ V, $L = DO3314-472ML$)

Figure 23. Start Up ($V_{OUT} = 16$ V, $R_{LOAD} = 530$ $\Omega$)

Figure 24. Shut Down ($V_{OUT} = 16$ V, $R_{LOAD} = 940$ $\Omega$)
8.2.2 Flash and Torch Application

LM4510 can be configured to drive white LEDs for the flash and torch functions. The flash/torch can be set up with the circuit shown in Figure 25 by using the resistor $R_T$ to determine the current in Torch Mode and $R_F$ to determine the current in Flash Mode. The amount of current can be estimated using Equation 11:

\[
I_{\text{Torch}} = \frac{V_{\text{FB}}}{R_T} \quad \text{(A)} \\
I_{\text{Flash}} = \frac{V_{\text{FB}}}{R_T / R_F} \quad \text{(A)}
\]

Figure 25. Typical Application Circuit for Flash/Torch

8.2.2.1 Design Requirements

See Design Requirements.

8.2.2.2 Detailed Design Procedure

See Detailed Design Procedure.

8.2.2.3 Application Curve

See Application Curves.
9 Power Supply Recommendations

The power supply for the applications using the LM4510 device should be big enough considering output power and efficiency at given input voltage condition. Minimum current requirement condition is \( \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times \text{efficiency}} \) and approximately 20 - 30% higher than this value is recommended.

10 Layout

10.1 Layout Guidelines

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM4510 device. Refer to Figure 26 as an example. Some additional guidelines to be observed:

1. \( C_{\text{IN}} \) must be placed close to the device and connected directly from VIN to PGND pins. This reduces copper trace resistance, which affects the input voltage ripple of the device. For additional input voltage filtering, typically a 0.1 \( \mu \text{F} \) bypass capacitor can be placed between VIN and AGND. This bypass capacitor should be placed near the device closer than \( C_{\text{IN}} \).

2. \( C_{\text{OUT}} \) must also be placed close to the device and connected directly from VOUT to PGND pins. Any copper trace connections for the \( C_{\text{OUT}} \) capacitor can increase the series resistance, which directly affects output voltage ripple and makes noise during output voltage sensing.

3. All voltage-sensing resistors (\( R_{\text{F1}}, R_{\text{F2}} \)) should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the voltage-sensing resistor should be connected directly to the AGND pin.

4. Trace connections made to the inductor should be minimized to reduce power dissipation, EMI radiation and increase overall efficiency. Also poor trace connection increases the ripple of SW.

5. \( C_{\text{S}}, C_{\text{C1}}, C_{\text{C2}}, R_{\text{C}} \) must be placed close to the device and connected to AGND.

6. The AGND pin should connect directly to the ground. Not connecting the AGND pin directly, as close to the chip as possible, may affect the performance of the LM4510 and limit its current driving capability. AGND and PGND should be separate planes and should be connected at a single point.

7. For better thermal performance, DAP should be connected to ground, but cannot be used as the primary ground connection. The PC board land may be modified to a "dog bone" shape to reduce SON thermal impedance. For detail information, refer to Application Note AN-1187.

10.2 Layout Example

![Figure 26. Evaluation Board Layout](image-url)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
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<tbody>
<tr>
<td>LM4510SD/NOPB</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L4510</td>
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<td>DSC</td>
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<td>4500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L4510</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

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<th>Package Type</th>
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<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>DSC</td>
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<td>DSC</td>
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<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
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</tbody>
</table>

*All dimensions are nominal.*

---

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*Images show the reel dimensions and quadrant assignments.*
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>35.0</td>
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<td>DSC</td>
<td>10</td>
<td>4500</td>
<td>346.0</td>
<td>346.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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