LM4937 Boomer® Audio Power Amplifier Series Audio Sub-System with OCL Stereo Headphone Output and RF Suppression

Check for Samples: LM4937

FEATURES

- **18-Bit Stereo DAC**
- **Multiple Distinct Output Modes**
- **Mono Speaker Amplifier**
- **Stereo Headphone Amplifier**
- **Mono Earpiece Amplifier**
- **Differential Mono Analog Input**
- **Independent Loudspeaker, Headphone and Mono Earpiece Volume Controls**
- **I^2C/SPI (Selectable) Compatible Interface**
- **Ultra Low Shutdown Current**
- **Click and Pop Suppression Circuit**

APPLICATIONS

- **Cell Phones**
- **PDAs**

KEY SPECIFICATIONS

- **P_{OUT}, BTL, 8Ω, 3.3V, 1%: 520 mW (typ)**
- **P_{OUT} H/P, 32Ω, 3.3V, 1%: 36 mW (typ)**
- **P_{OUT} Mono Earpiece, 32Ω, 1%: 55 mW (typ)**
- **Shutdown current: 0.6µA (typ)**
- **SNR (DAC + Amplifier): 85 dB (typ)**

DESCRIPTION

The LM4937 is an integrated audio sub-system designed for mono voice, stereo music cell phones connecting to base band processors with mono differential analog voice paths. Operating on a 3.3V supply, it combines a mono speaker amplifier delivering 520mW into an 8Ω load, a stereo headphone amplifier delivering 36mW per channel into a 32Ω load, and a mono earpiece amplifier delivering 55mW into a 32Ω load. It integrates the audio amplifiers, volume control, mixer, and power management control all into a single package. In addition, the LM4937 routes and mixes the single-ended stereo and differential mono inputs into multiple distinct output modes. The LM4937 features an I^2S serial interface for full range audio and an I^2C ™or SPI compatible interface for control. The full range music path features an SNR of 85dB with a 192kHz playback.

Boomer™ audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.

Block Diagram

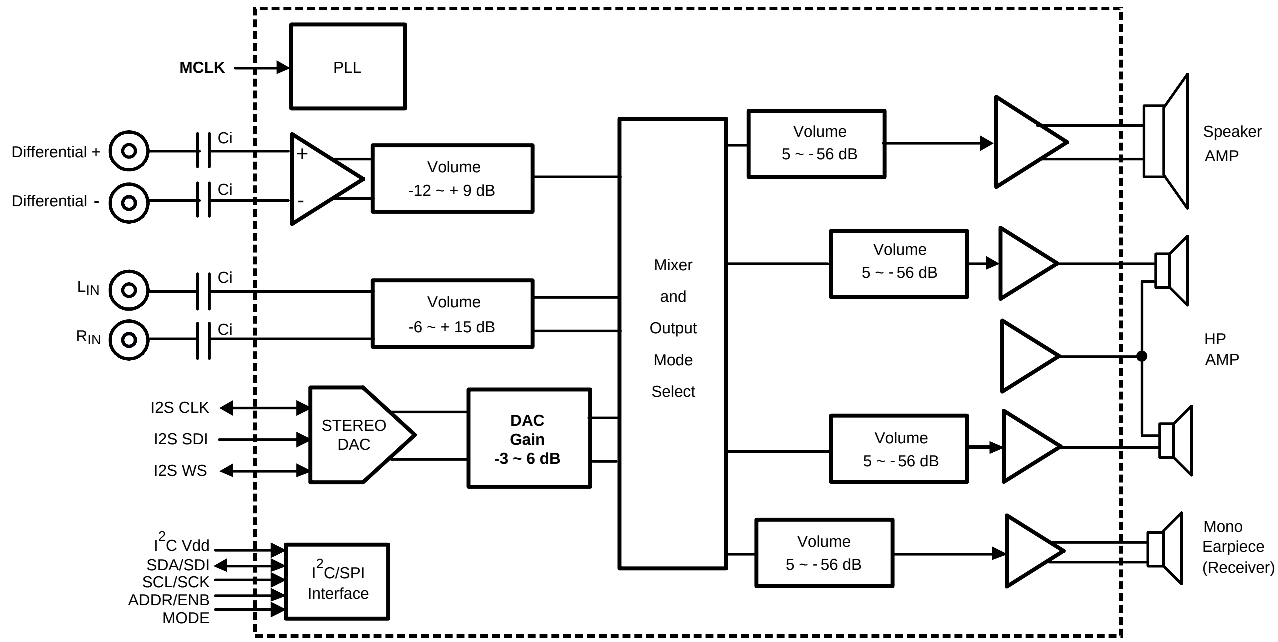

Figure 1. Audio Sub-System Block Diagram with OCL HP Outputs (HP outputs may also be configured as cap-coupled)

Connection Diagram

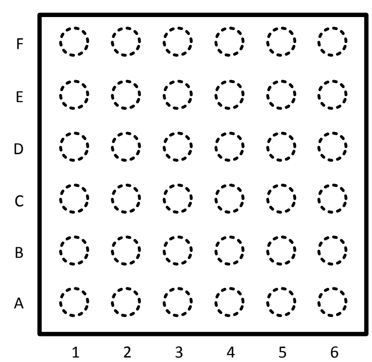

Figure 2. 36-Bump DSBGA Top View (Bump Side Down) See YPG0036 Package

PIN DESCRIPTIONS

Pin	Pin Name	Digital/Analog	I/O, Power	Description
A1	DGND	D	P	DIGITAL GND
A2	MCLK	D	I	MASTER CLOCK
A3	I2S_WS	D	I/O	I2S WORD SELECT
A4	SDA/SDI	D	I/O	I2C SDA OR SPI SDI
A5	DVDD	D	P	DIGITAL SUPPLY VOLTAGE
A6	VDD_IO	D	P	I/O SUPPLY VOLTAGE
B1	PLL_VDD	D	P	PLL SUPPLY VOLTAGE
B2	I2S_SDATA	D	I	I2S SERIAL DATA INPUT
B3	I2S_CLK	D	I/O	I2S CLOCK SIGNAL
B4	GPIO	D	O	TEST PIN (MUST BE LEFT FLOATING)
B5	I2C_VDD	D	P	I2C SUPPLY VOLTAGE
B6	SDL/SCK	D	I	I2C_SCL OR SPI_SCK
C1	PLL_GND	D	P	PLL GND
C2	PLL_OUT	D	O	PLL FILTER OUTPUT
C3	PLL_IN	D	I	PLL FILTER INPUT
C4	ADDR/ENB	D	I	I2C ADDRESS OR SPI ENB DEPENDING ON MODE
C5	BYPASS	A	I	HALF-SUPPLY BYPASS
C6	AVDD	A	P	ANALOG SUPPLY VOLTAGE
D1	AGND	A	P	ANALOG GND
D2	AGND	A	P	ANALOG GND
D3	NC			NO CONNECT
D4	MODE	D	I	SELECTS BETWEEN I2C OR SPI CONTROL
D5	RHP	A	O	RIGHT HEADPHONE OUTPUT
D6	CHP	A	O	HEADPHONE CENTER PIN OUTPUT (1/2 VDD or GND)
E1	DIFF_	A	I	ANALOG NEGATIVE DIFFERENTIAL INPUT
E2	LIN	A	I	ANALOG LEFT CHANNEL INPUT
E3	RIN	A	I	ANALOG RIGHT CHANNEL INPUT
E4	NC			NO CONNECT
E5	LHP	A	O	LEFT HEADPHONE OUTPUT
E6	AGND	A	P	ANALOG GND
F1	DIFF+	A	I	ANALOG POSITIVE DIFFERENTIAL INPUT
F2	EP_	A	O	MONO EARPIECE-
F3	EP+	A	O	MONO EARPIECE+
F4	LS-	A	O	LOUDSPEAKER OUT-
F5	AVDD	A	P	ANALOG SUPPLY VOLTAGE
F6	LS+	A	O	LOUD SPEAKER OUT+

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Analog Supply Voltage	6.0V
Digital Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to V_{DD} +0.3V
Power Dissipation(4)	Internally Limited
ESD Susceptibility(5)	2000V
ESD Susceptibility(6)	200V
Junction Temperature	150°C
Thermal Resistance: θ_{JA}	100°C/W
See AN-1279	

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} ,θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4937 typical application with V_{DD} = 3.3V, R_L = 8Ω stereo operation, the total power dissipation is TBDW. θ_{JA} = TBD°C/W.
(5) Human body model: 100pF discharged through a 1.5kΩ resistor.
(6) Machine model: 220pF - 240pF discharged through all pins.

OPERATING RATINGS

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	−40°C ≤ T_A ≤ +85°C
Supply Voltage	2.7V ≤ AV_{DD} ≤ 5.5V
	2.7V ≤ DV_{DD} ≤ 4.0V
	1.7V ≤ I^2CV_{DD} ≤ 4.0V
	1.7V ≤ VDD_IO ≤ 4.0V

AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS AV_{DD} = 3.0V, DV_{DD} = 3.0V(1)(2)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
I_{DD}	Supply Current	V_{IN} = 0, No Load All Amps On + DAC, OCL(6)	14	19	mA (max)
		Headphone Mode Only, OCL	4.6	6.25	mA (max)
		Mono Loudspeaker Mode Only(6)	7	11.5	mA (max)
		Mono Earpiece Speaker Mode Only D_6 = 0 (register 01h) D_6 = 1	3.7 3.3	5	mA (max) mA
		DAC Off, All Amps On (OCL)(6)	10	15.5	mA (max)
I_{SD}	Shutdown Current		0.6	2	μA (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Enabling mono bit (D_6 in Output Control Register 01h) will save 400μA (typ) from specified current.

AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS AV_{DD} = 3.0V, DV_{DD} = 3.0V(1)(2) (continued)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
P_O	Output Power	Speaker; THD = 1%; f = 1kHz, 8Ω BTL	420	370	mW (min)
		Headphone; THD = 1%; f = 1kHz, 32Ω SE	27	24	mW (min)
		Earpiece; THD = 1%; f = 1kHz, 32Ω BTL	45	40	mW (min)
$V_{FS\ DAC}$	Full Scale DAC Output		2.4		Vpp
THD+N	Total Harmonic Distortion	Speaker; P_O = 200mW; f = 1kHz, 8Ω BTL	0.04		%
		Headphone; P_O = 10mW; f = 1kHz, 32Ω SE	0.01		%
		Earpiece; P_O = 20mW; f = 1kHz, 32Ω BTL	0.04		%
V_{OS}	Offset Voltage	Speaker	10	55	mV (max)
		Earpiece	8	50	mV (max)
		Headphone (OCL)	8	40	mV (max)
ϵ_O	Output Noise	A = weighted; 0dB gain; See Table 1	Table 1		
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{ripple} = 200mV_{P-P} C_B = 2.2µF; See Table 2	Table 2		
Xtalk	Crosstalk	Headphone; P_O= 10mW f = 1kHz; OCL	–60		dB
T_{WU}	Wake-Up Time	C_B = 2.2µF, CD6 = 0	35		ms (max)
		C_B = 2.2µF, CD6 = 1	85		ms (max)
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{RMS} = 200mVpp	56		dB

AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS AV_{DD} = 5.0V, DV_{DD} = 3.3V(1)(2)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
I_{DD}	Supply Current	V_{IN} = 0, No Load All Amps On + DAC, OCL(6)	17.5		mA (max)
		Headphone Mode Only (OCL)	5.8		mA (max)
		Mono Loudspeaker Mode Only(6)	11.6		mA (max)
		Mono Earpiece Mode Only(6)	5		mA (max)
		DAC Off, All Amps On (OCL)(6)	12.9		mA (max)
I_{SD}	Shutdown Current		1.6		µA (max)
P_O	Output Power	Speaker; THD = 1%; f = 1kHz, 8Ω BTL	1.25		mW (min)
		Headphone; THD = 1%; f = 1kHz, 32Ω SE	80		mW (min)
		Earpiece; THD = 1%; f = 1kHz, 32Ω BTL	175		mW (min)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
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(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Enabling mono bit (D_6 in Output Control Register 01h) will save 400µA (typ) from specified current.

AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS AV_{DD} = 5.0V, DV_{DD} = 3.3V(1)(2) (continued)

The following specifications apply for the circuit shown in Figure 1 with all programmable gain set at 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
$V_{FS\ DAC}$	Full Scale DAC Output		2.4		Vpp
THD+N	Total Harmonic Distortion	Speaker; P_O = 500mW; f = 1kHz, 8Ω BTL	0.03		%
		Headphone; P_O = 30mW; f = 1kHz, 32Ω SE	0.01		%
		Earpiece; P_O = 40mW; f = 1kHz, 32Ω BTL; CD4 = 0	0.04		%
V_{OS}	Offset Voltage	Speaker	10		mV
		Earpiece	8		mV
		HP (OCL)	8		mV
ϵ_O	Output Noise	A = weighted; 0dB gain; See Table 1	Table 1		
PSRR	Power Supply Rejection Ratio	f = 217Hz; V_{ripple} = 200mV_{P-P} C_B = 2.2µF; See Table 3	Table 3		
Xtalk	Crosstalk	Headphone; P_O= 15mW f = 1kHz; OCL	–56		dB
T_{WU}	Wake-Up Time	C_B = 2.2µF, CD6 = 0	45		ms
		C_B = 2.2µF, CD6 = 1	130		ms

VOLUME CONTROL ELECTRICAL CHARACTERISTICS(1)(2)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
PGR	Stereo Analog Inputs PreAmp Gain Setting Range	minimum gain setting	–6	–7	dB (min)
				–5	dB (max)
		maximum gain setting	15	15.5	dB (max)
				14.5	dB (min)
	Differential Mono Analog Input PreAmp Gain Setting Range	minimum gain setting	–12	–13	dB (min)
				–11	dB (max)
		maximum gain setting	9	9.5	dB (max)
				8.5	dB (min)
VCR	Output Volume Control for Loudspeaker, Headphone Output, or Earpiece Output	minimum gain setting	–56	–59	dB (min)
				–53	dB (max)
		maximum gain setting	+5	4.5	dB (min)
				5.5	dB (max)
ΔA_{CH-CH}	Stereo Channel to Channel Gain Mismatch		0.3		dB
A_{MUTE}	Mute Attenuation	V_{in} = 1V_{rms}, Gain = 0dB with load			
		Headphone	<-90		dB (min)

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(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.

VOLUME CONTROL ELECTRICAL CHARACTERISTICS[(1)(2)] (continued)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937 Typical[(3)]	LM4937 Limits[(4)(5)]	Units (Limits)
R_{INPUT}	DIFF+, DIFF-, L_{IN} and R_{IN} Input Impedance		23	18	kΩ (min)
				28	kΩ (max)

DIGITAL SECTION ELECTRICAL CHARACTERISTICS[(1)(2)]

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937 Typical[(3)]	LM4937 Limits[(4)(5)]	Units (Limits)
DI_{SD}	Digital Shutdown Current	Mode 0, DV_{DD} = 3.0V			
		No MCLK	0.01		µA
DI_{DD}	Digital Power Supply Current	f_{MCLK} = 12MHz, DV_{DD} = 3.0V ALL MODES EXCEPT 0	5.3	6.5	mA (max)
$PLLI_{DD}$	PLL Quiescent Current	f_{MCLK} = 12MHz, DV_{DD} = 3.0V	4.8	6	mA (max)
Audio DAC (Typical numbers are with 6.144MHz audio clock and 48kHz sampling frequency					
R_{DAC}	Audio DAC Ripple	20Hz - 20kHz through headphone output	+/-0.1		dB
PB_{DAC}	Audio DAC Passband width	-3dB point	22.6		kHz
SBA_{DAC}	Audio DAC Stop band Attenuation	Above 24kHz	76		dB
DR_{DAC}	Audio DAC Dynamic Range	DC - 20kHz, –60dBFS; AES17 Standard See Table 4	Table 4		dB
SNR	Audio DAC-AMP Signal to Noise Ratio	A-Weighted, Signal = V_O at 0dBFS, f = 1kHz Noise = digital zero, A-weighted, See Table 4	Table 4		dB
SNR_{DAC}	Internal DAC SNR	A-weighted[(6)]	95		dB
PLL					
f_{IN}	Input Frequency on MCLK pin		12	10	MHz
				26	
SPI/I²C (1.7V ≤ I^2CV_{DD} ≤ 2.2V)					
f_{SPI}	Maximum SPI Frequency			1000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			250	ns (max)
$t_{SPISETENB}$	SPI ENB Setup Time			250	ns (max)
$t_{SPIHOLDD}$	SPI Data Hold Time			250	ns (max)
$t_{SPIHOLDENB}$	SPI ENB Hold Time			250	ns (max)
t_{SPICL}	SPI Clock Low Time			500	ns (max)
t_{SPICH}	SPI Clock High Time			500	ns (max)
f_{CLKI2C}	I²C_CLK Frequency			400	kHz (max)
$t_{I2CHOLD}$	I²C_DATA Hold Time			250	ns (max)
t_{I2CSET}	I²C_DATA Setup Time			250	ns (max)

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(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Internal DAC only with DAC modes 00 and 01.

DIGITAL SECTION ELECTRICAL CHARACTERISTICS(1)(2) (continued)

The following specifications apply for 3.0V ≤ AV_{DD} ≤ 5.0V and 2.7V ≤ DV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4937		Units (Limits)
			Typical(3)	Limits(4)(5)	
V_{IH}	I^2C/SPI Input High Voltage		I^2CV_{DD}	0.7 x I^2CV_{DD}	V (min)
V_{IL}	I^2C/SPI Input Low Voltage		0	0.25 x I^2CV_{DD}	V (max)
SPI/I^2C (2.2V ≤ I^2CV_{DD} ≤ 4.0V)					
f_{SPI}	Maximum SPI Frequency			4000	kHz (max)
$t_{SPISETD}$	SPI Data Setup Time			100	ns (max)
$t_{SPISETENB}$	SPI ENB Setup Time			100	ns (max)
$t_{SPIHOLDD}$	SPI Data Hold Time			100	ns (max)
$t_{SPIHOLENB}$	SPI ENB Hold Time			100	ns (max)
t_{SPICL}	SPI Clock Low Time			125	ns (max)
t_{SPICH}	SPI Clock High Time			125	ns (max)
f_{CLKI2C}	I^2C_CLK Frequency			400	kHz (max)
$t_{I2CHOLD}$	I^2C_DATA Hold Time			100	ns (max)
t_{I2CSET}	I^2C_DATA Setup Time			100	ns (max)
V_{IH}	I^2C/SPI Input High Voltage		I^2CV_{DD}	0.7 x I^2CV_{DD}	V (min)
V_{IL}	I^2C/SPI Input Low Voltage-		0	0.3 x I^2CV_{DD}	V (ax)
I^2S(1.7V ≤ VDD_IO ≤ 2.7V)					
f_{CLKI^2S}	I^2S_CLK Frequency	I^2S_RES = 1 I^2S_RES = 0	1536 3072	6144 12288	kHz (ax) kHz (max)
	I^2S_WS Duty Cycle		50	40 60	% %
V_{IH}	Digital Input High Voltage			0.75 x VDD_IO	V (min)
V_{IL}	Digital Input Low Voltage			0.25 x VDD_IO	V (max)
I^2S(2.7V ≤ VDD_IO ≤ 4.0V)					
f_{CLKI^2S}	I^2S_CLK Frequency	I^2S_RES = 0	1536 3072	6144 12288	kHz (max) kHz (max)
	I^2S_WS Duty Cycle	I^2S_RES = 1	50	40 60	% %
V_{IH}	Digital Input High Voltage			0.7 x VDD_IO	V (min)
V_{IL}	Digital Input Low Voltage			0.3x VDD_IO	V (max)

Table 1. Output Noise[1]

MODE	EP	LS	HP OCL	Units
1	22	22	8	μV
2	22	22	8	μV
3	22	22	8	μV
4	68	88	46	μV
5	38	48	24	μV
6	29	34	18	μV
7	38	48	24	μV

(1) Output Noise AV_{DD} = 5.0V and AV_{DD} = 3.0V. All gains set to 0dB. Units in μV. A - weighted

Table 2. PSRR AV_{DD} = 3.0V[1]

MODE	EP(Typ)	LS (Typ)	LS (Limit)	HP (Typ)	HP (Limit)	Units
1	69	76		72		dB
2	69	76	67	72	68	dB
3	69	76		72		dB
4	63	62		55		dB
5	69	68		61		dB
6	69	70		64		dB
7	69	68		61		dB

(1) PSRR AV_{DD} = 3.0V, f = 217Hz; V_{ripple} = 200mVp-p; C_B = 2.2μF.

Table 3. PSRR AV_{DD} = 5.0V[1]

MODE	EP (Typ)	LS (Typ)	HP (Typ)	Units
1	68	72	71	dB
2	68	72	71	dB
3	68	72	71	dB
4	68	66	69	dB
5	68	69	70	dB
6	69	72	71	dB
7	68	69	70	dB

(1) PSRR AV_{DD} = 5.0V. All gains set to 0dB. f = 217Hz; V_{ripple} = 200mVp-p; C_B = 2.2μF

Table 4. Dynamic Range and SNR[1]

	DR (Typ)	SNR (Typ)	Units
LS	95	85	dB
HP	95	85	dB
EP	97	85	dB

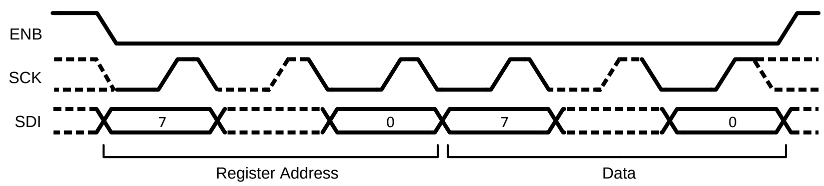
(1) Dynamic Range and SNR. 3.0V ≤ AV_{DD} ≤ 5.0V. All programmable gain set to 0dB. Units in dB.

SYSTEM CONTROL

The LM4937 is controlled via either a two wire I^{2}C compatible interface or three wire SPI interface, selectable with the MODE pin. This interface is used to configure the operating mode, interfaces, data converters, mixers and amplifiers. The LM4937 is controlled by writing 8 bit data into a series of write-only registers, the device is always a slave for both type of interfaces.

THREE WIRE, SPI INTERFACE (MODE = 1)

Three Wire Mode Write Bus Transaction



Three Wire Mode Write Bus Timing

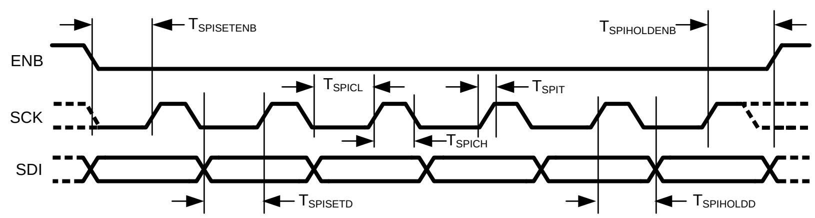


Figure 3. Three Wire Mode Write Bus

When the part is configured as an SPI device and the enable (ENB) line is lowered the serial data on SDI is clocked in on the rising edge of the SCK line. The protocol used is 16bit, MSB first. The upper 8 bits (15:8) are used to select an address within the device, the lower 8 bits (7:0) contain the updated data for this register.

TWO WIRE I^{2}C COMPATIBLE INTERFACE (MODE = 0)

Figure 4. Two Wire Mode Write Bus Transaction

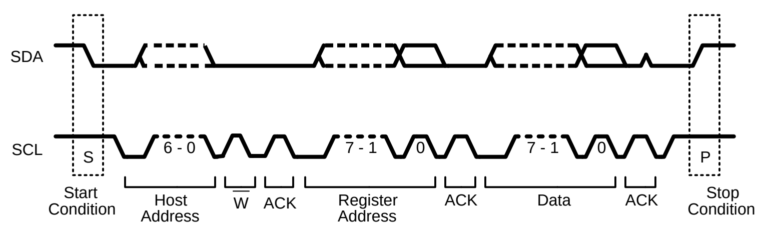


Figure 5. Two Wire Mode Write Bus Timing

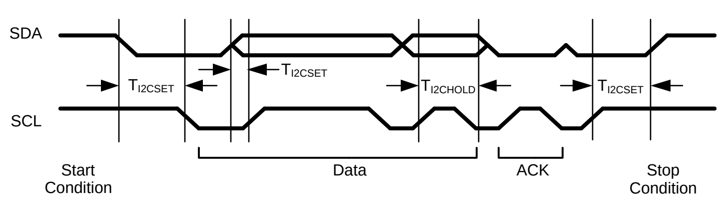


Figure 6. Two Wire Mode Write Bus

When the part is configured as an I^{2}C device then the LM4937 will respond to one of two addresses, according to the ADDR input. If ADDR is low then the address portion of the I^{2}C transaction should be set to write to 0010000. When ADDR is high then the address input should be set to write to 1110000.

Table 5. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	0	EC(1)	EC(1)	1	0	0	0	0
ADR = 0	0	0	0	1	0	0	0	0
ADR = 1	0	1	1	1	0	0	0	0

(1) EC — Externally configured by ADR pin

Table 6. Control Registers(1)

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00h	Mode Control	0	CD_6	0	OCL	CD_3	CD_2	CD_1	CD_0
01h	Output Control	0	D_6	0	0	HP_R_ OUTPUT	HP_L_ OUTPUT	LS_ OUTPUT	MONO_ OUTPUT
02h	Mono Volume Control	0	0	0	EP_VOL_4	EP_VOL_3	EP_VOL_2	EP_VOL_1	EP_VOL_0
03h	Loud Speaker Volume Control	0	0	0	LS_VOL_4	LS_VOL_3	LS_VOL_2	LS_VOL_1	LS_VOL_0
04h	RESERVED	0	0	0	0	0	0	0	0
05h	Headphone Left Volume Control	0	0	0	HP_L_VOL_4	HP_L_VOL_3	HP_L_VOL_2	HP_L_VOL_1	HP_L_VOL_0
06h	Headphone Right Volume Control	0	0	0	HP_R_VOL_4	HP_R_VOL_3	HP_R_VOL_2	HP_R_VOL_1	HP_R_VOL_0
07h	Analog R & L Input Gain Control	0	0	ANA_R_ GAIN_2	ANA_R_ GAIN_1	ANA_R_ GAIN_0	ANA_L_ GAIN_2	ANA_L _GAIN_1	ANA_L _GAIN_0
08h	Analog Mono & DAC Input Gain Control	0	DIG_R_ GAIN_1	DIG_R_ GAIN_0	DIG_L_ GAIN_1	DIG_L_ GAIN_0	MONO_IN_ GAIN_2	MONO_IN_ GAIN_1	MONO_IN_ GAIN_0
09h	Clock Configu ration	R_DIV_3	R_DIV_2	R_DIV_1	R_DIV_0	PLL_ ENABLE	AUDIO _CLK_SEL	PLL_INPUT	FAST_ CLOCK
0Ah	PLL M Divider	0	PLL_M_6	PLL_M_5	PLL_M_4	PLL_M_3	PLL_M_2	PLL_M_1	PLL_M_0
0Bh	PLL N Divider	PLL_N_7	PLL_N_6	PLL_N_5	PLL_N_4	PLL_N_3	PLL_N_2	PLL_N_1	PLL_N_0
0Ch	PLL N_MOD Divider and Dither Level	VCO_FAST	PLL_DITH_LEV_1	PLL_DITH_LEV_0	PLL_N_MOD_4	PLL_N_MOD_3	PLL_N_MOD_2	PLL_N_MOD_1	PLL_N_MOD_0
0Dh	PLL_P Divider	0	0	0	0	PLL_P_3	PLL_P_2	PLL_P_1	PLL_P_0
0Eh	DAC Setup	0	CUST_COMP	DITHER_ALW_ON	DITHER_OFF	MUTE_R	MUTE_L	DAC_MODE_1	DAC_MODE_0
0Fh	Interface	0	0	0	0	I2C_FAST	I2S_MODE	I2S_RESOL	I2S_M/S
10h	COMPENSATION _C OEFF0_LSB	COMP0_7	COMP0_6	COMP0_5	COMP0_4	COMP0_3	COMP0_2	COMP0_1	COMP0_0
11h	COMPENSATION _C OEFF0_MSB	COMP0_15	COMP0_14	COMP0_13	COMP0_12	COMP0_11	COMP0_10	COMP0_9	COMP0_8
12h	COMPENSATION _C OEFF1_LSB	COMP1_7	COMP1_6	COMP1_5	COMP1_4	COMP1_3	COMP1_2	COMP1_1	COMP1_0
13h	COMPENSATION _C OEFF1_MSB	COMP1_15	COMP1_14	COMP1_13	COMP1_12	COMP1_11	COMP1_10	COMP1_9	COMP1_8
14h	COMPENSATION _C OEFF2_LSB	COMP2_7	COMP2_6	COMP2_5	COMP2_4	COMP2_3	COMP2_2	COMP2_1	COMP2_0
15h	COMPENSATION _C OEFF2_MSB	COMP2_15	COMP2_14	COMP2_13	COMP2_12	COMP2_11	COMP2_10	COMP2_9	COMP2_8
16h	TEST_ REGISTER	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

(1) Note: All registers default to 0 on initial power-up.

SYSTEM CONTROLS

Table 7. Loudspeaker, Earpiece, HP Left or Right Volume Control

EP_VOL_4, LS_VOL_4, HP_L_VOL_4, HP_R_VOL_4	EP_VOL_3, LS_VOL_3, HP_L_VOL_3, HP_R_VOL_3	EP_VOL_2, LS_VOL_2, HP_L_VOL_2, HP_R_VOL_2	EP_VOL_1, LS_VOL_1, HP_L_VOL_1, HP_R_VOL_1	EP_VOL_0, LS_VOL_0, HP_L_VOL_0, HP_R_VOL_0	Gain (dB)
0	0	0	0	0	<–90 (MUTE)
0	0	0	0	1	–56
0	0	0	1	0	–52
0	0	0	1	1	–48
0	0	1	0	0	–45
0	0	1	0	1	–42
0	0	1	1	0	–39
0	0	1	1	1	–36
0	1	0	0	0	–33
0	1	0	0	1	–30
0	1	0	1	0	–28
0	1	0	1	1	–26
0	1	1	0	0	–24
0	1	1	0	1	–22
0	1	1	1	0	–20
0	1	1	1	1	–18
1	0	0	0	0	–16
1	0	0	0	1	–14
1	0	0	1	0	–12
1	0	0	1	1	–10
1	0	1	0	0	–8
1	0	1	0	1	–6
1	0	1	1	0	–4
1	0	1	1	1	–3
1	1	0	0	0	–2
1	1	0	0	1	–1
1	1	0	1	0	0
1	1	0	1	1	+1
1	1	1	0	0	+2
1	1	1	0	1	+3
1	1	1	1	0	+4
1	1	1	1	1	+5

Table 8. Mixer Code Control(1)

Mode	CD3	CD2	CD1	CD0	Mono Earpiece	Loudspeaker	Headphone L	Headphone R
0	0	0	0	0	SD	SD	SD	SD
1	1	0	0	1	M	M	M	M
2	1	0	1	0	AL+AR	AL+AR	AL	AR
3	1	0	1	1	M+AL+AR	M+AL+AR	M+AL	M+AR

(1) SD — Shutdown, M — Mono Differential Input
AL — Analog Left Channel, AR — Analog Right Channel
DL — I2S DAC Left Channel, DR — I2S DAC Right Channel, MUTE — Mute
Note: Power-On Default Mode is Mode 0

Table 8. Mixer Code Control[(1)] (continued)

4	1	1	0	0	DL+DR	DL+DR	DL	DR
5	1	1	0	1	DL+DR+ AL+AR	DL+AL AL+AR	DL+AL	DR+AR
6	1	1	1	0	M+DL+AL+ DR+AR	M+DL+AL+ DR+AR	M+DL+AL	M+DR+AR
7	1	1	1	1	M+DL+DR	M+DL+DR	M+DL	M+DR

Table 9. Output Control (01h)

Loudspeaker	LS_OUTPUT = 1	LS_OUTPUT = 0	
	Output On	Output Off	
Headphone Left Channel	HP_L_OUTPUT = 1	HP_L_OUTPUT = 0	
	Output On	Output Off (OCL = 0)	Output Mute (OCL = 1)
Headphone Right Channel	HP_R_OUTPUT = 1	HP_R_OUTPUT = 0	
	Output On	Output Off (OCL = 0)	Output Mute (OCL = 1)
Earpiece	EP_OUTPUT = 1	EP_OUTPUT = 0	
	Output On	Output Off	
All Outputs	CD3 = 1	CD3 = 0	
	Outputs Toggled Via Register Control	All Outputs Off	

Table 10. Mono Differential Amplifier Input Gain Select (08h)

MONO_IN_GAIN_2	MONO_IN_GAIN_1	MONO_IN_GAIN_0	Input Gain Setting
0	0	0	–12dB
0	0	1	–9dB
0	1	0	–6dB
0	1	1	–3dB
1	0	0	0dB
1	0	1	3dB
1	1	0	6dB
1	1	1	9dB

Table 11. Analog Single-Ended Input Amplifier Gain Select (07h)

ANA_L_GAIN_2 ANA_R_GAIN_2	ANA_L_GAIN_1 ANA_R_GAIN_1	ANA_L_GAIN_0 ANA_R_GAIN_0	Input Gain Setting
0	0	0	–6dB
0	0	1	–3dB
0	1	0	0dB
0	1	1	3dB
1	0	0	6dB
1	0	1	9dB
1	1	0	12dB
1	1	1	15dB

Table 12. DAC Gain Select (08h)

DIG_L_GAIN_1 DIG_R_GAIN_1	DIG_L_GAIN_0 DIG_R_GAIN_0	Input Gain Setting
0	0	–3dB
0	1	0dB
1	0	3dB
1	1	6dB

PLL CONFIGURATION REGISTERS

PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input divider of the PLL.

Table 13. PLL_M (0Ah) (Set = logic 1, Clear = logic 0)(1)

Bits	Register	Description	
6:0	PLL_M	Programs the PLL input divider to select:	
		PLL_M	Divide Ratio
		0	Divider Off
		1	1
		2	1.5
		3	2
		4	2.5
		...	3→
		126	63.5

(1) NOTES:
The M divider should be set such that the output of the divider is between 0.5 and 5MHz. See the PLL setup section for details.
The division of the M divider is derived from PLL_M as such:
M = (PLL_M+1) / 2

PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control PLL N divider.

Table 14. PLL_N (0Bh) (Set = logic 1, Clear = logic 0)(1)

Bits	Register	Description	
7:0	PLL_N	Programs the PLL feedback divider:	
		PLL_N	Divide Ratio
		0	Divider Off
		1 → 10	10
		11	11
		12	12
		...	...
		248	248
		249	249

(1) NOTES:
The N divider should be set such that the output of the divider is between 0.5 and 5MHz. See the PLL setup section for details. The N divider should never be set so that (Fin/M) * N > 55MHz (or 80MHz if FAST_VCO is set in the PLL_N_MOD register).
The non-sigma-delta division of the N divider is derived from the PLL_N as such:
N = PLL_N
Fin /M is often referred to as F_{comp} (Frequency of Comparison) or F_{ref} (Reference Frequency). In this document, F_{comp} is used.

PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the PLL's P divider.

Table 15. PLL_P (0Dh) (Set = logic 1, Clear = logic 0)(1)

Bits	Register	Description	
3:0	**PLL_P**	**Programs the PLL input divider to select:**	
		0	Divider Off
		1	1
		2	1.5
		3	2
		...	–> 2.5
		13	7
		14	7.5
		15	8

(1) NOTES:
The output of this divider should be either 12 or 24MHz in USB mode or 11.2896MHz, 12.288MHz or 24.576MHz in non-USB modes.
The division of the P divider is derived from PLL_P as such:
P = (PLL_P+1) / 2

PLL N MODULATOR AND DITHER SELECT CONFIGURATION REGISTER

This register is used to control the Fractional component of the PLL.

Table 16. PLL_N_MOD (0Ch) (Set = logic 1, Clear = logic 0)(1)

Bits	Register	Description	
4:0	PLL_N_MOD	This programs the PLL N Modulator's fractional component:	
		PLL_N_MOD	Fractional Addition
		0	0/32
		1	1/32
		2 → 30	2/32 → 30/32
6:5	DITHER_LEVEL	Allows control over the dither used by the N Modulator	
		DITHER_LEVEL	DAC Sub-system Input Source
		00	Medium (32)
		01	Small (16)
		10	Large (48)
7	FAST_VCO	If set the VCO maximum and minimum frequencies are raised:	
		FAST_VCO	Maximum F_{VCO}
		0	40–55MHz

(1) NOTES:
The complete N divider is a fractional divider as such:
N = PLL_N + (PLL_N_MOD/32)
If the modulus input is zero, then the N divider is simply an integer N divider. The output from the PLL is determined by the following formula:
Fout = (Fin * N) / (M * P)
Please see over for more details on the PLL and common settings.

Further Notes on PLL Programming

The sigma-delta PLL is designed to drive audio circuits requiring accurate clock frequencies of up to 25MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48kHz and 44.1kHz sample rates from any common clock source when the oversampling rate of the audio system is 125fs. In systems where 128x oversampling must be used (for example with an isochronous I2S data stream) a clock synchronous to the sample rate should be used as input to the PLL (typically the I2S clock). If no isochronous source is available then the PLL can be used to obtain a clock that is accurate to within typical crystal tolerances of the real sample rate.

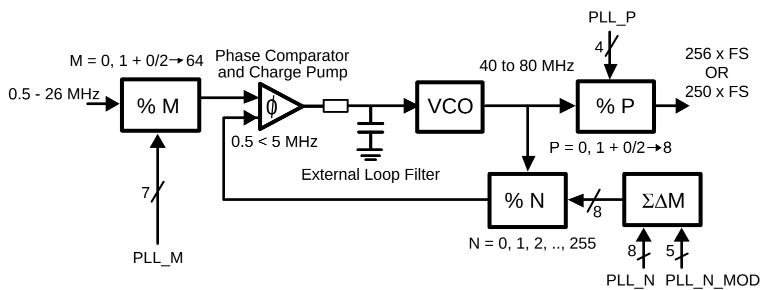


Table 17. Example Of PLL Settings For 48Khz Sample Rates

f_in (MHz)	fsamp (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	f_out (MHz)
11	48	11	60	5	21	60	0	9	12
12	48	5	25	5	9	25	0	9	12
12.288	48	4	19.53125	5	7	19	17	9	12
13	48	13	60	5	25	60	0	9	12

Table 17. Example Of PLL Settings For 48Khz Sample Rates (continued)

f_in (MHz)	fsamp (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	f_out (MHz)
14.4	48	9	37.5	5	17	37	16	9	12
16.2	48	27	100	5	53	100	0	9	12
16.8	48	14	50	5	27	50	0	9	12
19.2	48	13	40.625	5	25	40	20	9	12
19.44	48	27	100	6	53	100	0	11	12
19.68	48	20.5	62.5	5	40	62	16	9	12
19.8	48	16.5	50	5	32	50	0	9	12

Table 18. Example PLL Settings For 44.1Khz Sample Rates

f_in (MHz)	fsamp (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	f_out (MHz)
11	44.1	11	55.125	5	21	55	4	9	11.025000
11.2896	44.1	8	39.0625	5	15	39	2	9	11.025000
12	44.1	5	22.96875	5	9	22	31	9	11.025000
13	44.1	13	55.125	5	25	55	4	9	11.025000
14.4	44.1	12	45.9375	5	23	45	30	9	11.025000
16.2	44.1	9	30.625	5	17	30	20	9	11.025000
16.8	44.1	17	55.78125	5	33	55	25	9	11.025000
19.2	44.1	16	45.9375	5	31	45	30	9	11.025000
19.44	44.1	13.5	38.28125	5	26	38	9	9	11.025000
19.68	44.1	20.5	45.9375	4	40	45	30	7	11.025000
19.8	44.1	11	30.625	5	21	30	20	9	11.025000

These tables cover the most common applications, obtaining clocks for sample rates such as 22.05kHz and 192kHz should be done by changing the P divider value or the R divider in the clock configuration diagram.

If the user needs to obtain a clock unrelated to those described above, the following method is advised. An example of obtaining 11.2896 from 12.000MHz is shown below.

Choose a small range of P so that the VCO frequency is swept between 45 and 55MHz (or 60-80MHz if VCOFAST is used). Remembering that the P divider can divide by half integers. So for P = 4.0 → 7.0 sweep the M inputs from 2.5 → 24. The most accurate N and N_MOD can be calculated by:

N = FLOOR(((Fout/Fin)*(P*M)),1) (1)

N_MOD = ROUND(32*((((Fout)/Fin)*(P*M)-N),0) (2)

This shows that setting M = 11.5, N = 75 N_MOD = 47 P = 7 gives a comparison frequency of just over 1MHz, a VCO frequency of just under 80MHz (so VCO_FAST must be set) and an output frequency of 11.289596 which gives a sample rate of 44.099985443kHz, or accurate to 0.33 ppm.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used in the above mode. The I2S should be master on the LM4937 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

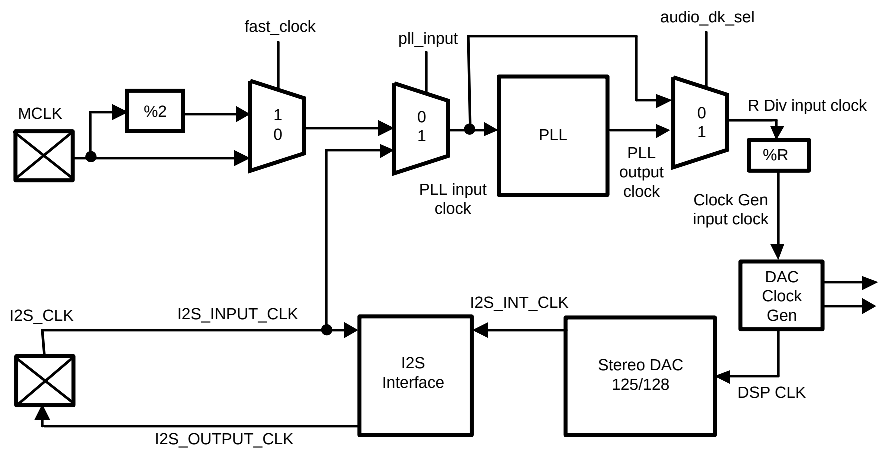
Where a system clock exists at an integer multiple of the required DAC clock rate it is preferable to use this rather than the PLL. The LM4937 is designed to work in 8,12,16,24,32, and 48kHz modes from a 12MHz clock without the use of the PLL. This saves power and reduces clock jitter.

CLOCK CONFIGURATION REGISTER

This register is used to control the multiplexers and clock R divider in the clock module.

Table 19. CLOCK (09h) (Set = logic 1, Clear = logic 0)

Bits	Register	Description	
0	FAST_CLOCK	If set master clock is divided by two.	
		FAST_CLOCK	MCLK Frequency
		0	Normal
		1	Divided by 2
1	PLL_INPUT	Programs the PLL input multiplexer to select:	
		PLL_INPUT	PLL Input Source
		0	MCLK
		1	I^2S Input Clock
2	AUDIO_CLK_SEL	Selects which clock is passed to the audio sub-system	
		DAC_CLK_SEL	DAC Sub-system Input Source
		0	PLL Input
		1	PLL Output
3	PLL_ENABLE	If set enables the PLL. (MODES 4–7 only)	
7:4	R_DIV	Programs the R divider	
		R_DIV	Divide Value
		0000	1
		0001	1
		0010	1.5
		0011	2
		0100	2.5
		0101	3
		0110	3.5
		0111	4
		1000	4.5
		1001	5
		1010	5.5
		1011	6
		1100	6.5
		1101	7
		1110	7.5
		1111	8



By default the stereo DAC operates at 250*fs, i.e. 12.000MHz (at the clock generator input clock) for 48kHz data. It is expected that the PLL be used to drive the audio system unless a 12.000MHz master clock is supplied. The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL.

Common Clock Settings for the DAC

The DAC can work in 4 modes, each with different oversampling rates, 125,128,64 & 32. In normal operation 125x oversampling provides for the simplest clocking solution as it will work from 12.000MHz (common in most systems with Bluetooth or USB) at 48kHz exactly. The other modes are useful if data is being provided to the DAC from an uncontrollable isochronous source (such as a CD player, DAB, or other external digital source) rather than being decoded from memory. In this case the PLL can be used to derive a clock for the DAC from the I2S clock.

The DAC oversampling rate can be changed to allow simpler clocking strategies, this is controlled in the DAC SETUP register but the oversampling rates are as follows:

DAC MODE	Over sampling Ratio Used
00	125
01	128
10	64
11	32

The following table describes the clock required at the clock generator input for various clock sample rates in the different DAC modes:

Fs (kHz)	DAC Oversampling Ratio	Required CLock at DAC Clock Generator Input (MHz)
8	125	2
8	128	2.048
11.025	125	2.75625
11.025	128	2.8224
12	125	3
12	128	3.072
16	125	4
16	128	4.096

Fs (kHz)	DAC Oversampling Ratio	Required CLock at DAC Clock Generator Input (MHz)
22.05	125	5.5125
22.05	128	5.6448
24	125	6
24	128	6.144
32	125	8
32	128	8.192
44.1	125	11.025
44.1	128	11.2896
48	125	12
48	128	12.288
88.2	64	11.2896
96	64	12.288
176.4	32	22.5792
192	32	24.576

Methods for producing these clock frequencies are described in the PLL CONFIGURATION REGISTERS section.

The R divider can be used when the master clock is exactly 12.00 MHz in order to generate different sample rates. The Table below shows different sample rates supported from 12.00MHz by using only the R divider and disabling the PLL. In this way we can save power and the clock jitter will be low.

R_DIV	Divide Value	DAC Clock Generator Input Frequency <MHz>	Sample Rate Supported <KHz>
11	6	2	8
9	5	2.4	9.6
7	4	3	12
5	3	4	16
4	2.5	4.8	19.2
3	2	6	24
2	1.5	8	32
0	1	12	48

The R divider can also be used along with the P divider in order to create the clock needed to support low sample rates.

DAC SETUP REGISTER

This register is used to configure the basic operation of the stereo DAC.

Table 20. DAC_SETUP (0Eh) (Set = logic 1, Clear = logic 0)

<table>
<tr><th>Bits</th><th>Register</th><th colspan="4">Description</th></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">DAC_MODE</td><td colspan="4">The DAC used in the LM4937 can operate in one of 4 oversampling modes.
The modes are described as follows:</td></tr>
<tr><td>DAC_MODE</td><td>Oversampling Rate</td><td>Typical FS</td><td>Clock Required</td></tr>
<tr><td>00</td><td>125</td><td>48KHz</td><td>12.000MHz (USB Mode)</td></tr>
<tr><td>01</td><td>128</td><td>44.1KHz
48KHz</td><td>11.2896MHz
12.288MHz</td></tr>
<tr><td>10</td><td>64</td><td>96KHz</td><td>12.288MHz</td></tr>
<tr><td>11</td><td>32</td><td>192KHz</td><td>24.576MHz</td></tr>
<tr><td>2</td><td>MUTE_L</td><td colspan="4">Mutes the left DAC channel on the next zero crossing.</td></tr>
<tr><td>3</td><td>MUTE_R</td><td colspan="4">Mutes the right DAC channel on the next zero crossing.</td></tr>
</table>

Table 20. DAC_SETUP (0Eh) (Set = logic 1, Clear = logic 0) (continued)

Bits	Register	Description
4	DITHER_OFF	If set the dither in DAC is disabled.
5	DITHER ALWAYS_ON	If set the dither in DAC is enabled all the time.
6	CUST_COMP	If set the DAC frequency response can be programmed manually via a 5 tap FIR “compensation” filter. This can be used to enhance the frequency response of small loudspeakers or provide a crude tone control. The compensation Coefficients can be set by using registers 10h to 15h.

INTERFACE CONTROL REGISTER

This register is used to control the I2S and I^2C compatible interface on the chip.

Table 21. INTERFACE (0Fh) (Set = logic 1, Clear = logic 0)(1)

Bits	Register	Description
0	I2S_MASTER_SLAVE	If set the LM4937 acts as a master for I2S, so both I2S clock and I2S word select are configured as outputs. If cleared the LM4937 acts as a slave where both I2S clock and word select are configured as inputs.
1	I2S_RESOLUTION	If set the I2S resolution is set to 32 bits. If clear, resolution is set to 16 bits. This bit only affects the I2S Interface in master mode. In slave mode the I2S Interface can support any I2S compatible resolution. In master mode the I2S resolution also depends on the DAC mode as the note below explains.
2	I2S_MODE	If set the I2S is configured in left justified mode timing. If clear, the I2S interface is configured in normal I2S mode timing.
3	I2C_FAST	If set enables the I2C to run in fast mode with an I2C clock up to 3.4MHz. If clear the I2C speed gets its default value of a maximum of 400kHz

(1) NOTES:
The master I2S format depends on the DAC mode. In USB mode the number of bits per word is 25 (i.e. 2.4MHz for a 48kHz sample rate). The duty cycle is 40/60. In non-USB modes the format is 32 or 16 bits per word, depending on I2S_RESOLTION and the duty cycle is always 50-50. In slave mode it will decode any I2S compatible data stream.

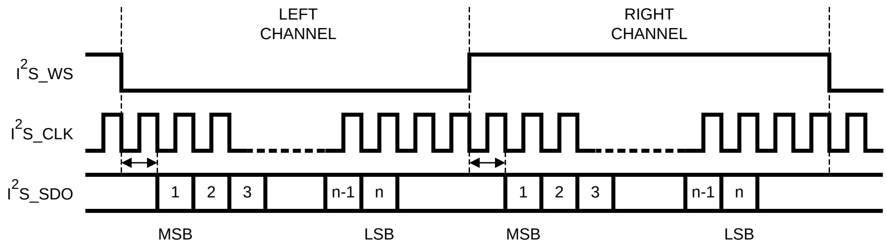


Figure 7. I2S Mode Timing

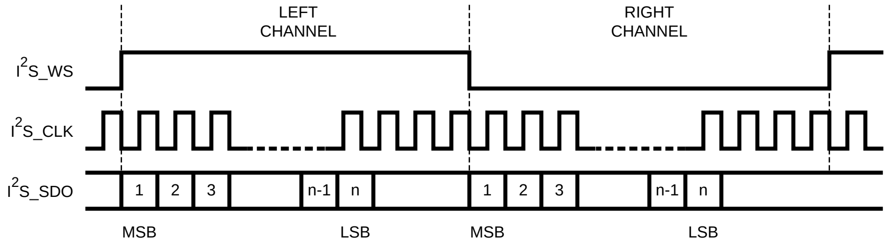


Figure 8. Left Justified Mode Timing

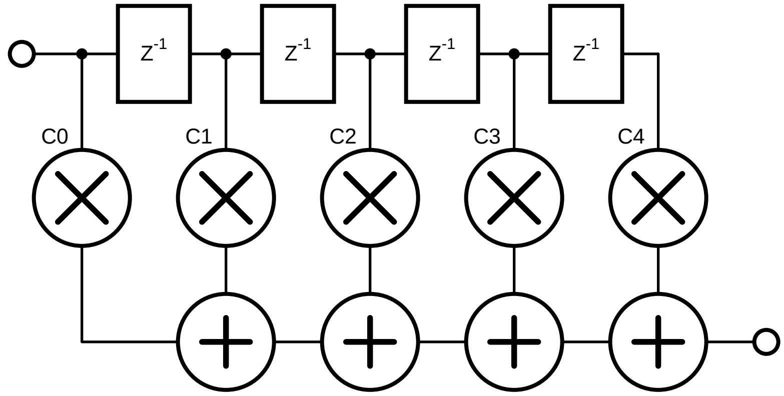
FIR Compensation Filter Configuration Registers

These registers are used to configure the DAC's FIR compensation filter. Three 16 bit coefficients are required and must be programmed via the I2C/SPI Interface in bytes as follows:

Table 22. COMP_COEFF (10h → 15h) (Set = logic 1, Clear = logic 0)(1)

Address	Register	Description
10h	COMP_COEFF0_LSB	Bits [7:0] of the 1st and 5th FIR tap (C0 and C4)
11h	COMP_COEFF0_MSB	Bits [15:8] of the 1st and 5th FIR tap (C0 and C4)
12h	COMP_COEFF1_LSB	Bits [7:0] of the 2nd and 4th FIR tap (C1 and C3)
13h	COMP_COEFF1_MSB	Bits [15:8] of the 2nd and 4th FIR tap (C1 and C3)
14h	COMP_COEFF2_LSB	Bits [7:0] of the 3rd FIR tap (C2)
15h	COMP_COEFF2_MSB	Bits [15:8] of the 3rd FIR tap (C2)

(1) NOTES:
The filter must be phase linear to ensure the data keeps the correct stereo imaging so the second half of the FIR filter must be the reverse of the 1st half.



If the CUST_COMP option in register 0Eh is not set the FIR filter will use its default values for a linear response from the DAC into the analog mixer, these values are:

DAC_OSR	C0, C4	C1, C3	C2
00	434	–2291	26984
01, 10, 11	61	–371	25699

If using 96 or 192kHz data then the custom compensation may be required to obtain flat frequency responses above 24kHz. The total power of any custom filter must not exceed that of the above examples or the filters within the DAC will clip. The coefficient must be programmed in 2's complement.

TYPICAL PERFORMANCE CHARACTERISTICS

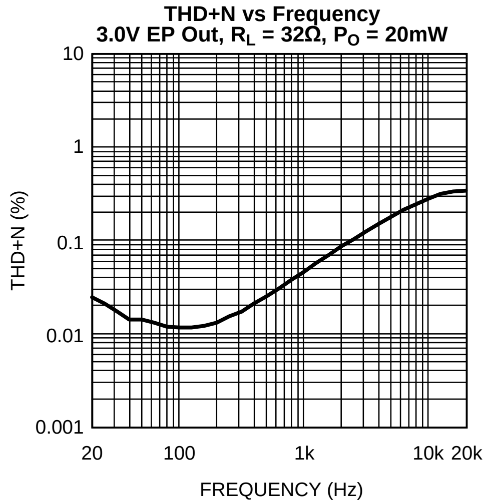


Figure 9.

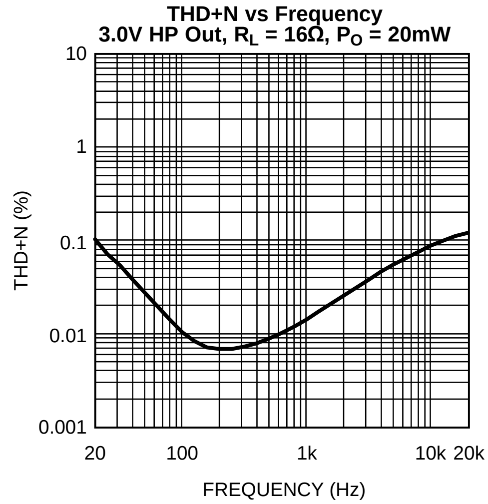


Figure 10.

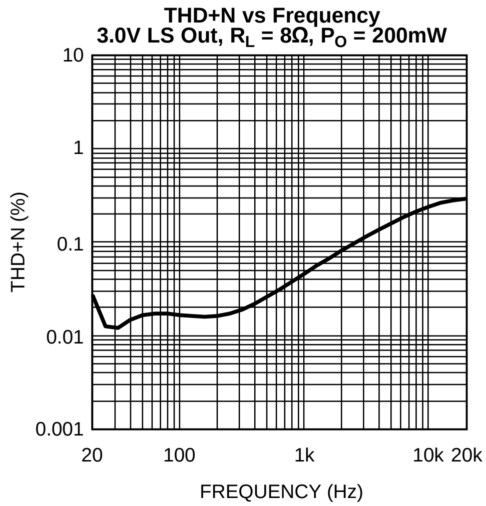


Figure 11.

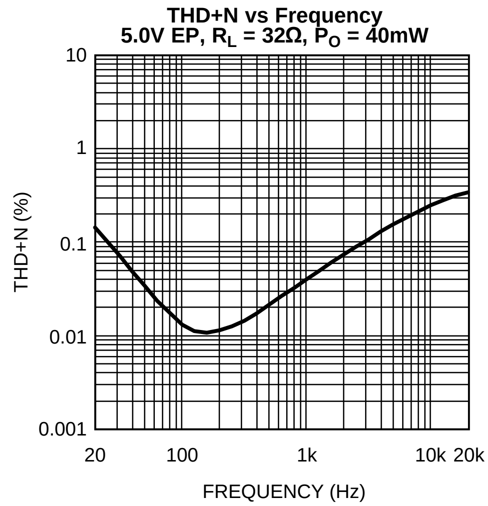


Figure 12.

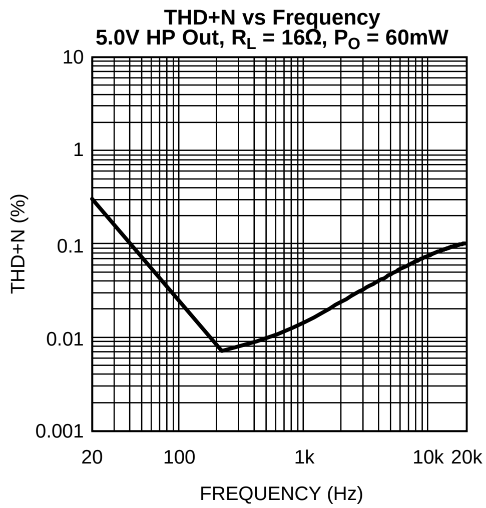


Figure 13.

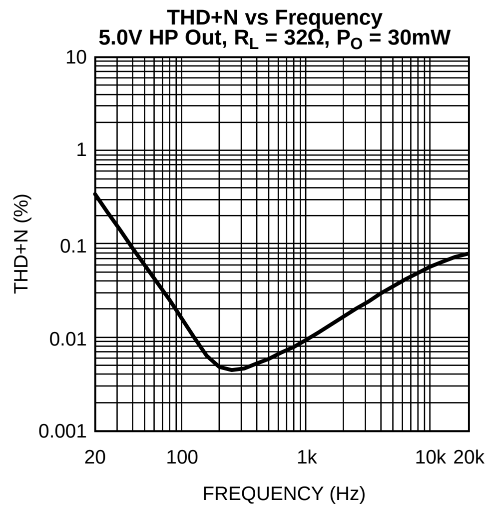


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

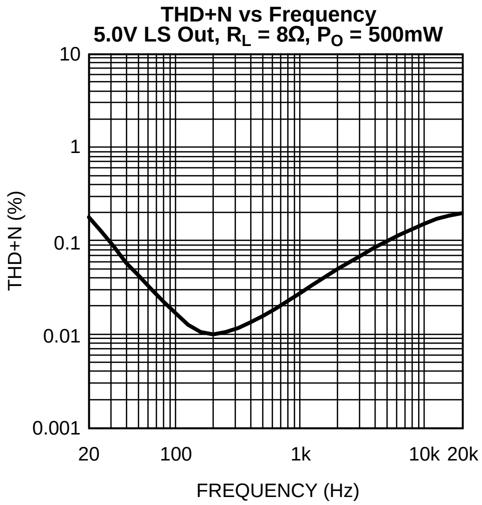


Figure 15.

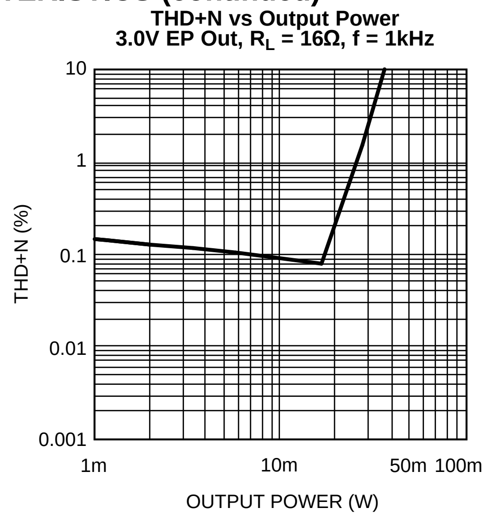


Figure 16.

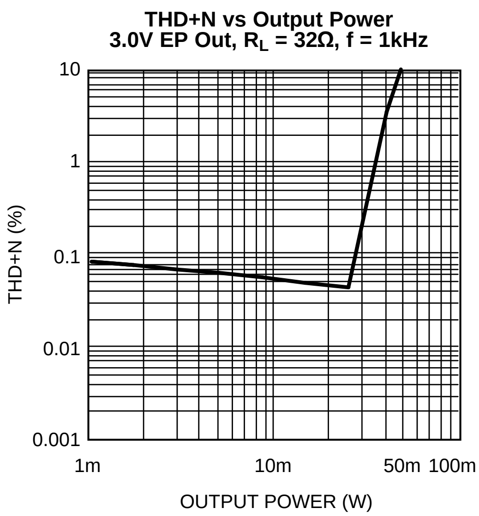


Figure 17.

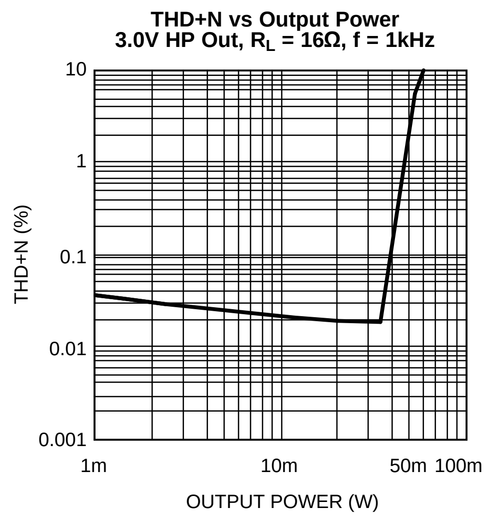


Figure 18.

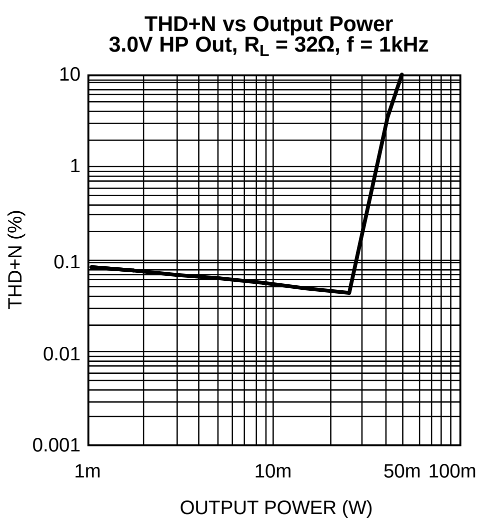


Figure 19.

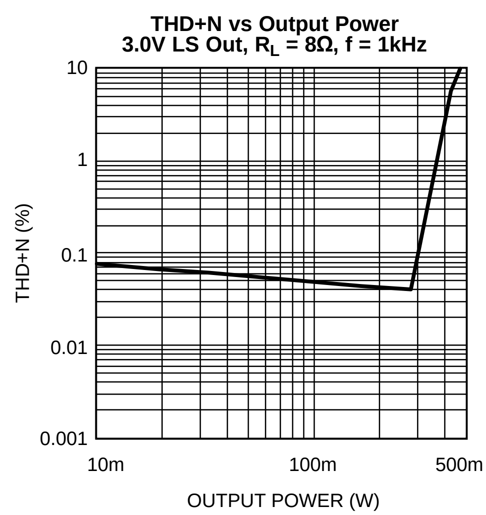


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Output Power
5.0V EP Out, R_L = 16Ω, f = 1kHz

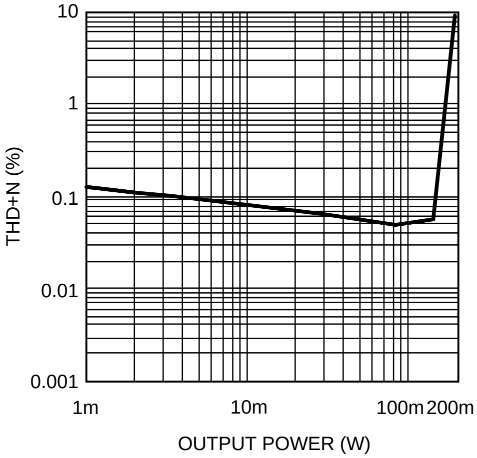


Figure 21.

THD+N vs Output Power
5.0V EP Out, R_L = 32Ω, f = 1kHz

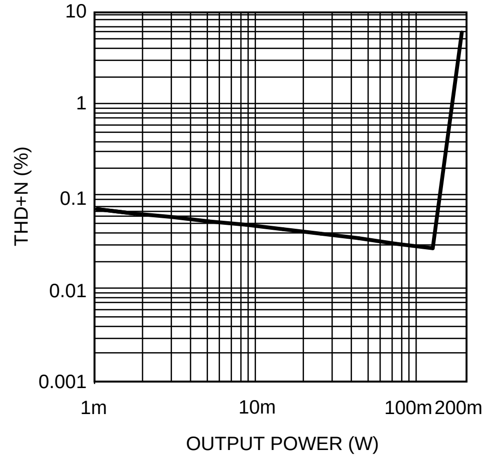


Figure 22.

THD+N vs Output Power
5.0V HP Out, R_L = 16Ω, f = 1kHz

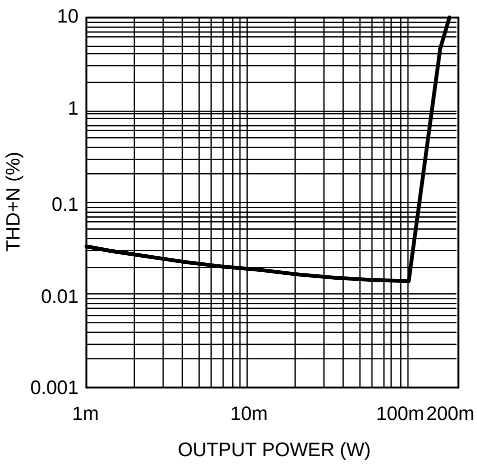


Figure 23.

THD+N vs Output Power
5.0V HP Out, R_L = 32Ω, f = 1kHz

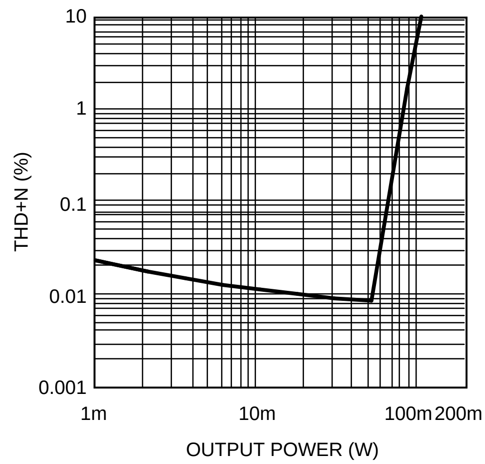


Figure 24.

THD+N vs Output Power
5.0V LS Out, R_L = 8Ω, f = 1kHz

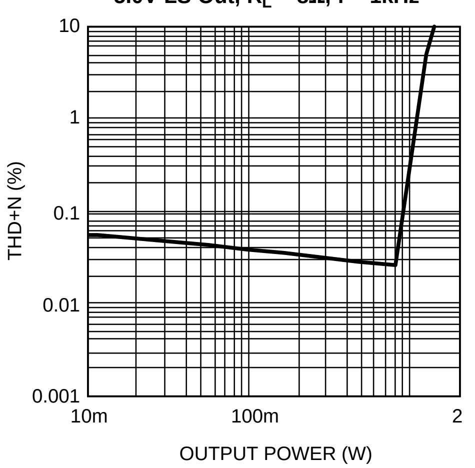


Figure 25.

THD+N vs I2S Level
EP Out

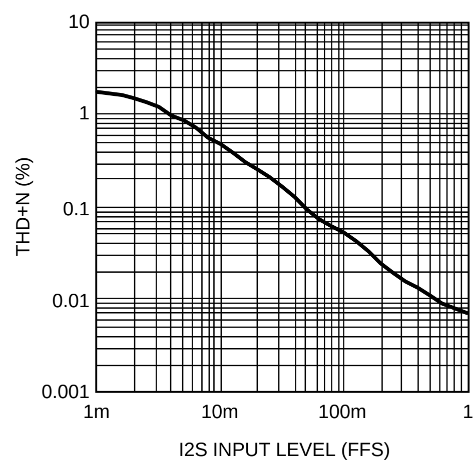


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs I2S Level
HP Out

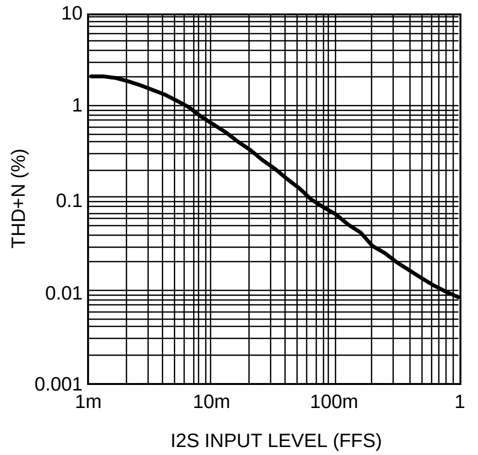


Figure 27.

THD+N vs I2S Level
LS Out

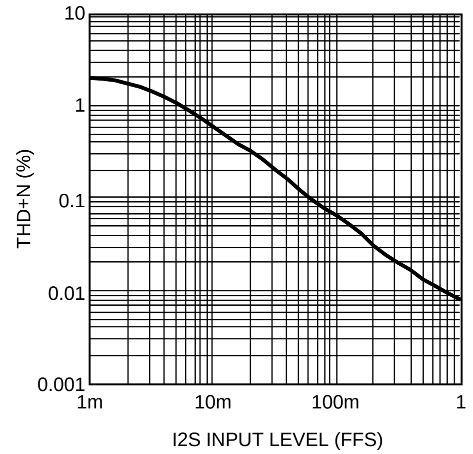


Figure 28.

PSRR vs Frequency
3.0V EP Out Mode 1

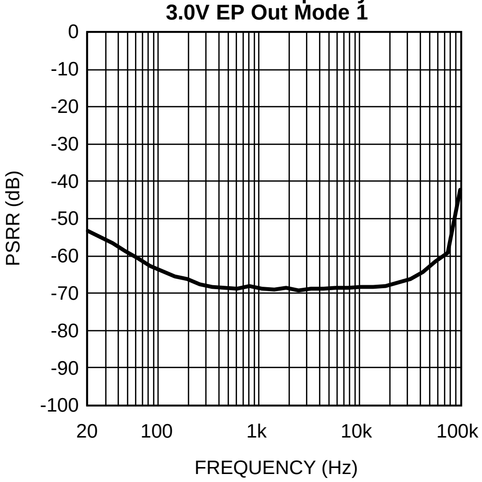


Figure 29.

PSRR vs Frequency
3.0V EP Out Mode 4

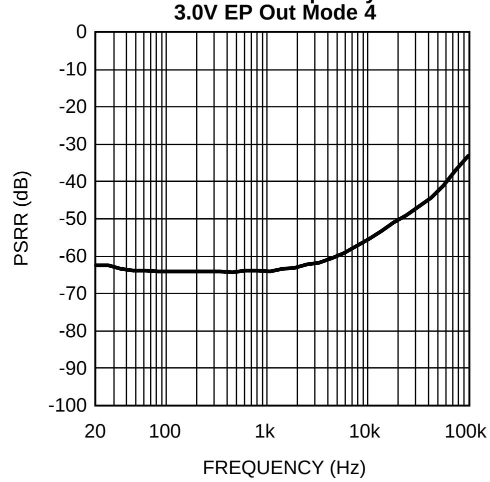


Figure 30.

PSRR vs Frequency
3.0V HP Out Mode 2

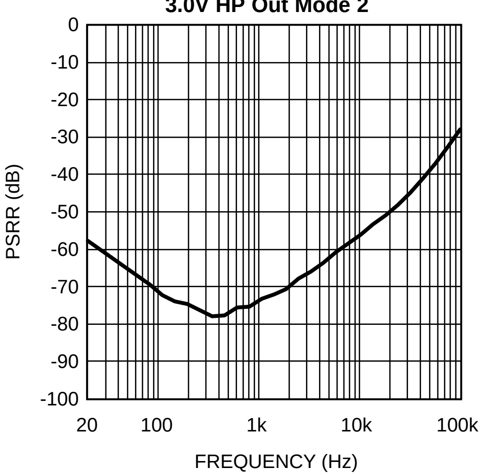


Figure 31.

PSRR vs Frequency
3.0V HP Out Mode 4

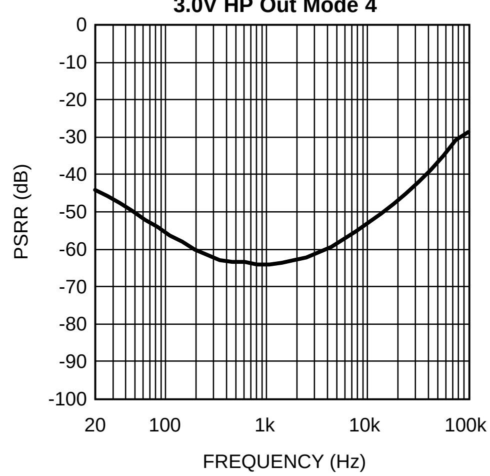


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
3.0V LS Out Mode 2

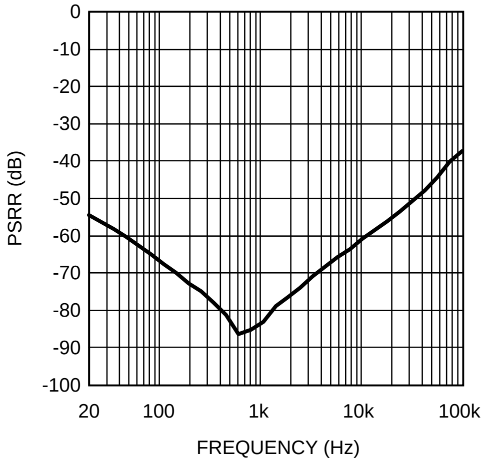


Figure 33.

PSRR vs Frequency
3.0V LS Out Mode 4

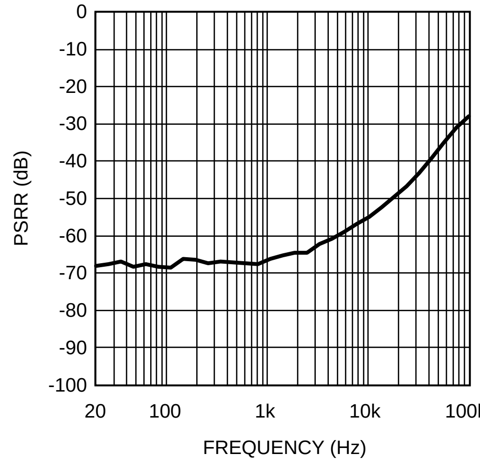


Figure 34.

PSRR vs Frequency
5.0V HP Out Mode 2

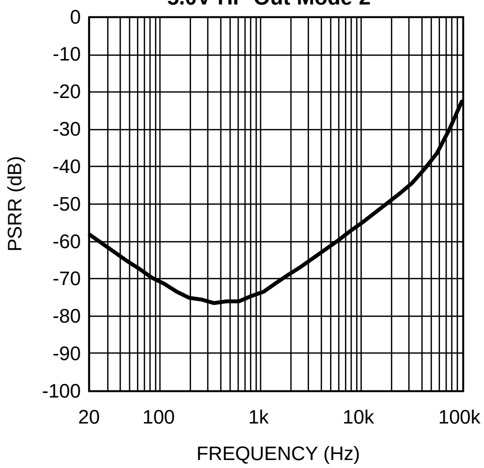


Figure 35.

PSRR vs Frequency
5.0V HP Out Mode 4

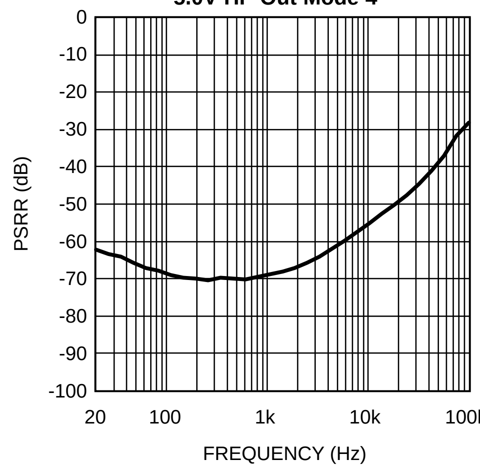


Figure 36.

PSRR vs Frequency
5.0V LS Out Mode 4

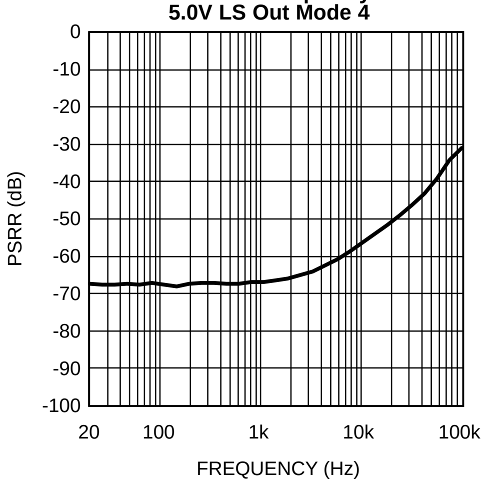


Figure 37.

PSRR vs Frequency
5.0V LS Out Mode 2

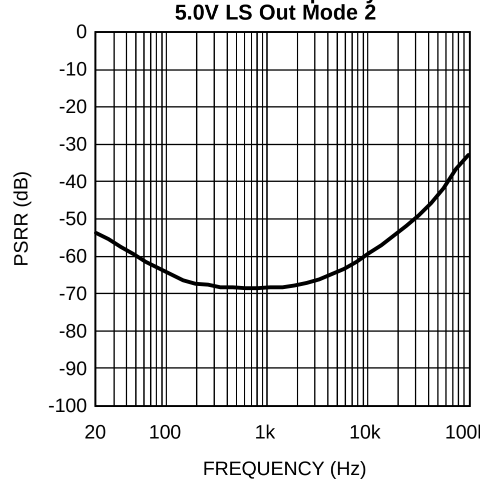


Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Power vs Supply Voltage
EP Out , R_L = 32Ω, 1% THD+N

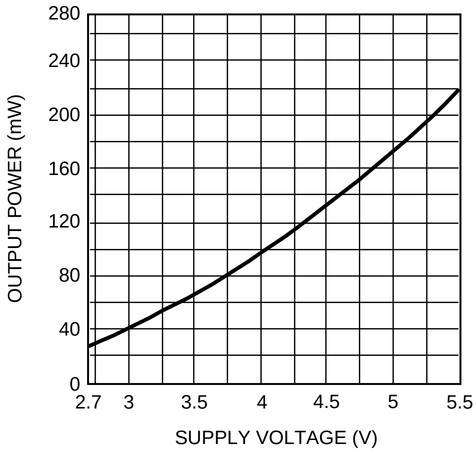


Figure 39.

Output Power vs Supply Voltage
HP Out , R_L = 32Ω, 1% THD+N

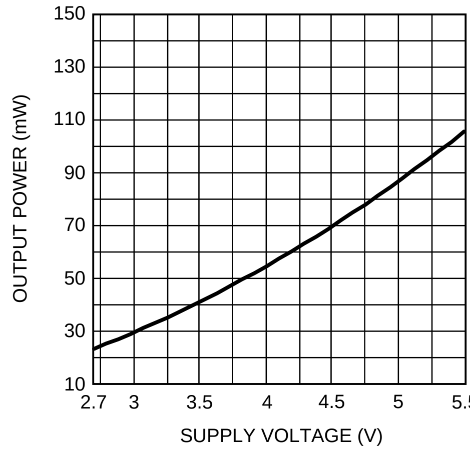


Figure 40.

Output Power vs Supply Voltage
LS Out , R_L = 8Ω, 1% THD+N

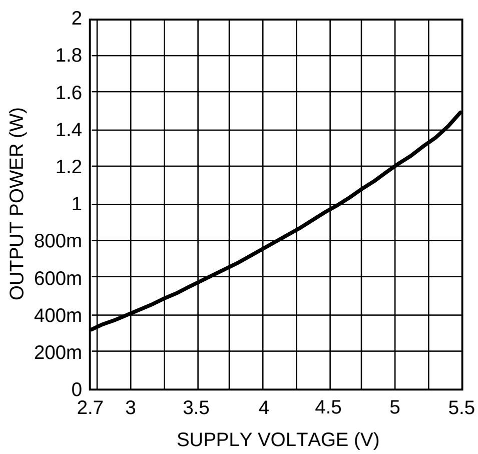
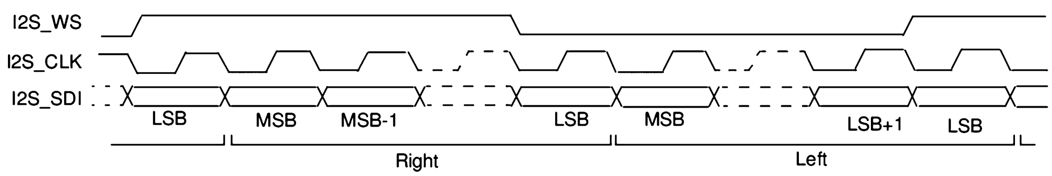


Figure 41.

APPLICATION INFORMATION

I²S

The LM4937 supports both master and slave I2S transmission at either 16 or 32 bits per word at clock rates up to 3.072MHz (48kHz stereo, 32bit). The basic format is shown below:



MONO ONLY SETTING

The LM4937 may be restricted to mono amplification only by setting D-6 in Output Control register 0x01h to 1. This may save an additional 400µA from I_{DD}.

LM4937 DEMOBOARD OPERATION

BOARD LAYOUT

DIGITAL SUPPLIES

- JP14 — Digital Power DVDD
- JP10 — I/O Power IOVDD
- JP13 — PLL Supply PLLVDD
- JP16 — USB Board Supply BBVDD
- JP15 — I2C VDD

All supplies may be set independently. All digital ground is common. Jumpers may be used to connect all the digital supplies together.

- S9 – connects VDD_PLL to VDD_D
- S10 – connects VDD_D to VDD_IO
- S11 – connects VDD_IO to VDD_I2C
- S12 – connects VDD_I2C to Analog VDD
- S17 – connects BB_VDD to USB3.3V (from USB board)
- S19 – connects VDD_D to USB3.3V (from USB board)
- S20 – connects VDD_D to SPDIF receiver chip

ANALOG SUPPLY

- JP11 — Analog Supply
- S12 — connects Analog VDD with Digital VDD (I2C_VDD)
- S16 — connects Analog Ground with Digital Ground
- S21 — connects Analog VDD to SPDIF receiver chip

INPUTS

Analog Inputs

- JP2 — Mono Differential Input
- JP6 — Left Input
- JP7 — Right Input

Digital Inputs

- JP19 — Digital Interface
  - Pin 1 — MCLK
  - Pin 2 — I2S_CLK
  - Pin 3 — I2S_SDI
  - Pin 4 — I2S_WS
- JP20 — Toslink SPDIF Input
- JP21 — Coaxial SPDIF Input

Coaxial and Toslink inputs may be toggled between by use of S25. Only one may be used at a time. Must be used in conjunction with on-board SPDIF receiver chip.

OUTPUTS

- JP5 — BTL Loudspeaker Output
- JP1 — Left Headphone Output (Single-Ended or OCL)
- JP3 — Right Headphone Output (Single-Ended or OCL)
- P1 — Stereo Headphone Jack (Same as JP1, JP2, Single-Ended or OCL)
- JP12 — Mono BTL Earpiece Output

CONTROL INTERFACE

- X1, X2 – USB Control Bus for I2C/SPI
- X1
  - Pin 9 – Mode Select (SPI or I2C)
- X2
  - Pin 1 – SDA
  - Pin 3 – SCL
  - Pin 15 – ADDR/END
  - Pin 14 – USB5V
  - Pin 16 – USB3.3V
  - Pin 16 – USB GND

MISCELLANEOUS

I2S BUS SELECT

S23, S24, S26, S27 – I2S Bus select. Toggles between on-board and external I2S (whether on-board SPDIF receiver is used). All jumpers must be set the same. Jumpers on top two pins selects external bus (JP19). Jumpers on bottom two pins selects on-board SPDIF receiver output.

HEADPHONE OUTPUT CONFIGURATION

Jumpers S1, S2, S3, and S4 are used to configure the headphone outputs for either cap-coupled outputs or output capacitorless (OCL) mode in addition to the register control internal to the LM4937 for this feature. Jumpers S1 and S3 bypass the output DC blocking capacitors when OCL mode is required. S2 connects the center amplifer HPCOUT to the headphone ring when in OCL mode. S4 connects the center ring to GND when cap-coupled mode is desired. S4 must be removed for OCL mode to function properly. Jumper settings for each mode:

- OCL (CD_6 = 1)
  - S1 = ON
  - S2 = ON
  - S3 = ON
  - S4 = OFF

- Cap-Coupled (CD_6 = 0)
  - S1 = OFF
  - S2 = OFF
  - S3 = OFF
  - S4 = ON

PLL FILTER CONFIGURATION

The LM4937 demo board comes with a simple filter setup by connecting jumpers S5 and S6. Removing these and connecting jumpers S7 and S8 will allow for an alternate PLL filter configuration to be used at R2 and C23.

ON-BOARD SPDIF RECEIVER

The SPDIF receiver present on the LM4937 demo board allows quick demonstration of the capabilities of the LM4937 by using the common SPDIF output found on most CD/DVD players today. There are some limitations in its useage, as the receiver will not work with digital supplies of less than 3.0V and analog supplies of less than 4V. This means low analog supply voltage testing of the LM4937 must be done on the external digital bus.

The choice of using on-board or external digital bus is made usign jumpers S23, S24, S26, and S27 as described above.

S25 selects whether the Toslink or Coaxial SPDIF input is used. The top two pins connects the toslink, the bottom two connect the coaxial input.

Power on the digital side is routed through S20 (connecting to the other digital supplies), while on the analog side it is interrupted by S21. Both jumpers must be in place for the receiver to function. The part is already configured for I2S standard outputs. Jumper S28 allows the DATA output to be pulled either high or low. Default is high (jumper on right two pins).

It may be necessary to quickly toggle S29 to reset the receiver and start it working upon initial power up.. A quick short across S29 should clear this condition.

LM4937 I^2C/SPI INTERFACE SOFTWARE

Convenient graphical user interface software is available for demonstration purposes of the LM4937. It allows for either SPI or I^2C control via either USB or parallel port connections to a Windows computer. Control options include all mode and output settings, volume controls, PLL and DAC setup, FIR setting and on-the-fly adjustment by an easy to use graphical interface. An advanced option is also present to allow direct, register-level commands. Software is available from www.ti.com and is compatible with Windows operating systems of Windows 98 or more (with USB support) with the latest .NET updates from Microsoft.

Demonstration Board Schematic

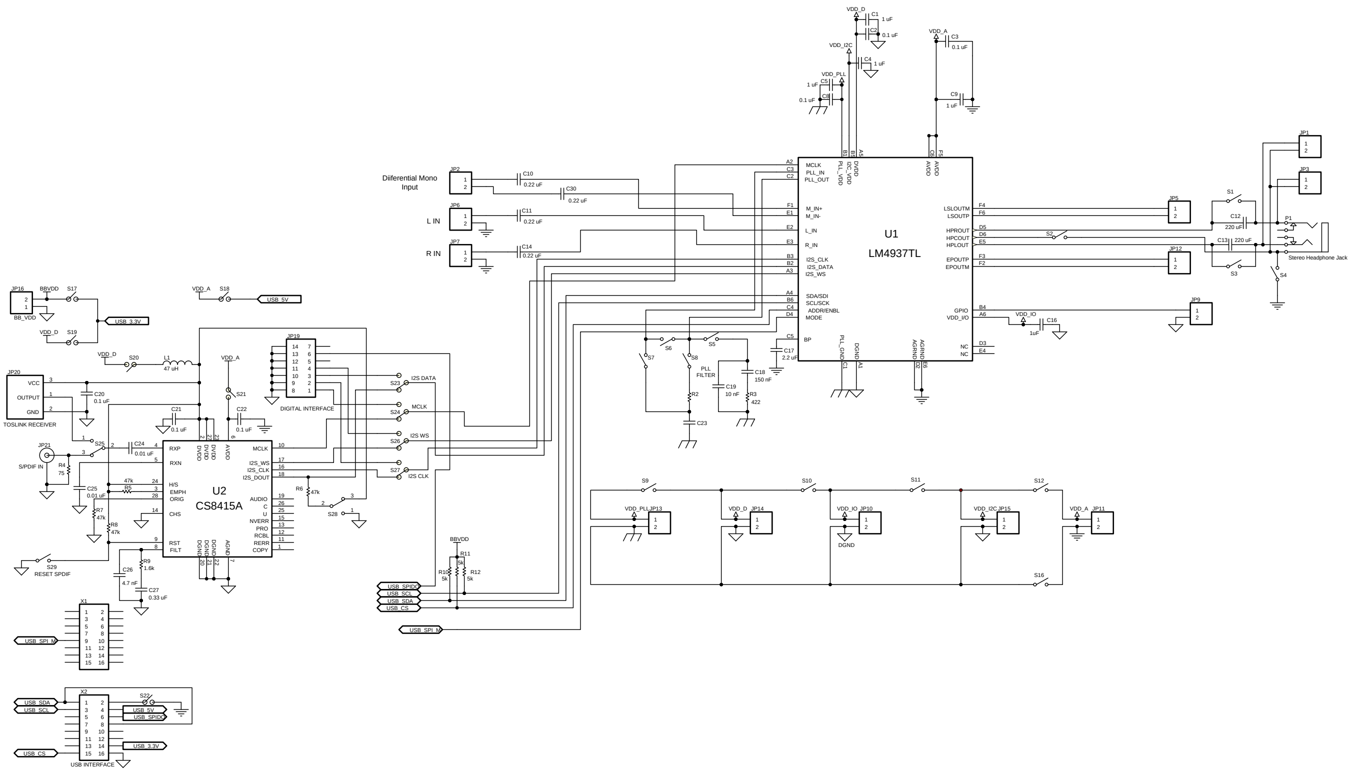


Figure 42. Complete Board Schematic

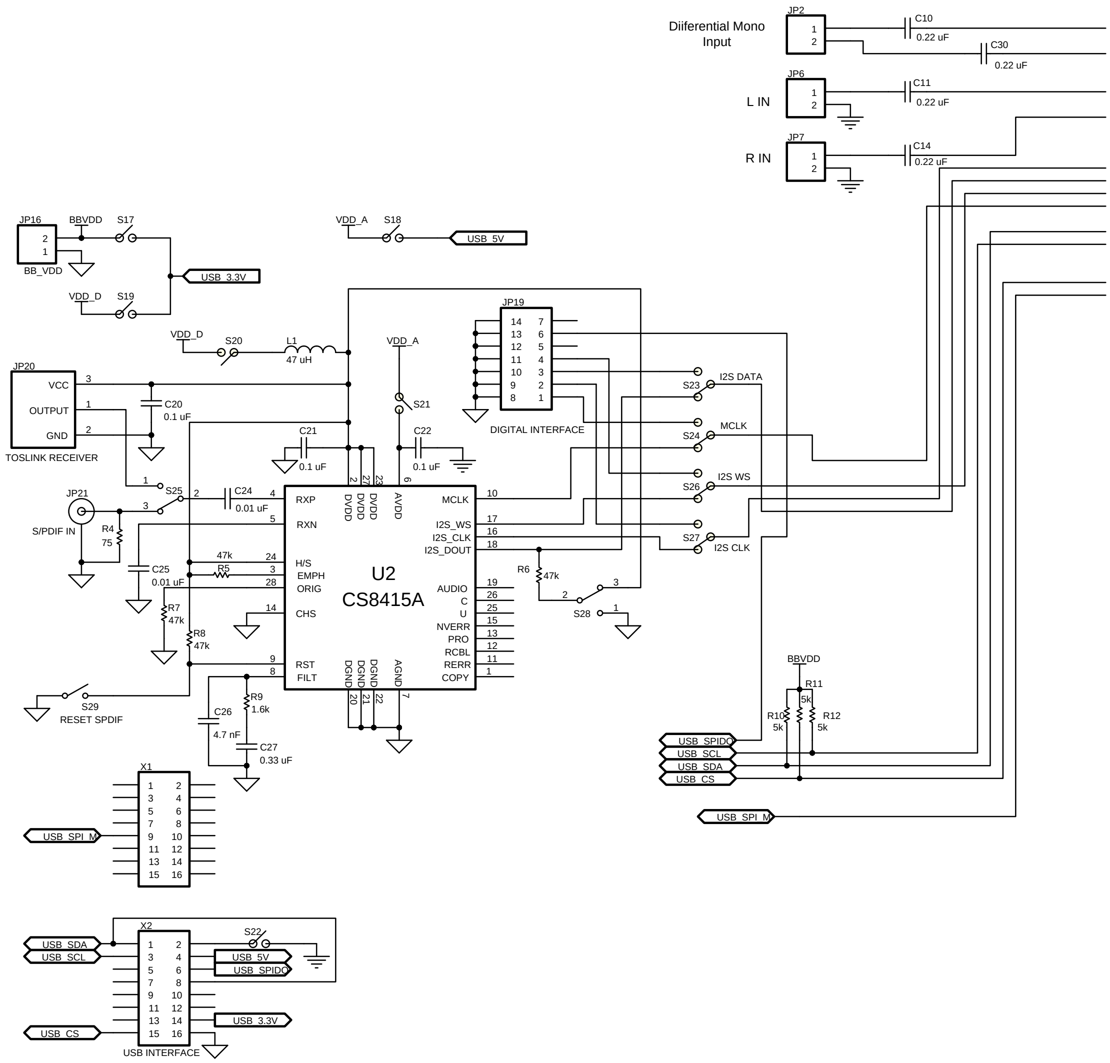


Figure 43. Enlarged Board Schematic Part 1 of 2

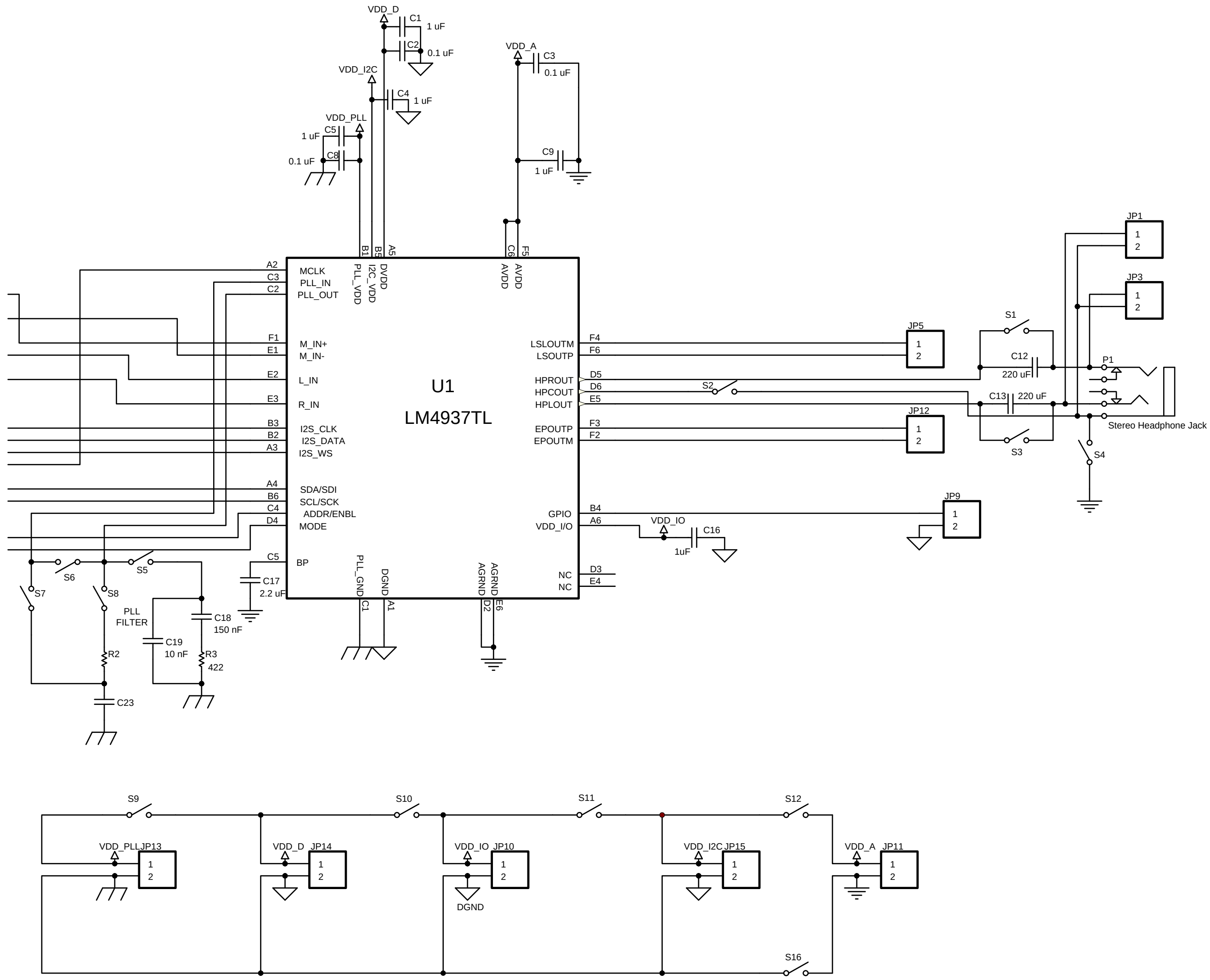


Figure 44. Enlarged Board Schematic Part 2 of 2

REVISION HISTORY

Rev	Date	Description
1.0	10/04/06	Initial release.
1.1	10/13/06	Text edits.
1.2	12/15/06	Changed the datasheet title from RF Resistant Topology to RF Suppression.
1.3	02/09/07	Replaced curve (THD+N vs Output Power, 3V LS Out) with the curve 20166975 from LM4934. These 2 curves have identical performance).
1.4	07/23/07	Changed the datasheet I^2C Vdd & VDD_IO to 1.7V.
1.5	07/30/07	Added more tables (SPI/I2S).
1.6	08/03/07	Text edits.
1.7	10/12/07	Edited 20202001 and 58 and input some text edits.
1.8	10/31/07	Added the RL package.
J	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4937RL/NOPB	OBSOLETE	DSBGA	YPG	36		TBD	Call TI	Call TI	-40 to 85	GJ3	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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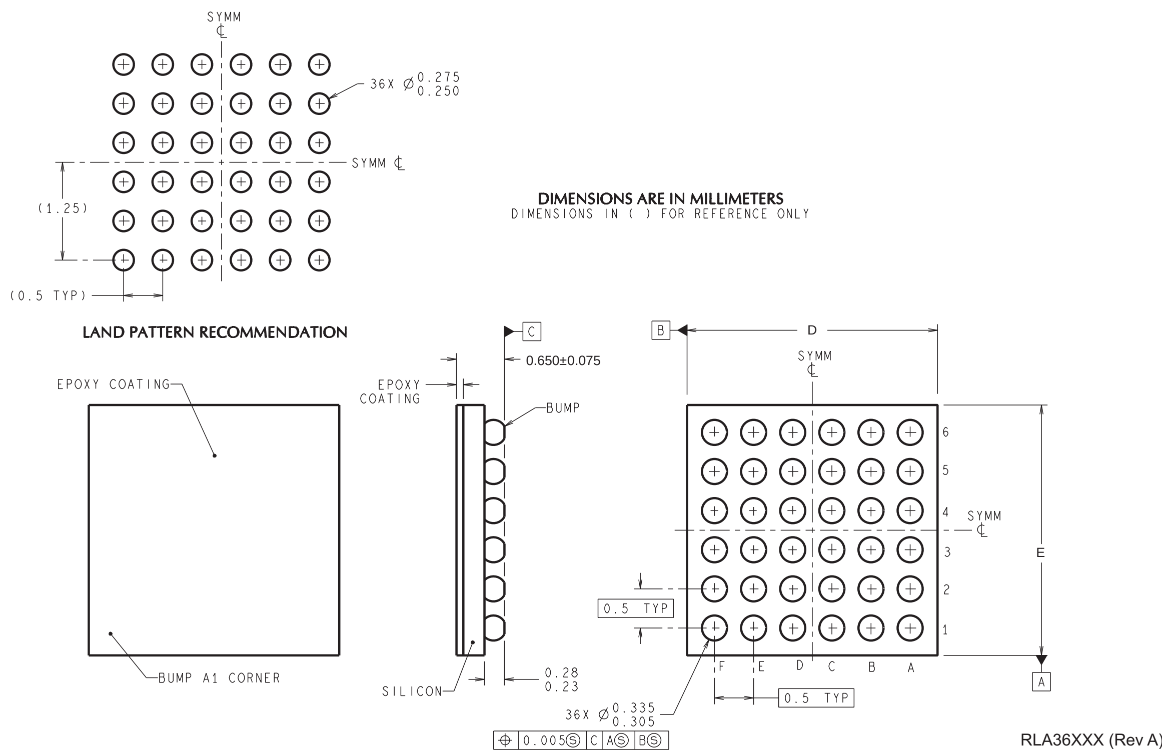

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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