TEXAS INSTRUMENTS
LM5150-Q1
SNVSAP6C – SEPTEMBER 2017 – REVISED OCTOBER 2021

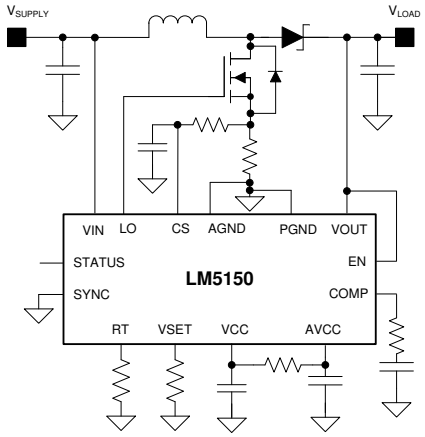
LM5150-Q1 Wide VIN Automotive Low I_Q Boost Controller

1 Features

- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide VIN input range from 1.5 V to 42 V when VOUT ≥ 5 V (65-V absolute maximum)
- Low shutdown current (I_Q ≤ 5 µA)
- Low standby current (I_Q ≤ 15 µA)
- Four programmable output voltage options and two selectable configurations
  - 6.8 V, 7.5 V, 8.5 V, or 10.5 V
  - Start-stop or e-call configurations
- Adjustable switching frequency from 220 kHz to 2.3 MHz
- Automatic wake-up and standby mode transition
- Optional clock synchronization
- Boost status indicator
- 1.5-A peak MOSFET gate driver
- Adjustable cycle-by-cycle current limit
- Thermal shutdown
- 16-pin WQFN with wettable and non-wettable flank options
- Create a custom design using the LM5150-Q1 with the WEBENCH® Power Designer

2 Applications

- Automotive start-stop system
- Automotive emergency call system
- Battery-powered boost converters



Typical Application Circuit

3 Description

The LM5150-Q1 device is a wide input range automatic boost controller. The device is suitable for use as a pre-boost converter which maintains the output voltage from a vehicle battery during automotive cranking or from a back-up battery during the loss of vehicle battery.

The LM5150-Q1 switching frequency is programmed by a resistor from 220 kHz to 2.3 MHz. Fast switching (≥ 2.2 MHz) minimizes AM band interference and allows for a small solution size and fast transient response.

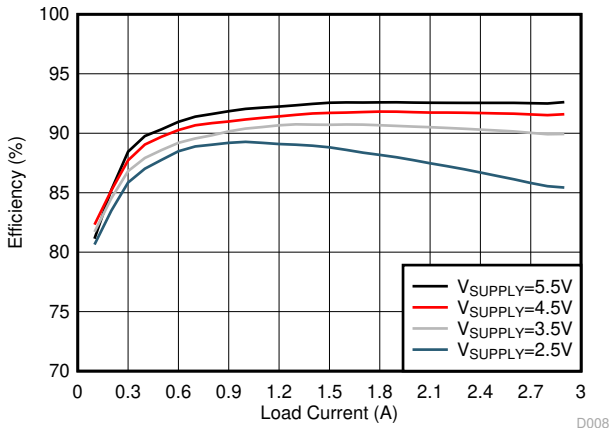
The LM5150-Q1 operates in low I_Q standby mode when the input or output voltage is above the preset standby thresholds and automatically wakes up when the output voltage drops below the preset wake-up threshold.

The device transients in and out of the low I_Q standby mode to extend battery life at light load. A single resistor programs the target output regulation voltage as well as the configuration. Additional features include low shutdown current, boost status indicator, adjustable cycle-by-cycle current limit, and thermal shutdown.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM5150-Q1	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency (V_{LOAD} = 6.8 V, F_{SW} = 440 kHz)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2020) to Revision C (October 2021)	Page
• Added non-wettable flank options	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Added Section 5	3

Changes from Revision A (February 2020) to Revision B (June 2020)	Page
• Added functional safety bullet to Section 1	1

5 Device Comparison Table

PART NUMBER	PACKAGE OUTLINE	WETTABLE (WF)/NON-WETTABLE FLANKS (NON-WF)
LM5150QRUMRQ1	RUM0016C	WF
LM5150QRUMTQ1		
LM5150QURUMRQ1	RUM0016F	Non-WF

6 Pin Configuration and Functions

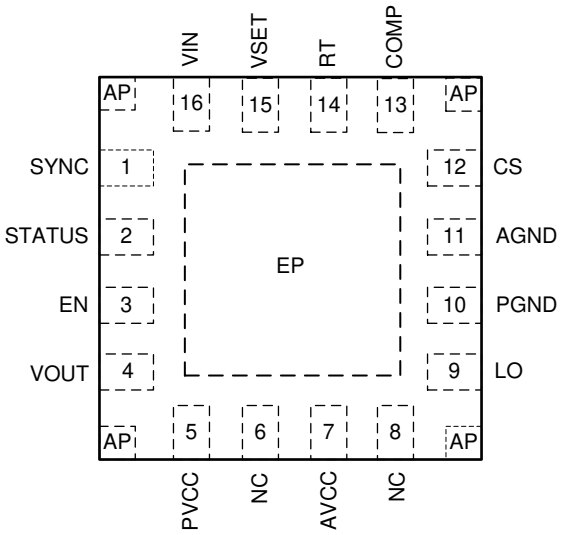


Figure 6-1. 16-Pin WQFN RUM Package (Top View)

Table 6-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	SYNC	I	External synchronization clock input pin. The internal oscillator is synchronized to an external clock by applying a pulse signal into the SYNC pin in the start-stop configuration. Connect directly to ground if not used or in emergency call configuration. Maximum duty cycle limit can be programmed by controlling the external synchronization clock frequency.
2	STATUS	O	Status indicator with an open-drain output stage. Internal pulldown switch holds the pin low when the device is not boosting. The pin can be left floating if not used.
3	EN	I	Enable pin. If EN is below 1 V, the device is in shutdown mode. The pin must be raised above 2 V to enable the device. Connect directly to VOUT pin for an automatic boost.
4	VOUT	I/P	Boost output voltage-sensing pin and input to VCC regulator. Connect to the output of the boost converter.
5	PVCC	O/P	Output of the VCC bias regulator. Decouple locally to PGND using a low-ESR or low-ESL ceramic capacitor located as close to the device as possible.
6	NC	—	No internal electrical connection. Leave the pin floating or connect directly to ground.
7	AVCC	I/P	Analog VCC supply input. Decouple locally to AGND using 0.1-µF low-ESR or low-ESL ceramic capacitor located as close to the device as possible. Connect to the PVCC pin through 10-Ω resistor.
8	NC	—	No internal electrical connection. Leave the pin floating or connect directly to ground.
9	LO	O	N-channel MOSFET gate drive output. Connect to the gate of the N-channel MOSFET through a short, low inductance path.
10	PGND	G	Power ground pin. Connect to the ground connection of the sense resistor through a wide and short path.
11	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
12	CS	I	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
13	COMP	O	Output of the internal transconductance error amplifier. The loop compensation components must be connected between this pin and AGND.
14	RT	I	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.
15	VSET	I	Configuration selection and VOUT regulation target programming pin. During initial power on, a resistor between the VSET pin and AGND configures the VOUT regulation target and the configuration.

Table 6-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
16	VIN	I	Boost input voltage sensing pin. Connect to the input supply of the boost converter.
—	EP	—	Exposed pad of the package. No internal electrical connection to silicon die. The EP is electrically connected to anchor pads. The EP must be connected to the large ground copper plain to reduce thermal resistance.
—	AP	—	Anchor pad of the package. No internal electrical connection to silicon die. The AP is electrically connected to the EP. The AP can be left floating or soldered to the ground copper.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input	VIN to AGND	–0.3	65	V
	VOUT to AGND	–0.3	65	
	EN to AGND	–0.3	65	
	RT to AGND(2)	–0.3	AVCC + 0.3	
	SYNC to AGND	–0.3	7	
	VSET to AGND	–0.3	7	
	CS to AGND (DC)	–0.3	AVCC + 0.3	
	CS to AGND (40-ns transient)	–1.0	AVCC + 0.3	
	CS to AGND (20-ns transient)	–2.0	AVCC + 0.3	
	PGND to AGND	–0.3	0.3	
Output	LO to AGND (DC)	–0.3	PVCC + 0.3	V
	LO to AGND (40-ns transient)	–1.0	PVCC + 0.3	
	LO to AGND (20-ns transient)	–2.0	PVCC + 0.3	
	STATUS to AGND(3)	–0.3	65	
	COMP to AGND(2)	–0.3	AVCC + 0.3	
	AVCC to AGND	–0.3	7	
	PVCC to AVCC	–0.3	0.3	
T_J	Junction temperature(4)	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The pin voltage is clamped by an internal circuit, and is not specified to have an external voltage applied.
(3) STATUS can go below ground during the STATUS low-to-high transition. The negative voltage on STATUS during this transition is clamped by an internal diode and it does not damage the device.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	–750	750	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
V_{VIN}	Boost input voltage sense	1.5		42	V
V_{VOUT}	Boost output voltage sense(2)	5		42	V
V_{EN}	EN input	0		42	V
V_{PVCC}	PVCC voltage(3)	4.5	5	5.5	V
V_{SYNC}	SYNC input	0		5.5	V
V_{CS}	Current sense input	0		0.3	V
F_{SW}	Typical switching frequency	220		2300	kHz

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
F_{SYNC}	Synchronization pulse frequency	220		2300	kHz
T_J	Operating junction temperature(4)	–40		150	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics.*
(2) The device requires minimum 5V at VOUT pin to start up
(3) V_{PVCC} should be less than V_{VOUT} + 0.3 V
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC(1)		LM5150-Q1 RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{VOUT} = 6.8 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN(VOUT)}$	VOUT shutdown current	V_{VOUT} = 12 V, V_{EN} = 0 V		5	12	µA
$I_{STANDBY(VOUT)}$	VOUT standby current (PVCC in regulation, STATUS is low)	V_{VOUT} = 12 V, V_{EN} = 3.3 V, R_{SET} = 90.9 kΩ		15	25	µA
$I_{WAKEUP(VOUT)}$	VOUT operating current (exclude current into RT resistor)	V_{VOUT} = 10.5 V, V_{EN} = 2.5 V, non-switching, R_T = 9.09 kΩ		1.2	2.0	mA
$I_{SHUTDOWN(VIN)}$	VIN shutdown current	V_{VIN} = 12 V, V_{EN} = 0 V		0.1	0.5	µA
$I_{STANDBY(VIN)}$	VIN standby current	V_{VIN} = 12 V, V_{EN} = 3.3 V, R_{SET} = 29.4 kΩ		0.1	0.5	µA
$I_{WAKEUP(VIN)}$	VIN operating current	V_{VIN} = 10.5 V, V_{EN} = 2.5 V, non-switching, R_T = 9.09 kΩ		30	45	µA
VCC REGULATOR						
$V_{VCC-REG-NOLOAD}$	PVCC regulation	V_{VOUT} = 6.0 V, No load, wake-up mode	4.75	5	5.25	V
$V_{VCC-REG-FULLLOAD}$	PVCC regulation	V_{VOUT} = 5.0 V, I_{PVCC} = 70 mA	4.5	4.8		V
$V_{VCC-UVLO-RISING}$	AVCC UVLO threshold	AVCC rising	4.1	4.3	4.5	V
$V_{VCC-UVLO-FALLING}$	AVCC UVLO threshold	AVCC falling	3.9	4.1	4.3	V
$V_{VCC-UVLO-HYS}$	AVCC UVLO hysteresis			0.2		V
I_{VCC-CL}	PVCC sourcing current limit	V_{PVCC} = 0 V, wake-up mode	75			mA
ENABLE						
$V_{EN-RISING}$	Enable threshold	EN rising		1.7	2	V
$V_{EN-FALLING}$	Enable threshold	EN falling	1	1.3		V
I_{EN}	EN bias current	V_{EN} = 42 V			100	nA
6.8-V SETTING						

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{VOUT} = 6.8 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VOUT-REG}$	VOUT regulation target	R_{SET} = 29.4 kΩ or 90.9 kΩ	6.66	6.80	6.98	V
$V_{VOUT-WAKEUP}$	VOUT wake-up threshold ($V_{VOUT-REG}$ + 3%)	R_{SET} = 29.4 kΩ or 90.9 kΩ, VOUT falling	6.83	7.00	7.14	V
$V_{VOUT-STANDBY1}$	VOUT standby threshold ($V_{VOUT-REG}$ + 6%, EC config)	R_{SET} = 90.9 kΩ, VOUT rising	7.02	7.21	7.35	V
$V_{VOUT-STATUS-OFF}$	VOUT status off threshold ($V_{VOUT-REG}$ + 12%, EC config)	R_{SET} = 90.9 kΩ, VOUT rising	7.42	7.62	7.81	V
$V_{VOUT-STANDBY2}$	VOUT standby threshold ($V_{VOUT-REG}$ + 24%, SS config)	R_{SET} = 29.4 kΩ, VOUT rising	8.22	8.43	8.60	V
$V_{VIN-STANDBY}$	VIN standby threshold ($V_{VOUT-WAKEUP}$ + 1.0 V, SS config)	R_{SET} = 29.4 kΩ, VIN rising	7.82	8.00	8.19	V
7.5-V SETTING						
$V_{VOUT-REG}$	VOUT regulation target	R_{SET} = 19.1 kΩ or 71.5 kΩ	7.37	7.50	7.67	V
$V_{VOUT-WAKEUP}$	VOUT wake-up threshold ($V_{VOUT-REG}$ + 3%)	R_{SET} = 19.1 kΩ or 71.5 kΩ, VOUT falling	7.52	7.73	7.88	V
$V_{VOUT-STANDBY1}$	VOUT standby threshold ($V_{VOUT-REG}$ + 6%, EC config)	R_{SET} = 71.5 kΩ, VOUT rising	7.74	7.95	8.11	V
$V_{VOUT-STATUS-OFF}$	VOUT status off threshold ($V_{VOUT-REG}$ + 12%, EC config)	R_{SET} = 71.5 kΩ, VOUT rising	8.19	8.40	8.61	V
$V_{VOUT-STANDBY2}$	VOUT standby threshold ($V_{VOUT-REG}$ + 24%, SS config)	R_{SET} = 19.1 kΩ, VOUT rising	9.07	9.30	9.46	V
$V_{VIN-STANDBY}$	VIN standby threshold ($V_{VOUT-WAKEUP}$ + 1.0 V, SS config)	R_{SET} = 19.1 kΩ, VIN rising	8.50	8.73	8.93	V
8.5-V SETTING						
$V_{VOUT-REG}$	VOUT regulation target	R_{SET} = 9.53 kΩ or 54.9 kΩ	8.37	8.50	8.69	V
$V_{VOUT-WAKEUP}$	VOUT wake-up threshold ($V_{VOUT-REG}$ + 3%)	R_{SET} = 9.53 kΩ or 54.9 kΩ, VOUT falling	8.52	8.76	8.93	V
$V_{VOUT-STANDBY1}$	VOUT standby threshold ($V_{VOUT-REG}$ + 6%, EC config)	R_{SET} = 54.9 kΩ, VOUT rising	8.78	9.01	9.19	V
$V_{VOUT-STATUS-OFF}$	VOUT status off threshold ($V_{VOUT-REG}$ + 12%, EC config)	R_{SET} = 54.9 kΩ, VOUT rising	9.28	9.52	9.75	V
$V_{VOUT-STANDBY2}$	VOUT standby threshold ($V_{VOUT-REG}$ + 24%, SS config)	R_{SET} = 9.53 kΩ, VOUT rising	10.29	10.54	10.72	V
$V_{VIN-STANDBY}$	VIN standby threshold ($V_{VOUT-WAKEUP}$ + 1.0 V, SS config)	R_{SET} = 9.53 kΩ, VIN rising	9.50	9.76	9.98	V
10.5-V SETTING						
$V_{VOUT-REG}$	VOUT regulation target	R_{SET} = GND or 41.2 kΩ	10.31	10.50	10.75	V
$V_{VOUT-WAKEUP}$	VOUT wake-up threshold ($V_{VOUT-REG}$ + 3%)	R_{SET} = GND or 41.2 kΩ, VOUT falling	10.53	10.82	11.02	V
$V_{VOUT-STANDBY1}$	VOUT standby threshold ($V_{VOUT-REG}$ + 6%, EC config)	R_{SET} = 41.2 kΩ, VOUT rising	10.84	11.13	11.33	V
$V_{VOUT-STATUS-OFF}$	VOUT status off threshold ($V_{VOUT-REG}$ + 12%, EC config)	R_{SET} = 41.2 kΩ, VOUT rising	11.46	11.76	12.04	V
$V_{VOUT-STANDBY2}$	VOUT standby threshold ($V_{VOUT-REG}$ + 24%, SS config)	R_{SET} = GND, VOUT rising	12.70	13.02	13.24	V
$V_{VIN-STANDBY}$	VIN standby threshold ($V_{VOUT-WAKEUP}$ + 1.0 V, SS config)	R_{SET} = GND, VIN rising	11.47	11.82	12.11	V
RT						
V_{RT-REG}	RT regulation voltage			1.2		V
CLOCK SYNCHRONIZATION						
$V_{SYNC-RISING}$	SYNC rising threshold			2.0	2.4	V

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C. Unless otherwise stated, V_{VOUT} = 6.8 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SYNC-FALLING}$	SYNC falling threshold		0.4	1.5		V
PULSE WIDTH MODULATION AND OSCILLATOR						
F_{SW1}	Switching frequency	R_T = 93.1 kΩ	204	239	270	kHz
F_{SW2}	Switching frequency	R_T = 9.09 kΩ	2100	2300	2500	kHz
F_{SW3}	Switching frequency	R_T = 9.09 kΩ, F_{SYNC} = 2.0 MHz		2000		kHz
T_{ON-MIN}	Forced minimum on time	SS config, V_{COMP} = 0 V	30	50	70	ns
D_{MIN}	Minimum duty cycle limit (EC config)	R_T = 9.09 kΩ, V_{VIN} = 1.5 V, V_{VOUT} = 6.8 V, V_{COMP} = 0 V		60%		
		R_T = 93.1 kΩ, V_{VIN} = 8.4 V, V_{VOUT} = 10.5 V, V_{COMP} = 0 V		16%		
D_{MAX}	Maximum duty cycle limit	SS config, R_T = 9.09 kΩ	83%	87%	91.5%	
		EC config, R_T = 93.1 kΩ	83%	87%	91.5%	
CURRENT SENSE						
V_{CSTH}	Current limit threshold (CS-AGND)(1)	V_{VIN} = 5.1 V, V_{VOUT} = 6.8 V at 25% DC	102	120	138	mV
		V_{VIN} = 3.4 V, V_{VOUT} = 6.8 V at 50% DC	102	120	138	mV
		V_{VIN} = 1.7 V, V_{VOUT} = 6.8 V at 75% DC	102	120	138	mV
ERROR AMPLIFIER						
Gm	Transconductance			2		mA/V
	COMP souring current	V_{COMP} = 0 V	312			µA
	COMP sinking current	V_{COMP} = 1.5 V	120			µA
	COMP clamp voltage		2.4	2.6		V
	COMP to PWM offset			0.3		V
STATUS						
	Low-state voltage drop	1-mA sinking		0.1		V
	STATUS rise to LO delay	5-kΩ pullup to 5 V	4	5	6	µs
MOSFET DRIVER						
	High-state voltage drop	50-mA sinking		0.075		V
	Low-state voltage drop	50-mA sourcing		0.055		V
THERMAL SHUTDOWN (TSD)						
	Thermal shutdown threshold	Temperature rising		175		°C
	Thermal shutdown hysteresis			15		°C

(1) V_{CL} at the current limit comparator input is 10 x V_{CSTH}

7.6 Typical Characteristics

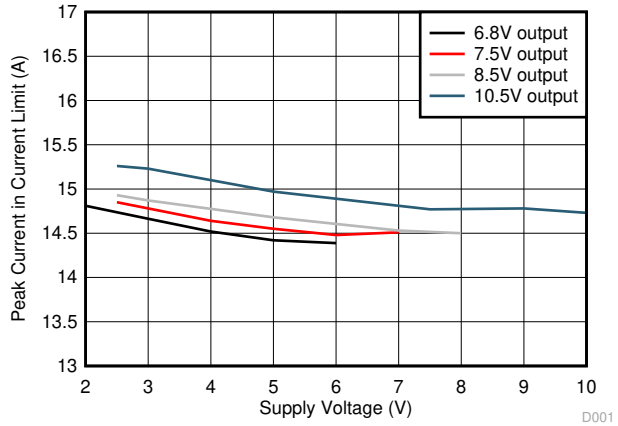


Figure 7-1. Peak Inductor Current vs Supply Voltage (F_{SW} = 250 kHz, R_S = 8 mΩ)

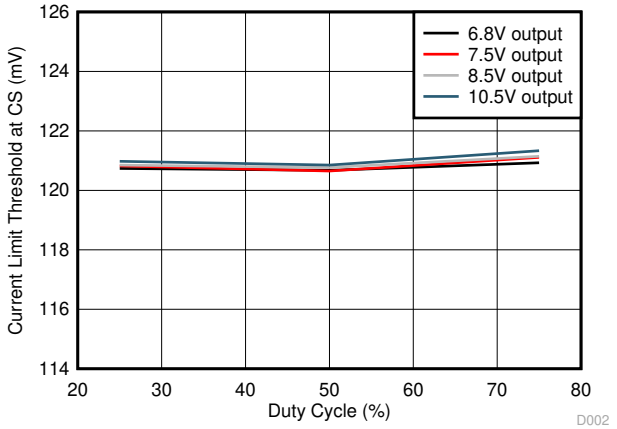


Figure 7-2. Current Limit Threshold at CS vs Duty Cycle

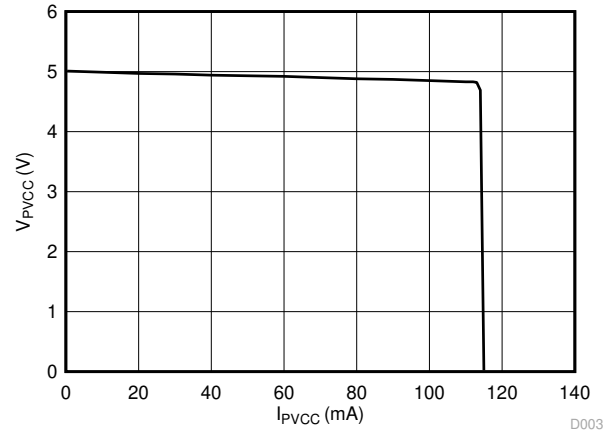


Figure 7-3. V_{PVCC} vs I_{PVCC} (VOUT = 6 V)

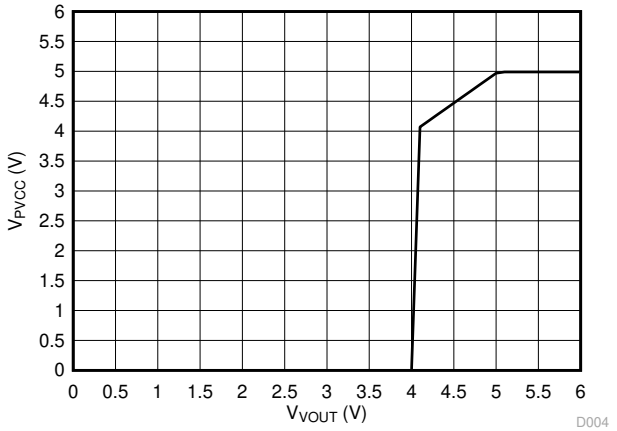


Figure 7-4. V_{PVCC} vs V_{VOUT} (EN = 3.3 V, I_{PVCC} = 10 mA, VOUT Rising)

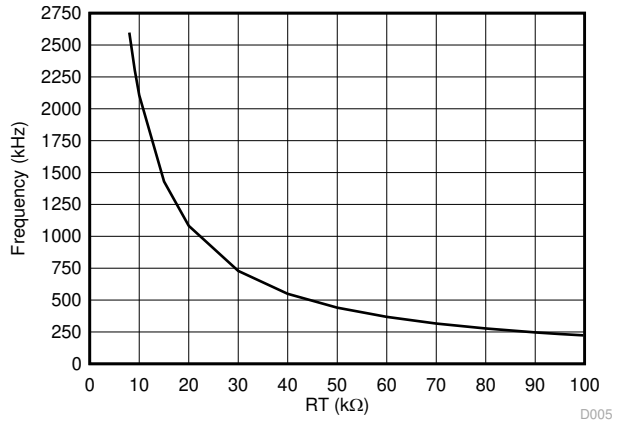


Figure 7-5. Frequency vs RT

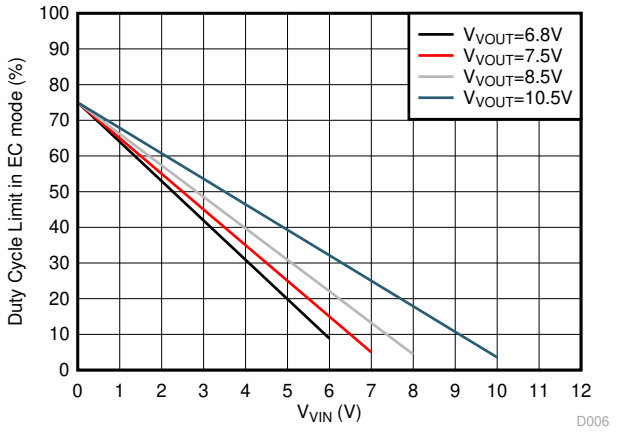


Figure 7-6. Duty Cycle Limit in EC Configuration vs V_{VIN}

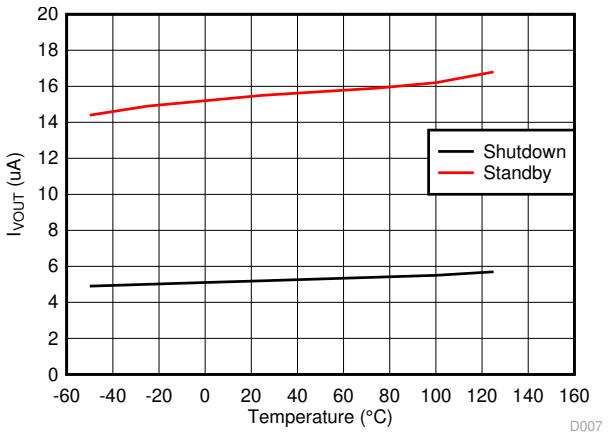


Figure 7-7. I_{VOUT} vs Temperature

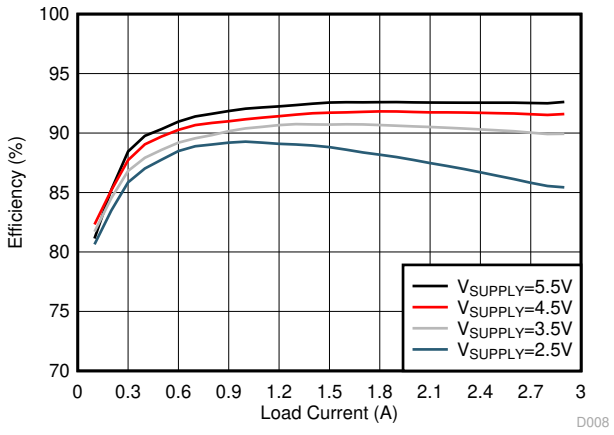


Figure 7-8. Efficiency vs Load Current (V_{LOAD} = 6.8 V, F_{SW} = 440 kHz, SS Configuration)

8 Detailed Description

8.1 Overview

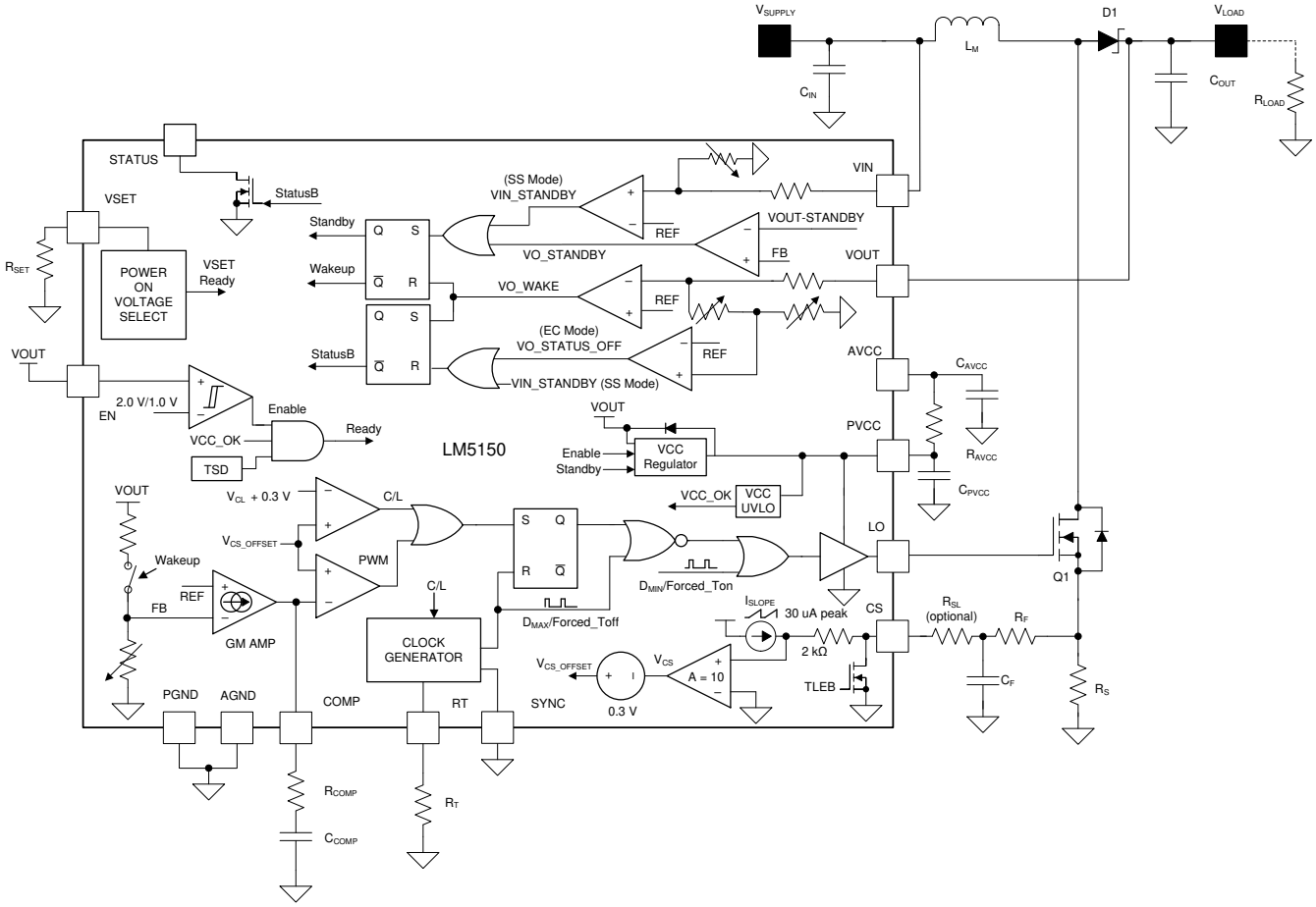
The LM5150-Q1 device is a wide input range automotive boost controller designed for automotive start-stop or emergency-call applications. The device can maintain the output voltage from a vehicle battery during automotive cranking or from a back-up battery during the loss of vehicle battery. The wide input range of the device covers automotive load dump transient. The control method is based upon peak current mode control.

To extend the battery life time, the LM5150-Q1 features a low I_Q standby mode with automatic wake-up and standby control. The device stays in low I_Q standby mode when the boost operation is not required, and automatically enters wake-up mode when the output voltage drops below the preset wake-up threshold. High value feedback resistors are included inside the device to minimize leakage current in the low I_Q standby mode.

The LM5150-Q1 operates in one of two selectable configurations when waking up. In Start-Stop configuration (SS configuration), the device runs at a fixed switching frequency without any pulse skipping until it enters standby mode, which helps to have a fixed EMI spectrum. In Emergency-Call configuration (EC configuration), the device will skip pulses as it automatically alternates between low I_Q standby mode and wake-up mode to extend the battery life in light load conditions.

The LM5150-Q1 switching frequency is programmable from 220 kHz to 2.3 MHz. Fast switching (≥ 2.2 MHz) minimizes AM band interference and allows for a small solution size and fast transient response. A single resistor at the VSET pin programs the target output regulation voltage as well as the configuration. This eliminates the need for an external feedback resistor divider which enables low I_Q operation. The device also features clock synchronization in the SS configuration, low quiescent current in shutdown mode, a boost status indicator, adjustable cycle-by-cycle current will limit, and thermal shutdown protection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN Pin)

When the EN pin voltage is less than 1 V, the LM5150-Q1 is in shutdown mode with all other functions disabled. To turn on the internal VCC regulator and begin start-up sequence, the EN pin voltage must be greater than 2 V. If the EN pin is controlled by user input, it is recommended to supply a voltage greater than 3 V at the EN pin. If the EN pin is not controlled by user input, connect the EN pin to the VOUT pin directly. See Section 8.4 for more detailed information.

8.3.2 High Voltage VCC Regulator (PVCC, AVCC Pin)

The LM5150-Q1 contains an internal high voltage VCC regulator. The VCC regulator turns on when the EN pin voltage is greater than 2 V. The VCC regulator is sourced from the VOUT pin and provides 5 V (typical) bias supply for the N-channel MOSFET driver and other internal circuits.

The VCC regulator sources current into the capacitor connected to the PVCC pin with a minimum of 75-mA capability when the LM5150-Q1 is in the wake-up mode and during the device configuration period. The maximum sourcing capability is decreased to 17 mA in standby mode. The recommended PVCC capacitor is 4.7 µF to 10 µF. In normal operation, the PVCC pin voltage is either 5 V or V_{VOUT} + 0.3 V, whichever is lower.

The AVCC pin is the analog bias supply input of the LM5150-Q1. The recommended AVCC capacitor is 0.1-µF. Connect to the PVCC pin through 10-Ω resistor.

8.3.3 Power-On Voltage Selection (VSET Pin)

During initial power on, the VOUT regulation target and the configuration are configured by a resistor connected between the VSET and the AGND pins. The configuration starts when the EN pin voltage is greater than 2 V and the AVCC voltage crosses the AVCC UVLO threshold, and requires typically 50 µs to finish. To reset and reconfigure, EN should be toggled below 1 V or AVCC/VOUT must be fully discharged.

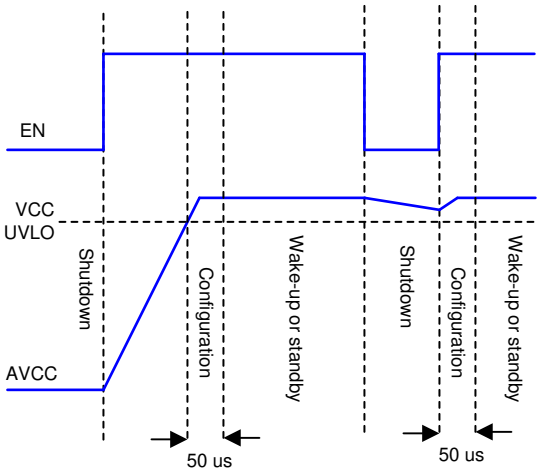


Figure 8-1. Power-On Voltage Selection

The VOUT regulation target can be programmed to 6.8 V, 7.5 V, 8.5 V, or 10.5 V with the appropriate resistor with 5% tolerance. The configuration can be selected as either SS or EC configuration. The LM5150-Q1 will not switch during the 50-µs configuration time.

Table 8-1. VSET Resistors(1)

CONFIGURATION	EMERGENCY-CALL				START-STOP			
VOUT regulation target	6.8 V	7.5 V	8.5 V	10.5 V	6.8 V	7.5 V	8.5 V	10.5 V
R_{SET} [Ω]	90.9 k	71.5 k	54.9 k	41.2 k	29.4 k	19.1 k	9.53 k	Ground

(1) If other output regulation targets are required, contact the sales office/distributors for availability.

8.3.4 Switching Frequency (RT Pin)

The switching frequency of the LM5150-Q1 is set by a single RT resistor connected between the RT and the AGND pins. The resistor value to set the switching frequency (F_{SW}) is calculated using Equation 1.

$$R_T = \frac{2.233 \times 10^{10}}{F_{SW\_RT(TYPICAL)}} - 619\,\Omega \quad (1)$$

The RT pin is regulated to 1.2 V by the internal RT regulator during wake-up.

8.3.5 Clock Synchronization (SYNC Pin in SS Configuration)

In SS configuration, the switching frequency of the LM5150-Q1 can be synchronized to an external clock by directly applying a pulse signal to the SYNC pin. The internal clock of the LM5150-Q1 is synchronized at the rising edge of the external clock. The device ignores the rising edge input during forced off-time.

The external synchronization pulse must be greater than the 2.4 V in the high logic state and must be less than 0.4 V in the low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum pulse width should be greater than 100 ns. Because the maximum duty cycle limit and the peak current limit threshold are affected by synchronizing the switching frequency to an external synchronization pulse, take extra care when using the clock synchronization function. See Section 8.3.11 and Section 8.3.7 for more detailed information.

If the minimum input supply voltage of the boost converter is greater than ¼ of the VOUT regulation target ($V_{VOUT-REG}$), the frequency of the external synchronization pulse (F_{SYNC}) should be within +15% and –15% of the typical free-running switching frequency ($F_{SW(TYPICAL)}$)

$$0.85 \times F_{SW\_RT(TYPICAL)} \le F_{SYNC} \le 1.15 \times F_{SW\_RT(TYPICAL)} \quad (2)$$

In this range, a maximum 1:4 (V_{SUPPLY}:V_{LOAD}) step-up ratio is allowed.

A higher step-up ratio can be achieved by supplying a lower frequency synchronization pulse. 1:5 step-up ratio can be achieved by selecting F_{SYNC} within –25% and –15% of the $F_{SW\_RT(TYPICAL)}$.

$$0.75 \times F_{SW\_RT(TYPICAL)} \le F_{SYNC} \le 0.85 \times F_{SW\_RT(TYPICAL)} \quad (3)$$

In this range, a maximum 1:5 (V_{SUPPLY}:V_{LOAD}) step-up ratio is allowed.

8.3.6 Current Sense, Slope Compensation, and PWM (CS Pin)

The LM5150-Q1 features a low-side current sense amplifier with a gain of 10, and provides an internal slope compensation ramp to prevent subharmonic oscillation at high duty cycle. The device generates the slope compensation ramp using a sawtooth current source with a slope of 30 µA × F_{SW} (typical). This current flows through an internal 2-kΩ resistor and out of the CS pin. The slope compensation ramp is determined by the RT resistor and is 60 mV × F_{SW} (typical) at the input of the current sense amplifier and 600 mV × F_{SW} (typical) at the output of the current sense amplifier. The slope compensation ramp can be increased by adding an external slope resistor (R_{SL}) between the sense resistor (R_S) and the CS pin, but take extra care when using R_{SL}, because the peak current limit is affected by adding R_{SL}. See Section 8.3.7 for more detailed information.

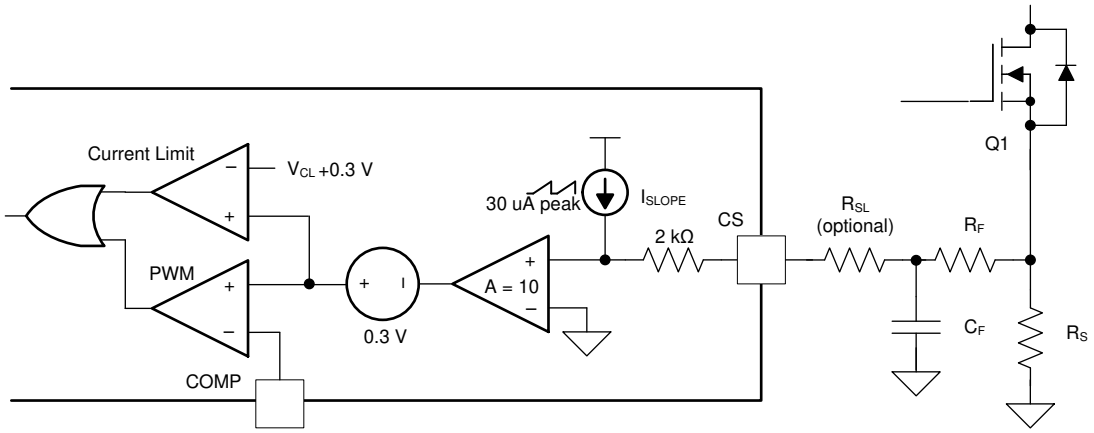


Figure 8-2. Current Sensing and Slope Compensation

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of slope compensation should satisfy the following inequality:

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times R_S \times \text{Margin} < 30\mu A \times (2k\Omega + R_{SL}) \times F_{SW} \quad (4)$$

V_F is a forward voltage drop of D1, the external diode. 1.2 is recommended as a margin to cover non-ideal factors.

If required, R_{SL} can be added to increase the slope of the compensation ramp from half to 82% of the slope of the sensed inductor current during the falling slope. The typical R_{SL} value is calculated using Equation 5. The maximum R_{SL} value is 1 kΩ

$$0.82 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times R_S = 30\mu A \times (2k\Omega + R_{SL}) \times F_{SW} \quad (5)$$

The PWM comparator in Figure 8-2 compares the sum of sensed inductor current, the slope compensation ramp, and a 0.3-V (typical) internal COMP-to-PWM offset with the COMP pin voltage (V_{COMP}), and terminates the present cycle if the sum is greater than V_{COMP}.

8.3.7 Current Limit (CS Pin)

The LM5150-Q1 features cycle-by-cycle peak current limit without subharmonic oscillation at high duty cycle. If the sum of the sensed inductor current and the slope compensation ramp exceeds the current limit threshold at the current limit comparator input (V_{CL}), the current limit comparator immediately terminates the present cycle. To minimize the peak current limit variation due to changes in either the supply voltage or the output voltage, the device features a variable current limit threshold which is calculated using Equation 6.

$$V_{CL} = 1.2 + 0.6 \times \frac{(V_{VOUT} - V_{VIN})}{V_{VOUT\text{-}REG}} [V] \quad (6)$$

Cycle-by-cycle peak inductor current limit ($I_{PEAK\text{-}CL}$) in steady state calculated as follows:

$$I_{PEAK-CL} = \frac{V_{CL} - 10 \times 30\mu A \times (2k\Omega + R_{SL}) \times \frac{F_{SW\_RT}}{F_{SYNC}} \times D}{10 \times R_S} \quad (7)$$

$$D = 1 - \frac{V_{SUPPLY}}{V_{LOAD} + V_F} \quad (8)$$

F_{SYNC} is included in the equation because the peak amplitude of the slope compensation varies with the frequency of the external synchronization clock. Substitute F_{SW_RT} for F_{SYNC} if clock synchronization is not used.

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Due to this path, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage.

A small external RC filter (R_F, C_F) at the CS pin is required to overcome the leading edge spike of the current sense signal. Select an R_F value which is greater than 30 Ω and a C_F value which is greater than 1 nF. Due to the effect of the filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F.

8.3.8 Feedback and Error Amplifier (COMP Pin)

The LM5150-Q1 includes internal feedback resistors which are set based on the VSET pin resistor selection. These feedback resistors are disconnected from the VOUT pin in standby mode to minimize quiescent current. The feedback resistor divider is connected to an internal transconductance error amplifier which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz). The internal transconductance error amplifier sources current which is proportional to the difference between the feedback resistor divider voltage and the internal reference. The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network.

R_{COMP}, C_{COMP} and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency (F_{DP}), a mid-band zero (F_{Z_EA}), and a high frequency pole (F_{P_EA}). See Section 9.2.2.8 for more detailed information.

8.3.9 Automatic Wake-Up and Standby

The LM5150-Q1 wakes up when V_{VOUT} drops below the VOUT wake-up threshold. The device goes into standby when V_{VOUT} rises above the VOUT standby threshold in EC or SS configuration or when V_{VIN} rises above the VIN standby threshold in SS configuration. The VOUT wake-up threshold is typically 3% higher than the VOUT regulation target. The STATUS output is released in 3 µs (with a 50-kΩ pullup resistor to 5 V) after the wake-up event. The LO driver is enabled 6 µs after the STATUS output starts rising.

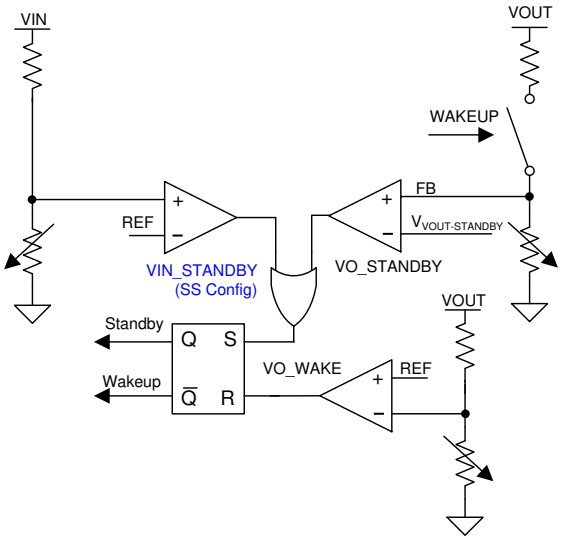


Figure 8-3. Automatic Wake-Up and Standby Control

In SS configuration, the VOUT standby threshold is typically 24% higher than the VOUT regulation target. The VIN standby threshold is typically 1 V higher than the VOUT wake-up threshold in SS configuration. To prevent chatter, the forward voltage drop of diode D1 must be less than 0.95 V. See Figure 8-7.

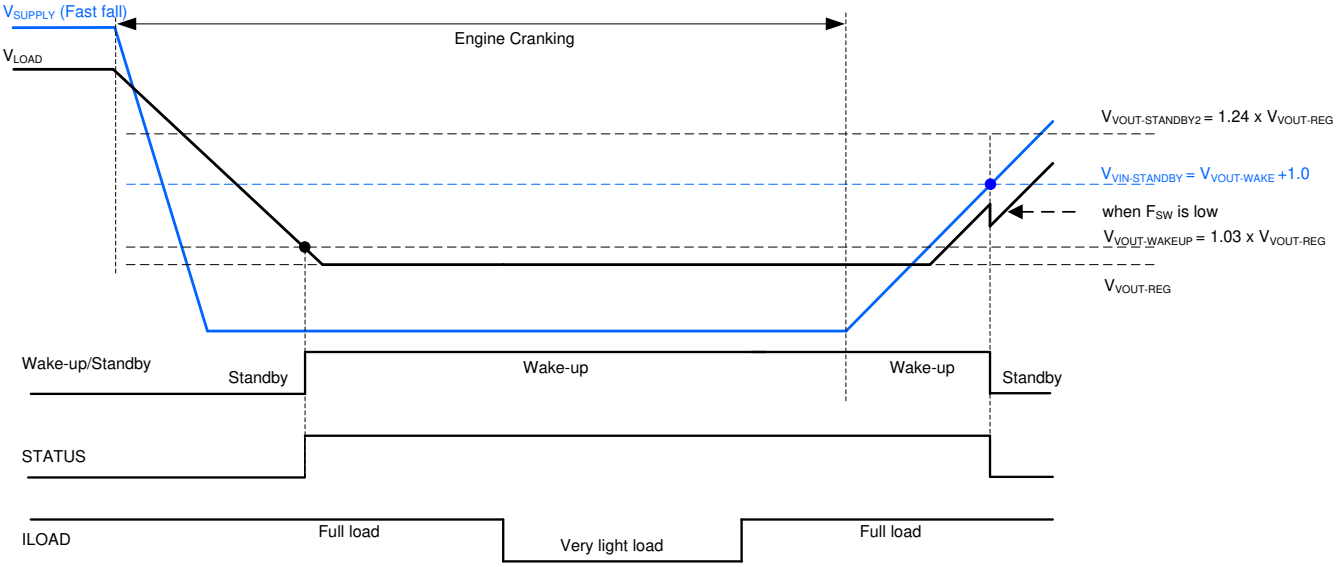


Figure 8-4. Automatic Wake-Up and Standby Operation in the SS Configuration (With Fast V_{SUPPLY} Fall and Slow Switching)

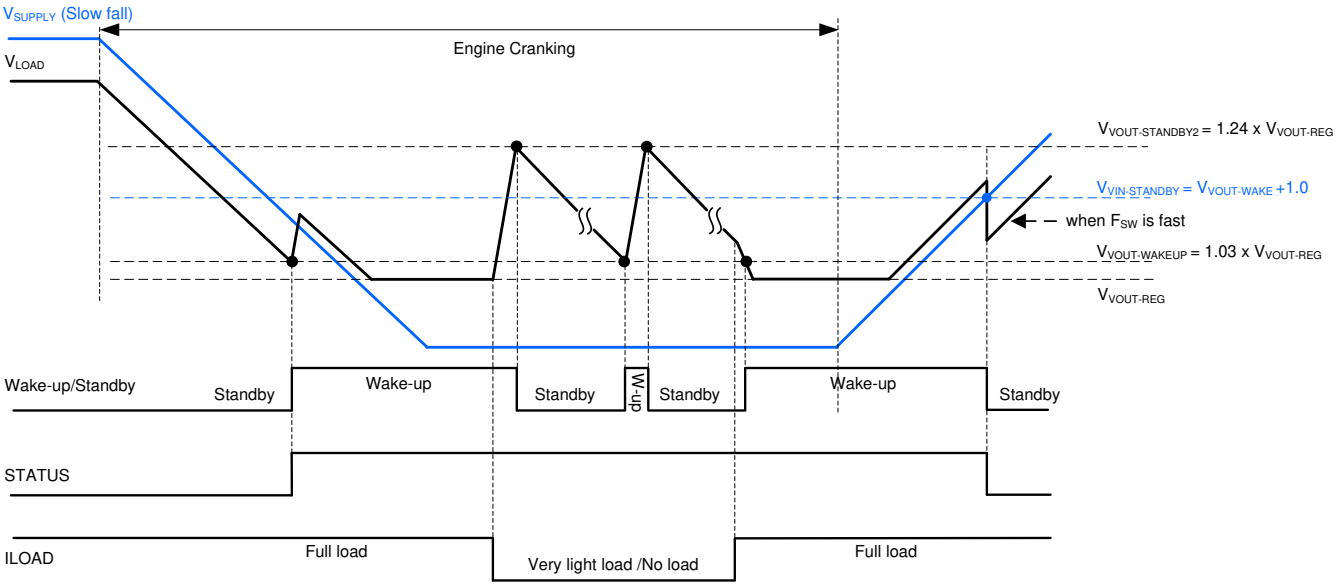


Figure 8-5. Automatic Wake-Up and Standby Operation in the SS Configuration (With Slow V_{SUPPLY} Fall and Fast Switching)

In EC configuration, the VOUT standby threshold is typically 6% higher than the VOUT regulation target. Because of the minimum duty cycle limit (see Section 8.4.3.2), the LM5150-Q1 alternates between the wake-up and the low I_Q standby modes at medium or light load. See Figure 8-8.

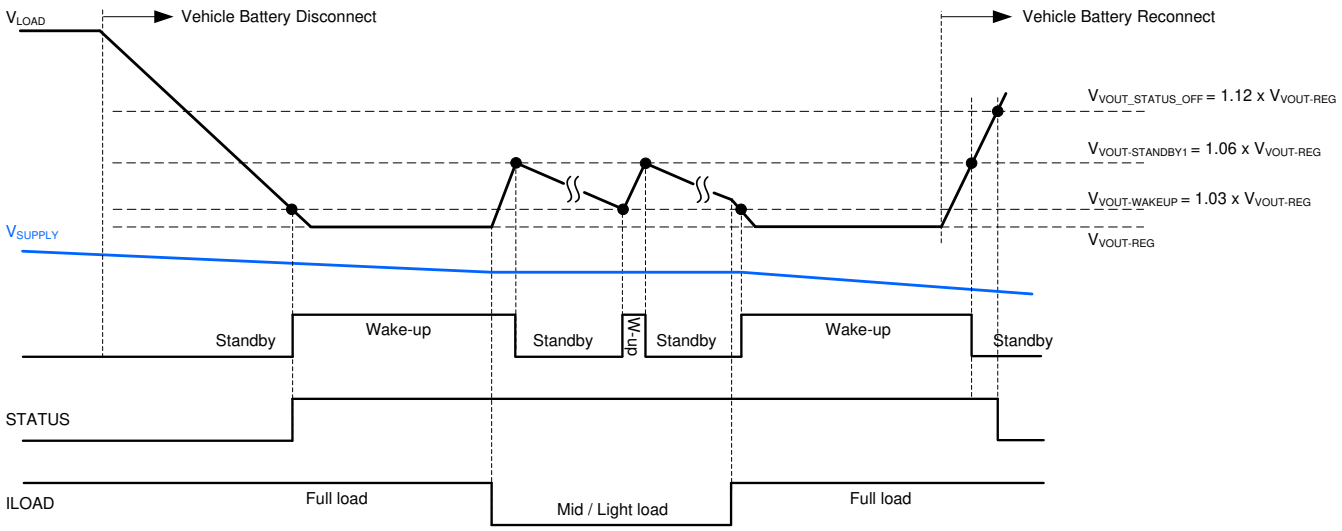


Figure 8-6. Automatic Wake-Up and Standby Operation in EC Configuration

To minimize output undershoot when waking up, the LM5150-Q1 boosts the VOUT regulation target during the first 128 cycles after the wake-up event. The regulation target becomes 3% higher than the original regulation target for 64 cycles, 2% higher for the next 32 cycles and 1% higher for the final 32 cycles. The VOUT pin voltage can rise up above the VOUT standby threshold even if switching stops at the VOUT standby threshold because the energy stored in the inductor transfers to the output capacitor when switching stops. See Section 8.4 for more information about the automatic wake-up and standby operation.

8.3.10 Boost Status Indicator (STATUS Pin)

STATUS is an open-drain output and requires a pullup resistor between 5 kΩ and 100 kΩ. The pin is pulled up after V_{VOUT} falls below the VOUT wake-up threshold, and is toggled to a low logic state when V_{VIN} rises above the VIN standby threshold in SS configuration or when V_{VOUT} rises above the VOUT status off-threshold in EC configuration. The pin is also pulled to ground when EN < 1 V and VOUT is greater than about 2 V, when AVCC < $V_{VCC-UVLO-FALLING}$ or during thermal shutdown.

8.3.11 Maximum Duty Cycle Limit, Minimum Input Supply Voltage

When designing a boost converter, the maximum duty cycle should be reviewed at the minimum supply voltage. The minimum input supply voltage which can achieve the target output voltage is estimated from Equation 9.

$$V_{SUPPLY(MIN)} \approx (V_{VOUT-REG} + V_F) \times (1 - D_{MAX}) \times \frac{F_{SYNC}}{F_{SW\_RT}} + I_{SUPPLY(MAX)} \times R_{DCR} + I_{SUPPLY(MAX)} \times (R_{DS(ON)} + R_S) \times D_{MAX} \quad (9)$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current
- R_{DCR} is the DC resistance of the inductor
- $R_{DS(ON)}$ is the on-resistance of the MOSFET

Substitute F_{SW_RT} for F_{SYNC} if the clock synchronization is not used. The minimum input supply voltage can be decreased by supplying F_{SYNC} which is less than F_{SW_RT}.

This maximum duty cycle limit (D_{MAX}) is 87% (typical), but can fall down below 80% if the external synchronization clock frequency is higher than 0.85 × $F_{SW\ (TYPICAL)}$. Select an F_{SYNC} which is within –25% and –15% of the $F_{SW\ (TYPICAL)}$ if 1:5 step-up ratio is required with clock synchronization. The minimum input supply voltage can be further decreased by supplying a lower frequency external synchronization clock. See Section 8.3.5 for more information.

8.3.12 MOSFET Driver (LO Pin)

The LM5150-Q1 provides an N-channel MOSFET driver which can source or sink a peak current of 1.5 A. The driver is powered by the 5-V VCC regulator and is enabled when the EN pin voltage is greater than 2 V and the AVCC pin voltage is greater than the AVCC UVLO threshold.

8.3.13 Thermal Shutdown

Internal thermal shutdown is provided to protect the LM5150-Q1 if the junction temperature exceeds 175°C (typical). When thermal shutdown is activated, the device is forced into a low power thermal shutdown state with the MOSFET driver and the VCC regulator disabled. After the junction temperature is reduced (typical hysteresis is 15ºC), the device is re-enabled.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

If the EN pin voltage is below 1 V, the LM5150-Q1 is in shutdown mode with all functions disabled except EN. In shutdown mode, the device reduces the VOUT pin current consumption to below 5.25 µA (typical) and the STATUS pin is pulled to ground. The device can be enabled by raising the EN pin above 2 V and operates in either the standby mode or the wake-up mode if V_{AVCC} is greater than the AVCC UVLO threshold.

Table 8-2. State of Each Pin in Shutdown Mode

STATUS	SYNC	RT	COMP	EN	VOUT	PVCC/AVCC	LO	CS	VIN	VSET
Grounded	Disabled	Disabled	Disabled	Enabled	$I_Q \le 5$ µA	Disabled	Grounded	Disabled	$I_Q \approx 0.1$ µA	Disabled

8.4.2 Standby Mode

If VOUT is greater than the VOUT standby threshold or VIN is greater than the VIN standby threshold in the SS mode, the LM5150-Q1 enters into standby mode.

In standby mode, most functions are disabled, including the thermal shutdown, to minimize the current consumption. The VOUT wake-up monitor is enabled in standby mode to allow wake-up if the VOUT voltage drops below the VOUT wake-up threshold. The VCC regulator reduces the sourcing capability to 17 mA in standby mode and the AVCC UVLO comparator is disabled.

The VOUT standby threshold effectively fulfills the overvoltage protection (OVP) function.

Table 8-3. State of Each Pin in Standby Mode

STATUS	SYNC	RT	COMP	EN	VOUT	PVCC/AVCC	LO	CS	VIN	VSET
Released or Grounded	Disabled	Disabled	Disabled	Enabled	$I_Q \le 15$ µA. VOUT wake-up monitor enabled	Enabled I_{PVCC} capability ≈ 17 mA	Grounded	Disabled	$I_Q \approx 0.1$ µA	Disabled

8.4.3 Wake-Up Mode

The LM5150-Q1 wakes up from standby mode if VOUT drops below the VOUT wake-up threshold. There are two configurations when the device wakes up. One is start-stop configuration (SS configuration) and the other is emergency-call configuration (EC configuration). The configuration is selectable by the VSET resistor (see Table 8-1).

8.4.3.1 Start-Stop Configuration (SS Configuration)

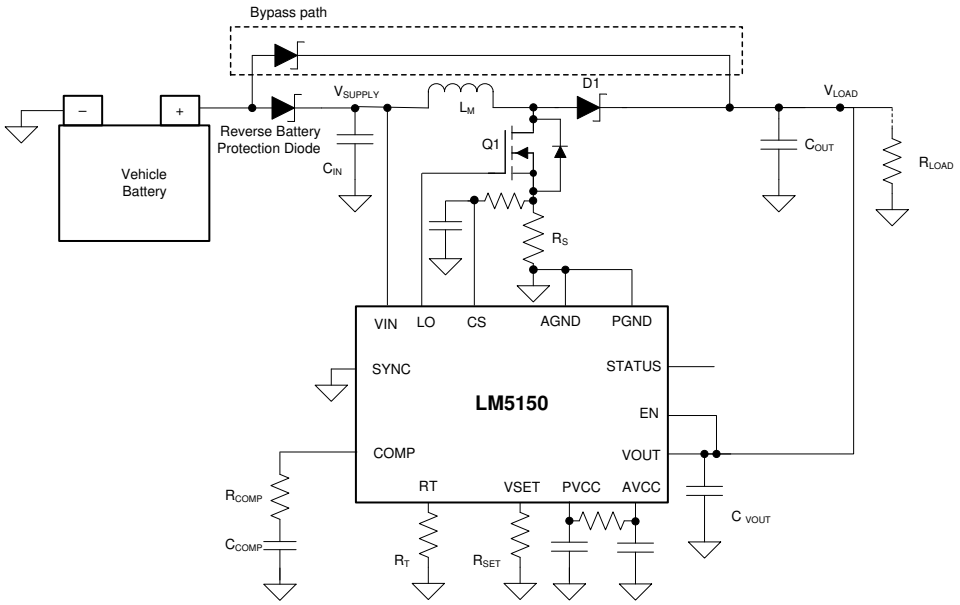


Figure 8-7. Typical Start-Stop Application

The LM5150-Q1 runs at fixed switching frequency without any pulse skipping in SS configuration. The device turns on the LO driver every cycle with T_{ON-MIN} until entering into standby mode, which helps to prevent EMI spectrum shifts. Because the MOSFET turns on every cycle, the boost converter output can be above the regulation target if the required on-time is less than T_{ON-MIN} when the boost supply voltage is close to the VOUT regulation target or the load current is very small. The output voltage will rise above the VOUT regulation target if the one of the inequalities below is true.

$$D \times \frac{1}{F_{SW}} < T_{ON-MIN} \tag{10}$$

$$\frac{(V_{SUPPLY} \times T_{ON-MIN})^2}{2 \times L_M} \times \frac{F_{SW}}{(V_{LOAD} + V_F - V_{SUPPLY})} > I_{LOAD} \tag{11}$$

In SS configuration, the LM5150-Q1 enters into the standby mode if VOUT is greater than the VOUT standby threshold—which is 24% higher than the VOUT regulation target—or if VIN is greater than the VIN standby threshold.

8.4.3.2 Emergency-Call Configuration (EC Configuration)

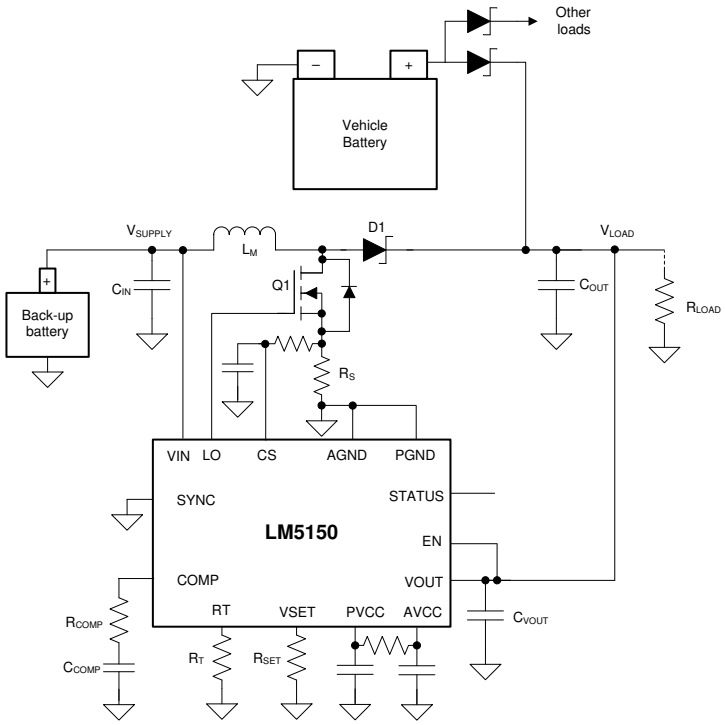


Figure 8-8. Typical Emergency Call Application

The EC configuration achieves high efficiency at light/medium load by alternating between the wake-up and low I_Q standby modes. In EC configuration, the LM5150-Q1 limits the minimum duty cycle programmed by V_{VOUT} and V_{VIN}. The minimum duty cycle limit is calculated using Equation 12.

$$D_{MIN} = 0.75 \times \left(1 - \frac{V_{VIN}}{V_{VOUT-REG}}\right) \tag{12}$$

Due to this minimum duty cycle limit, the boost converter sources more current than required when the load current is relatively small. As a result, the output voltage increases and eventually crosses the VOUT standby threshold which is typically 6% higher than the VOUT regulation target. The LM5150-Q1 then goes into the low I_Q standby mode. The LM5150-Q1 wakes up when VOUT drops below the VOUT wake-up threshold which is typically 3% higher than the VOUT regulation target. The device alternates between these two modes when the inequality below is true.

$$\frac{\left(V_{SUPPLY} \times \frac{D_{MIN}}{F_{SW}}\right)^2}{2 \times L_M} \times \frac{F_{SW}}{(V_{LOAD} + V_F - V_{SUPPLY})} > I_{LOAD} \tag{13}$$

Assuming V_{LOAD} = V_{VOUT} = $V_{VOUT-REG}$ and V_{SUPPLY} = V_{VIN}, the skip cycle operation starts when the inequality below is true.

$$\frac{\left(V_{SUPPLY} \times 0.75 \times \left(\frac{V_{LOAD} - V_{SUPPLY}}{V_{LOAD}}\right)\right)^2}{2 \times L_M \times F_{SW} \times (V_{LOAD} + V_F - V_{SUPPLY})} > I_{LOAD} \tag{14}$$

In EC configuration, the LM5150-Q1 does not generate any pulse if V_{COMP} is less than the 0.3 V and the required minimum duty cycle limit is zero.

If the peak current limit is triggered before reaching the minimum duty cycle, the device terminates the LO driver output immediately.

If VOUT is greater than the VOUT status-off threshold (typically 12% higher than the VOUT regulation target), the LM5150-Q1 pulls the STATUS pin low.

In EC configuration, light load efficiency is proportional with the inductor current ripple ratio.

Table 8-4. State of Each Pin in Wake-Up Mode

STATUS	SYNC	RT	COMP	EN	VOUT	PVCC/AVCC	LO	CS	VIN	VSET
Released	Enabled in SS configuration	Enabled	Enabled	Enabled	VOUT standby monitor is enabled. VOUT status-off monitor is enabled in EC configuration.	Enabled I_{PVCC} capability ≈ 75 mA	PWM	Enabled	I_Q ≈ 30 µA. VIN status-off monitor is enabled in SS configuration	Disabled

Table 8-5. Start-Stop versus Emergency-Call Configuration

CONFIGURATION	START-STOP	EMERGENCY-CALL
VOUT regulation options	6.8 V, 7.5 V, 8.5 V, 10.5 V	
VSET resistor value [Ω]	29.4 k, 19.1 k, 9.53 k, GND	90.9 k, 71.5 k, 54.9 k, 41.2 k
Clock Synchronization	Yes	No, SYNC should be grounded
VOUT wake-up threshold [V]	$V_{VOUT-REG}$ × 1.03	
VOUT standby threshold [V]	$V_{VOUT-REG}$ × 1.24	$V_{VOUT-REG}$ × 1.06
VOUT status-off threshold [V]	N/A	$V_{VOUT-REG}$ × 1.12
VIN standby threshold [V]	$V_{VOUT-REG}$ × 1.03 + 1.0 V	N/A
STATUS pin control (Open-drain with pullup resistor)	Released by VOUT wake-up Pulled down by VIN standby	Released by VOUT wake-up Pulled down by VOUT status-off
At heavy load when V_{VIN} « V_{VOUT}	Pulse width modulation (PWM)	
At light/no load when V_{VIN} « V_{VOUT}	LO turns on at every cycle in wake-up configuration. Skip cycle operation by alternating between wake-up and standby configurations.	
	Minimum on-time is limited	Minimum duty cycle is limited
When V_{VIN} ≈ V_{VOUT} or V_{VIN} ≥ V_{VOUT}	LO turns on at every cycle in wake-up configuration. On-time is limited by T_{ON-MIN}. VOUT goes out of regulation.	Duty cycle can drop to 0%. No pulses if V_{COMP} < 0.3 V and D_{MIN} ≤ 0%.
Maximum duty-cycle limit	Typically 87%	

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM5150-Q1 is a non-synchronous boost controller. The following design procedure can be used to select the external components for the LM5150-Q1. Alternately, the WEBENCH® software can be used to generate complete designs. The WEBENCH software uses an iterative design procedure and accesses comprehensive data bases of components when generating a design. This section presents a simplified discussion of the design process.

9.1.1 Bypass Switch / Disconnection Switch Control

The STATUS pin can be used to control an external bypass switch, which turns on when the boost is in standby mode, or to control an external disconnection switch that turns off when the boost is in standby mode. In Figure 9-1, a P-channel MOSFET is used to connect the boost supply input to the load directly when the boost is in standby mode. This bypass switch can be turned on slowly, but it must be turned off fast after the STATUS pin is pulled up by the wake-up event. The STATUS pin is rated to the absolute maximum 65 V.

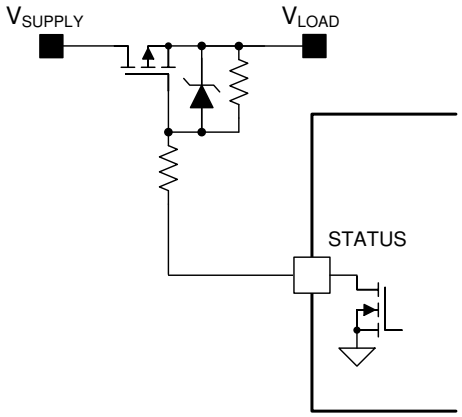


Figure 9-1. Bypass Switch Control Example

In Figure 9-2, a P-channel MOSFET is used to disconnect the boost supply output from the battery when boost is not required. This disconnection switch can be turned off slowly, but it must be turned on fast after the STATUS pin is pulled up by the wake-up event.

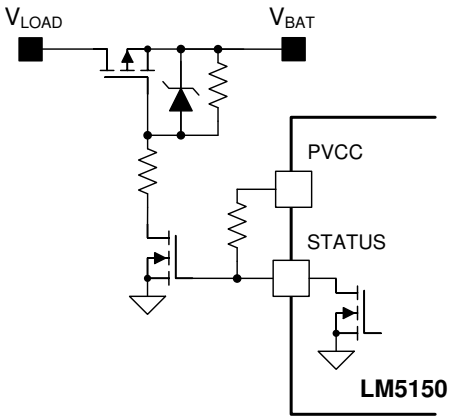


Figure 9-2. Disconnection Switch Control Example

9.1.2 Loop Response

The open-loop transfer function of a boost regulator is defined as the product of modulator transfer function and feedback transfer function.

The modulator transfer function of a current mode boost regulator including a power stage with an embedded current loop can be simplified as a one load pole (F_{LP}), one ESR zero (F_{Z_ESR}), and one Right Half Plane (RHP) zero (F_{RHP}) system, which can be explained as follows.

Modulator transfer function is defined as follows:

$$\frac{\hat{V}_{LOAD}(s)}{\hat{V}_{COMP}(s)} = A_M \times \frac{\left(1+\frac{s}{2\pi \times F_{Z\_ESR}}\right)\times\left(1-\frac{s}{2\pi \times F_{RHP}}\right)}{\left(1+\frac{s}{2\pi \times F_{LP}}\right)} \quad (15)$$

where

- $A_M = \frac{R_{LOAD}}{R_S \times 10} \times \frac{D'}{2}$
- $F_{LP} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}$ [Hz]
- $F_{Z_{ESR}} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$ [Hz]
- $F_{RHP} = \frac{R_{LOAD} \times (D')^2}{2\pi \times L_M}$ [Hz]

R_{ESR} is the equivalent series resistance (ESR) of the output capacitor which is specified in the capacitor data sheet.

R_{COMP}, C_{COMP}, and C_{HF} (see Figure 9-3) configure the error amplifier gain and phase characteristics to produce a stable voltage loop with fast response. This compensation network creates a dominant pole at low frequency (F_{DP_EA}), a mid-band zero (F_{Z_EA}), and a high frequency pole (F_{P_EA}).

The feedback transfer function is defined as follows:

$$-\frac{\hat{V}_{COMP(S)}}{\hat{V}_{LOAD(S)}} = A_{FB} \times \frac{\left(1+\frac{s}{2\pi \times F_{Z\_EA}}\right)}{\left(1+\frac{s}{2\pi \times F_{DP\_EA}}\right) \times \left(1+\frac{s}{2\pi \times F_{P\_EA}}\right)} \quad (16)$$

where

- $A_{FB} = \frac{1.2}{V_{LOAD}} \times R_O \times Gm$
- $F_{DP\_EA} = \frac{1}{2\pi \times R_O \times C_{COMP}}[Hz]$
- $F_{Z\_EA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}[Hz]$
- $F_{P\_EA} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)} \approx \frac{1}{2\pi \times R_{COMP} \times C_{HF}}[Hz]$

R_O (≈ 10 MΩ) is the output resistance of the error amplifier and Gm (≈ 2 mA/V) is the transconductance of the error amplifier.

Assuming F_{LP} is canceled by F_{Z_EA}, F_{RHP} is much higher than crossover frequency (F_{CROSS}), and F_{Z_ESR} is either canceled by F_{P_EA} or F_{Z_ESR} is much higher than F_{CROSS}, the open-loop transfer function can be simplified as follows:

$$T(s) = A_M \times A_{FB} \times \frac{1}{\left(1+\frac{s}{2\pi \times F_{DP\_EA}}\right)} \quad (17)$$

Because |T(s)| = 1 at the crossover frequency, the crossover frequency can be simply estimated using those assumptions.

$$F_{CROSS} \approx \frac{\sqrt{[A_M \times A_{FB}]^2 - 1}}{2\pi \times R_O \times C_{COMP}}[Hz] \quad (18)$$

9.2 Typical Application

The LM5150-Q1 requires a minimum number of external components to work. Figure 9-3 includes all optional components as an example.

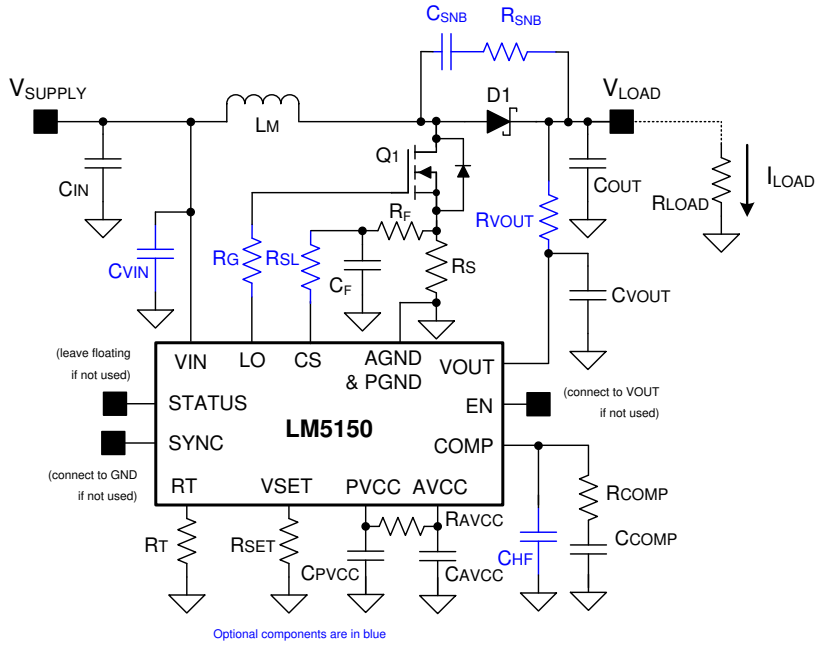


Figure 9-3. Typical Circuit With Optional Components

9.2.1 Design Requirements

Table 9-1 lists the design parameters for Figure 9-3.

Table 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Target Application	Start-stop
Minimum Input Supply Voltage ($V_{SUPPLY(MIN)}$)	2.5 V
Target Output Voltage (V_{LOAD})	8.5 V
Maximum Load Current (I_{LOAD})	2.94 A (≈ 25 Watt)
Switching Frequency (F_{SW})	440 kHz
D1 Diode Forward Voltage Drop	0.7 V
Maximum Inductor Current Ripple Ratio (RR)	0.6 (= 60%)
Estimated Full Load Efficiency (Eff)	0.8 (= 80%)
Current Limit Margin (M_{CL})	1.2 (= 120%)
F_{LP} over F_{CROSS} (K1)	0.15 (F_{LP} = 0.15 × F_{CROSS})
F_{Z_EA} over F_{LP} (K2)	3 (F_{Z_EA} = 3 × F_{LP})

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5150-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 R_{SET} Resistor

Select the value of R_{SET}, referring to Table 8-1. 9.53 kΩ is chosen to target 8.5 V in SS configuration. In general, about 5% to approximately 10% output undershoot should be considered when selecting the VOUT regulation target.

9.2.2.3 R_T Resistor

The value of R_T for 440-kHz switching frequency is calculated as follows:

$$R_T = \frac{2.233 \times 10^{10}}{F_{SW\_RT(TYPICAL)}} - 619 = \frac{2.233 \times 10^{10}}{440\,k} - 619 = 50.1\,k\Omega \quad (19)$$

A standard value of 49.9 kΩ is chosen for RT.

In general, higher frequency boost converters are smaller and faster, but they also have higher switching losses and lower efficiency.

9.2.2.4 Inductor Selection (L_M)

When selecting the inductor, consider three key parameters: inductor current ripple ratio (RR), falling slope of the inductor current, and RHP zero frequency (F_{RHP}).

Inductor current ripple ratio is selected to have a balance between core loss and copper loss. The falling slope of the inductor current must be low enough to prevent subharmonic oscillation at high duty cycle (additional R_{SL} resistor is required if not). Higher F_{RHP} (= lower inductance) allows a higher crossover frequency and is always preferred when using a smaller value output capacitor.

The inductance value can be selected to set the inductor current ripple between 30% and 70% of the average inductor current as a good compromise between RR, F_{RHP}, and inductor falling slope. In this example, 60% ripple ratio (RR = 0.6) is selected as the maximum inductor current ripple ratio (the inductor current ripple ratio is the biggest when D = 0.33). The target inductance value is calculated as follows:

$$L_{M(TARGET)} = \frac{0.14 \times R_{LOAD}}{RR \times F_{SW}} = \frac{0.14 \times \frac{8.5}{2.94}}{0.6 \times 440k} = 1.53\mu[H] \quad (20)$$

$$L_{M(GUIDE)} = \frac{\left(V_{LOAD} - V_{SUPPLY(MIN)}\right) \times V_{SUPPLY(MIN)}}{F_{SW} \times V_{LOAD} \times I_{LOAD}} = \frac{(8.5 - 2.5) \times 2.5}{440k \times 8.5 \times 2.94} = 1.36\mu[H] \quad (21)$$

If the target inductance is smaller than the value calculated using Equation 21, consider adding the slope compensation resistor (R_{SL}), as mentioned in Section 9.2.2.6, or select a smaller RR and recalculate the inductance using Equation 20.

A standard value of 1.5 µH is chosen for L_M. The required inductor saturation current rating is estimated after selecting R_S and R_{SL}.

9.2.2.5 Current Sense (R_S)

Based on the assumptions that 20% of current limit margin (M_{CL} = 1.2), 80% estimated efficiency (Eff = 0.8) at full load and no R_{SL} populated, R_S is calculated using Equation 22 and Equation 23.

$$R_S = \frac{1.2 + 0.6 \times \frac{(V_{VOUT} - V_{VIN})}{V_{VOUT-REG}} - 10 \times 30\mu A \times (2k\Omega + R_{SL}) \times \frac{F_{SW\_RT}}{F_{SYNC}} \times D}{10 \times \left(\frac{V_{LOAD} \times I_{LOAD}}{V_{SUPPLY(MIN)} \times Eff} + \frac{1}{2} \times \frac{V_{SUPPLY(MIN)} \times D \times \frac{1}{F_{SYNC}}}{L_M} \right) \times M_{CL}} [\Omega] \quad (22)$$

$$R_S = \frac{1.2 + 0.6 \times \frac{(8.5 - 2.5)}{8.5} - 10 \times 30\mu \times (2k + 0) \times 1 \times \left(1 - \frac{2.5}{8.5 + 0.7}\right)}{10 \times \left(\frac{8.5 \times 2.94}{2.5 \times 0.8} + \frac{1}{2} \times \frac{2.5 \times \left(1 - \frac{2.5}{8.5 + 0.7}\right) \times \frac{1}{440k}}{1.5u} \right) \times 1.2} = 7.12m[\Omega] \quad (23)$$

Substitute F_{SW_RT} for F_{SYNC} if the clock synchronization is not used.

A standard value of 7 mΩ is chosen for R_S. A low-ESL resistor is recommended to minimize the error caused by the ESL.

9.2.2.6 Slope Compensation Ramp (R_{SL})

The minimum inductance value which can prevent subharmonic oscillation without R_{SL} is calculated using Equation 24. If the selected inductance value is less than the minimum inductance calculated using Equation 24, add a slope compensation resistor (R_{SL}) externally.

$$L_{M(MIN)} = 0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY(MIN)}}{60m \times F_{SW}} \times R_S \times Margin = 0.5 \times \frac{(8.5 + 0.7) - 2.5}{60m \times 440k} \times 7m \times 1.2 = 1.07\mu[H] \quad (24)$$

1.2 is the recommended margin to cover non-ideal factors.

If needed, use Equation 25 to find the R_{SL} value which matches the typical amount of slope compensation.

$$R_{SL} = 0.82 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY(MIN)}}{L_M \times F_{SW} \times 30\mu A} \times R_S - 2k[\Omega] \quad (25)$$

In this example, R_{SL} is not populated because the selected inductance value, 1.5 µH, is greater than the minimum required inductance from Equation 24.

After selecting R_S and R_{SL}, the peak inductor current at current limit ($I_{PEAK-CL}$) can be calculated. Setting the inductor saturation current rating higher than the $I_{PEAK-CL}$ is recommended.

$$I_{PEAK-CL} = \frac{V_{CL} - 10 \times 30\mu A \times (2k\Omega + R_{SL}) \times \frac{F_{SW\_RT}}{F_{SYNC}} \times D}{10 \times R_S} + \frac{V_{SUPPLY(MIN)}}{L_M} \times T_D[A] \quad (26)$$

$$I_{PEAK-CL} = \frac{1.2 + 0.6 \times \frac{(8.5 - 2.5)}{8.5} - 10 \times 30\mu \times 2k \times 1 \times \left(1 - \frac{2.5}{8.5 + 0.7}\right)}{10 \times 7m} + \frac{2.5}{1.5u} \times 20n = 16.9[A] \quad (27)$$

T_D is the typical propagation delay of current limit.

9.2.2.7 Output Capacitor (C_{OUT})

There are a few ways to select the proper value of output capacitor (C_{OUT}). The output capacitor value can be selected based on output voltage ripple, output overshoot, or undershoot due to load transient. In this example, C_{OUT} is selected based on output undershoot because the waking up performance is similar with no-load to full-load transient performance.

The output undershoot becomes smaller by increasing F_{CROSS} or by decreasing F_{LP}: a smaller C_{OUT} is allowed by increasing F_{CROSS} or by decreasing F_{LP}.

To increase F_{CROSS}, F_{SW}, and F_{RHP} must be increased because the maximum F_{CROSS} is, in general, limited at 1/10 of F_{RHP} at $V_{SUPPLY(MIN)}$ or 1/10 of F_{SW} whichever is lower.

F_{RHP} is calculated using Equation 28.

$$F_{RHP} = \frac{R_{LOAD} \times \left(\frac{V_{SUPPLY(MIN)}}{V_{LOAD} + V_F}\right)^2}{2\pi \times L_M} = \frac{\frac{8.5}{2.94} \times \left(\frac{2.5}{8.5 + 0.7}\right)^2}{2\pi \times 1.5u} = 22.6k[Hz] \quad (28)$$

F_{CROSS} is selected at 1/10 of F_{RHP} or 1/10 of F_{SW}, whichever is lower.

$$\frac{F_{RHP}}{10} = 2.27\ kHz \quad (29)$$

$$\frac{F_{SW}}{10} = \frac{440\ k}{10} = 44\ kHz \quad (30)$$

In this example, 2.27 kHz is selected as a target F_{CROSS} and F_{LP} is selected to be 340 Hz (K1 = 0.15).

In general, there is about 5% or less undershoot with F_{LP} = 0.1 × F_{CROSS} (K1 = 0.1) and 10% or less undershoot with F_{LP} = 0.2 × F_{CROSS} (K1 = 0.2) during 0% to 100% load transient. The recommended K1 factor range is from 0.02 to 0.2.

F_{LP} is calculated using Equation 31.

$$F_{LP} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}[Hz] \quad (31)$$

The minimum required output capacitance value is calculated using Equation 32.

$$C_{OUT} = \frac{2}{2\pi \times R_{LOAD} \times F_{LP}} = \frac{2}{2\pi \times \frac{8.5}{2.94} \times 340} = 324\ \mu F \quad (32)$$

The maximum output ripple current is calculated at the minimum input supply voltage as follows:

$$I_{RIPPLE\_COUT(MAX)} = \frac{V_{LOAD} \times I_{LOAD}}{2 \times V_{SUPPLY(MIN)}} = \frac{8.5 \times 2.94}{2 \times 2.5} = 5[A] \quad (33)$$

The ripple current rating of the output capacitors must be enough to handle the output ripple current. By using multiple output capacitors, the ripple current can be split. In practice, ceramic capacitors are placed closer to the diode and the MOSFET than the bulk aluminum capacitors to absorb the majority of the ripple current.

In this example, three 100-µF capacitors are placed in parallel to ensure ripple current capability. If high-ESR capacitors are used for the output capacitor, additional 10-µF ceramic capacitors can be placed close to the switching components to minimize switching noise.

9.2.2.8 Loop Compensation Component Selection and Maximum ESR

Based on Equation 18, C_{COMP} is calculated as follows:

$$C_{COMP(over\ damping)} = \frac{\sqrt{\left[A_M \times A_{FB}\right]^2 - 1}}{2\pi \times R_O \times F_{CROSS}} = \frac{\sqrt{\left[\frac{R_{LOAD}}{R_S \times 10} \times \frac{D'}{2} \times \frac{1.2}{V_{LOAD}} \times R_O \times Gm\right]^2 - 1}}{2\pi \times R_O \times F_{CROSS}} \quad (34)$$

$$C_{COMP(over\ damping)} = \frac{\sqrt{\left[\frac{\frac{8.5}{2.94}}{7m \times 10} \times \frac{\frac{2.5}{8.5+0.7}}{2} \times \frac{1.2}{8.5} \times 10M \times 2m\right]^2 - 1}}{2\pi \times 10M \times 2.27\,k} = 111\,nF \quad (35)$$

By selecting C_{COMP} following Equation 34, the typical phase margin is set to 90º and the loop response is overdamped. In this example, F_{Z_EA} is placed at three times higher frequency than F_{LP} to have lower phase margin but faster settling time (K2 = 3, target F_{Z_EA} is 1.02 kHz). Recommended range of F_{Z_EA} is from 1 × F_{LP} to 4 × F_{LP} (1 ≤ K2 ≤ 4). Practical crossover frequency will vary with K2 with a range of 0.5 × F_{CROSS} to 1.0 × F_{CROSS}.

$$C_{COMP} = \frac{C_{COMP(over\ damping)}}{K2} = \frac{111\,n}{3} = 37\,nF \quad (36)$$

A standard value of 33 nF is chosen for C_{COMP}.

R_{COMP} is selected to set the error amplifier zero at 1.02 kHz.

$$R_{COMP} = \frac{1}{2\pi \times C_{COMP} \times F_{Z\_EA}} = \frac{1}{2\pi \times 33\,n \times 1.02\,k} = 4.73\,k\Omega \quad (37)$$

A standard value of 4.64 kΩ is chosen for R_{COMP}.

C_{HF} is usually used to create a pole at high frequency (F_{P_EA}) to cancel F_{Z_ESR}. By using a small ESR capacitor, which can place F_{Z_ESR} greater than 10 × F_{CROSS}, the output capacitor ESR would not affect the loop stability. The maximum ESR, which does not affect the loop response, is calculated using Equation 38.

$$R_{ESR(MAX)} = \frac{1}{2\pi \times C_{OUT} \times F_{CROSS} \times 10} = \frac{1}{2\pi \times 330\,\mu F \times 2.27\,k\Omega \times 10} = 21\,m\Omega \quad (38)$$

;

9.2.2.9 PVCC Capacitor, AVCC Capacitor, and AVCC Resistor

The PVCC capacitor supplies the peak transient current to the LO driver. The value of PVCC capacitor (C_{PVCC}) must be 4.7 µF or higher and must be a high-quality, low-ESR, ceramic capacitor. C_{PVCC} must be placed close to the PVCC pin and the PGND pin. A value of 4.7 µF is selected for this design example. The AVCC capacitor must be placed close to the device. The recommended AVCC capacitor value is 0.1 µF. The AVCC resistor should be placed between PVCC and AVCC pins. The recommended AVCC resistor value is 10 Ω.

9.2.2.10 VOUT Filter (C_{VOUT}, R_{VOUT})

The VOUT pin is the input of the internal VCC regulator and also is the input of the output voltage sensing. To minimize noise at the VOUT pin, a 1-µF capacitor must be placed at the VOUT pin in most cases. If multiple output capacitors are used, one of them can be placed at the VOUT pin as C_{VOUT}. The VOUT capacitor must be a high-quality, low-ESR, ceramic capacitor and must be placed close to the device. A resistor can be added at the VOUT pin (R_{VOUT}) to form a RC filter (see Figure 9-3). In this case, the maximum resistor value should be less than or equal to 2 Ω.

9.2.2.11 Input Capacitor

The input capacitors reduce the input voltage ripple. Assuming high-quality ceramic capacitors are used for the input capacitors, the maximum input voltage ripple can be calculated by using Equation 39.

$$V_{RIPPLY(CIN)} = \frac{V_{LOAD}}{32 \times L_M \times C_{IN} \times F_{SW}^2} [V] \quad (39)$$

The required input capacitor value is a function of the impedance of the source power supply. More input capacitors are required if the impedance of the source power supply is not low enough. In the example, three 10-µF ceramic capacitors are used.

9.2.2.12 MOSFET Selection

The MOSFET gate driver of the LM5150-Q1 is powered by the internal 5-V VCC regulator. The MOSFET driven by the LM5150-Q1 must have a logic-level gate threshold with its on-resistance specified at 4.5 V or lower and must be rated to handle the maximum output voltage plus any switch node ringing. The maximum gate charge is limited by the 75-mA PVCC sourcing current limit, and is calculated as follows:

$$Q_{G(@5V)} < \frac{75m}{F_{SW}} [C] \quad (40)$$

A leadless package is preferred for high switching-frequency designs. The MOSFET gate capacitance should be small enough so that the gate voltage is fully discharged during the off-time.

9.2.2.13 Diode Selection

A Schottky is the preferred type for D1 diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current. To prevent chatter between wake-up and standby, the forward voltage drop of the D1 diode must be less than 0.95 V at full load.

9.2.2.14 Efficiency Estimation

The total loss of the boost converter (P_{TOTAL}) can be expressed as the sum of the losses in the LM5150-Q1 (P_{IC}), MOSFET power losses (P_Q), diode power losses (P_D), inductor power losses (P_L), and the loss in the sense resistor (P_{RS}).

$$P_{TOTAL} = P_{IC} + P_Q + P_D + P_L + P_{RS} [W] \quad (41)$$

P_{IC} can be separated into gate driving loss (P_G) and the losses caused by quiescent current (P_{IQ}).

$$P_{IC} = P_G + P_{IQ} [W] \quad (42)$$

Each power loss is approximately calculated as follows:

$$P_G = Q_{G(@5V)} \times V_{VOUT} \times F_{SW} [W] \quad (43)$$

$$P_{IQ} = V_{VOUT} \times I_{VOUT} + V_{VIN} \times I_{VIN} [W] \quad (44)$$

I_{VIN} and I_{VOUT} values in each mode can be found in the supply current section of Section 7.5.

P_Q can be separated into switching loss ($P_{Q(SW)}$) and conduction loss ($P_{Q(COND)}$).

$$P_Q = P_{Q(SW)} + P_{Q(COND)} [W] \quad (45)$$

Each power loss is approximately calculated as follows:

$$P_{Q(SW)} = 0.5 \times (V_{VOUT} + V_F) \times I_{SUPPLY} \times (t_R + t_F) \times F_{SW} [W] \quad (46)$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. I_{SUPPLY} is the input supply current of the boost converter.

$$P_{Q(COND)} = D \times {I_{SUPPLY}}^2 \times R_{DS(ON)} [W] \quad (47)$$

$R_{DS(ON)}$ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the $R_{DS(ON)}$ increase due to self-heating.

P_D can be separated into diode conduction loss (P_{VF}) and reverse recovery loss (P_{RR}).

$$P_D = P_{VF} + P_{RR} [W] \quad (48)$$

Each power loss is approximately calculated as follows:

$$P_{VF} = (1 - D) \times V_F \times I_{SUPPLY} [W] \quad (49)$$

$$P_{RR} = V_{LOAD} \times Q_{RR} \times F_{SW} [W] \quad (50)$$

Q_{RR} is the reverse recovery charge of the diode and is specified in the diode data sheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the output voltage is high.

P_L is the sum of DCR loss (P_{DCR}) and AC core loss (P_{AC}). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_L = P_{DCR} + P_{AC} [W] \quad (51)$$

Each power loss is approximately calculated as follows:

$$P_{DCR} = {I_{SUPPLY}}^2 \times R_{DCR} [W] \quad (52)$$

$$P_{AC} = K \times \Delta I^{\beta} {F_{SW}}^{\alpha} [W] \quad (53)$$

$$\Delta I = \frac{V_{SUPPLY} \times D \times \frac{1}{F_{SYNC}}}{L_M} \quad (54)$$

ΔI is the peak-to-peak inductor current ripple. K, α, and β are core dependent factors which can be provided by the inductor manufacturer.

P_{RS} is calculated as follows:

$$P_{RS} = D \times {I_{SUPPLY}}^2 \times R_S [W] \quad (55)$$

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \times 100[\%] \quad (56)$$

9.2.3 Application Curves

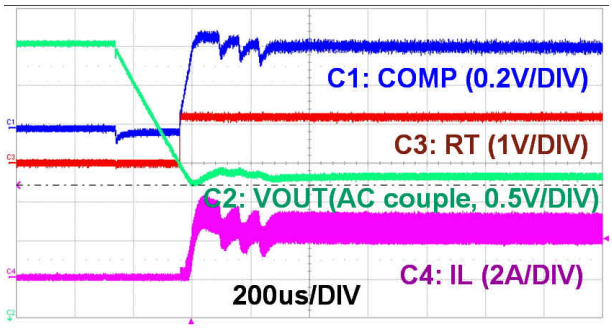


Figure 9-4. Automatic Wake-Up

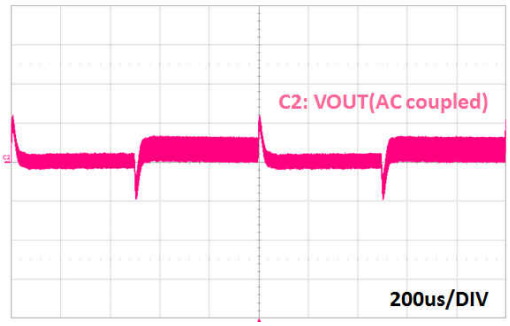


Figure 9-5. Load Transient (3 A to 1.5 A, 0.1 V/DIV)

9.3 System Examples

9.3.1 Lower Standby Threshold in SS Configuration

By connecting the VIN pin to the VOUT pin, the current limit threshold at the current limit comparator input (V_{CL}) is set to 1.2 V. In SS configuration, the VOUT standby threshold is ignored. The device goes into the standby mode when VOUT > VIN standby threshold.

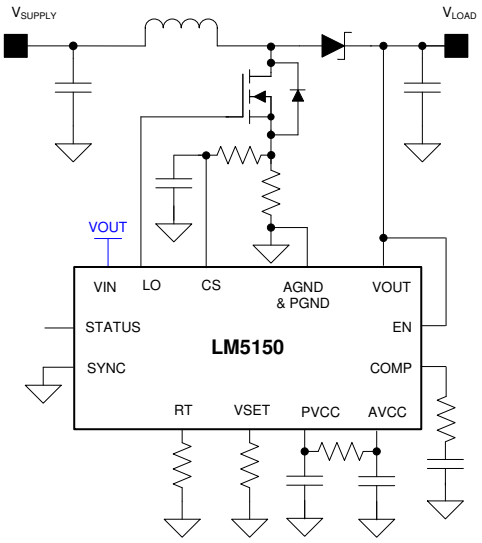


Figure 9-6. Lower Standby Threshold in SS Configuration

9.3.2 Dithering Using Dither Enabled Device

Dithering is achieved by connecting DITH output to the RT pin through a resistor.

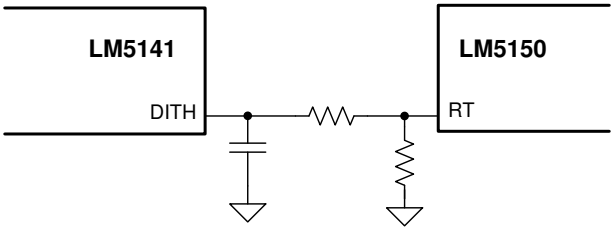


Figure 9-7. Dithering Using Dither Enabled Device LM5141

9.3.3 Clock Synchronization With LM5140

Clock synchronization can be achieved by connecting SYNCOUT of the LM5140 to SYNC.

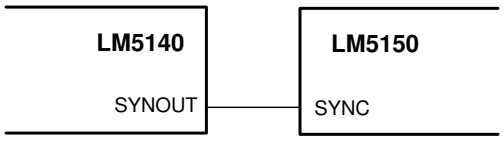


Figure 9-8. Clock Synchronization With LM5140

9.3.4 Dynamic Frequency Change

Switching frequency can be changed dynamically during operation by changing the RT resistor.

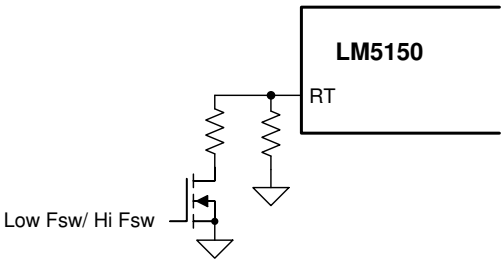


Figure 9-9. Dynamic Frequency Change

9.3.5 Dithering Using an External Clock

If a low-frequency clock is available, dithering can be achieved by injecting a ramp signal into RT.

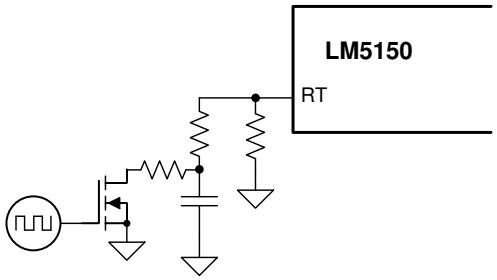


Figure 9-10. Dithering Using an External Clock

10 Power Supply Recommendations

The LM5150-Q1 is designed to operate from a power supply or a battery whose voltage range is from 1.5 V to 42 V. The input power supply should be able to supply the maximum boost supply voltage and handle the maximum input current at 1.5 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors can be required at the supply input of the converter.

11 Layout

11.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Place Q1, D1, and R_S first.
- Place ceramic C_{OUT} and make the switching loop (C_{OUT}-D1-Q1-R_S-C_{OUT}) as small as possible.
- Leave copper area next to D1 for thermal dissipation.
- Place LM5150-Q1 close to R_S.
- Place C_{PVCC} as close to the device as possible between PVCC and PGND.
- Connect PGND directly to the center of the sense resistor using a wide and short trace.
- Connect CS to the center of the sense resistor. Connect through vias if required. Connect filter capacitor between CS pin and exposed pad.
- Connect AGND directly to the analog ground plain and connect to R_{SET}, R_T, and C_{COMP}.
- Connect the exposed pad to the analog ground plain and the power ground plain through vias.
- Connect LO directly to the gate of Q1.
- Make the switching signal loop (LO-Q1-R_S-PGND-LO) as small as possible.
- Place C_{VOUT} as close to the device as possible.
- The LM5150-Q1 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

11.2 Layout Example

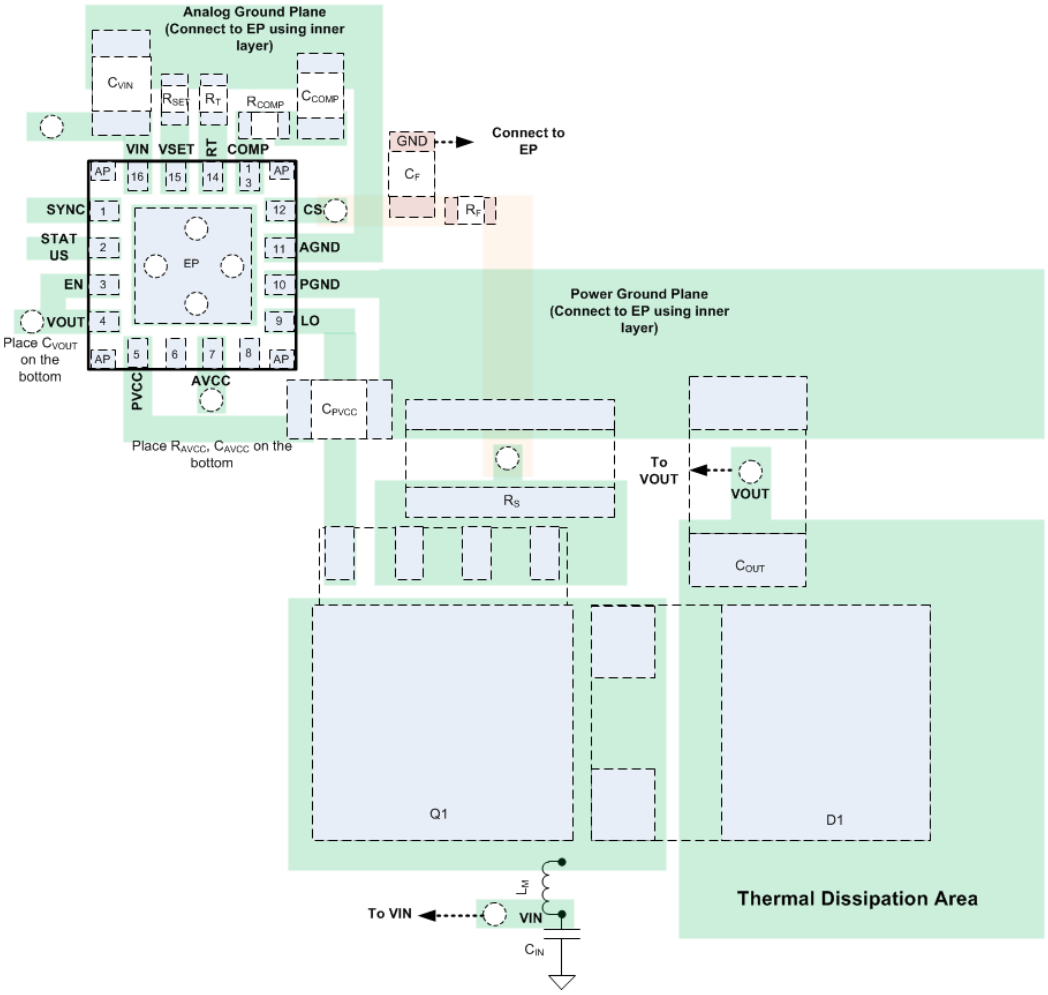


Figure 11-1. LM5150-Q1 PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5150-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5150QRUMRQ1	Active	Production	WQFN (RUM) | 16	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	LM5150 Q
LM5150QRUMTQ1	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	LM5150 Q
LM5150QURUMRQ1	Active	Production	WQFN (RUM) | 16	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	LM5150 QU
LM5150QWRUMRQ1	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5150 QW
LM5150QWRUMTQ1	Active	Production	WQFN (RUM) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5150 QW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

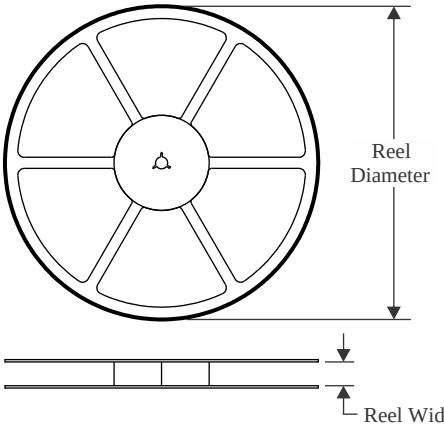
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

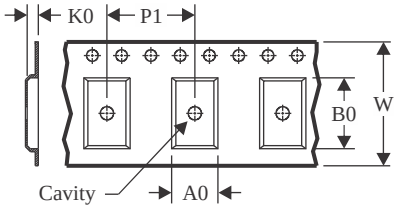
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

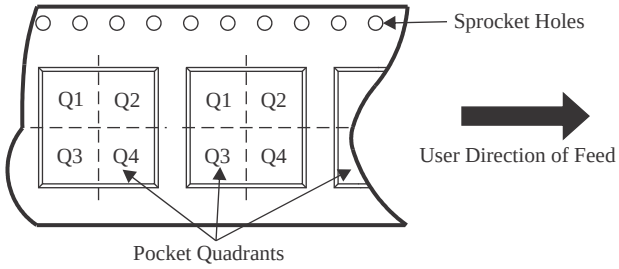


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

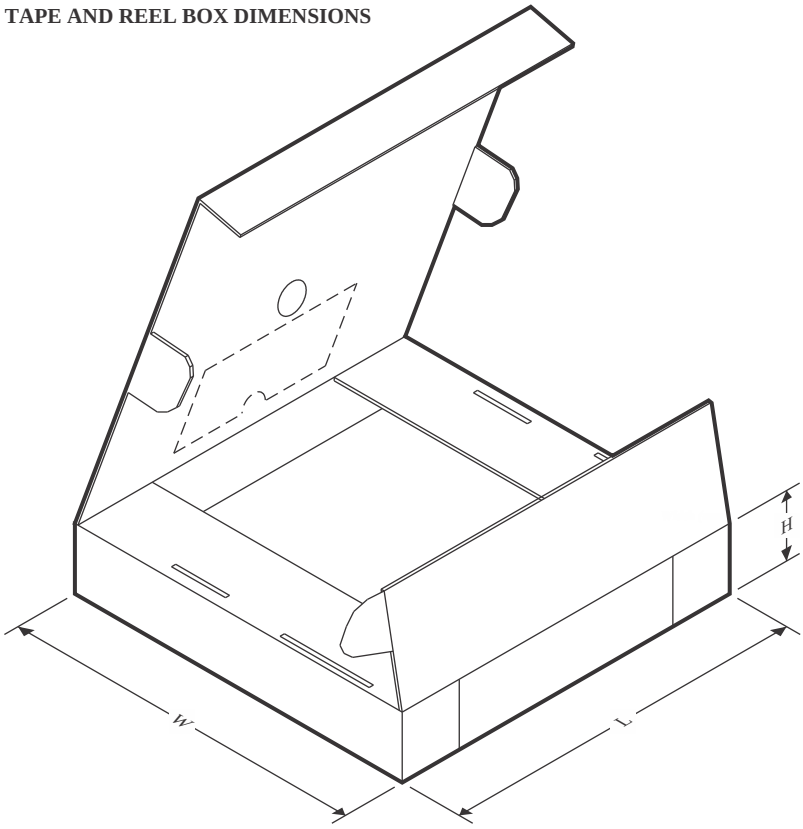
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5150QRUMRQ1	WQFN	RUM	16	2000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5150QRUMTQ1	WQFN	RUM	16	250	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5150QURUMRQ1	WQFN	RUM	16	2000	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5150QWRUMTQ1	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

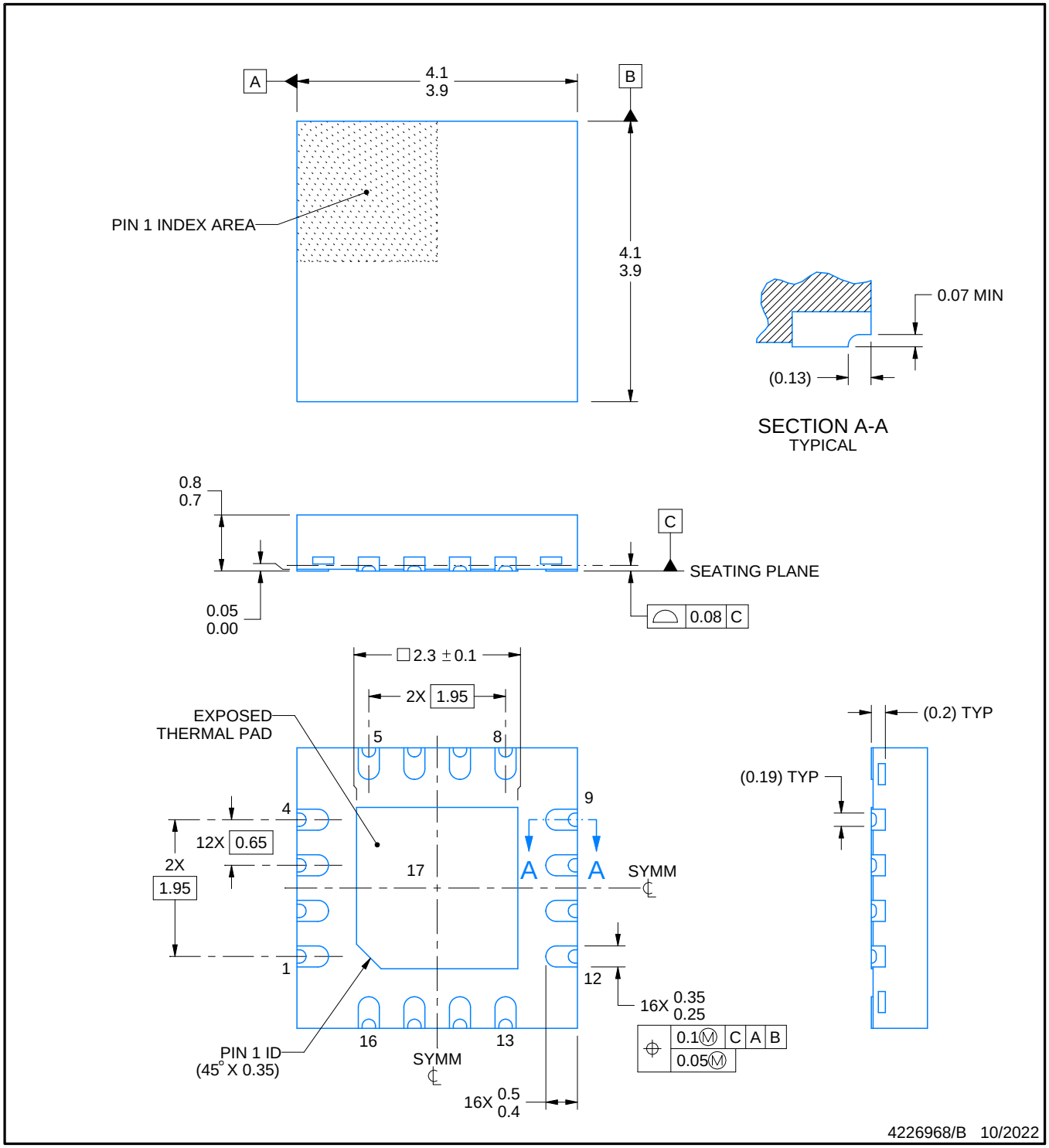
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5150QRUMRQ1	WQFN	RUM	16	2000	367.0	367.0	38.0
LM5150QRUMTQ1	WQFN	RUM	16	250	213.0	191.0	35.0
LM5150QURUMRQ1	WQFN	RUM	16	2000	367.0	367.0	38.0
LM5150QWRUMTQ1	WQFN	RUM	16	250	210.0	185.0	35.0

RUM0016G

PACKAGE OUTLINE

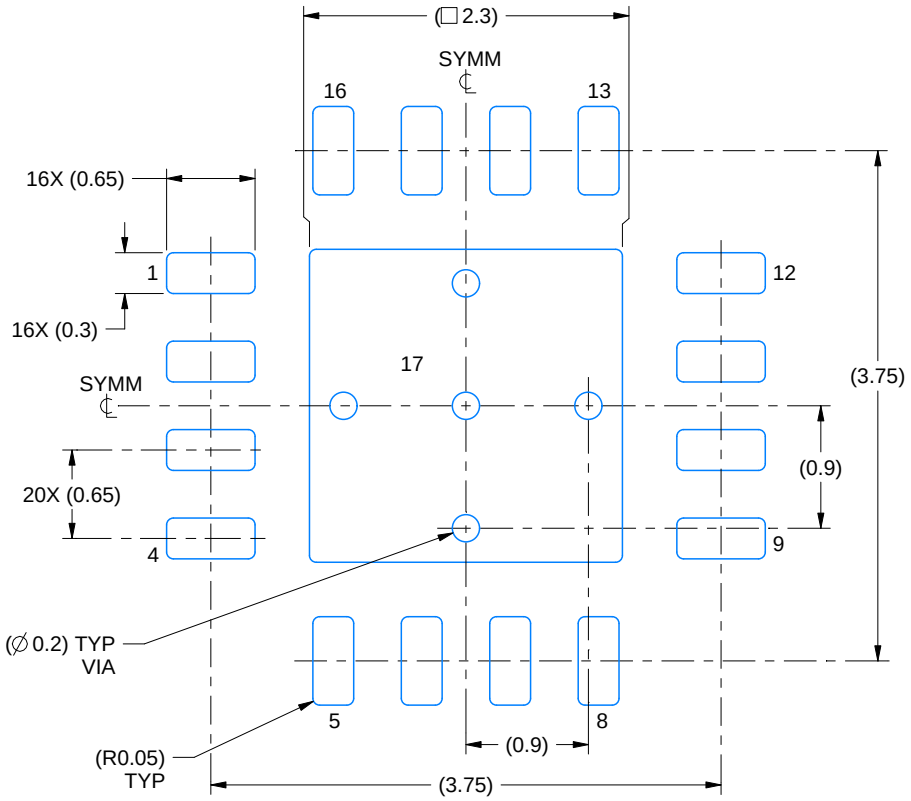
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

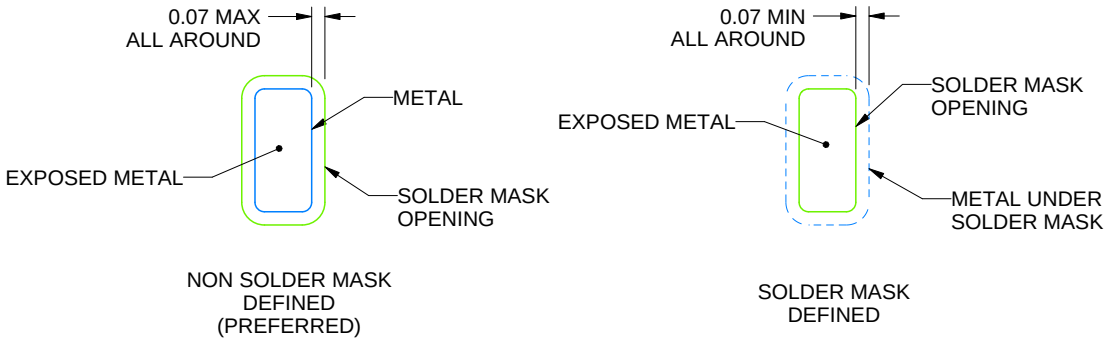


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

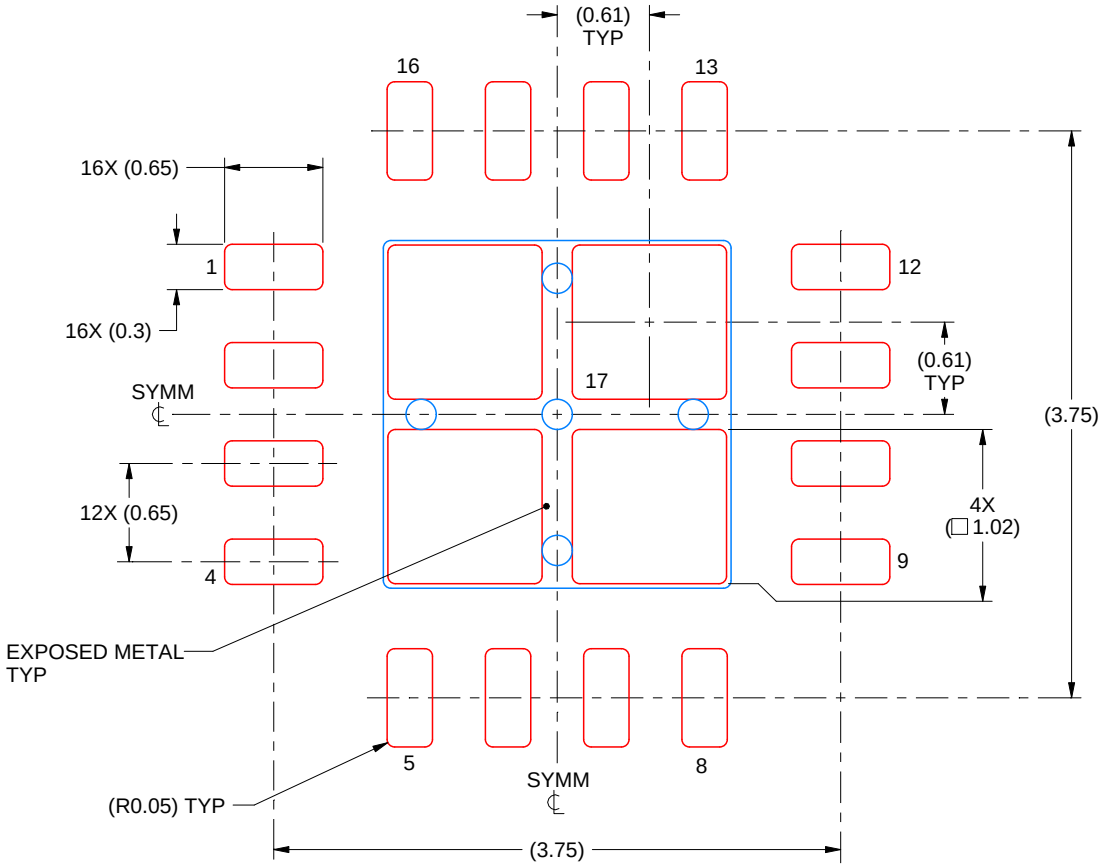


SOLDER MASK DETAILS

4226968/B 10/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
THERMAL PAD 17: 79% - PADS A1, A2, A3 & A4: 94%
SCALE:20X

4226968/B 10/2022

NOTES: (continued)

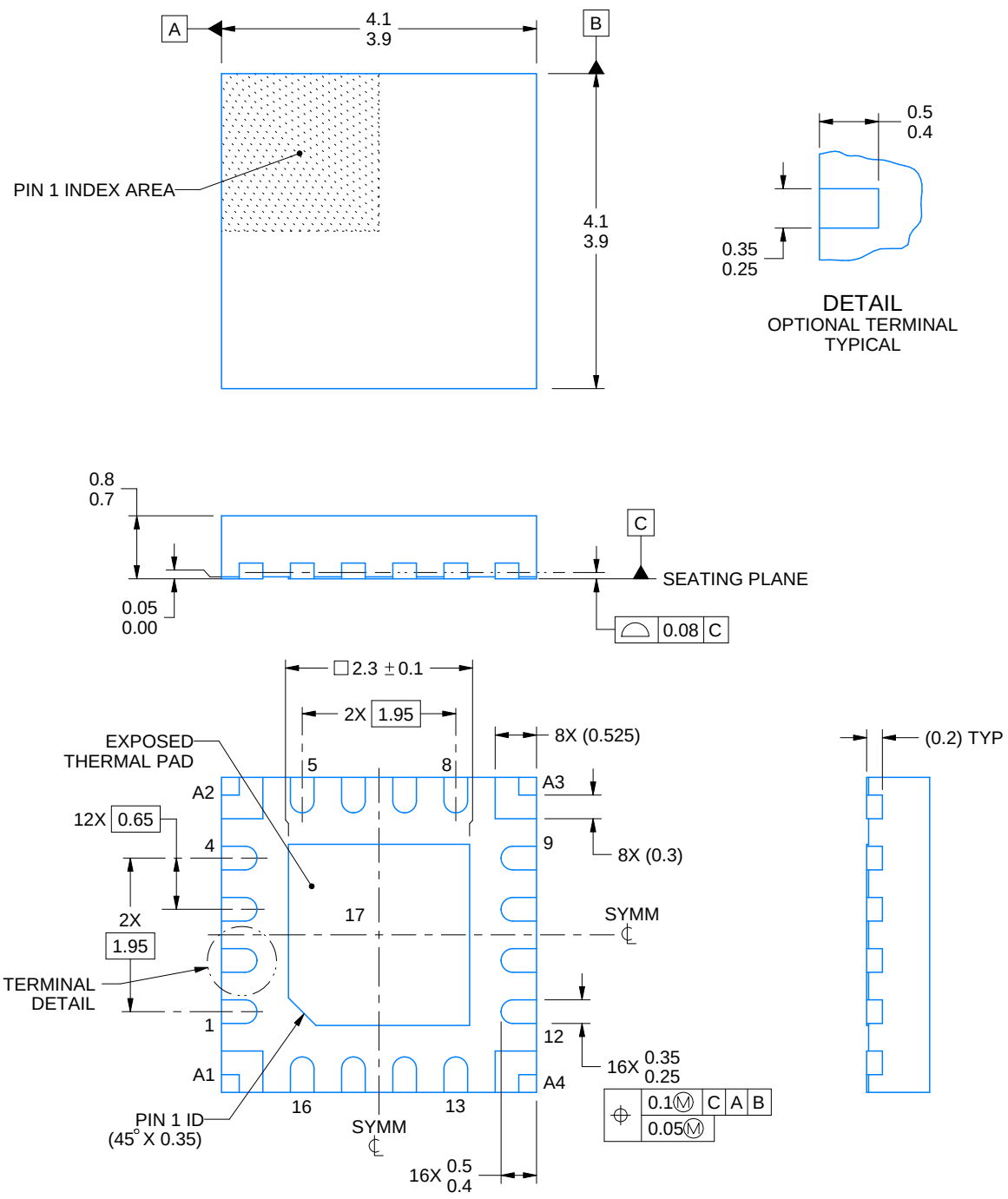
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUM0016F

PACKAGE OUTLINE

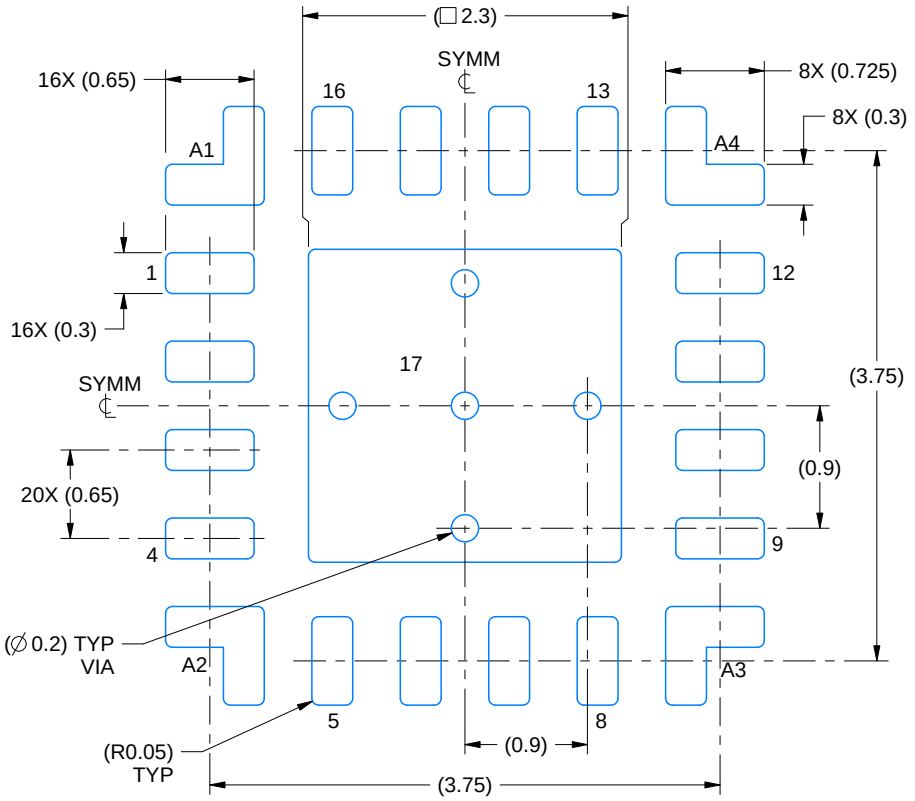
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

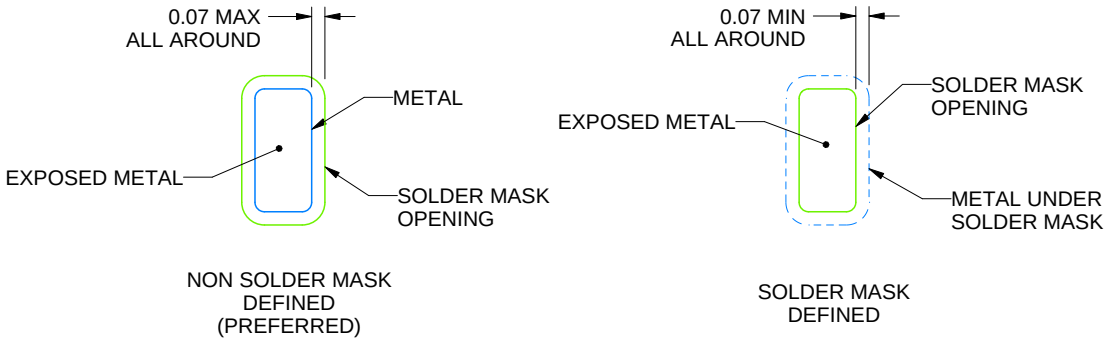


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

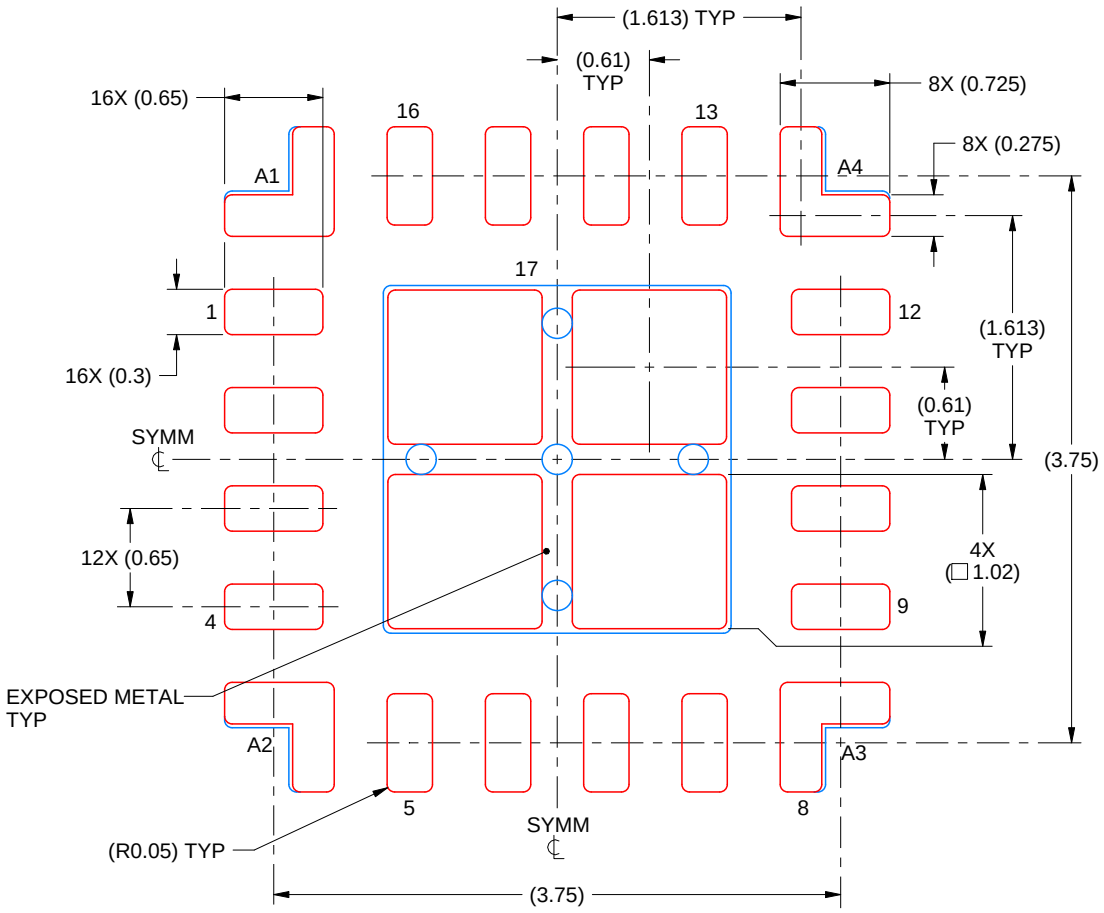


SOLDER MASK DETAILS

4226734/B 10/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
THERMAL PAD 17: 79% - PADS A1, A2, A3 & A4: 94%
SCALE:20X

4226734/B 10/2022

NOTES: (continued)

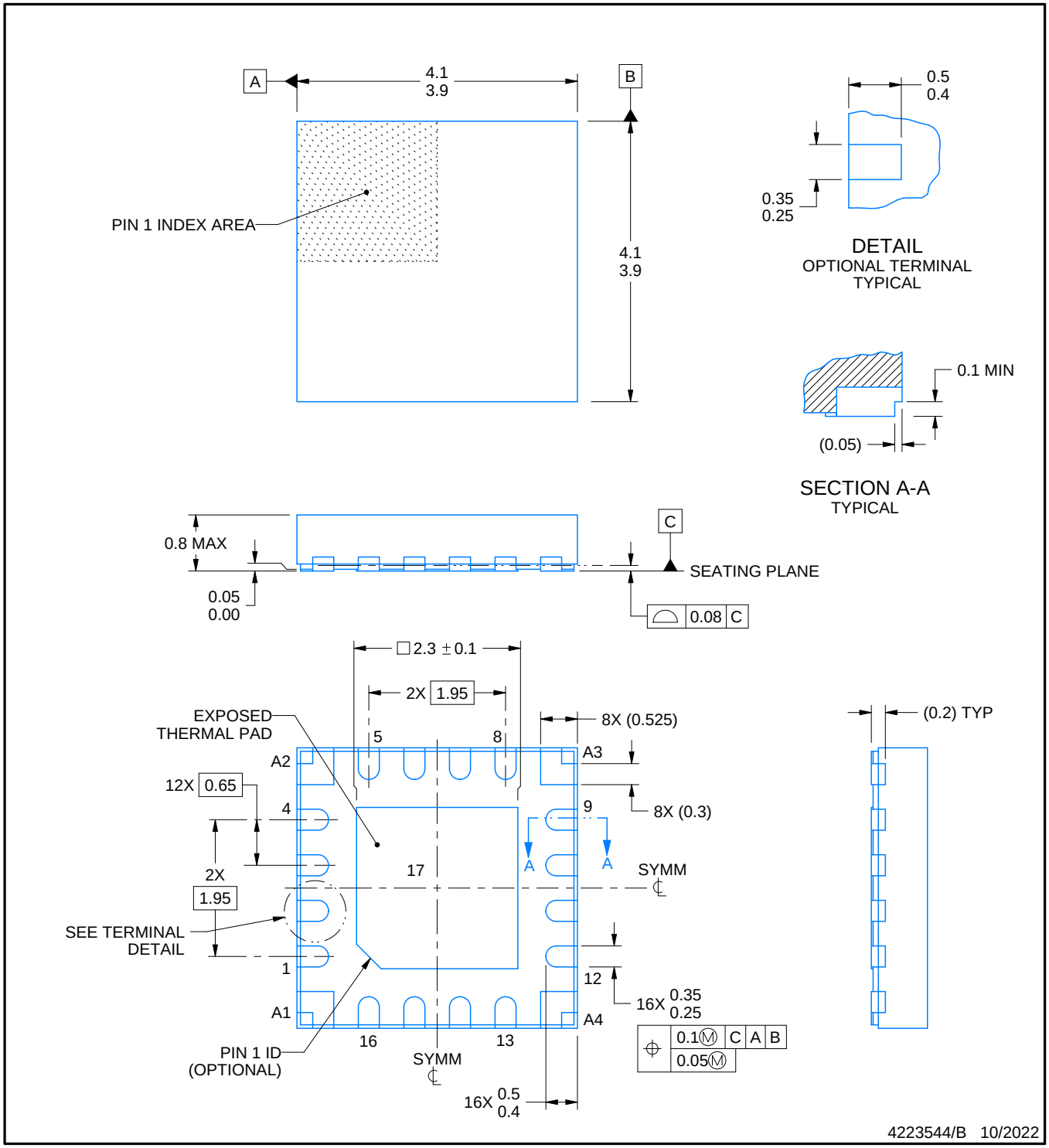
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUM0016C

PACKAGE OUTLINE

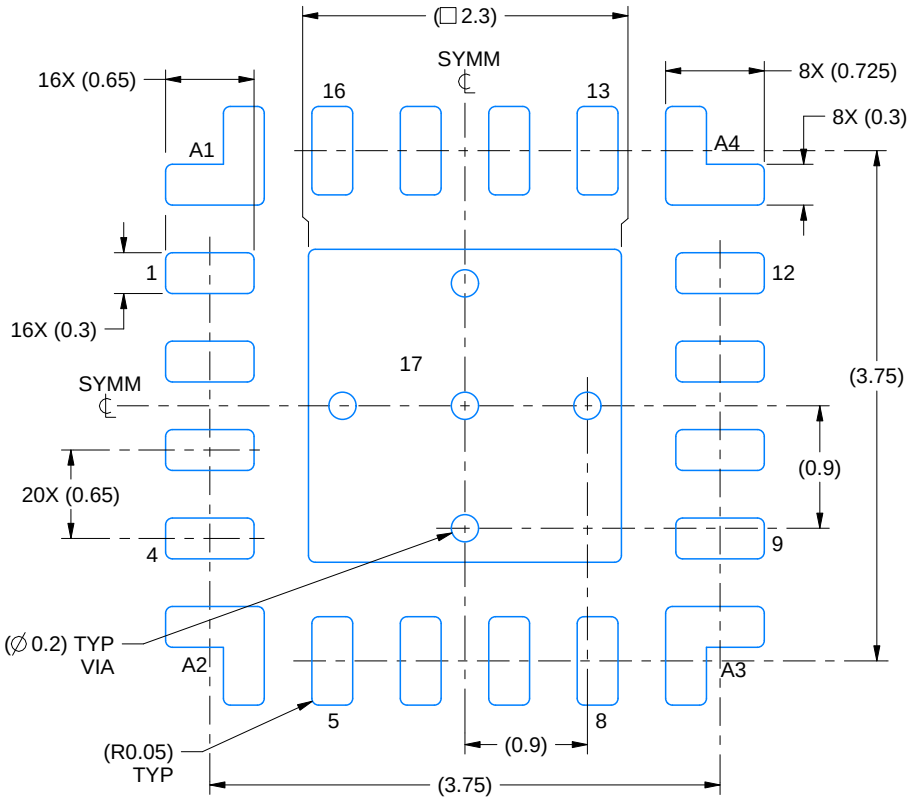
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

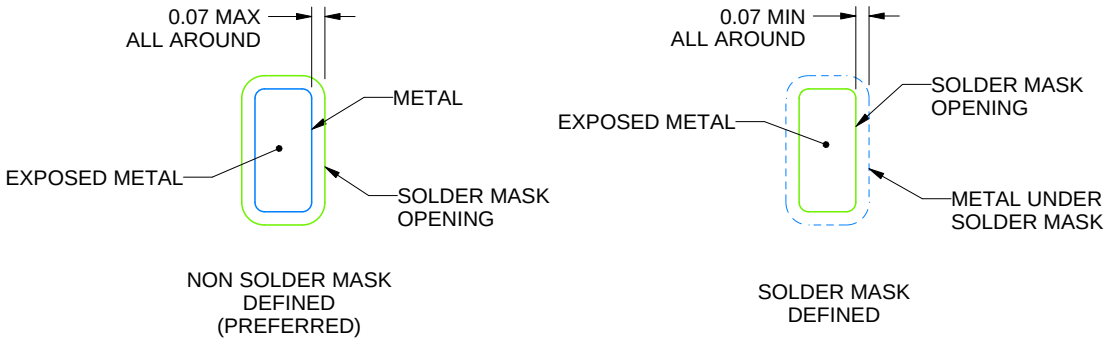


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

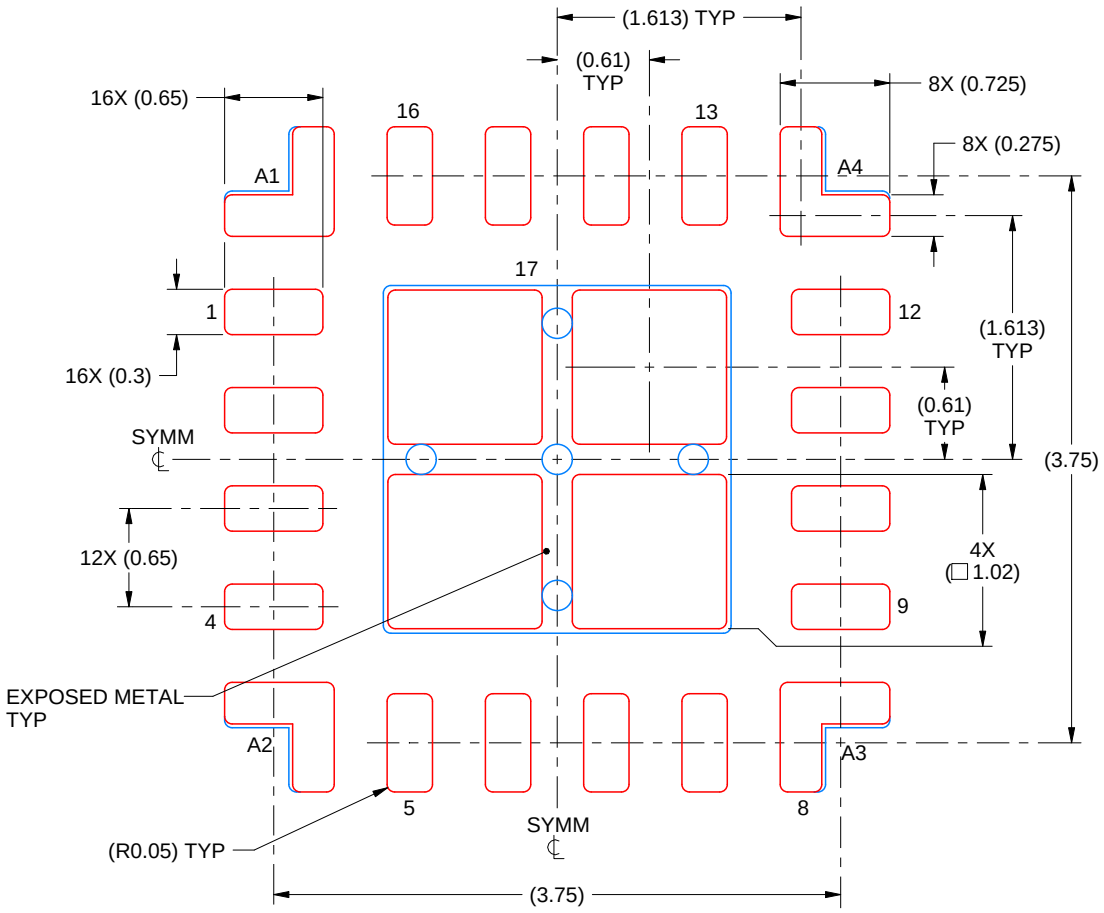


SOLDER MASK DETAILS

4223544/B 10/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
THERMAL PAD 17: 79% - PADS A1, A2, A3 & A4: 94%
SCALE:20X

4223544/B 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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