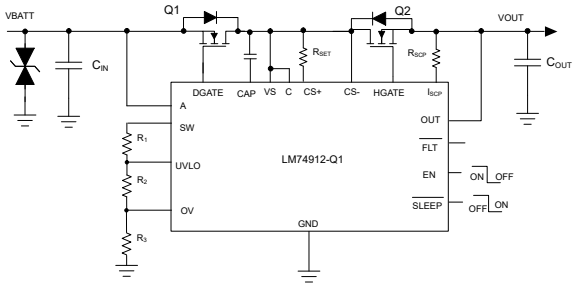
LM74912-Q1 Automotive Ideal Diode Controller With Fault Output and Overvoltage, Undervoltage, and Short Circuit Protection

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3-V to 65-V input range
- Reverse input protection down to –65 V
- Drives external back-to-back N-channel MOSFETs in common drain configuration
- Ideal diode operation with 10.5-mV A to C forward voltage drop regulation
- Low reverse detection threshold (–10.5 mV) with fast response (0.5 µs)
- 20-mA peak gate (DGATE) turn-on current
- 2.6-A peak DGATE turn-off current
- Adjustable overvoltage and undervoltage protection
- Output short circuit protection with MOSFET latched off state
- Ultra low power mode with 2.5-µA shutdown current (EN=Low)
- SLEEP mode with 6-µA current (EN=High, SLEEP=Low)
- Meets automotive ISO7637 transient requirements with a suitable transient voltage suppressor (TVS) diode
- Available in 4 mm × 4 mm 24-pin VQFN package

2 Applications

- Automotive battery protection
  - ADAS domain controller
  - Infotainment and cluster
  - Automotive external amplifier
- Active ORing for redundant power



Typical Application Circuit

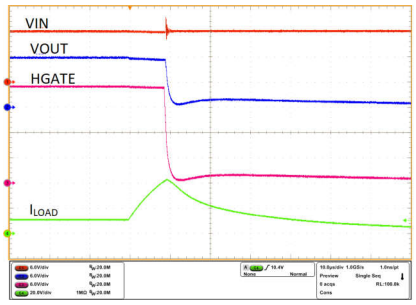
3 Description

The LM74912-Q1 ideal diode controller drives and controls external back to back N-channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control with overvoltage, undervoltage and output short circuit protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) in case of overcurrent and overvoltage events using HGATE control. The device has integrated current sense amplifier which provides external MOSFET VDS sense based short circuit protection with an adjustable current limit. When short circuit condition is detected on the output then device latches off the load disconnect MOSFET. The device features an adjustable overvoltage cut-off protection feature. The device features a SLEEP mode which enables ultra low quiescent current consumption (6 µA) and at the same time providing refresh current to the always ON loads when vehicle is in the parking state. The LM74912-Q1 has a maximum voltage rating of 65 V.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM74912-Q1	RGE (VQFN, 24)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Short Circuit Response

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4 Revision History

Changes from Revision * (July 2023) to Revision A (September 2023)	Page
• Changed the document status From: *Advance Information* To: *Production Data*	1

5 Pin Configuration and Functions

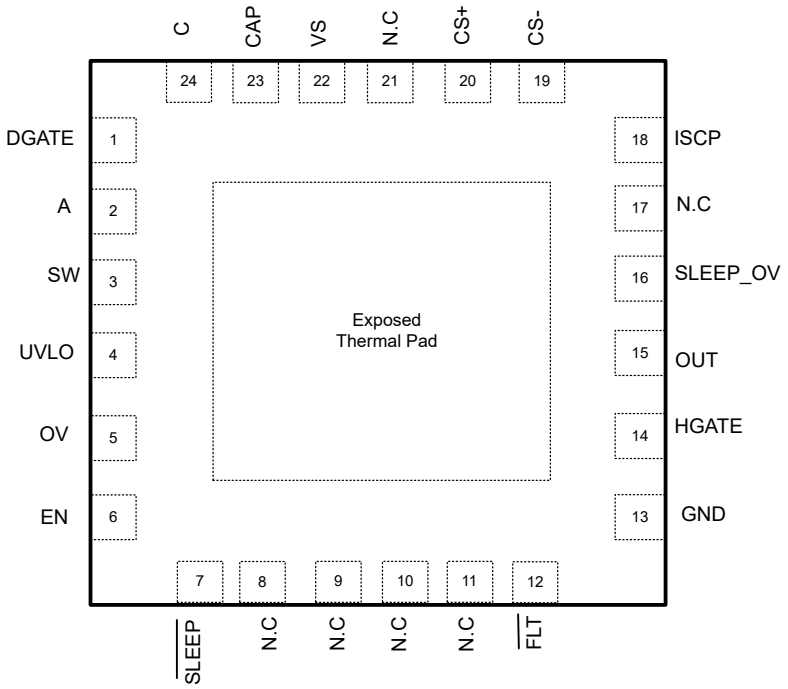


Figure 5-1. RGE Package, 24-Pin VQFN (Transparent Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DGATE	1	O	Diode controller gate drive output. Connect to the GATE of the external MOSFET.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET.
SW	3	I	Voltage sensing disconnect switch terminal. A and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN/$\overline{\text{SLEEP}}$ is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current. If the internal disconnect switch between A and SW is not used then SW pin can be left floating or pulled to A.
UVLO	4	I	Adjustable undervoltage threshold input. Connect a resistor ladder across SW to UVLO terminal to GND. When the voltage at UVLO goes below the undervoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes above the UVLO falling threshold.
OV	5	I	Adjustable overvoltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OV exceeds the overvoltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OV falling threshold.
EN	6	I	EN input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling it low below $V_{(ENF)}$ makes the device enter into low Iq shutdown mode.
$\overline{\text{SLEEP}}$	7	I	Active low SLEEP mode input. Can be driven from the micro-controller. When pulled low device enters into low power state with charge pump and gate drive turned off. Internal bypass switch provides output voltage with limited current capacity. When not used, should be tied to EN or VS.
N.C.	8	—	No connection. Keep this pin floating.
N.C.	9	—	No connection. Keep this pin floating.
N.C.	10	—	No connection. Keep this pin floating.
N.C.	11	—	No connection. Keep this pin floating.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{FLT}$	12	O	Open drain fault output. $\overline{FLT}$ pin is pulled low in case of undervoltage, overvoltage or output short circuit event.
GND	13	G	Connect to the system ground plane.
HGATE	14	O	GATE driver output for the HSFET. Connect to the GATE of the external FET.
OUT	15	I	Connect to the output rail (external MOSFET source).
SLEEP_OV	16	I	SLEEP mode over voltage protection pin. Connect this pin to Vs for over voltage cut-off functionality. Connect to OUT for over voltage clamp functionality.
N.C.	17	—	No connection. Keep this pin floating.
ISCP	18	I	Current sense negative input for adjustable short circuit protection. When ISCP is connected to output, device monitors external HFET voltage drop between CS+ and ISCP pins against an internal fix threshold of 50-mV typical.
CS–	19	I	Current sense amplifier supply input.
CS+	20	I	Current sense positive input for adjustable short circuit protection.
N.C.	21	—	No connection. Keep this pin floating.
VS	22	P	Input power supply to the IC. Connect VS to middle point of the common drain back to back MOSFET configuration. Connect a 100-nF capacitor across VS and GND pins.
CAP	23	O	Charge pump output. Connect a 100-nF capacitor across CAP and VS pin.
C	24	I	Cathode of the ideal diode. Connect to the drain of the external MOSFET.
RTN	Thermal pad	—	Leave exposed pad floating. Do not connect to GND plane.

(1) I = input, O = output, I/O = input and output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	A to GND	–65	70	V
	VS, CS+, CS-, ISCP to GND	–1	70	
	OUT, SLEEP_OV to GND	–1	70	
	C, SW, EN, $\overline{SLEEP}$, UVLO, OV to GND, $V_{(A)}$ > 0 V	–0.3	70	
	C, SW, EN, $\overline{SLEEP}$, UVLO, OV to GND, $V_{(A)}$ ≤ 0 V	$V_{(A)}$	(70 + $V_{(A)}$)	
	RTN to GND	–65	0.3	
	I_{SW} ,I_{FLT}	–1	10	mA
	I_{EN}, I_{SLEEP} ,I_{OV}, I_{UVLO} $V_{(A)}$ > 0 V	–1		
	I_{EN}, I_{SLEEP} ,I_{OV}, I_{UVLO} $V_{(A)}$ ≤ 0 V	Internally limited		
Output pins	CAP to VS	–0.3	15	V
	CAP to A	–0.3	85	
	DGATE to A	–0.3	15	
	$\overline{FLT}$ to GND	–1	70	
	HGATE to OUT	–0.3	15	
Output to input pins	C to A	–5	85	V
	OUT to VS	–65	5	
Operating junction temperature, T_j (2)	Operating junction temperature, T_j	–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (DGATE, GND, EN, ISCP, CS-, C) and)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	A to GND	–60		65	V
	VS, SW, CS+, CS–, ISCP to GND	0		65	V
	EN,UVLO, OV, $\overline{SLEEP}$ to GND	0		65	V
Output pins	FLT to GND	0		65	V
External capacitance	CAP to A, VS to GND, A to GND	0.1			µF
External MOSFET maximum gate-to-source rating	DGATE to A and HGATE to OUT	15			V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Tj	Operating junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC		LM74912-Q1 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	°C/W

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(\overline{SLEEP})}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3		65	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.4	2.65	2.9	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		2.2	2.45	2.7	V
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN)}$ = 0 V		2.5	5	µA
$I_{(SLEEP)}$	SLEEP mode current, $I_{(GND)}$	$V_{(EN)}$ = 2 V, $V_{(SLEEP)}$ = 0 V		5.5	10	µA
$I_{(Q)}$	Total system quiescent current, $I_{(GND)}$	$V_{(EN)}$ = 2 V		610	730	µA
		$V_{(A)}$ = $V_{(VS)}$ = 24 V, $V_{(EN)}$ = 2 V		615	735	µA
$I_{(REV)}$	$I_{(A)}$ leakage current during reverse polarity	0 V ≤ $V_{(A)}$ ≤ – 65 V	–100	–35		µA
	$I_{(OUT)}$ leakage current during reverse polarity		–1	–0.3		µA
ENABLE						
$V_{(ENR)}$	Enable threshold voltage for low Iq shutdown, rising			0.8	1.05	V
$V_{(ENF)}$	Enable falling threshold voltage for low Iq shutdown		0.41	0.7		V
$I_{(EN)}$		$V_{(EN)}$ = 65 V		55	200	nA
UNDERVOLTAGE LOCKOUT COMPARATOR						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		0.585	0.6	0.63	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		0.533	0.55	0.573	V
$I_{(UVLO)}$	UVLO pin leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 5 V		52	200	nA
SLEEP MODE						
$V_{(\overline{SLEEP}R)}$	$\overline{SLEEP}$ threshold voltage for low I_Q mode			0.8	1.05	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(\overline{SLEEP})}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(\overline{SLEEP}F)}$	$\overline{SLEEP}$ threshold voltage for low Iq shutdown, falling		0.41	0.7		V
$I_{(\overline{SLEEP})}$	$\overline{SLEEP}$ input leakage current	0 V ≤ $V_{(SLEEP)}$ ≤ 12 V		100	160	nA
Overcurrent threshold	SLEEP mode overcurrent threshold		150	250	310	mA
Overvoltage threshold	Overvoltage comparator rising threshold		19.3	21.5	23	V
	Overvoltage comparator falling threshold		18.4	21.04	22.2	V
FET resistance	SLEEP mode bypass FET resistance		4.5	7.5	11.5	Ω
TSD	Thermal shutdown rising threshold during SLEEP mode			155		℃
OVERVOLTAGE PROTECTION AND BATTERY SENSING INPUT						
$R_{(SW)}$	Battery sensing disconnect switch resistance	3 V ≤ $V_{(SNS)}$ ≤ 65 V	10	22	46	Ω
$V_{(OVR)}$	Overvoltage threshold input, rising		0.585	0.6	0.63	V
$V_{(OVF)}$	Overvoltage threshold input, falling		0.533	0.55	0.573	V
$I_{(OV)}$	OV pin Input leakage current	0 V ≤ $V_{(OV)}$ ≤ 5 V		52	200	nA
CURRENT SENSE AMPLIFIER						
I_{CS+}	CS+ pin sink current		10	11	11.85	µA
I_{SCP}	ISCP pin bias current		10	11	11.85	µA
$V_{(SNS\_SCP)}$	Short circuit protection threshold	R_{ISCP} = R_{SET} = 0 Ω	47.3	50	53.4	mV
		R_{SET} = 1 kΩ, R_{ISCP} = 0 Ω		61		mV
		R_{ISCP} = 1 kΩ, R_{SET} = 0 Ω		39		mV
FAULT						
R_$\overline{FLT}$	$\overline{FLT}$ pull-down resistance		11	25	60	Ω
I_$\overline{FLT}$	$\overline{FLT}$ pin leakage current		–100		400	nA
CHARGE PUMP						
$I_{(CAP)}$	Charge pump source current	$V_{(CAP)}$ – $V_{(A)}$ = 7 V, 6 V ≤ $V_{(S)}$ ≤ 65 V	2.5	4		mA
VCAP – VS	Charge pump turn on voltage		11	12.2	13.2	V
	Charge pump turn off voltage		11.9	13.2	14.1	V
$V_{(CAP\ UVLO)}$	Charge pump UVLO voltage threshold, rising		5.4	6.6	7.9	V
	Charge pump UVLO voltage threshold, falling		4.4	5.4	6.6	V
IDEAL DIODE MOSFET CONTROL						
$V_{(A\_PORR)}$	$V_{(A)}$ POR threshold, rising		2.2	2.4	2.7	V
$V_{(A\_PORF)}$	$V_{(A)}$ POR threshold, falling		2	2.2	2.45	V
$V_{(AC\_REG)}$	Regulated forward $V_{(A)}$ – $V_{(C)}$ threshold		3.6	10.5	13.4	mV
$V_{(AC\_REV)}$	$V_{(A)}$ – $V_{(C)}$ threshold for fast reverse current blocking		–16	–10.5	–5	mV
$V_{(AC\_FWD)}$	$V_{(A)}$ – $V_{(C)}$ threshold for reverse to forward transition		150	177	200	mV
$V_{(DGATE)}$ – $V_{(A)}$	Gate drive voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	9.2	11.5	14	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(\overline{SLEEP})}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(DGATE)}$	Peak gate source current	$V_{(A)} – V_{(C)}$ = 300 mV, $V_{(DGATE)} – V_{(A)}$ = 1 V		20		mA
	Peak gate sink current	$V_{(A)} – V_{(C)}$ = –12 mV, $V_{(DGATE)} – V_{(A)}$ = 11 V		2670		mA
	Regulation sink current	$V_{(A)} – V_{(C)}$ = 0 V, $V_{(DGATE)} – V_{(A)}$ = 11 V	6	15		µA
$I_{(C)}$	Cathode leakage current	$V_{(A)}$ = –14 V, $V_{(C)}$ = 12 V	4	9	32	µA
HIGH SIDE MOSFET CONTROL						
$V_{(HGATE)} – V_{(OUT)}$	Gate drive voltage	3 V < $V_{(S)}$ < 5 V	7			V
		5 V < $V_{(S)}$ < 65 V	10	11.1	14	V
$I_{(HGATE)}$	Source current		39	55	75	µA
	Sink current		128	180		mA
$V_{(HGATE –OUT)\_SCP}$	HGATE-OUT threshold for short circuit protection enable			6.4		V

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(OUT)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 0.1 µF, $V_{(EN)}$, $V_{(\overline{SLEEP})}$= 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGATE\_OFF(dly)}$	DGATE turn off delay during reverse voltage detection	$V_{(A)} – V_{(C)}$ = +30 mV to –100 mV to $V_{(DGATE–A)}$ < 1 V, $C_{(DGATE–A)}$ = 10 nF		0.5	0.95	µs
$t_{DGATE\_ON(dly)}$	DGATE turn on delay during forward voltage detection	$V_{(A)} – V_{(C)}$ = –20 mV to +700 mV to $V_{(DGATE–A)}$ > 5 V, $C_{(DGATE–A)}$ = 10 nF		0.8	1.6	µs
$t_{EN(dly)\_DGATE}$	DGATE turn on delay during device enable	EN↑ to $V_{(DGATE–A)}$ > 5 V		185	270	µs
$t_{UVLO\_OFF(deg)\_HGATE}$	HGATE turn off de-glitch during UVLO	UVLO↓ to HGATE ↓		5	7	µs
$t_{UVLO\_ON(deg)\_HGATE}$	HGATE turn on de-glitch during UVLO	UVLO ↑ to HGATE ↑		7		µs
$t_{OVP\_OFF(deg)\_HGATE}$	HGATE turn off de-glitch during OV	OV ↑ to HGATE ↓, $C_{(HGATE–OUT)}$ = 4.7 nF		4	7	µs
$t_{OVP\_ON(deg)\_HGATE}$	HGATE turn on de-glitch during OV	OV ↓ to HGATE ↑		7		µs
t_{SCP_DLY}	Short-circuit protection turn off delay	(V_{CS+}–V_{ISCP}) = 0-mV to 100-mV, HGATE↓, $C_{(HGATE–OUT)}$ = 10 nF		2	4.5	µs
t_{FLT_ASSERT}	Fault assert delay during short-circuit condition	(V_{CS+}–V_{ISCP})↑ to FLT↓		2.5		µs
$t_{FLT\_DE-ASSERT}$	Fault de-assert delay	(V_{CS+}–V_{ISCP}) ↓ to FLT↑		3.5		µs
$t_{SLEEP\_OCP\_LATCH}$	SLEEP OCP Latch delay	$\overline{SLEEP}$ = Low, EN = High		3.5	7.5	µs
$t_{SLEEP\_OV\_OFF}$	Overvoltage turn off response delay in sleep mode	$\overline{SLEEP}$ = Low, EN = High		3.5		µs
$t_{SLEEP\_MODE\_ENTRY}$	Sleep Mode Entry Delay	$\overline{SLEEP}$ = Low, EN = High		100		µs

6.7 Typical Characteristics

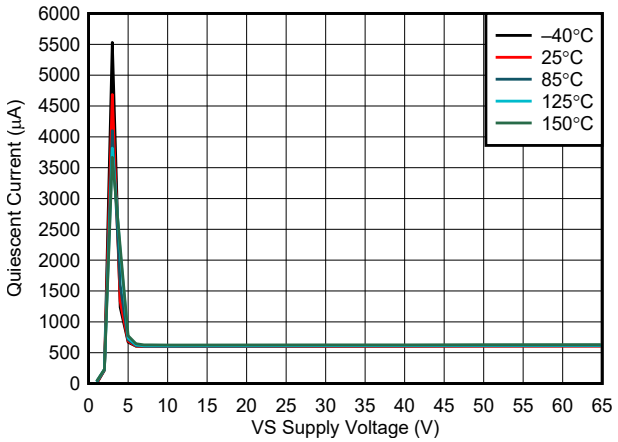


Figure 6-1. Operating Quiescent Current vs Supply Voltage

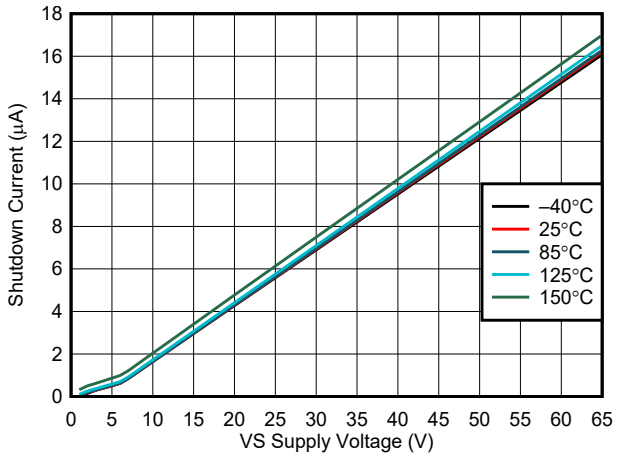


Figure 6-2. Shutdown Current vs Supply Voltage

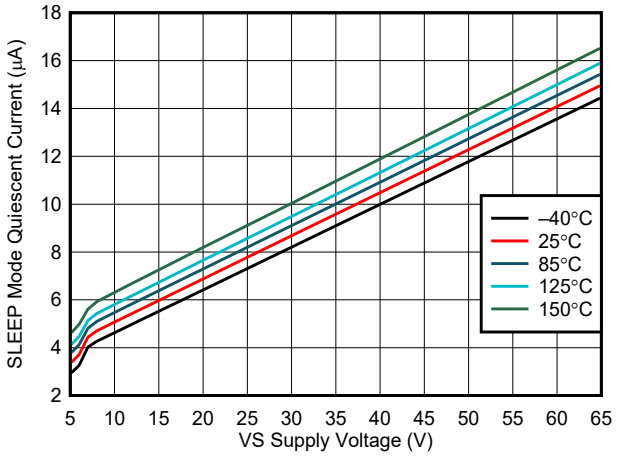


Figure 6-3. SLEEP Mode Current vs Supply Voltage

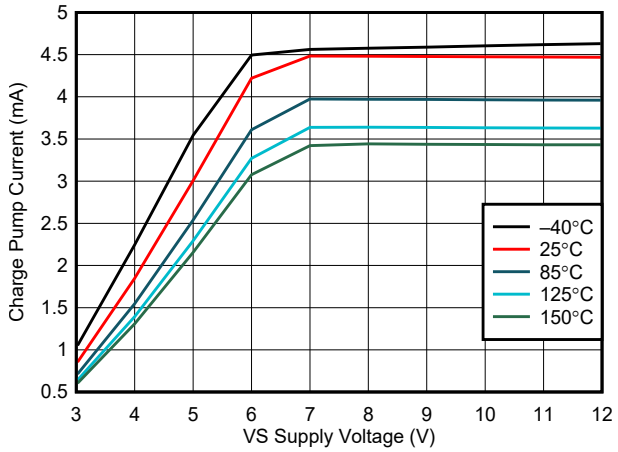


Figure 6-4. Charge Pump Current vs Supply Voltage at CAP – VS ≥ 6 V

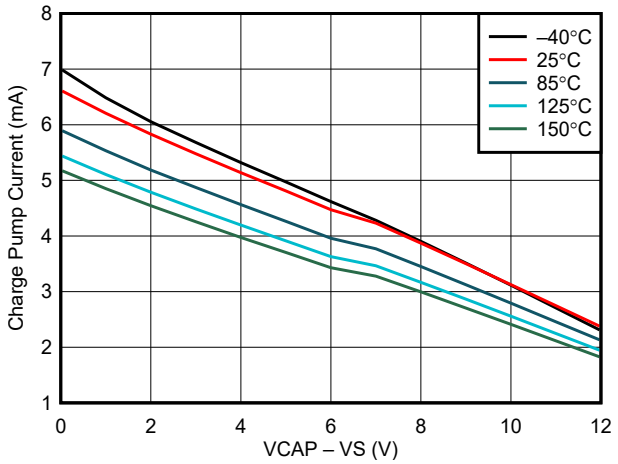


Figure 6-5. Charge Pump V-I Characteristics at VS ≥ 12 V

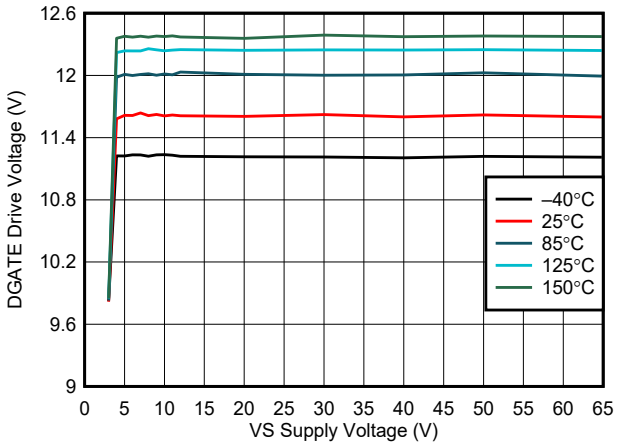


Figure 6-6. DGATE Drive Voltage vs Supply Voltage

6.7 Typical Characteristics (continued)

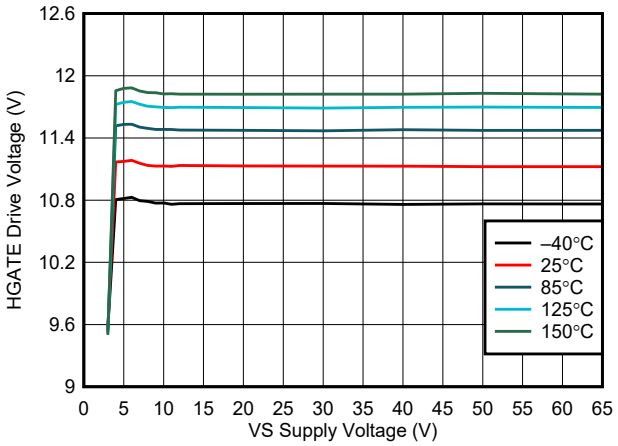


Figure 6-7. HGATE Drive Voltage vs Supply Voltage

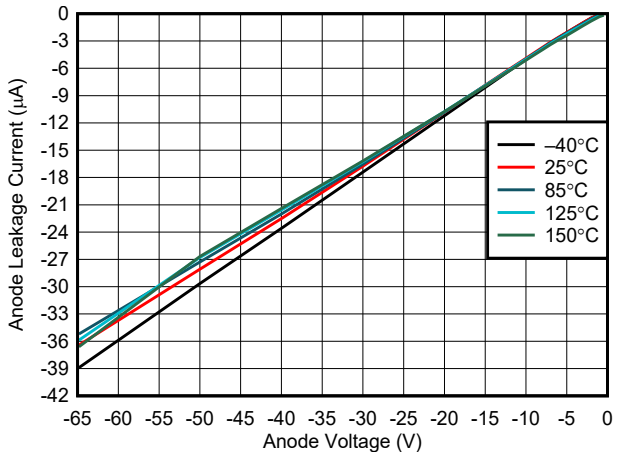


Figure 6-8. ANODE Leakage Current vs Reverse ANODE Voltage

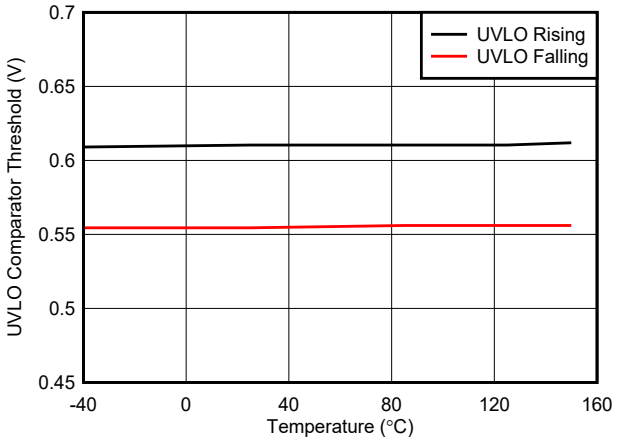


Figure 6-9. UVLO Thresholds vs Temperature

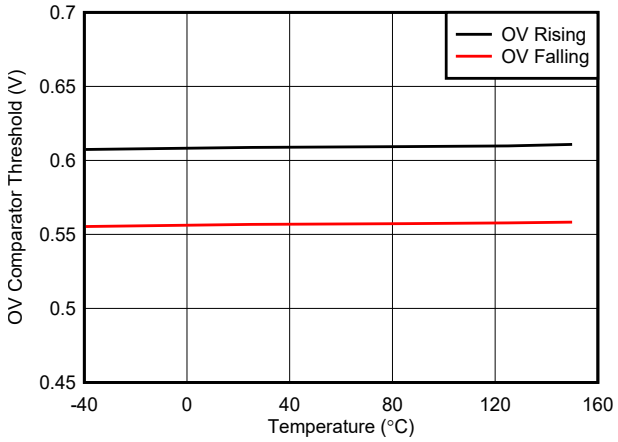


Figure 6-10. OVP Thresholds vs Temperature

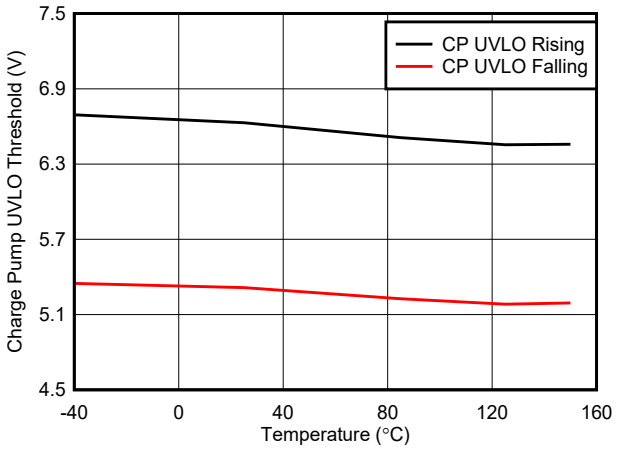


Figure 6-11. Charge Pump UVLO Threshold vs Temperature

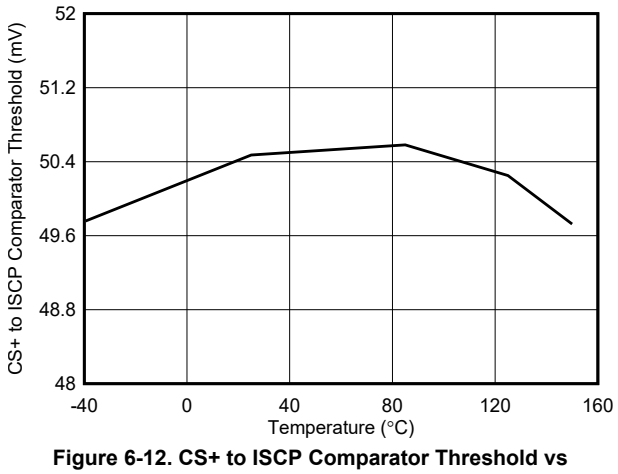


Figure 6-12. CS+ to ISCP Comparator Threshold vs Temperature

6.7 Typical Characteristics (continued)

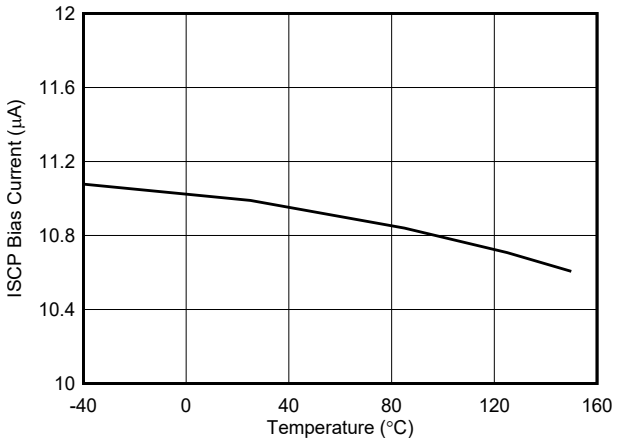


Figure 6-13. ISCP Bias Current vs Temperature

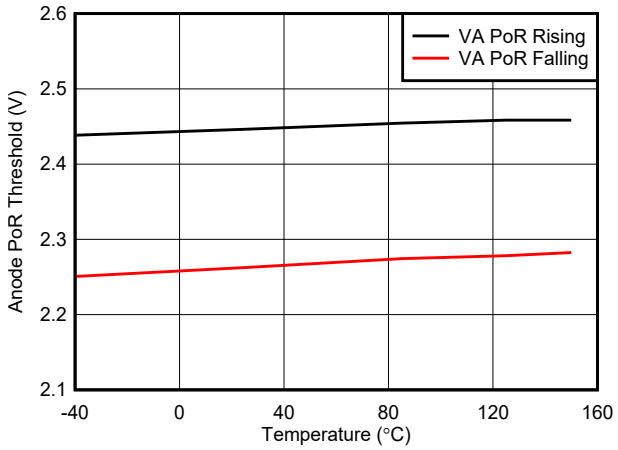


Figure 6-14. VA POR Threshold vs Temperature

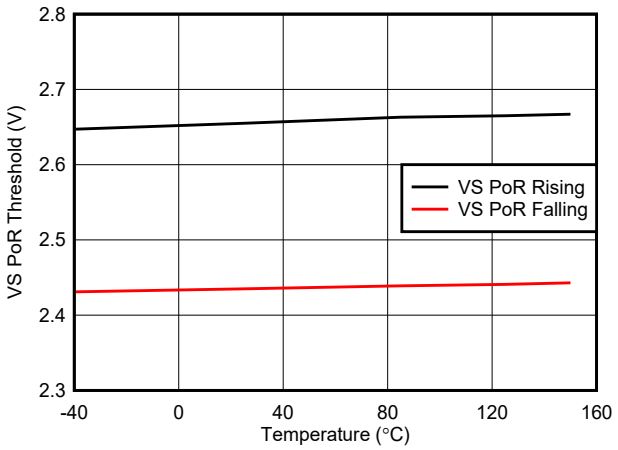


Figure 6-15. VS POR Threshold vs Temperature

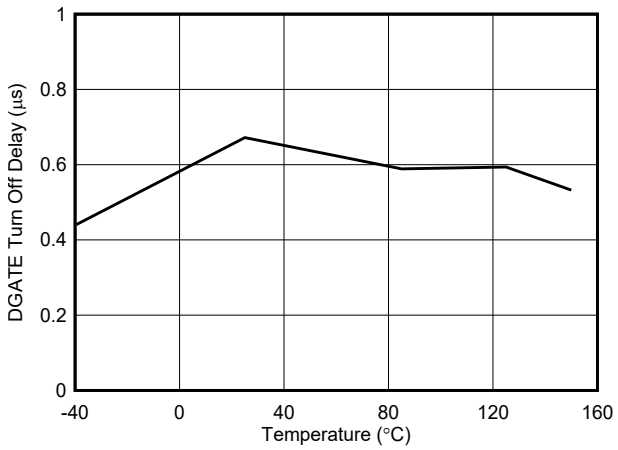


Figure 6-16. DGATE Turn OFF Delay

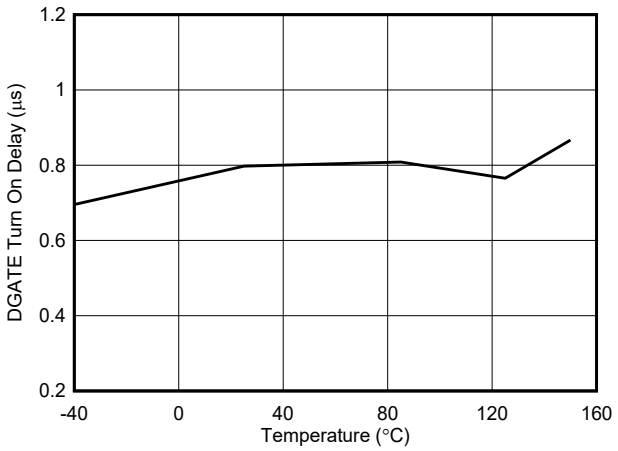


Figure 6-17. DGATE Turn On Delay During Forward Conduction

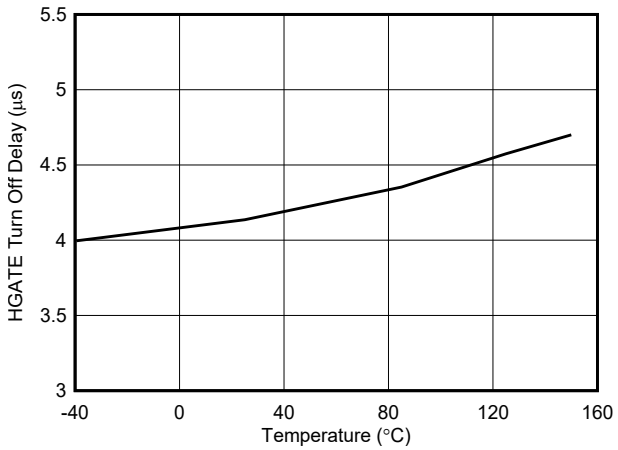


Figure 6-18. HGATE Turn OFF Delay During Overvoltage

6.7 Typical Characteristics (continued)

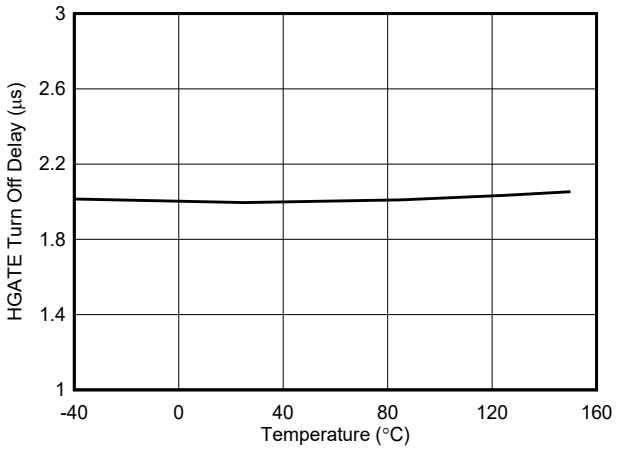


Figure 6-19. HGATE Turn OFF Delay During Short Circuit

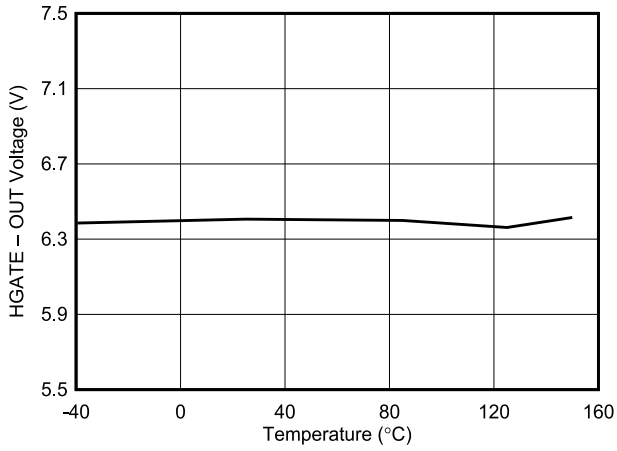


Figure 6-20. Short Circuit Detection Enable Threshold Voltage (HGATE-OUT)

7 Parameter Measurement Information

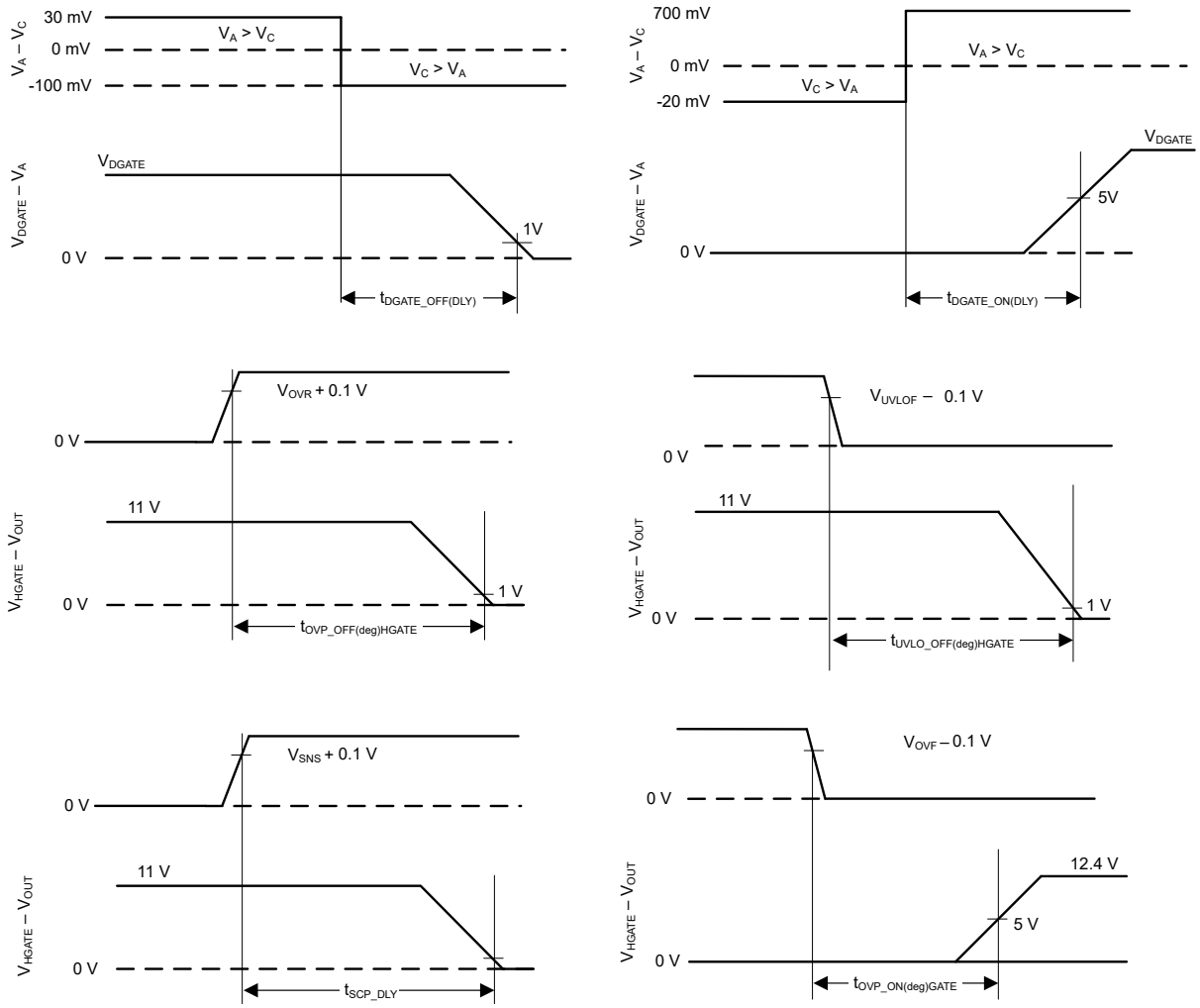


Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74912-Q1 Ideal Diode controller drive back-to-back external N-Channel MOSFETs to realize low loss power path protection with short circuit, under and overvoltage protection functionality.

The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and overvoltage protection using HGATE control. The device features an adjustable overvoltage cut-off protection feature. With common drain configuration of the power MOSFETs, the mid-point can be utilized for OR-ing designs using another ideal diode. The LM74912-Q1 has a maximum voltage rating of 65 V.

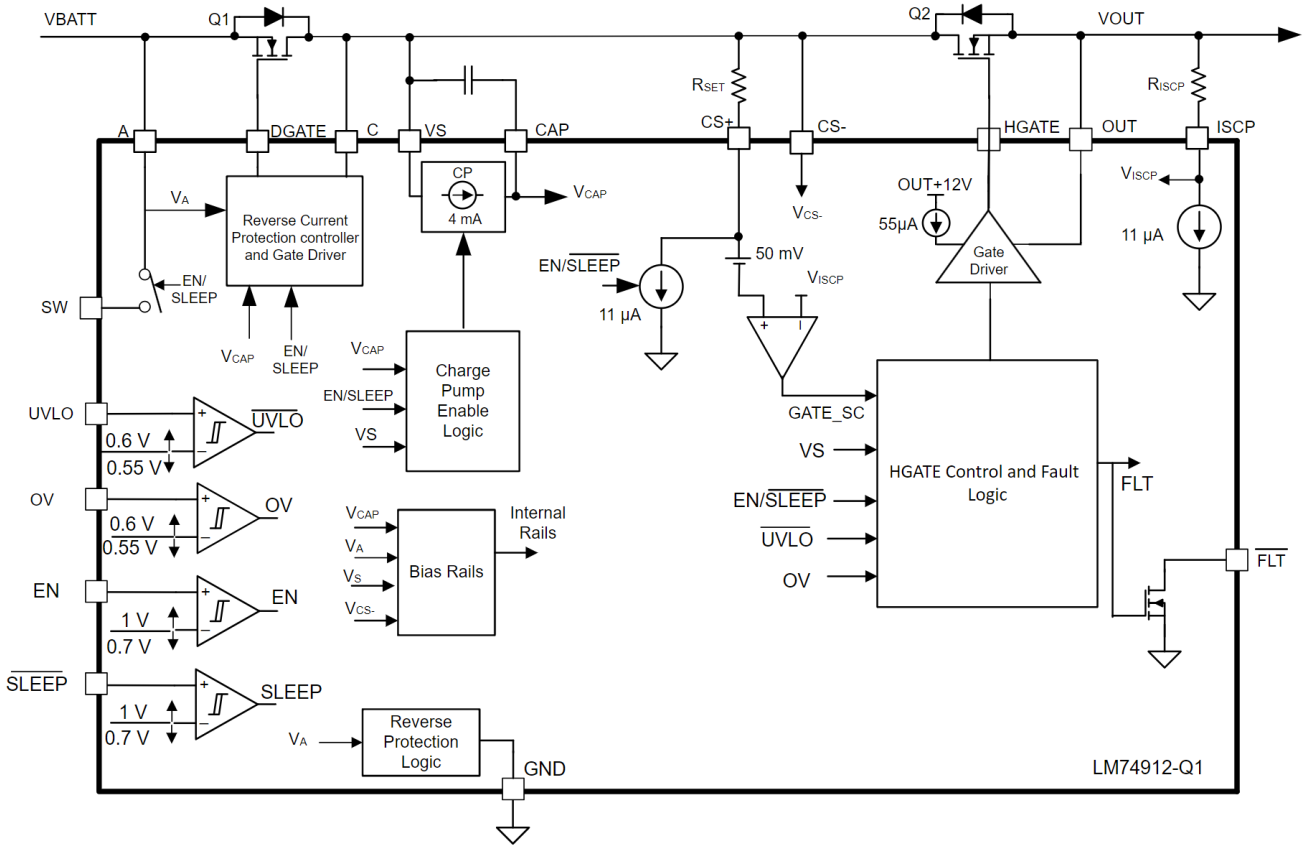
It has integrated current sense amplifier which monitors external MOSFET (Q2) VDS voltage to provide short circuit protection. The device has default short circuit comparator threshold- at 50-mV with complete flexibility to shift this threshold using external components (R_{ISCP} and R_{SET}). Once short circuit condition is detected then device latches off MOSFET Q2 until either the EN, $\overline{SLEEP}$ or the VS pin is toggled from low to high.

The device offers adjustable overvoltage and undervoltage protection, providing robust load disconnect in case of voltage transient events.

LM74912-Q1 features two different low power modes based on status of EN and $\overline{SLEEP}$ pin. In SLEEP mode ($\overline{SLEEP}$=Low, EN=High) the device consumes only 5.5-µA current by turning off both the external MOSFET gate drives and internal charge pump but at the same time providing internal bypass path to power up always ON loads with limited current capacity. With the enable pin low, device enters into ultra low power mode by completely cutting off loads with typical current consumption of 2.5 µA. The high voltage rating of LM74912-Q1 helps to simplify the system designs for automotive ISO7637 protection. The LM74912-Q1 is also suitable for ORing applications.

8.2 Functional Block Diagram

This section shows functional block diagram of LM74912-Q1.



8.3 Feature Description

8.3.1 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the EN and $\overline{\text{SLEEP}}$ pin voltage must be above the specified input high threshold. When enabled the charge pump sources a charging current of 4-mA typical. If EN or $\overline{\text{SLEEP}}$ pin is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the CAP to VS voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 175\ \mu s + \frac{C_{(CAP)} \times V_{(CAP\_UVLOR)}}{4\ mA} \quad (1)$$

where

- $C_{(CAP)}$ is the charge pump capacitance connected across VS and CAP pins
- $V_{(CAP\_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive approximately 1 V of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the CAP to VS voltage reaches 13.2 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the CAP to VS voltage is below to 12.2 V typically at which point the charge pump is enabled. The voltage between CAP and VS continue to charge and discharge between 12.2 V and 13.2 V as shown in Figure 8-1. By

enabling and disabling the charge pump, the operating quiescent current of the LM74912-Q1 is reduced. When the charge pump is disabled it sinks 15 µA.

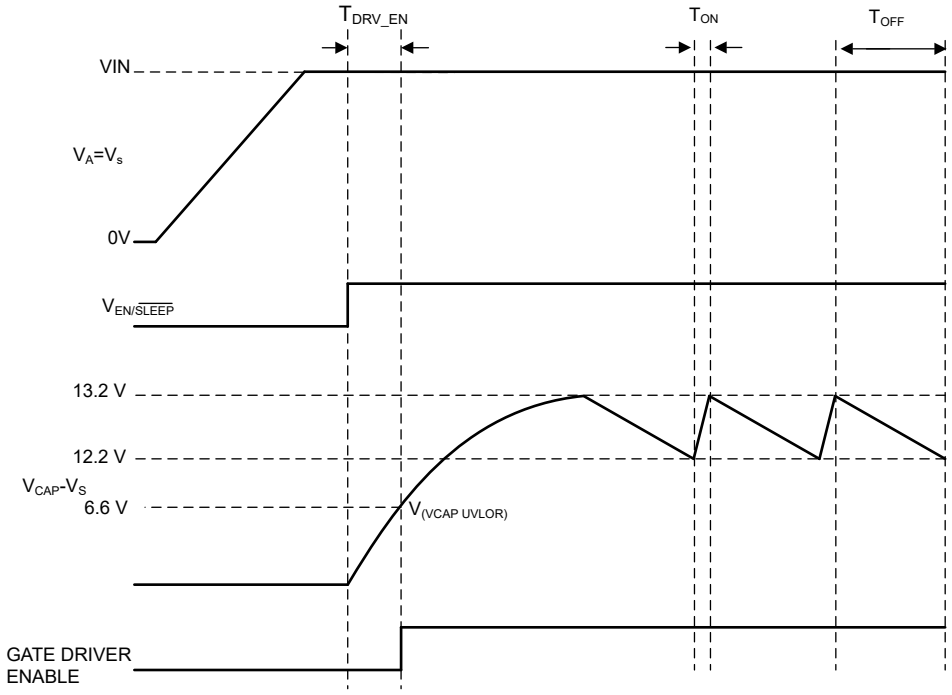


Figure 8-1. Charge Pump Operation

8.3.2 Dual Gate Control (DGATE, HGATE)

The LM74912-Q1 feature two separate gate control and driver outputs i.e DGATE and HGATE to drive back to back N-channel MOSFETs.

8.3.2.1 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises the ideal diode stage. Connect the source of the external MOSFET to A, drain to C, and gate to DGATE. The LM74912-Q1 has integrated reverse input protection down to –65 V.

Before the DGATE driver is enabled, the following conditions must be achieved:

- The EN and $\overline{\text{SLEEP}}$ pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at A pin must be greater than VA POR rising threshold.
- Voltage at VS pin must be greater than VS POR rising threshold.

If the above conditions are not achieved, then the DGATE pin is internally connected to the A pin, assuring that the external MOSFET is disabled.

In LM74912-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 10.5 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74912-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{(AC\_REV)}$ threshold then the DGATE goes low within 0.5 µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{(AC\_FWD)}$ threshold within 0.8 µs (typ).

8.3.2.2 Load Disconnect Switch Control (HGATE, OUT)

HGATE and OUT comprises the load disconnect switch control stage. Connect the source of the external MOSFET to OUT and gate to HGATE.

Before the HGATE driver is enabled, the following conditions must be achieved:

- The EN and $\overline{\text{SLEEP}}$ pin voltage must be greater than the specified input high voltage.
- The CAP to VS voltage must be greater than the undervoltage lockout voltage.
- Voltage at VS pin must be greater than Vs POR rising threshold.

If the above conditions are not achieved, then the HGATE pin is internally connected to the OUT pin, assuring that the external MOSFET is disabled.

For Inrush Current limiting, connect C_{dVdT} capacitor and R_1 as shown in Figure 8-2.

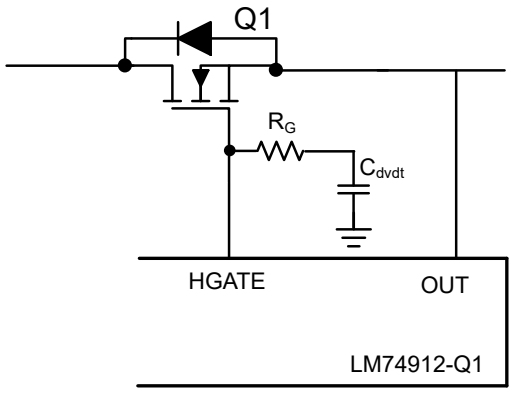


Figure 8-2. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use Equation 2 to calculate C_{dVdT} capacitance value.

$$C_{(dVdT)} = C_{OUT} \times \frac{I_{(HGATE\_DRV)}}{I_{INRUSH}} \quad (2)$$

where I_{HATE_DRV} is 55 µA (typ), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn off time.

HGATE response is slowed down with additional C_{dVdT} capacitor connected for inrush current limiting. This can cause slower HGATE recovery and in turn HGATE-OUT effective voltage to drop from the nominal value when there is positive line transient on the input line.

8.3.3 Short Circuit Protection (CS+, CS-, ISCP)

LM74912-Q1 offers fast response to output short circuit events with the short circuit protection feature. The internal short circuit comparator is enabled when HGATE-OUT voltage is higher than 6.4-V typical. This is to ensure that external FET is fully enhanced and there are no false short circuit triggers during device start-up. When short circuit condition appears at the output and the voltage across CS+ and ISCP exceeds the default short circuit comparator threshold of 50-mV typical, HGATE is pulled to OUT within 2-µs protecting the HFET. $\overline{\text{FLT}}$ asserts low at the same time. Once short circuit condition is detected then device latches off MOSFET Q2 until either the EN, $\overline{\text{SLEEP}}$ or the VS pin is toggled from low to high.

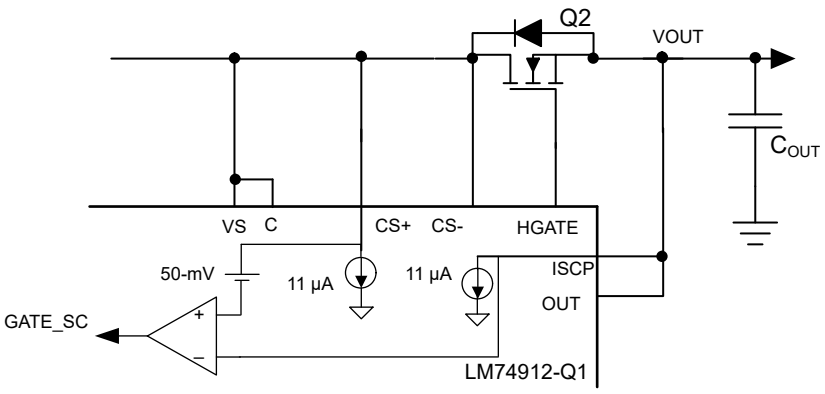


Figure 8-3. Short Circuit Protection Comparator

Short circuit protection threshold can be increased or decreased from the default 50-mV threshold by using an external series resistor R_{SET} from CS+ pin or R_{ISCP} from ISCP pin as shown in Figure 8-4. The R_{SET} resistor shifts the threshold in positive direction while R_{ISCP} resistor shifts the threshold in negative direction. The shift in the short circuit protection threshold can be calculated using Equation 3 and Equation 4.

$$V_{DS\_SNS} = 50\ mV + (11\ \mu A \times R_{SET}) \quad (3)$$

$$V_{DS\_SNS} = 50\ mV - (11\ \mu A \times R_{ISCP}) \quad (4)$$

An additional de-glitch capacitor C_{ISCP} can be added from CS+ pin to ISCP pin as shown in Figure 8-4 to provide blanking on any short spurious current spikes to avoid false short circuit trigger in case of fast automotive transients such as Input Micro cuts (LV124, E-10), AC superimpose (LV124, E-06), ISO7637-2 Pulse 2A.

Also when MOSFET Q2 is turned off due to short circuit condition, there can be voltage oscillations on the supply line due to inductive effect of board parasitic and input wiring harness inductance. To avoid these oscillations from reaching to the device supply pin VS and causing false reset, additional series resistor R_{VS} can be inserted. This series resistor R_{VS} forms a R-C low pass filter with VS side decoupling capacitor C_{VS} and helps with damping the oscillations.

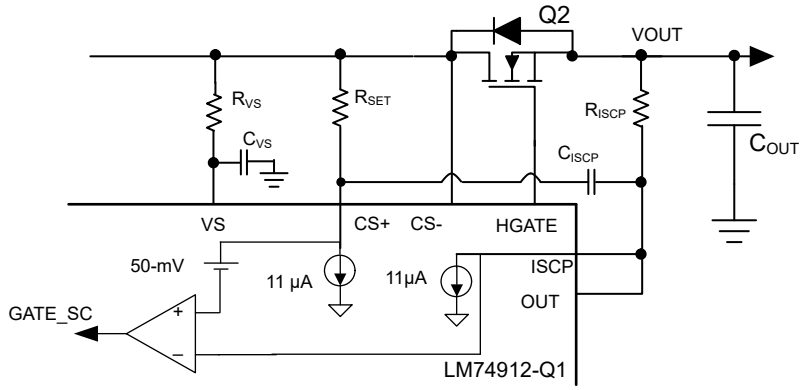


Figure 8-4. Short Circuit Protection With De-glitch Filter

The LM74912-Q1 is intended for applications where precise current sensing is not required, but some level of fault protection is needed. Examples are applications where inductance or impedance in the power path limits the current rise in a short circuit condition.

The Safe Operating Area (SOA) of the external N-Channel MOSFET must be carefully considered to make sure the peak drain-to-source current and the duration of the short circuit protection response time is within the SOA rating of the MOSFET. Also note that the RDS(ON) variations of the external N-Channel MOSFET over given temperature range affect the accuracy of the overcurrent detection.

8.3.4 Overvoltage Protection and Battery Voltage Sensing (SW, OV, UVLO)

Connect a resistor ladder as shown in Figure 8-5 for overvoltage and undervoltage threshold programming.

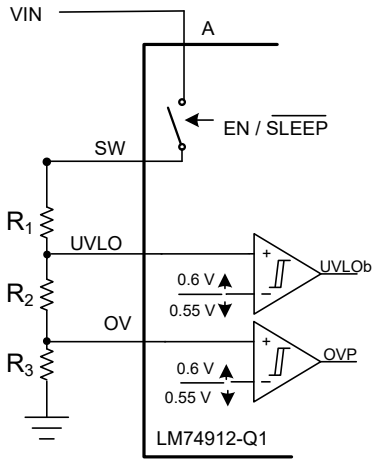


Figure 8-5. Programming Overvoltage Threshold and Battery Sensing

A disconnect switch is integrated between A and SW pins. This switch is turned OFF when EN or $\overline{\text{SLEEP}}$ pin is pulled low. This helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

When overvoltage or undervoltage condition is removed from input side then HGATE is turned on again.

8.3.5 Low IQ SLEEP Mode ($\overline{\text{SLEEP}}$, SLEEP_OV)

LM74912-Q1 supports low IQ SLEEP mode operation. This mode can be enabled by pulling SLEEP pin low (EN = High). In SLEEP mode, device turns off internal charge pump, SW switch and disables DGATE and HGATE drive thus achieving low current consumption of 5.5-µA typical. However at the same time device power up always on loads connected on OUT pin through an internal low power MOSFET with typical on resistance of 7 Ω. In this mode device can support peak load current of 100 mA. As load is increased, voltage drop across internal MOSFET increases. Device offers overcurrent protection during sleep mode with typical overcurrent threshold of 250 mA. In case of overcurrent event during sleep mode, device protects internal FET by disconnecting the internal MOSFET switch and latching off the device. As an additional layer of protection, device also features thermal shutdown with latch off feature in SLEEP mode in case of any overheating of the device in SLEEP mode. To put the device out of the latch mode user has to toggle the SLEEP or EN pin.

In SLEEP mode LM74912-Q1 offers protection against input overvoltage events. Device can be configured in either overvoltage cut-off (SLEEP_OV connected to C) or overvoltage clamp mode (SLEEP_OV connected to V_{OUT}) with default overvoltage threshold of 21-V typical.

If SLEEP mode feature is not required then $\overline{\text{SLEEP}}$ pin should be tied to EN. When not used SLEEP_OV pin can be left floating.

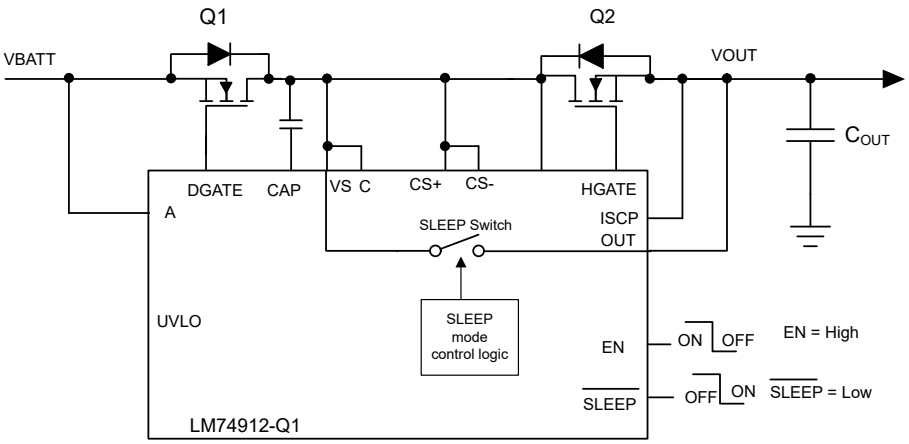


Figure 8-6. LM74912-Q1 SLEEP Mode

A higher overvoltage threshold for SLEEP mode can be achieved by adding an external Zener diode between SLEEP_OV pin to OUT/C as shown in Figure 8-7. This feature is useful while configuring overvoltage threshold for 24-V or 48-V powered systems.

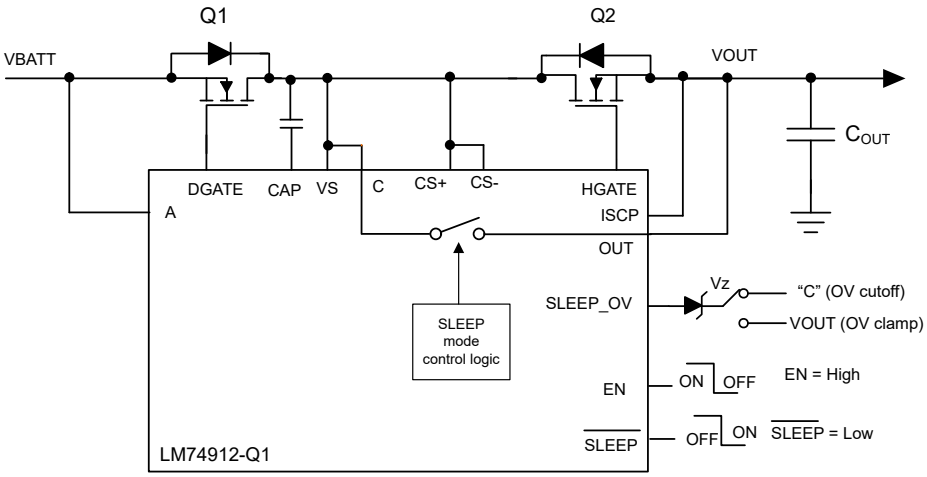


Figure 8-7. Extending Overvoltage Threshold in SLEEP Mode

8.4 Device Functional Modes

Shutdown Mode

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in Charge Pump. If EN pin voltage is less than the input low threshold, $V_{(ENF)}$, the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM74912-Q1 in shutdown mode with ultra-low-current consumption of 2.5-µA. The EN pin can withstand a maximum voltage of 65 V. For always ON operation, connect EN pin to VS.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

LM74912-Q1 controls two N-channel power MOSFETs with DGATE used to control diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during a overcurrent, overvoltage, or undervoltage events. HGATE controlled MOSFET can be used to clamp the output during overvoltage or load dump conditions. LM74912-Q1 can be placed into low quiescent current mode using EN or $\overline{\text{SLEEP}}$, where both DGATE and HGATE are turned OFF. The device has a separate supply input pin (VS). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM74912-Q1 device drives back to back connected MOSFET in common drain topology thus enabling various system architectures such as power supply ORing and power supply priority MUX applications. With these various topologies, the system designers can design the front-end power system to meet various system design requirements.

The device has a separate supply input pin (VS). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM74912-Q1 device drives back to back connected MOSFET in common drain topology thus enabling various system architectures such as power supply ORing and power supply priority MUX applications. With these various topologies, the system designers can design the front-end power system to meet various system design requirements.

9.2 Typical 12-V Reverse Battery Protection Application

A typical application circuit of LM74912-Q1 configured in **common-drain topology** to provide reverse battery protection with overvoltage protection is shown in Figure 9-1.

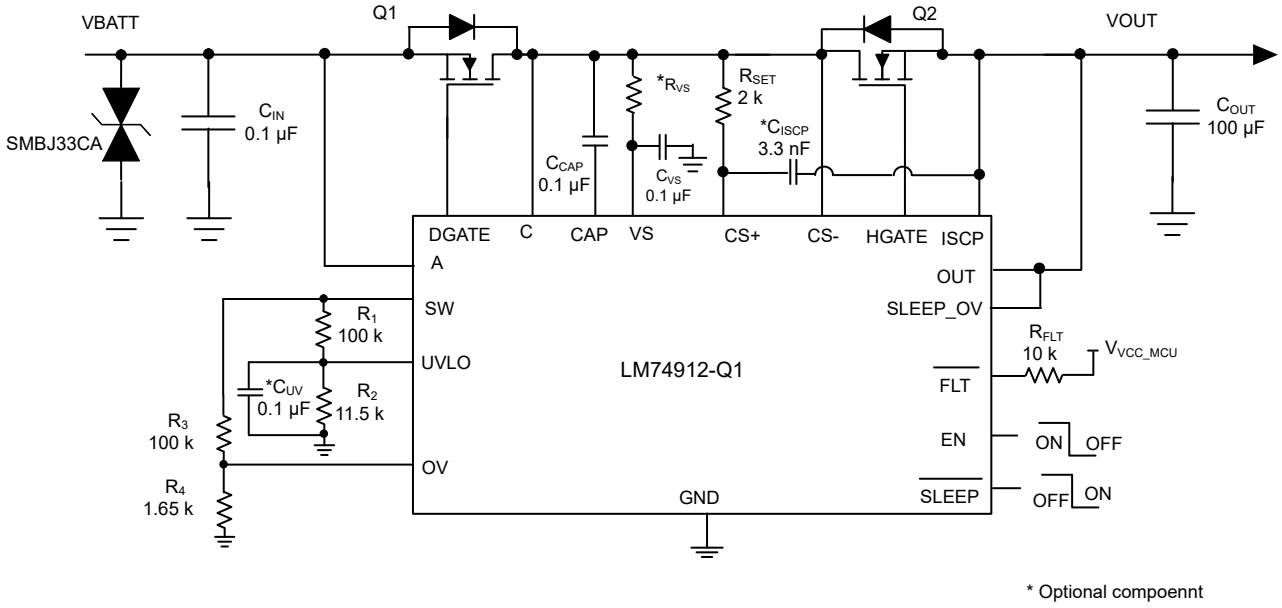


Figure 9-1. Typical Application Circuit – 12-V Reverse Battery Protection and Overvoltage Protection

9.2.1 Design Requirements for 12-V Battery Protection

The system design requirements are listed in Table 9-1.

Table 9-1. Design Parameters - 12-V Reverse Battery Protection and Overvoltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	12-V battery, 12-V nominal with 3.2-V Cold Crank and 35-V Load Dump
Output Power	50 W
Output Current Range	4-A Nominal, 5-A maximum
Short Circuit Current Level	14-A
Input Capacitance	0.1-µF minimum
Output Capacitance	0.1-µF minimum, (optional 100 µF for E-10 functional class A performance)
Overvoltage Cut-off	37.0 V, output cut-off > 37.0 V
AC Super Imposed Test	2-V Peak-Peak 30 KHz, extendable to 6-V Peak-Peak 30 KHz
Automotive Transient Immunity Compliance	ISO 7637-2, ISO 16750-2 and LV124

9.2.2 Automotive Reverse Battery Protection

The LM74912-Q1 feature two separate gate control and driver outputs, DGATE and HGATE, to drive back to back N-channel MOSFETs. This enables LM74912-Q1 to provide comprehensive immunity with robust system protection during various automotive transient tests as per ISO 7637-2 and ISO 16750-2 standard as well as other automotive OEM standards. For more information, see the *Automotive EMC-compliant reverse-battery protection with ideal-diode controllers* article.

LM74912-Q1 gate drive output DGATE controls MOSFET Q1 to provide reverse battery protection and true reverse current blocking functionality. HGATE controls MOSFET Q2 to turn off the power path during input overvoltage condition. Resistor network R1, R2 and R3 connected to OV and SW can be configured for overvoltage protection and also for battery monitoring under normal operating conditions as well as reverse battery conditions. Bi-directional TVS D1 clamps the automotive transient input voltages on the 12-V battery, both positive and negative transients, to voltage levels safe for MOSFET Q1 and LM74912-Q1.

Fast reverse current blocking response and quick reverse recovery enables LM74912-Q1 to turn ON/OFF MOSFET Q1 during AC super imposed input specified by ISO 16750-2 and LV124 E-06 and provide active rectification of the AC input superimposed on DC battery voltage. Fast reverse current blocking response of LM74912-Q1 helps to turn off MOSFET Q1 during negative transients inputs such as –150-V 2-ms Pulse 1 specified in ISO 7637-2 and input micro short conditions such as LV124 E-10 test.

9.2.2.1 Input Transient Protection: ISO 7637-2 Pulse 1

ISO 7637-2 Pulse 1 specifies negative transient immunity of electronic modules connected in parallel with an inductive load when the battery is disconnected. A typical pulse 1 specified in ISO 7637-2 starts with battery disconnection where supply voltage collapses to 0 V followed by –150 V 2 ms applied with a source impedance of 10 Ω at a slew rate of 1 µs on the supply input. LM74912-Q1 blocks reverse current and prevents the output voltage from swinging negative, protecting the rest of the electronic circuits from damage due to negative transient voltage. MOSFET Q1 is quickly turned off within 0.5 µs by fast reverse comparator of LM74912-Q1. A single bi-directional TVS is required at the input to clamp the negative transient pulse within the operating maximum voltage across cathode to anode of 85 V and does not violate the MOSFET Q1 drain-source breakdown voltage rating.

ISO 7637-2 Pulse 1 performance of LM74912-Q1 is shown in Figure 9-2.

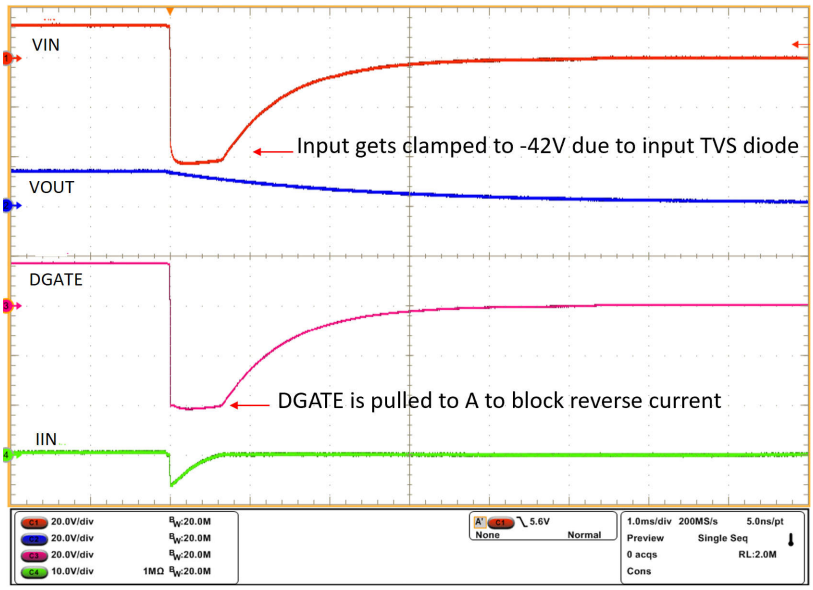


Figure 9-2. ISO 7637-2 Pulse 1

9.2.2.2 AC Super Imposed Input Rectification: ISO 16750-2 and LV124 E-06

Alternators are used to power the automotive electrical system and charge the battery during normal runtime of the vehicle. Rectified alternator output contains residual AC ripple voltage superimposed on the DC battery voltage due to various reasons which includes engine speed variation, regulator duty cycle with field switching ON/OFF and electrical load variations. On a 12-V battery supply, alternator output voltage is regulated by a voltage regulator between 14.5 V to 12.5 V by controlling the field current of alternator's rotor. All electronic modules are tested for proper operation with superimposed AC ripple on the DC battery voltage. AC super imposed test specified in ISO 16750-2 and LV124 E-06 requires AC ripple of 2-V Peak-Peak on a 13.5-V DC battery voltage, swept from 15 Hz to 30 KHz. LM74912-Q1 rectifies the AC superimposed voltage by turning the MOSFET Q1 OFF quickly to cut-off reverse current and turning the MOSFET Q1 ON quickly during forward conduction. Fast turn off and quick turn ON of the MOSFET reduces power dissipation in the MOSFET Q1 and active rectification reduces power dissipation in the output hold-up capacitor's ESR by half. Active rectification of 2-V peak-peak 30-KHz AC input is shown in Figure 9-3.

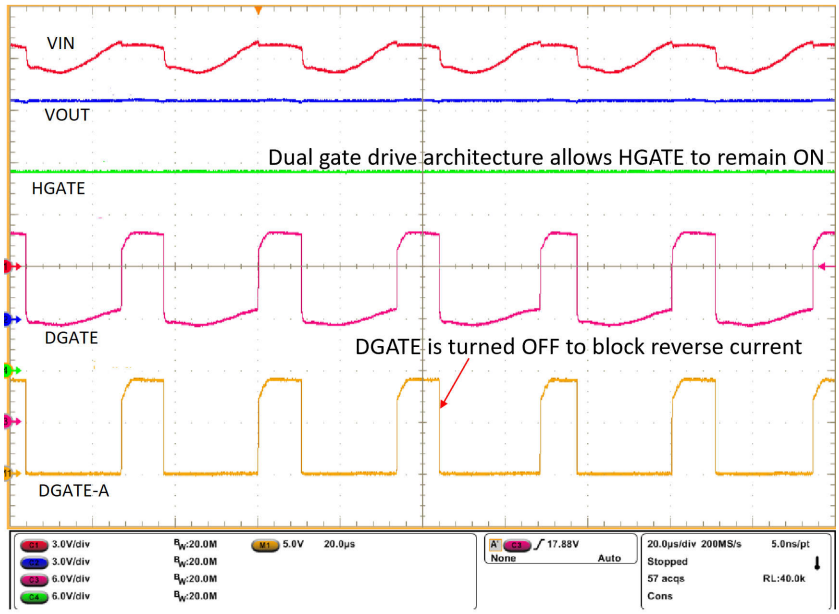


Figure 9-3. AC Super Imposed Test - 2-V Peak-Peak 30 KHz

9.2.2.3 Input Micro-Short Protection: LV124 E-10

E-10 test specified in LV124 standard checks for immunity of electronic modules to short interruptions in power supply input due to contact issues or relay bounce. During this test (case 2), micro-short is applied on the input for a duration as low as 10 µs to several ms. For a functional pass status A, electronic modules are required to run uninterrupted during the E-10 test (case 2) with 100-µs duration. Dual-Gate drive architecture of LM74912-Q1 - DGATE and HGATE - enables to achieve a functional pass status A with optimum hold up capacitance on the output when compared to a single gate drive controller. When input micro-short is applied for 100 µs, LM74912-Q1 quickly turns off MOSFET Q1 by shorting DGATE to ANODE (source of MOSFET) within 0.5µs to prevent the output from discharging and the HGATE remains ON keeping MOSFET Q2 ON, enabling fast recovery after the input short is removed.

Performance of LM74912-Q1 during E10 input power supply interruption test case 2 is shown in Figure 9-4. After the input short is removed, input voltage recovers and MOSFET Q1 is turned back ON within 130 µs. Note that dual-gate drive topology allows MOSFET Q2 to remain ON during the test and helps in restoring the input power faster. Output voltage remains unperturbed during the entire duration, achieving functional status A.

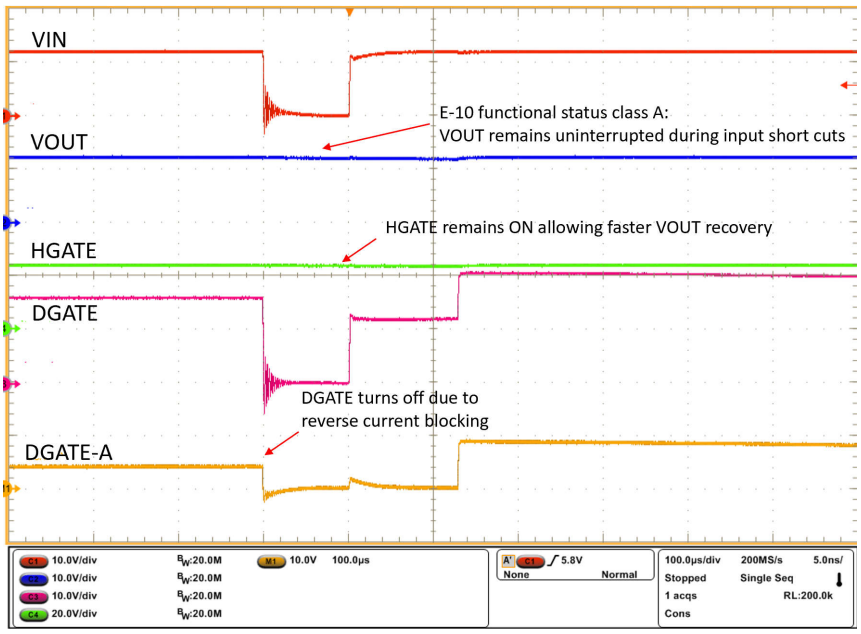


Figure 9-4. Input Micro-Short - LV124 E10 TC 2 100 µs

9.2.3 Detailed Design Procedure

9.2.3.1 Design Considerations

Table 9-1 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with overvoltage cut-off. During power up, inrush current through MOSFET Q2 needs to be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2 and maximum operating voltage determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q2 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple and ISO 7637-2 pulse 1 requirements. overvoltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2 and LM74912-Q1.

9.2.3.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capacitance of Q2 $C_{ISS(MOSFET)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET\_Q1)}$ + $C_{ISS(MOSFET\_Q2)}$) (µF)

9.2.3.3 Input , Supply and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended. VS pin acts as a power supply input- to the device. A decoupling capacitor of 0.1 µF minimum is recommended from VS pin to ground.

9.2.3.4 Hold-Up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning off the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74912-Q1 is based on the UVLO settings of downstream DC-DC converters. For this design, drop from 12-V to 6.5V in output voltage for 100 µs is considered (assuming downstream converter with 5-V output) and the minimum hold-up capacitance required is calculated by

$$C_{HOLD\_UP\_MIN} = \frac{I_{LOAD} \times 100\ \mu s}{\Delta V_{OUT}} \tag{5}$$

Minimum hold-up capacitance required for 5.5-V drop in 100 µs is 100 µF. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

9.2.3.5 Overvoltage Protection and Battery Monitor

Resistors R1, R2 and R3, R4 connected from SW pin to ground is used to program the undervoltage and overvoltage threshold. The resistor values required for setting the undervoltage threshold (VUVLO to 5.5 V) and overvoltage threshold (VOV to 37.0 V) a are calculated by solving Equation 6 and Equation 6.

$$V_{UVLOF} = \frac{R_2 \times V_{UVSET}}{(R_1 + R_2)} \tag{6}$$

$$V_{OVR} = \frac{R_4 \times V_{OVSET}}{(R_3 + R_4)} \tag{7}$$

For minimizing the input current drawn from the battery through resistors R_1, R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum

leakage current into the OV pin is 1 µA and choosing (R_1 + R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{UVLOF} is 0.55 V. Select R1 = 100 kΩ. Solving Equation 14 gives R_2 = 11.5 kΩ. Solving Equation 15 with R_3 selected as 100 kΩ and V_{OVR} = 0.6V gives R_4 = 1.65 kΩ as standard 1% resistor values closest to the calculated resistor values.

An optional capacitor C_{UV} can be placed in parallel with R2 on UVLO resistor ladder in order to filter out any fast undervoltage transients on battery lines to avoid false UVLO trigger.

For this application example separate resistor ladder is selected to program overvoltage and undervoltage threshold. However common resistor ladder from SW pin to ground can also be used as shown in Section 8.3.4

9.2.3.6 Selecting Short Circuit Current Threshold

LM74912-Q1 has integrated current sense amplifier which monitors the VDS drop across external MOSFET and compares it against internal 50-mV default threshold. When voltage drop across external MOSFET exceeds 50-mV threshold then MOSFET Q2 is turned off in latched state.

External MOSFET Q2 R_{DSON} can be selected as per

$$RDS_{ON} = \frac{50\ mV}{I_{SCP}} \tag{8}$$

MOSFET RDS_{ON} typically can vary as much as two times across temperature range of -40C to 125C with R_{DSON} being higher at 125C. This can affect the short circuit current detection accuracy and need to be taken into consideration.

9.2.3.6.1 Selection of Scaling Resistor R_{SET} and R_{ISCP} for Short Circuit Protection

R_{SET} is the resistor connected between common drain point and CS+ pins. This resistor scales the short circuit protection threshold voltage in positive direction while resistor R_{ISCP} connected from ISCP pin to VOUT scales short circuit threshold in negative direction. The shift in the VDS sense threshold voltage for short circuit detection can be calculated per the following equations

$$V_{DS\_SNS} = 50\ mV + (11\ \mu A \times R_{SET}) \tag{9}$$

$$V_{DS\_SNS} = 50\ mV - (11\ \mu A \times R_{ISCP}) \tag{10}$$

An additional de-glitch filter (optional) consisting of R_{SCP} and C_{SCP} can be added from ISCP pin to CS– pin, as shown in Figure 9-1, to avoid any false short circuit trigger in case of fast automotive transients such as Input Micro cuts (LV124, E-10), AC superimpose (LV124, E-06), or ISO7637-2 Pulse 2A.

9.2.4 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include all the automotive transient events and any anticipated fault conditions. It is recommended to use MOSFETs with V_{DS} voltage rating of 60 V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back to back at the input.

The maximum V_{GS} LM74912-Q1 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level, but this would result in increased I_Q current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to

LM74912-Q1 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point.

For active rectification of AC super imposed ripple on the battery supply voltage, gate-source charge Q_{GS} of Q1 must be selected to meet the required AC ripple frequency. Maximum gate-source charge Q_{GS} (at 4.5-V V_{GS}) for active rectification every cycle is:

$$Q_{GS\_MAX} = \frac{2.5\ mA}{F_{AC\_RIPPLE}} \tag{11}$$

Where 2.5 mA is minimum charge pump current at 7 V ($V_{DGATE} – V_A$). F_{AC_RIPPLE} is frequency of the AC ripple superimposed on the battery and Q_{GS_MAX} is the Q_{GS} value specified in manufacturer data sheet at 6-V V_{GS}.

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.5 MOSFET Selection: Hot-Swap MOSFET Q2

The V_{DS} rating of the MOSFET Q2 should be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12-V design, transient overvoltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2 A 50 V for 50 µs. Further, ISO 7637-2 Pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors and the maximum voltage on the 12-V battery can be limited to < 40 V the minimum recommended input capacitance of 0.1 µF. The 50-V SO 7637-2 Pulse 2 A can also be absorbed by input and output capacitors and its amplitude could be reduced to 40-V peak by placing sufficient amount of capacitance at input and output. However for this 12-V design, maximum system voltage is 50 V and a 60-V V_{DS} rated MOSFET is selected.

The VGS rating of the MOSFET Q2 should be higher than that maximum HGATE-OUT voltage 15 V.

Inrush current through the MOSFET during input hot-plug into the 12-V battery is determined by output capacitance. External capacitor on HGATE, C_{dVdT} is used to limit the inrush current during input hot-plug or startup. The value of inrush current determined by Equation 2 need to be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA).

MOSFET BUK7Y4R8-60E having 60-V V_{DS} and ±20-V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET's safe operating area (SOA).

9.2.6 TVS Selection

A 600-W SMBJ series TVS such as SMBJ33CA is recommended for input transient clamping and protection. For detailed explanation on TVS selection for 12-V battery systems, refer to *TVS Selection for 12-V Battery Systems*.

9.2.7 Application Curves

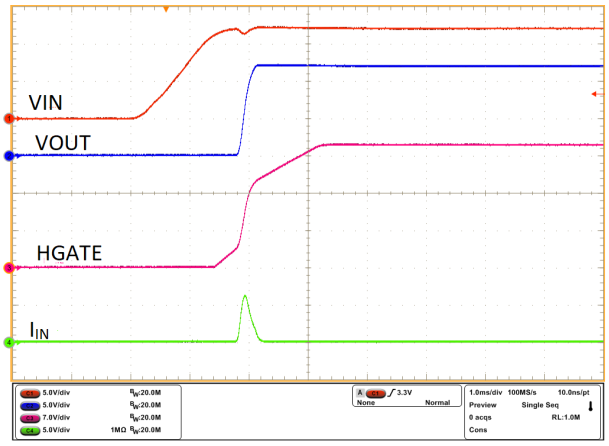


Figure 9-5. Startup 12 V with EN Pulled to VS

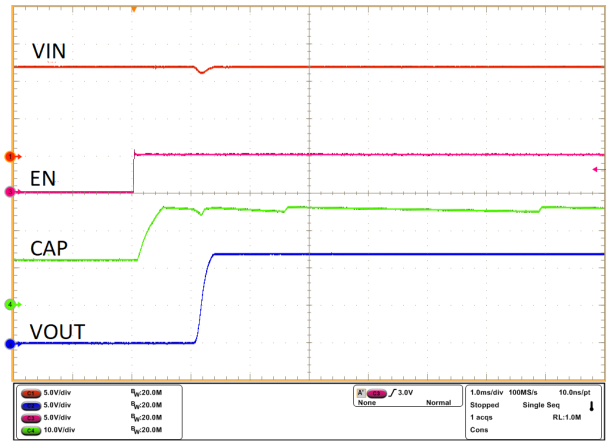


Figure 9-6. Startup with EN Going Low to High

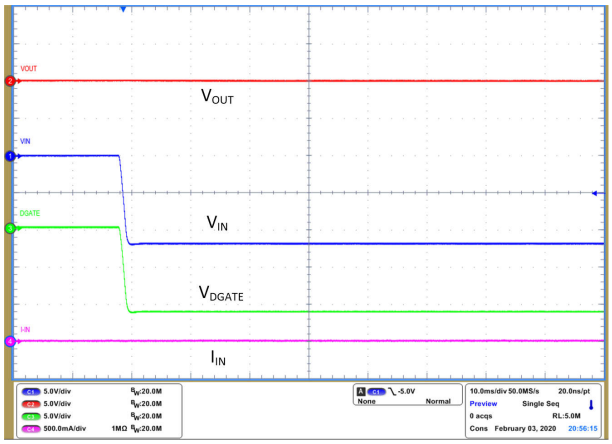


Figure 9-7. Reverse Input Voltage –14 V

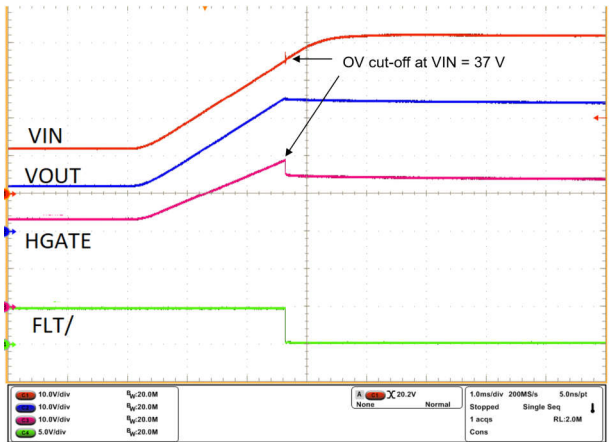


Figure 9-8. Overvoltage Protection

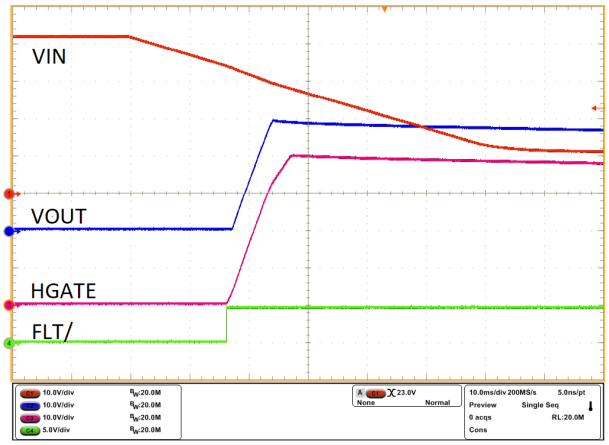


Figure 9-9. Overvoltage Recovery

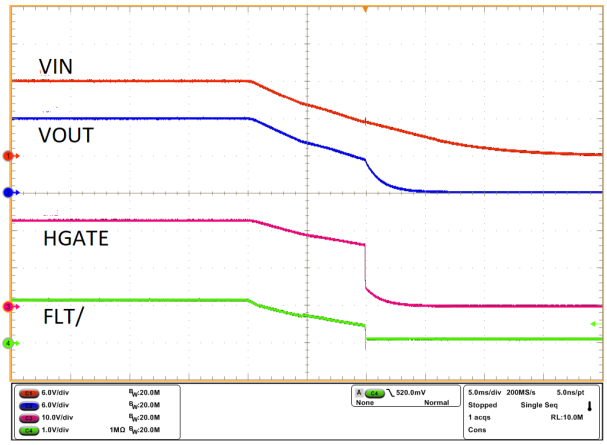


Figure 9-10. Undervoltage Cut-Off Response

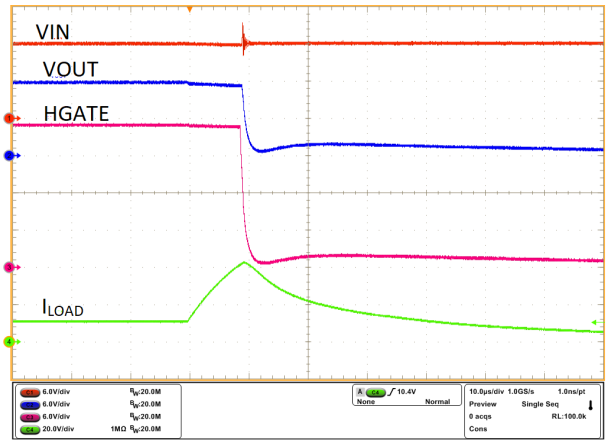


Figure 9-11. Short Circuit Protection

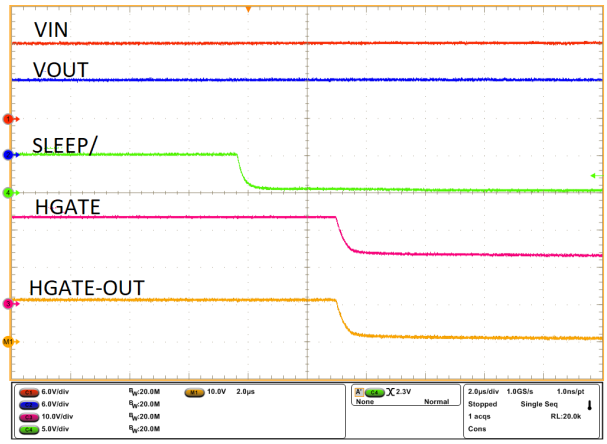


Figure 9-12. SLEEP Mode Entry

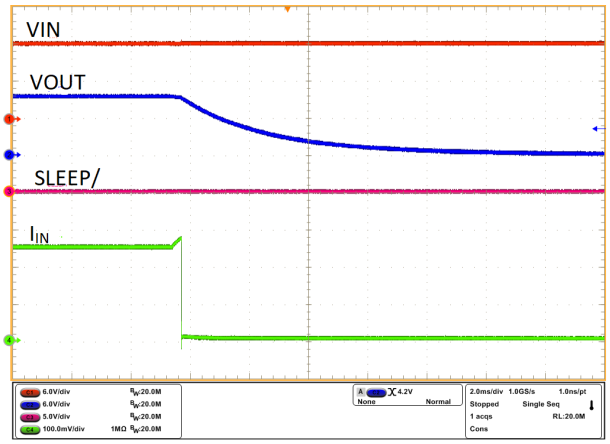


Figure 9-13. SLEEP Mode Overcurrent Protection

9.3 Best Design Practices

Leave exposed pad (RTN) of the IC floating. Do not connect it to the GND plane. Connecting RTN to GND disables the Reverse Polarity protection feature.

9.4 Power Supply Recommendations

9.4.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as overcurrent, overvoltage undervoltage cut-off, reverse current blocking causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Section 6.1* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device.
- Using large PCB GND plane.
- Use of a Schottky diode across the output and GND to absorb negative spikes.
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 12.

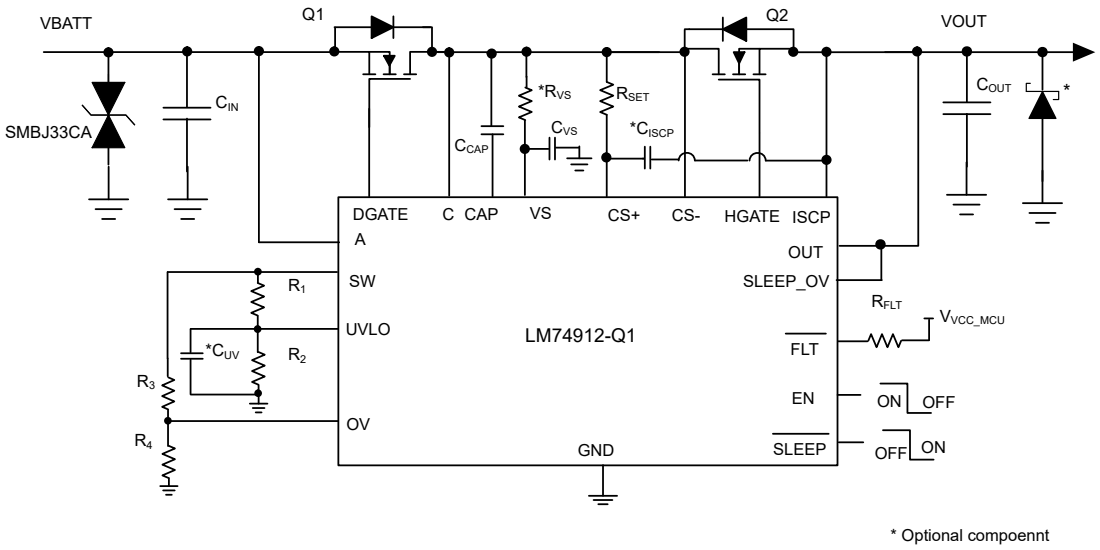
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (12)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional transient voltage suppressor (TVS) to prevent transients from exceeding the *Section 6.1* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

The circuit implementation with optional protection components (a ceramic capacitor, TVS, and Schottky diode) is shown in Figure 9-14



* Optional components needed for suppression of transients

Figure 9-14. Circuit Implementation With Optional Protection Components for LM74912-Q1

9.4.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74912-Q1 (65 V). The breakdown voltage of TVS- should be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM74912-Q1 (85 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM74912-Q1 is pulled down by the ISO pulse, clamped by TVS- and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- should not exceed, (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current as shown and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS' are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

9.4.3 TVS Selection for 24-V Battery Systems

For 24-V battery protection application, the TVS and MOSFET in Figure 9-1 needs to be changed to suit 24-V battery requirements.

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74912-Q1 (70 V) and should withstand 65-V suppressed load dump. The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12-A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (-TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- should not exceed, 85 V – 32 V = 53 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65V, maximum clamping voltage is ≤ 53 V and the clamping voltage cannot be less than the breakdown voltage. Two uni-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ28A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ28A and SMBJ58A connected back-back at the input.

9.5 Layout

9.5.1 Layout Guidelines

- For the ideal diode stage, connect A, DGATE and C pins of LM74912-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- For the load disconnect stage, connect HGATE and OUT pins of LM74912-Q1 close to the MOSFET's GATE and SOURCE pins.
- The high current path for this solution is through the MOSFET, therefore it is important to use thick and short traces for source and drain of the MOSFET to minimize resistive losses.
- The DGATE pin of the LM74912-Q1 must be connected to the MOSFET GATE with short trace.
- Place transient suppression components close to LM74912-Q1.
- Place the decoupling capacitor, C_{VS} close to VS pin and chip GND.
- The charge pump capacitor across CAP and VS pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- Keep device exposed pad (RTN) floating. Do not connect RTN to ground plane.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and to produce good results.

9.5.2 Layout Example

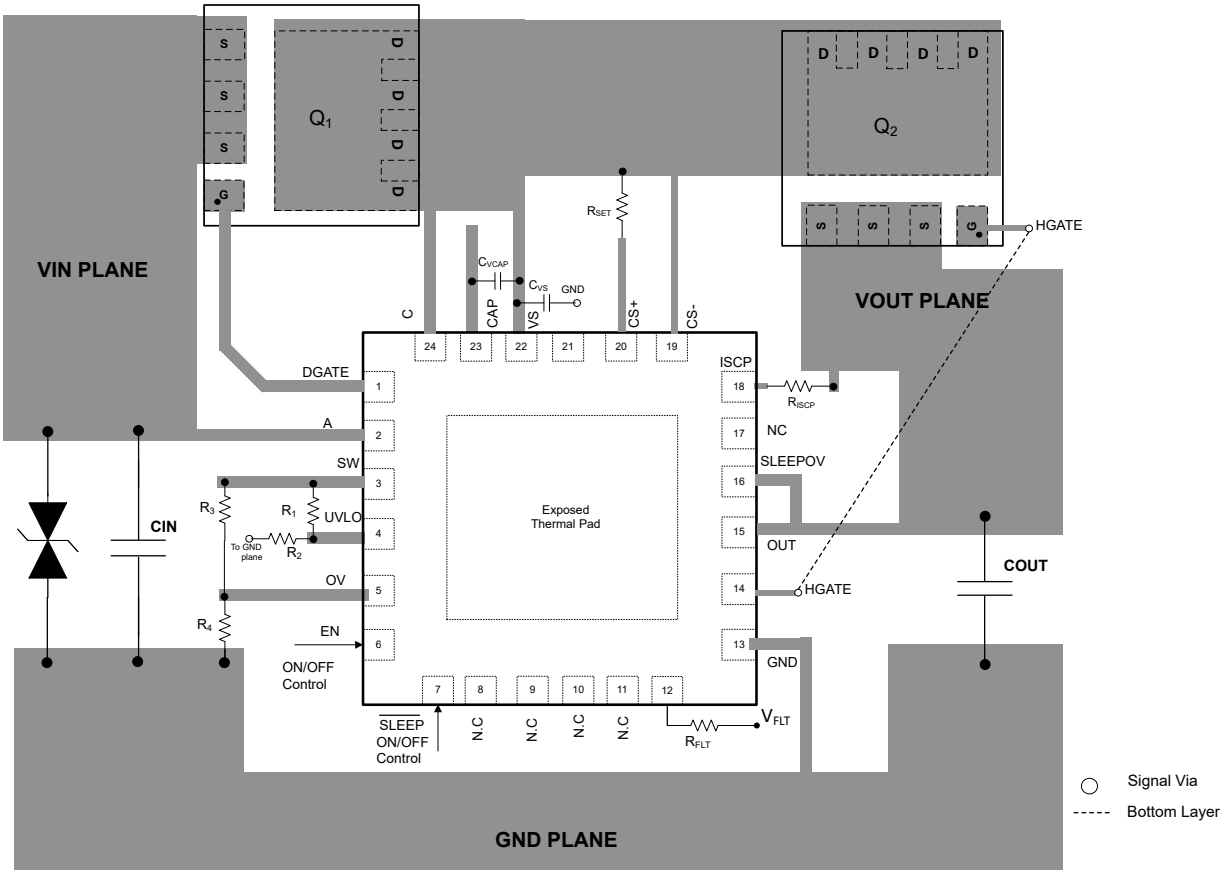


Figure 9-15. PCB Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM74912QRGERQ1	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 74912Q
PLM74912QRGERQ1	Active	Preproduction	VQFN (RGE) | 24	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

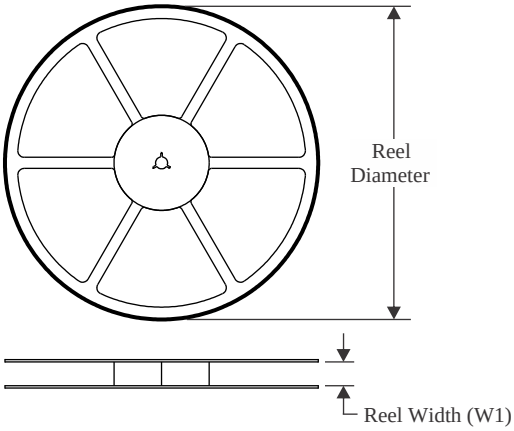
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

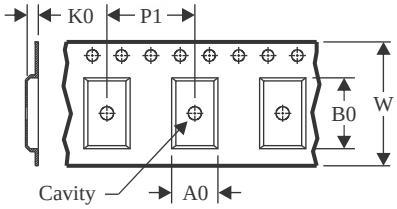
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

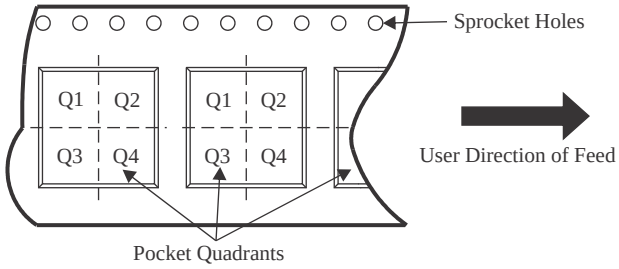


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

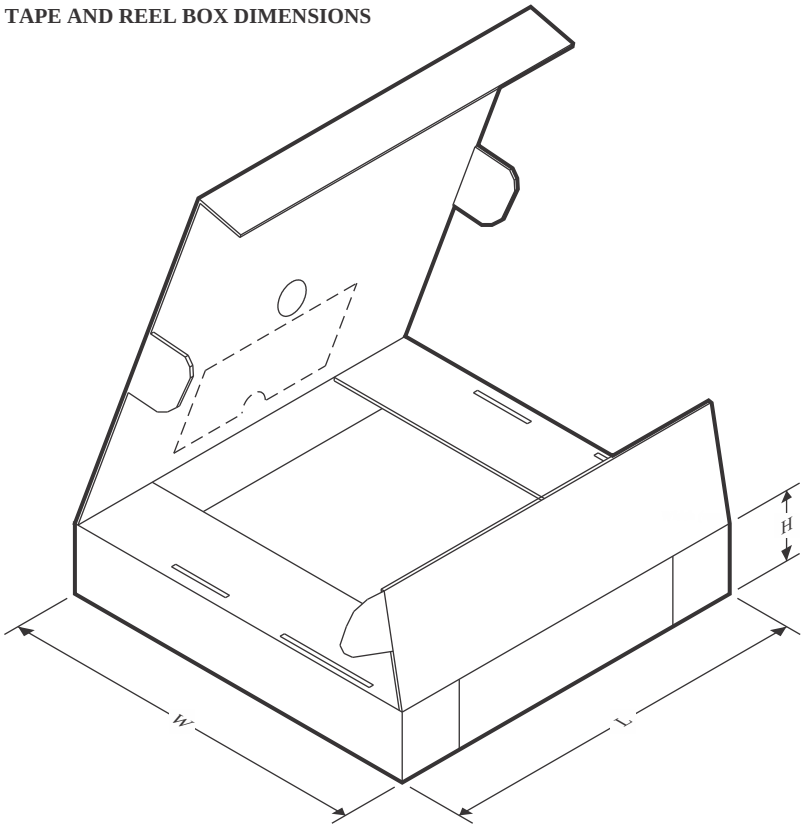
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74912QRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



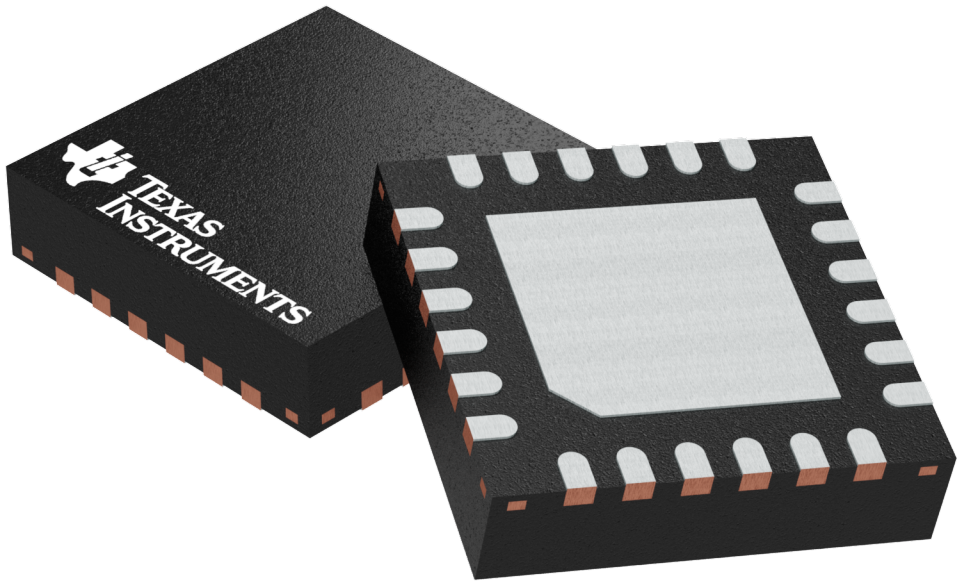
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74912QRGERQ1	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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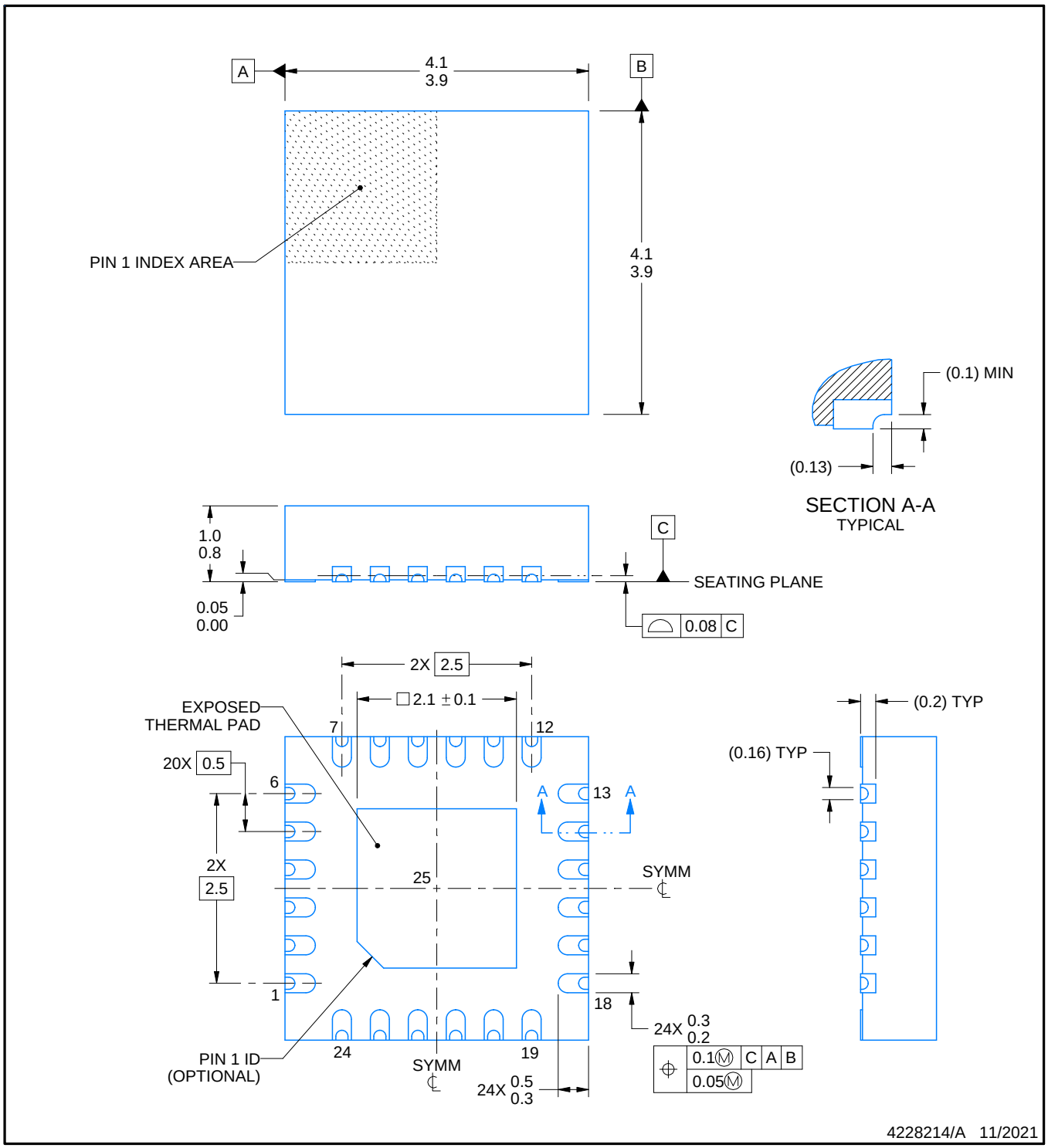
RGE0024T

PACKAGE OUTLINE

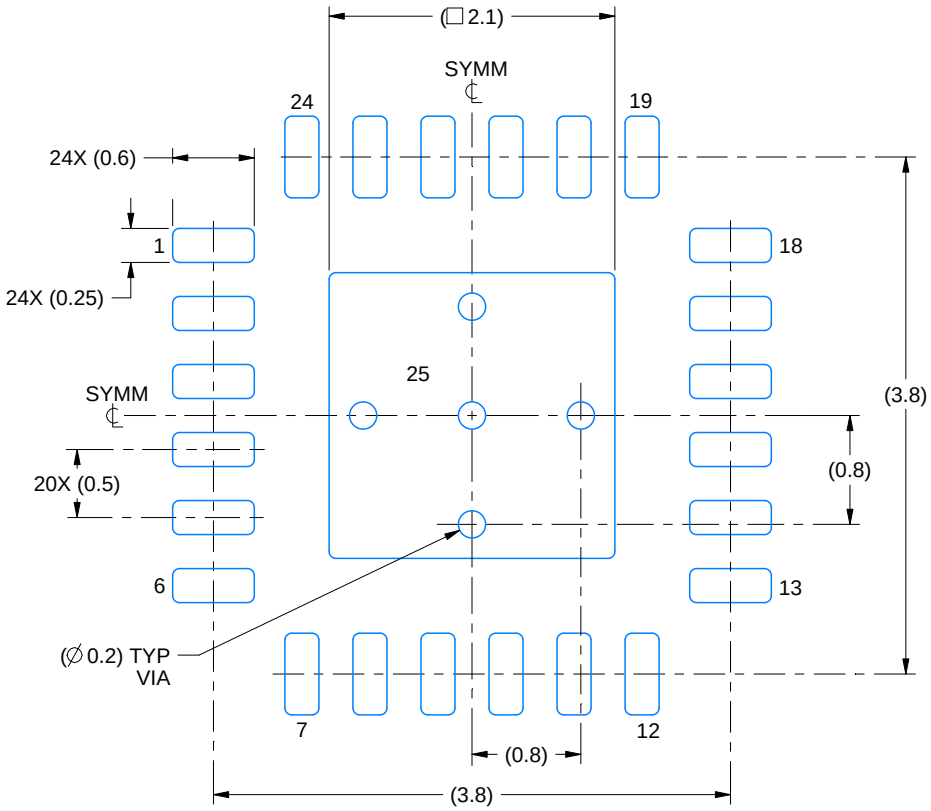
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

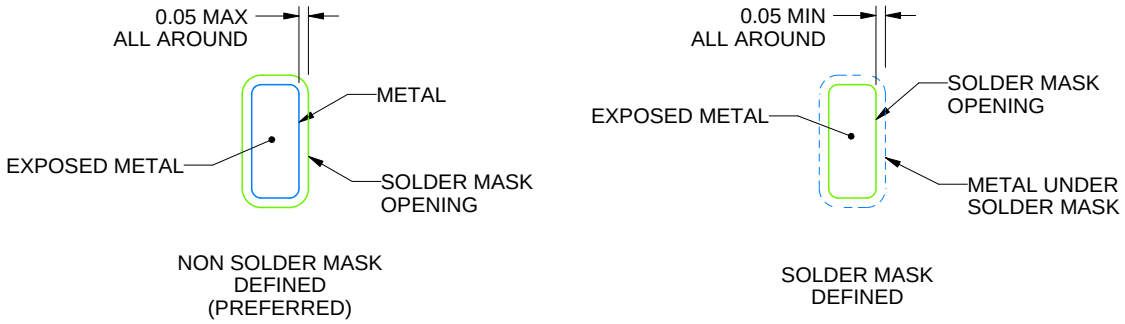


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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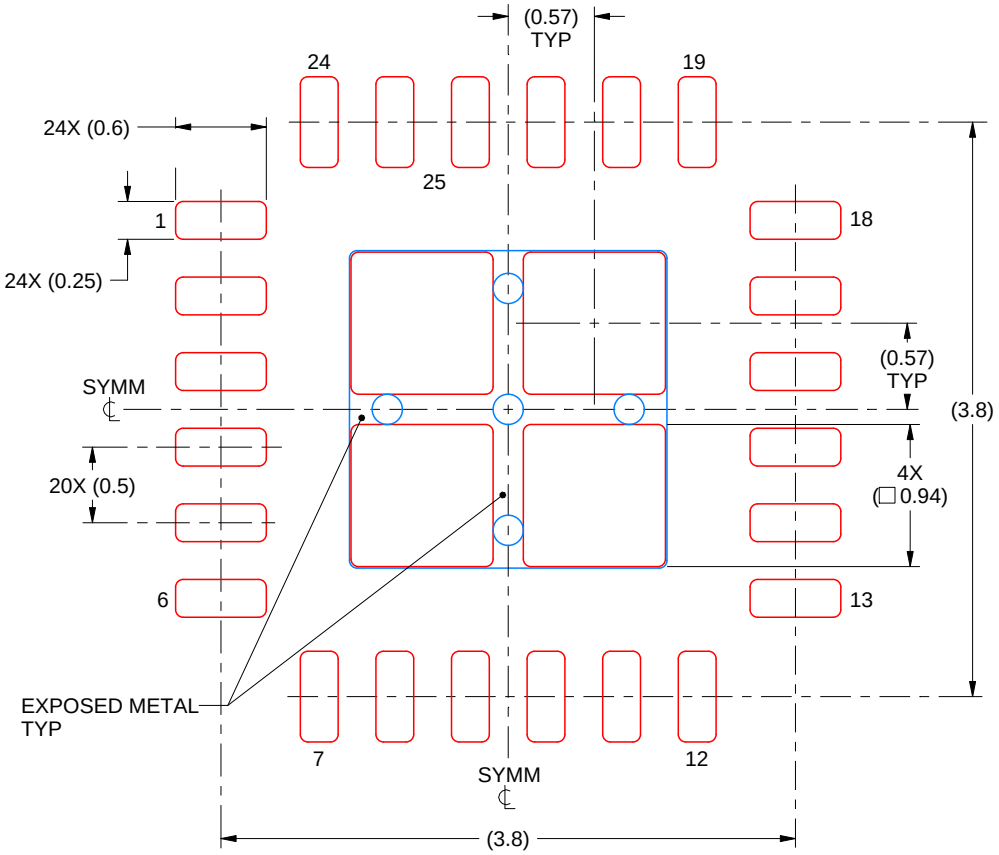
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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