LM8207 TFT 18 Gamma Buffer + V_{COM} Driver + Voltage Reference

Check for Samples: LM8207

FEATURES

- **Gamma Buffers 1-2 Swing to V_{DD}**
- **Gamma Buffers 17-18 Swing to V_{SS}**
- **Large Output Current V_{COM} Driver (I_{SC} = 300 mA)**
- **Stable (1%) Internal 1.295V Reference, to Improve Picture Quality and Reduce Variations**
- **48-pin TSSOP Package**

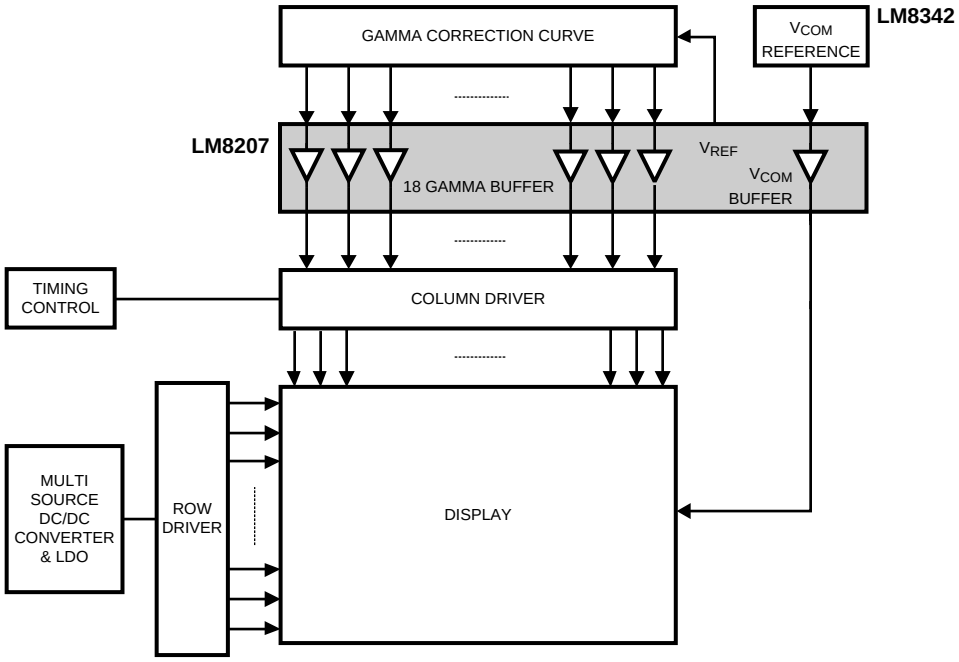
APPLICATIONS

- **TFT Gamma Curve Connection and V_{COM} Voltage Buffering**

DESCRIPTION

The LM8207 is a combination of 18-channel gamma buffers, a V_{COM} driver and a temperature compensated internal voltage reference. It is designed for buffering voltage levels and driving high capacitive loads in large TFT panels. The gamma buffers are individually optimized to the input/output requirements of their respective gamma position to cover the whole voltage range from rail to rail. Any desired gamma correction curve can be obtained by combining the gamma buffers with external resistors. The V_{COM} driver has a high output current capability and is stable with large capacitive loads, typical for large panel sizes. This will result in a fast recovery time for large voltage variations at the output. The internal band gap reference can be used to form a highly stable voltage to generate the gamma correction voltages. In combination with the internal amplifier, the reference voltage can be programmed to voltages up to the positive rail. The LM8207 is offered in a 48-pin TSSOP package.

TFT Panel Block Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body	2.5 kV
	Machine Model	250V
Supply Voltage (V_{DD} - V_{SS})		18V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(4)		+150°C
Soldering Information		
Infrared or Convection (20 sec.)		230°C
Wave Soldering (10 sec.)		260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) When the output of the V_{COM} buffer exceeds the supply rails, while sinking or sourcing 100 mA, the V_{COM} output is susceptible to latch.
(3) Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Operating Temperature Range		−40°C to +105°C
Operating Voltage Range		6V to 16V
Package Thermal Resistance, θ_{JA}(2)	48-Pin TSSOP	84°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

16V Electrical Characteristics[1]

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V, & C_{LOAD} = 100 pF (Gamma & V_{COM} Buffers). **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min[2]	Typ[3]	Max[2]	Units
Gamma Buffers							
BW_Gamma	−3 dB Bandwidth				2		MHz
SR_Gamma	Slew Rate[4]				1		V/µs
T_{REC}_Gamma	Output Recovery Time[5]				400		ns
V_{IN}_Gamma	Input Voltage Range	Buffer 1-2	Positive		V_{DD}		V
			Negative		V_{SS} +0.6		
		Buffer 3-8 & 11-16	Positive		V_{DD}-0.6		
			Negative		V_{SS} +0.6		
		Buffer 9	Positive		V_{DD} −0.6		
			Negative		V_{SS}		
		Buffer 10	Positive		V_{DD}-0.6		
			Negative		V_{SS} +0.6		
		Buffer 17-18	Positive		V_{DD} −0.6		
			Negative		V_{SS}		
V_{OUT}_Gamma	Output Voltage Range	Buffer 1-2, No Load	Positive	V_{DD} -0.25	V_{DD} -0.1		V
			Negative		V_{SS} +1.5	V_{SS} +1.6	
		Buffer 3-8 & 11-16 No Load	Positive	V_{DD} −1.2	V_{DD} -1.1		
			Negative		V_{SS} +0.6	V_{SS} +0.7	
		Buffer 9, No Load	Positive	V_{DD} −1.0	V_{DD} -0.8		
			Negative		V_{SS} +0.8	V_{SS} +0.9	
		Buffer 10, No Load	Positive	V_{DD} –1.2	V_{DD} –1.1		
			Negative		V_{SS} +0.6	V_{SS} +0.7	
		Buffer 17-18, No Load	Positive	V_{DD} –1.6	V_{DD} –1.5		
			Negative		V_{SS} +0.1	V_{SS} +0.25	
I_{BIAS}_Gamma	Absolute, Input Bias Current	Within Gamma Buffer Output Voltage Range			30		nA
V_{OS}_Gamma	Input Offset Voltage	Buffer 1-2, V_{IN} = 8V			5	10	mV
		Buffer 3-8, 11-16, V_{IN} = 8V			1	5	
		Buffer 9, V_{IN} = 8V			1	5	
		Buffer 10, V_{IN} = 8V			1	5	
		Buffer 17-18, V_{IN} = 8V			5	10	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing condition result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical table under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are specified by design or statistical analysis.
(3) Typical values represent the parametric norm at the time of characterization.
(4) Slew Rate is measured for V_{IN} = 4 V_{PP}. 10% -90% values are used. Slew rate is the average of the rising and falling slew rates
(5) 4 V_{PP} pulse (50 ns rise time) applied to one side of 100 pF series output capacitance, other side connected to output of buffer. Output to within 0.1% of input voltage.

16V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V, & C_{LOAD} = 100 pF (Gamma & V_{COM} Buffers). **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min[2]	Typ[3]	Max[2]	Units
I_{OUT}_Gamma	Linear Output Current[6]	Buffer 1-2	Sourcing	20	46		mA
			Sinking	0.2	0.33		
		Buffer 3-8 & 11-16	Sourcing	10	24.5		
			Sinking	3.5	5.5		
		Buffer 9	Sourcing	4.5	9.4		
			Sinking	15	27		
		Buffer 10	Sourcing	23	34.8		
			Sinking	3.5	5.5		
		Buffer 17-18	Sourcing	0.2	0.33		
			Sinking	20	50		
PSRR	Power Supply Rejection Ratio	V_{DD} - V_{SS} = 6V to 16V		75	88		dB
V_{COM} Driver							
BW_V_{COM}	Bandwidth				10		MHz
SR_ V_{COM}	Slew Rate[4]				4.5		V/µs
$T_{\_REC\_V_{COM}}$	Output Recovery Time[5]				200		ns
V_{IN}_V_{COM}	Input Voltage Range	Positive			V_{DD}		V
		Negative			V_{SS} +0.6		
V_{OUT}_V_{COM}	Output Voltage Range	No Load	Positive	V_{DD} –1.0	V_{DD} –0.7		V
			Negative		V_{SS} +0.9	V_{SS} +1.2	
I_{BIAS}_V_{COM}	Input Bias Current	Within V_{COM} Buffer Output Voltage Range			50		nA
V_{OS}_V_{COM}	Input Offset Voltage	V_{IN} = 8 V			1	10	mV
I_{OUT_LIN}_V_{COM}	Linear Output Current[6][7]	Sourcing			160		mA
		Sinking			150		
I_{OUT}_SC_V_{COM}	Short Circuit Output Current[7][8]	Sourcing		220	300		mA
		Sinking		220	300		
PSRR	Power Supply Rejection Ratio	V_{DD} - V_{SS} = 6V to 16V		75	88		dB
Voltage Reference Section							
V_{REF}	Voltage	No Load		1.28	1.295	1.31	V
Reg_{LOAD}	Load Regulation	I_{OUT} = 0 to 10 mA			0.14		mV/mA
V_{REF_ACC}	Voltage Accuracy	No Load, V_{REF} = 1.295V			1		%
V_{REF_MAX}	Max Programming Range	I_{OUT} = 4 mA			V_{DD} −0.3		V
I_{IN}_V_{REF}	Input Bias Current	Within V_{REF} Output Voltage Range			10	50	nA
TC_V_{REF}	Temperature Stability				70		ppm/°C
I_{OUT}_V_{REF}	Max Output Current	Sourcing, V_{OUT} = 1.295 V			71		mA
PSRR	Power Supply Rejection Ratio (Line Regulation)			70	80		dB
Miscellaneous							
I_S	Supply Current			4.5	6.5	8.5 **9.5**	mA

(6) Linear output current measured at $|V_{OUT} - V_{IN}|$ = 0.1V.
(7) This is a momentary test. Continuous large output currents may result in exceeding the maximum power dissipation and damage the device.
(8) Short circuit current measured at $|V_{OUT} - V_{IN}|$ = 1V.

Connection Diagram

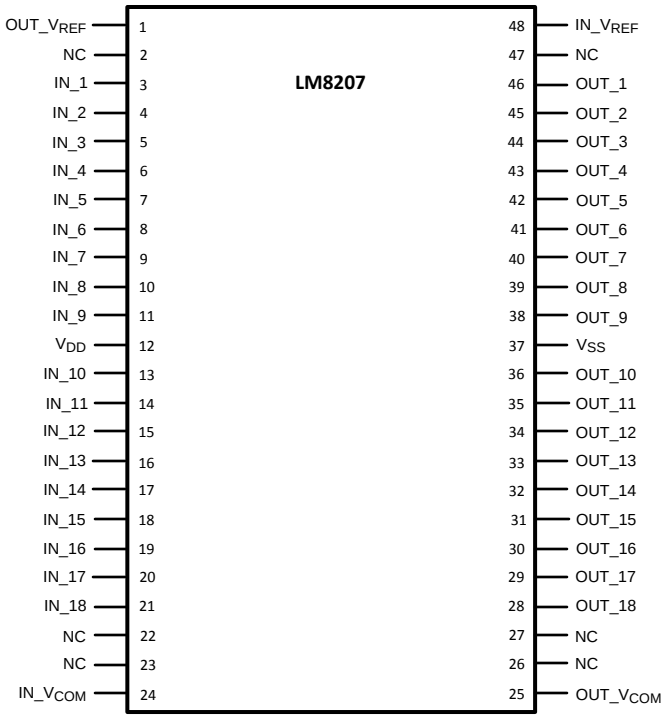


Figure 1. 48-Pin TSSOP
Top View

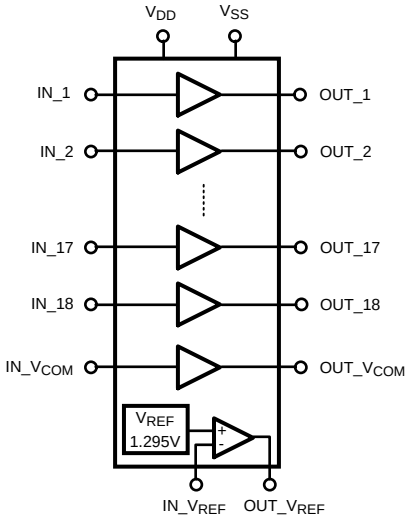
PIN DESCRIPTIONS

Pin #	Description	Remark
1	OUT_V_{REF}	Reference voltage amplifier output
2	NC	No connection
3	IN_1	Input gamma buffer 1
4	IN_2	Input gamma buffer 2
5	IN_3	Input gamma buffer 3
6	IN_4	Input gamma buffer 4
7	IN_5	Input gamma buffer 5
8	IN_6	Input gamma buffer 6
9	IN_7	Input gamma buffer 7
10	IN_8	Input gamma buffer 8
11	IN_9	Input gamma buffer 9
12	V_{DD}	Positive supply voltage (V_{DD})
13	IN_10	Input gamma buffer 10
14	IN_11	Input gamma buffer 11
15	IN_12	Input gamma buffer 12
16	IN_13	Input gamma buffer 13
17	IN_14	Input gamma buffer 14
18	IN_15	Input gamma buffer 15
19	IN_16	Input gamma buffer 16
20	IN_17	Input gamma buffer 17
21	IN_18	Input gamma buffer 18
22,23	NC	No connection

PIN DESCRIPTIONS (continued)

24	IN_V_{COM}	Input V_{COM}
25	OUT_V_{COM}	Output V_{COM}
26,27	NC	No connection
28	OUT_18	Output gamma buffer 18
29	OUT_17	Output gamma buffer 17
30	OUT_16	Output gamma buffer 16
31	OUT_15	Output gamma buffer 15
32	OUT_14	Output gamma buffer 14
33	OUT_13	Output gamma buffer 13
34	OUT_12	Output gamma buffer 12
35	OUT_11	Output gamma buffer 11
36	OUT_10	Output gamma buffer 10
37	V_{SS}	Negative supply voltage (V_{SS})
38	OUT_9	Output gamma buffer 9
39	OUT_8	Output gamma buffer 8
40	OUT_7	Output gamma buffer 7
41	OUT_6	Output gamma buffer 6
42	OUT_5	Output gamma buffer 5
43	OUT_4	Output gamma buffer 4
44	OUT_3	Output gamma buffer 3
45	OUT_2	Output gamma buffer 2
46	OUT_1	Output gamma buffer 1
47	NC	No connection
48	IN_V_{REF}	Reference voltage amplifier feedback input

Block Diagram



Typical Performance Characteristics

At T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V. Unless otherwise specified.

Output Voltage Swing (Negative rail)

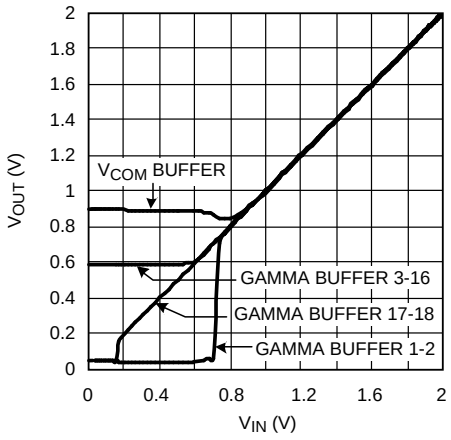


Figure 2.

Output Voltage Swing (Positive rail)

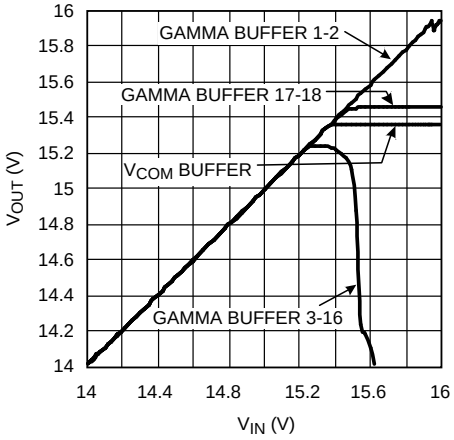


Figure 3.

Voltage Drop vs. Output Current (V_{COM} Buffer)

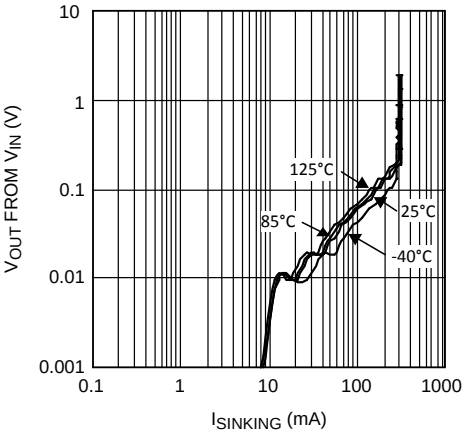


Figure 4.

Voltage Drop vs. Output Current (V_{COM} Buffer)

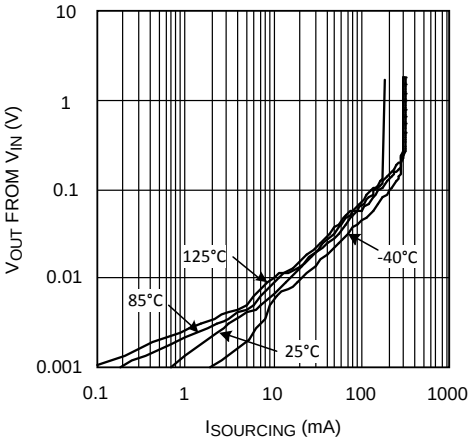


Figure 5.

Voltage Drop vs. Output Current (Gamma Buffer)

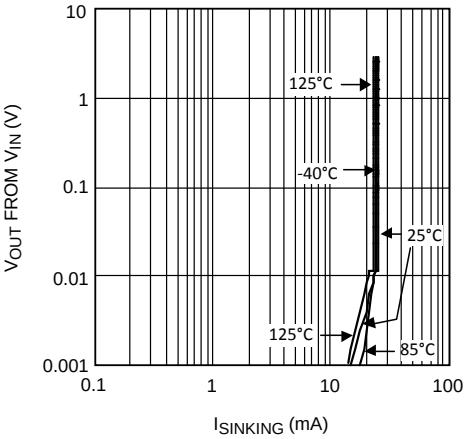


Figure 6.

Voltage Drop vs. Output Current (Gamma Buffer)

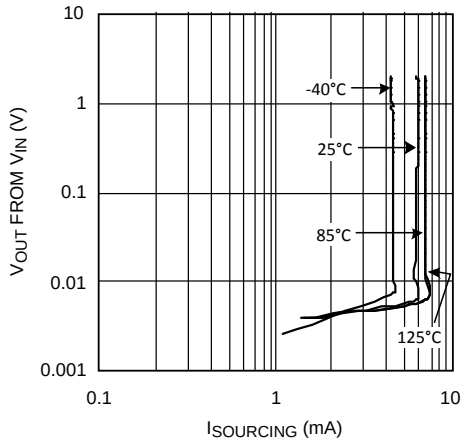


Figure 7.

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V. Unless otherwise specified.

Offset Voltage vs. Supply Voltage (Gamma Buffer)

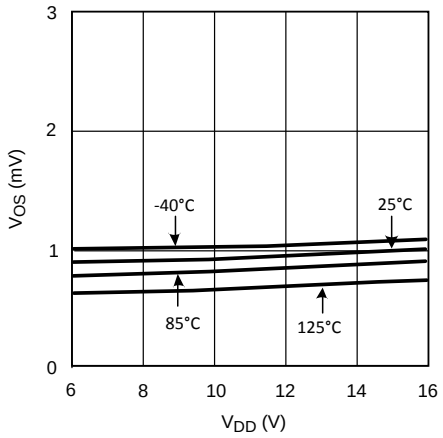


Figure 8.

Offset Voltage vs. Supply Voltage (V_{COM} Buffer)

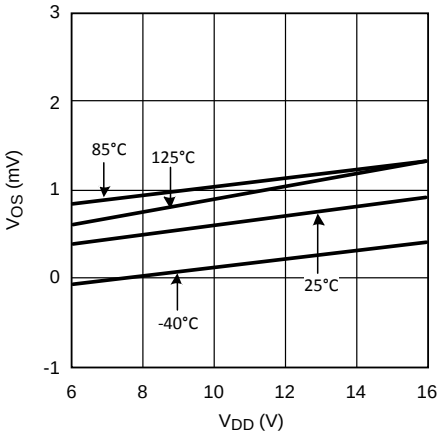


Figure 9.

Recovery Time (V_{COM} Buffer) Negative Slope (C_L = 100 pF)

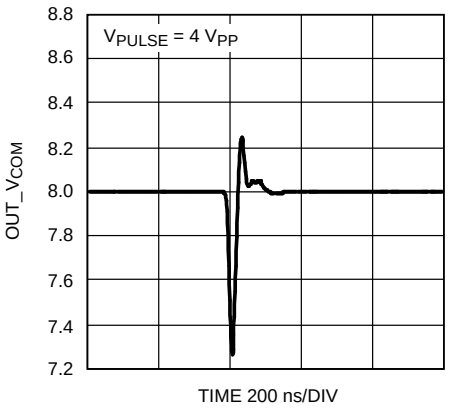


Figure 10.

Recovery Time (V_{COM} Buffer) Positive Slope (C_L = 100 pF)

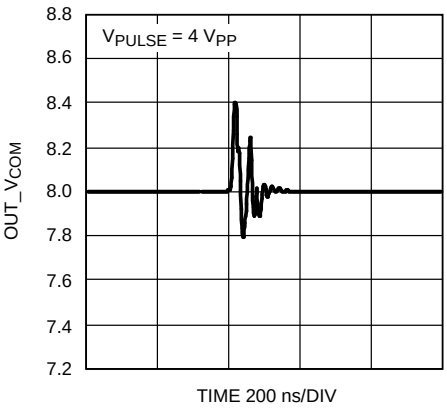


Figure 11.

Large Signal Transient Response (V_{COM} Buffer) Negative Slope (C_L = 100 pF)

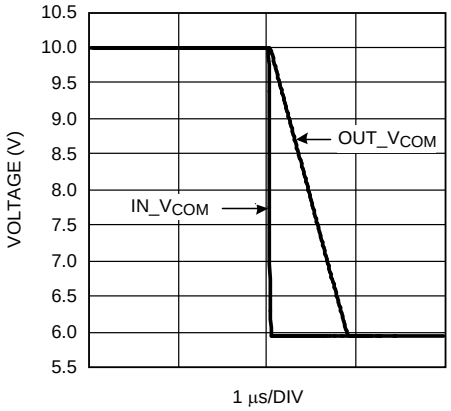


Figure 12.

Large Signal Transient Response (V_{COM} Buffer) Positive Slope (C_L = 100 pF)

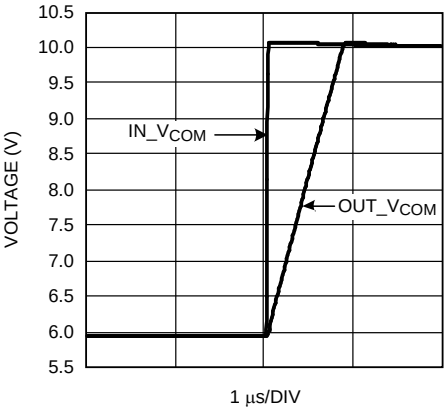


Figure 13.

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V. Unless otherwise specified.

Frequency Response for Various Temperature (V_{COM} Buffer)

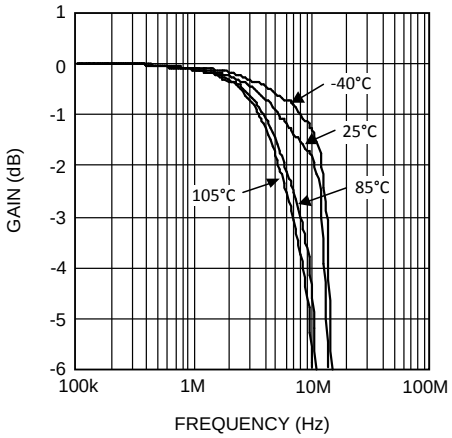


Figure 14.

Frequency Response for Various Load (V_{COM} Buffer)

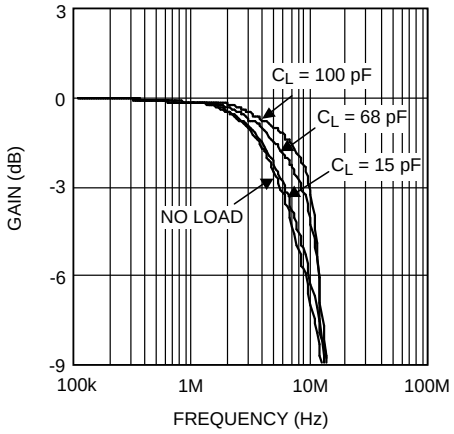


Figure 15.

Gain/Phase (Gamma Buffer) (C_L = 100 pF)

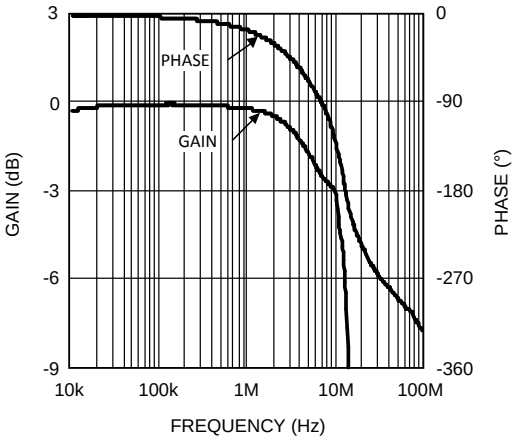


Figure 16.

PSRR (V_{COM} Buffer)

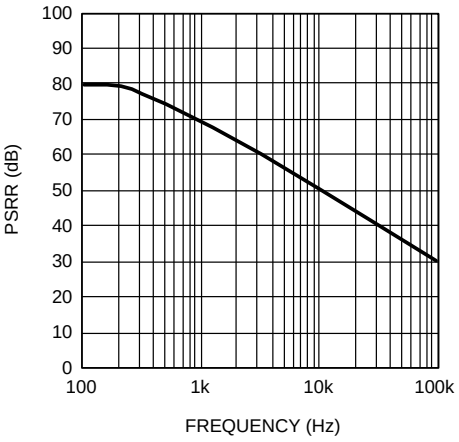


Figure 17.

Recovery Time (Gamma Buffer 3-16) Negative Slope (C_L = 100 pF)

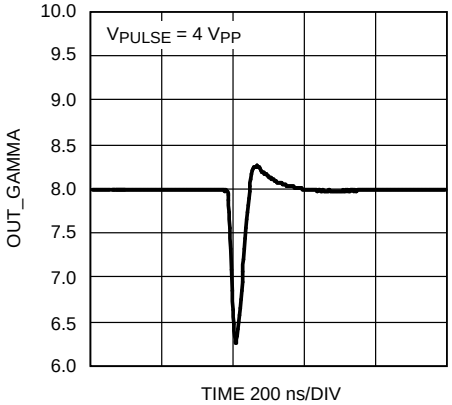


Figure 18.

Recovery Time (Gamma Buffer 3-16) Positive Slope (C_L = 100 pF)

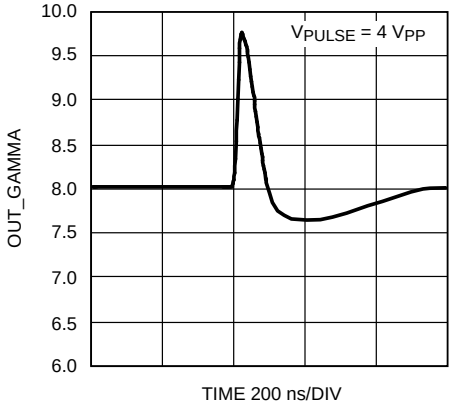


Figure 19.

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V. Unless otherwise specified.

Large Signal Transient Response (Gamma Buffer 3-16) Negative slope (C_L = 100 pF)

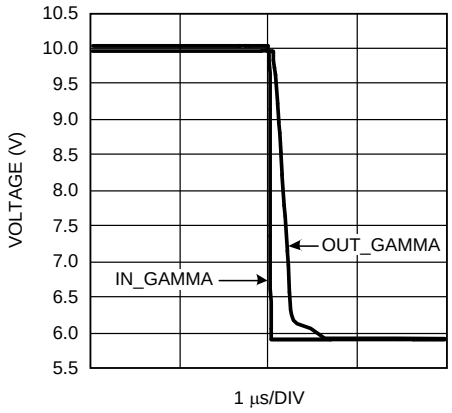


Figure 20.

Large Signal Transient Response (Gamma Buffer 3-16) Positive slope (C_L = 100 pF)

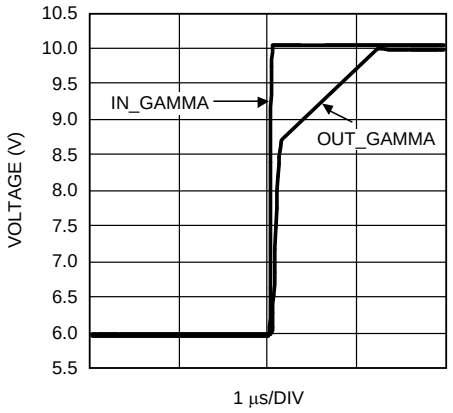


Figure 21.

Frequency Response for Various Load (Gamma Buffer)

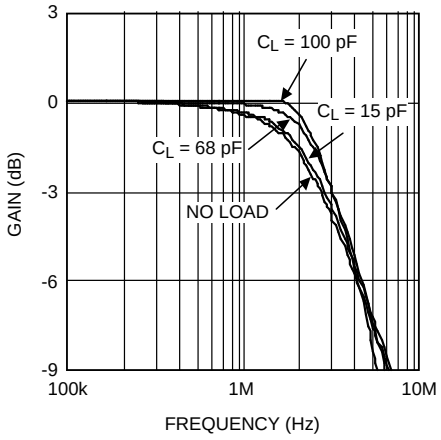


Figure 22.

Frequency Response for Various Temperature (Gamma Buffer)

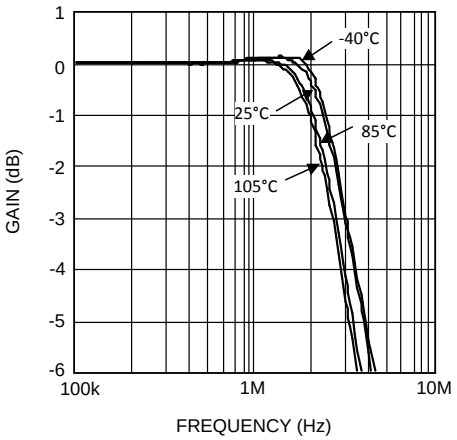


Figure 23.

Gain/Phase (Gamma Buffer) (C_L = 100 pF)

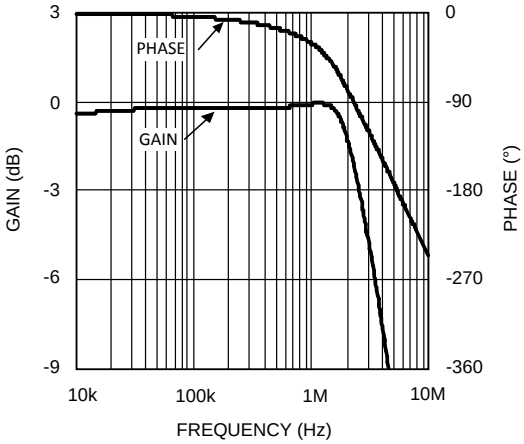


Figure 24.

PSRR (Gamma Buffer)

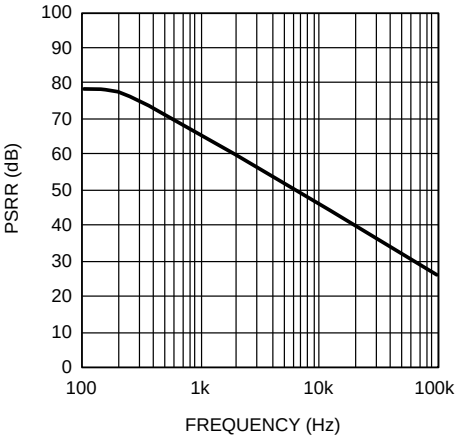


Figure 25.

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 16V, V_{SS} = 0V. Unless otherwise specified.

Supply Current vs. Supply Voltage

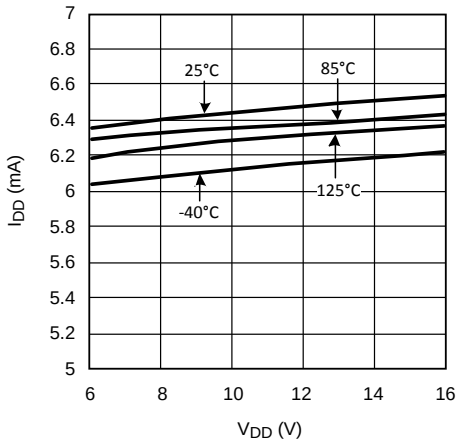


Figure 26.

Voltage Reference vs. Output Current

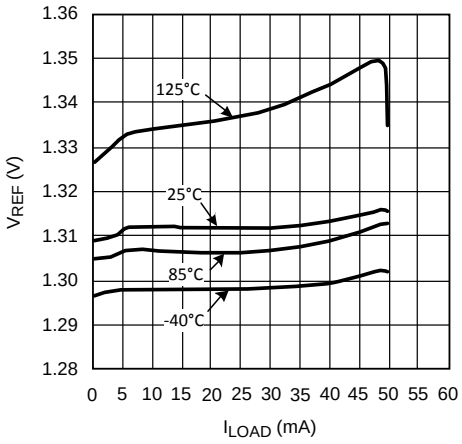


Figure 27.

Voltage Reference vs. Supply Voltage

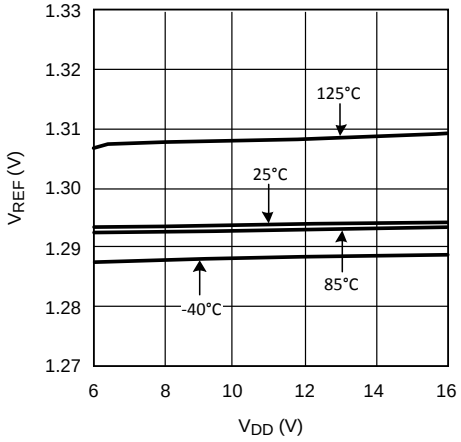


Figure 28.

Voltage Reference PSRR (Line Regulation)

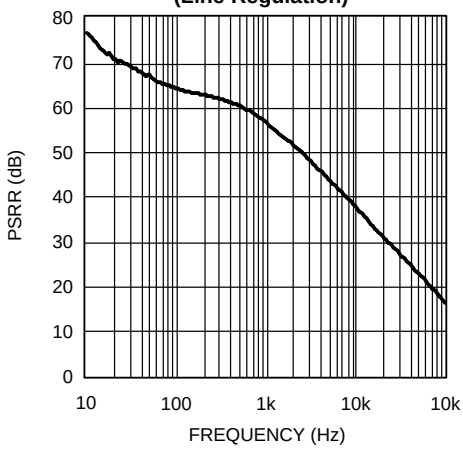


Figure 29.

APPLICATION SECTION

INTRODUCTION

The performance capabilities of TFT-LCD's increase rapidly, with constant improvements such as larger sizes, higher resolution, and greater brightness. Today's LCD's have screen resolutions of over 1 Mega pixel and higher. The LM8207 can be used to improve the performance of an LCD. It is designed for buffering 18 gamma voltage levels and driving the V_{COM} level. These voltage levels can be derived from a highly stable Voltage Reference, which is included in the LM8207. The LM8207 meets the design requirements that combine technical improvement with the demand for cost effective solutions.

The following sections discuss the principle operation of a TFT-LCD and the principle operation of the LM8207 which includes sections on each of the following: the Voltage Reference, the Gamma Buffers, and the V_{COM} Buffer. After this, the next sections present a typical LM8207 configuration and consider the maximum power dissipation. The end of this application section introduces the evaluation board and presents layout recommendations.

PRINCIPLE OPERATION OF A TFT-LCD

This section offers a brief overview of the principle operating of TFT-LCD's. There is a detailed description of how information is presented on the display. An explanation of how data is written to the screen pixels and how the pixels are selected is also included.

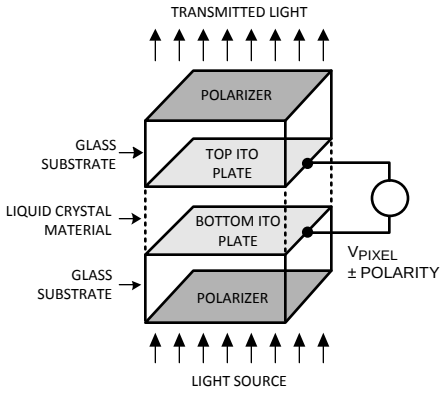


Figure 30. Individual LCD Pixel

Figure 30 shows a simplified illustration of an individual LCD pixel. The top and bottom plates of a pixel consist of Indium-Tin Oxide (ITO), which is a transparent, electrically conductive material. ITO lies on the inner surfaces of two glass substrates that are the front and back glass panels of a TFT display. Sandwiched between two ITO plates is an insulating material (liquid crystal). This alters the polarization of light, depending on how much voltage (V_{PIXEL}) is applied across the two plates. Polarizer's are placed on the outer surfaces of the two glass substrates. In combination with the liquid crystal, the polarizer's create a variable light filter that modulates light transmitted from the back to the front of a display. A pixel's bottom plate lies on the backside of a display where a light source is applied, and the top plate lies on the front, facing the viewer. For most TFT displays, a pixel transmits the greatest amount of light when $V_{PIXEL} \leq \pm 0.5$ V, and it becomes less transparent as the voltage increases with either a positive or negative polarity.

For color displays, each pixel is built with three individual sub pixels. Each sub pixel represents a primary color. These colors are Red, Green and Blue (RGB). Combining these three primary colors every user-defined color can be created.

Figure 31 shows a simplified diagram of a TFT display, showing how individual pixels are connected to the row, column and V_{COM} driver. Each pixel is represented by a capacitor with a NMOS transistor connected to its top plate. Pixels in a TFT panel are arranged in rows and columns. Row lines are connected to the NMOS gates, and column lines to the NMOS sources. The back plate of every pixel is connected to a common voltage called V_{COM}. The voltage applied to the top plates (also called gamma voltage) controls the pixel brightness. The

column drivers supply this gamma voltage via the column lines, and 'write' this voltage to the pixels one row at a time. This is accomplished by having the row drivers selecting an individual row of pixels when the column driver writes the gamma voltage levels. The row drivers sequentially apply a large positive pulse (typically 25V to 35V) to each row line. This turns on the NMOS transistors connected to an individual row, allowing voltage from the column lines to be written to the pixels.

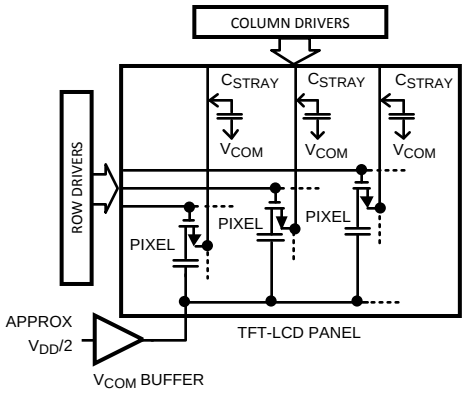


Figure 31. TFT Display

The V_{COM} driver (buffer) supplies a common voltage (V_{COM}) to all the pixels in a TFT panel. V_{COM} is a constant DC voltage that is in the middle of the gamma voltage range. As a result, when a column driver writes to a row of pixels, the applied voltages are either positive or negative with respect to V_{COM}. In fact, the polarity of a pixel is reversed each time a row is selected, preventing a pattern from being 'burned' into the LCD.

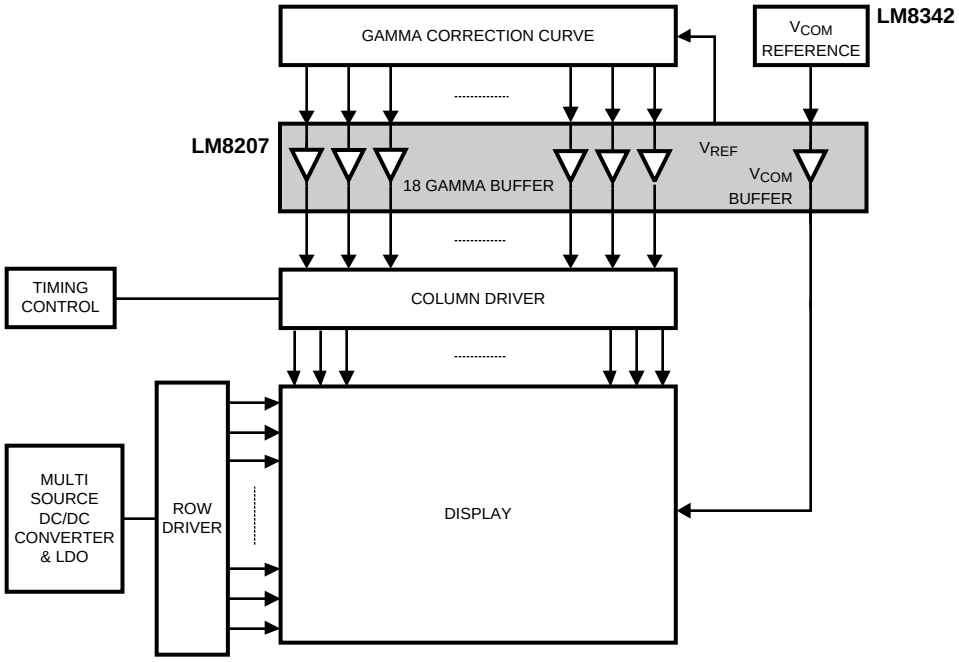


Figure 32. Block Diagram of a Typical TFT-LCD

Figure 32 shows how the display information is refreshed. Using the row and column drivers, one pixel is addressed at the display. The column driver receives the digital color data from the timing controller. The corresponding gamma voltage will be determined, using the gamma correction curve. In fact, the gamma correction curve is just a voltage reference with 18 output tabs, which presets the color intensity settings. This gamma voltage is written to the pixel. The column driver selects one column at the time; the changing in the load may affect the 'tabs' of the gamma correction curve. This problem can be solved using 'gamma buffers' to isolate the gamma correction curve from the column driver.

PRINCIPLE OPERATION of the LM8207

The LM8207 combines three basic functions used in TFT displays:

- **Voltage Reference**
  - To improve picture quality and to reduce brightness variations, a highly stable reference voltage is available. It has a low drift over the operation temperature range. This output voltage (OUT_V_{REF}) is used as the reference voltage to define the gamma correction values.
- **Gamma Buffers**
  - The gamma correction curve can be defined easily using an external chain of precision resistors. To ensure load independent gamma correction levels, 18 gamma buffers, each having a low output resistance, can be used to drive the TFT display column drivers.
- **V_{COM} Buffer**
  - The V_{COM} buffer supplies a common voltage, which is applied to the back plate of all the pixels. Writing color information to all the pixels will cause high current variations at the V_{COM} level so this V_{COM} buffer is designed for driving large output currents.

These three functions are discussed in detail in the following sections.

VOLTAGE REFERENCE

The internal Voltage Reference of the LM8207 can be used to improve picture stability. This accurate reference is highly stable over the operation temperature range. The output voltage (OUT_V_{REF}) of the Voltage Reference can be set using two external resistors. In the next two sections, the possibilities for setting the output voltage of the Voltage Reference and the operating range of the Voltage Reference are discussed.

SETTING THE OUTPUT VOLTAGE OF THE VOLTAGE REFERENCE

The output voltage of the Voltage Reference Amplifier (OUT_V_{REF}) can be set using the internal reference in combination with the internal amplifier and two external resistors. In Figure 33 a typical application circuit for V_{REF} is given.

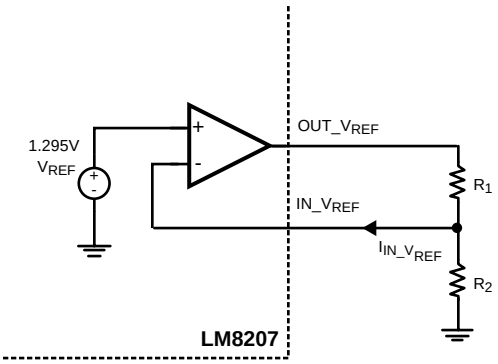


Figure 33. Typical Application Circuit for V_{REF}

To calculate the output voltage of the Voltage Reference Amplifier (OUT_V_{REF}) use the following equation:

$$OUT\_V_{REF} = 1.295 \times \left(\frac{R_1 + R_2}{R_2} \right) + R_1 \times I_{IN\_V_{REF}} \quad (1)$$

As can be seen in the 16V Electrical Characteristics table, $I_{IN\_V_{REF}}$ has a typical value of −10 nA. Using resistor values for R_1 = 9 kΩ and R_2 = 1 kΩ this results in a gain of 10 and OUT_V_{REF} = 12.95 V an error will be introduced of −10 nA*9 kΩ = −90 µV. This error can be neglected. The simplified formula for calculating the OUT_V_{REF} is:

$$OUT\_V_{REF} = 1.295 \times \left(\frac{R_1 + R_2}{R_2} \right) \quad (2)$$

Example:

V_{DD} = 16V

OUT_V_{REF} = 14.4V

Choose R_2 = 5 kΩ. Using Equation 2, this will result in R_1 = 50.6 kΩ

THE OPERATING RANGE OF THE VOLTAGE REFERENCE

The output of the Voltage Reference Amplifier has a minimum of 1.295V (R_1 = 0). This is determined by the value of the internal reference. The maximum output voltage (OUT_V_{REFMAX}) can approach the positive supply rail V_{DD}. The voltage is limited by the output resistance (R_{OUT}) of the output stage of the internal amplifier and depends on the load current. Figure 34 shows the operating output voltage range.

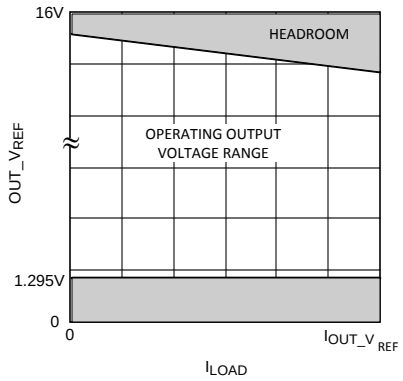


Figure 34. Operating Output Voltage Range

The minimum headroom (OUT_V_{REF} with respect to the positive supply rail V_{DD}) can be measured using the test circuit shown in Figure 35.

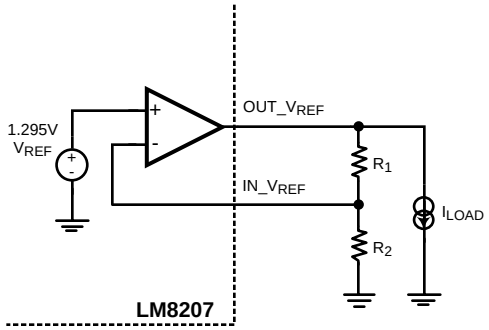


Figure 35. Headroom Test Circuit with Variable Output Current Load

The headroom is measured by varying both the supply voltage and the output current (I_{LOAD}) for a fixed programmed value of OUT_V_{REF}. As shown in Figure 36, the minimum headroom slightly increases for a constant V_{DD} when the load current increases.

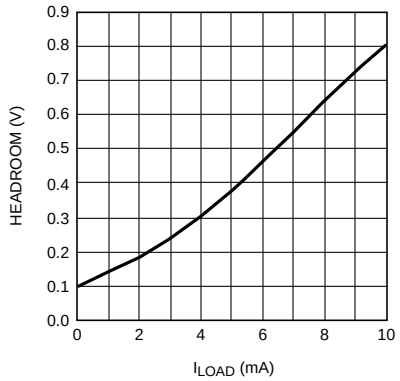


Figure 36. Voltage Reference Headroom vs. Load Current

GAMMA BUFFERS

This section gives an overview for the applications of the gamma buffers and also defines the gamma correction curve. Specifications for the buffers are derived from their operation range. Also included are the formulas for the realization of the gamma correction curve using external resistors. An overview is given for the gamma voltage accuracy, using the LM8207 in combination with external resistors.

As discussed in the section entitled “Principle Operation of a TFT-LCD,” the basic function of the gamma buffers is to make the gamma correction curve independent of the behavior of the column driver. Writing data to each subsequent pixel will cause load variations. The gamma buffers have a low impedance output and can handle these variations without changing the gamma correction curve. A typical gamma correction curve is given in Figure 37.

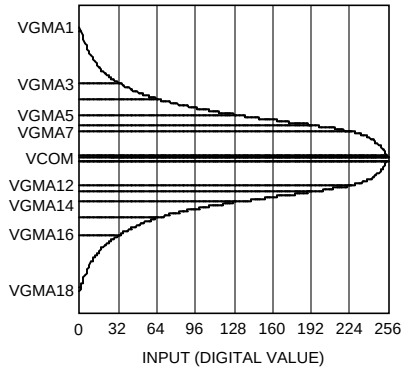


Figure 37. Typical Gamma Correction Curve

Each buffer covers a part of the correction curve and, therefore, has its own specifications. All buffers require that the output should recover quickly from disturbances caused by the switching of the column driver. The gamma voltage level of each buffer (VGMA1…VGMA18) depends on its position for the levels decrease sequentially. To best utilize the LM8207, each buffer is optimized for its position in the gamma correction curve.

- **Gamma Buffers 1-2**
  - Operating voltage range: V_{DD} to V_{SS} +2V. Due to the operating voltage, only negative transitions at the output are possible. Positive transitions will exceed the supply voltage V_{DD}. These buffers are able to source current to bias the resistive load of the column driver having an open collector structure. To meet the operating voltage range, these outputs need a resistive load connected to a lower potential sourcing an output current of at least 1 mA.
- **Gamma Buffers 3-16**
  - Operating voltage range: V_{DD} – 1V to V_{SS} + 1V. Due to the operating range, both positive and negative transitions at the outputs are possible.

- **Gamma Buffers 17-18**
  - Operating voltage range: V_{DD} - 2 to V_{SS}. Due to the operating voltage, only positive transitions at the output are possible. Negative transitions will exceed the negative supply voltage V_{SS}. These buffers are able to sink current from the resistive load of the column driver having an open collector structure. To meet the operating voltage range, these outputs need a resistive load connected to a higher potential sinking an output current of at least 1 mA

Example:

A typical application using the LM8207 is given in Figure 38. The corresponding gamma correction curve (VGMA1...VGMA18) is defined in Table 1. The Voltage Reference supplies the 14.4V to the resistor network. The calculations for the resistor values and for setting the Voltage Reference are shown in the section "Voltage Reference."

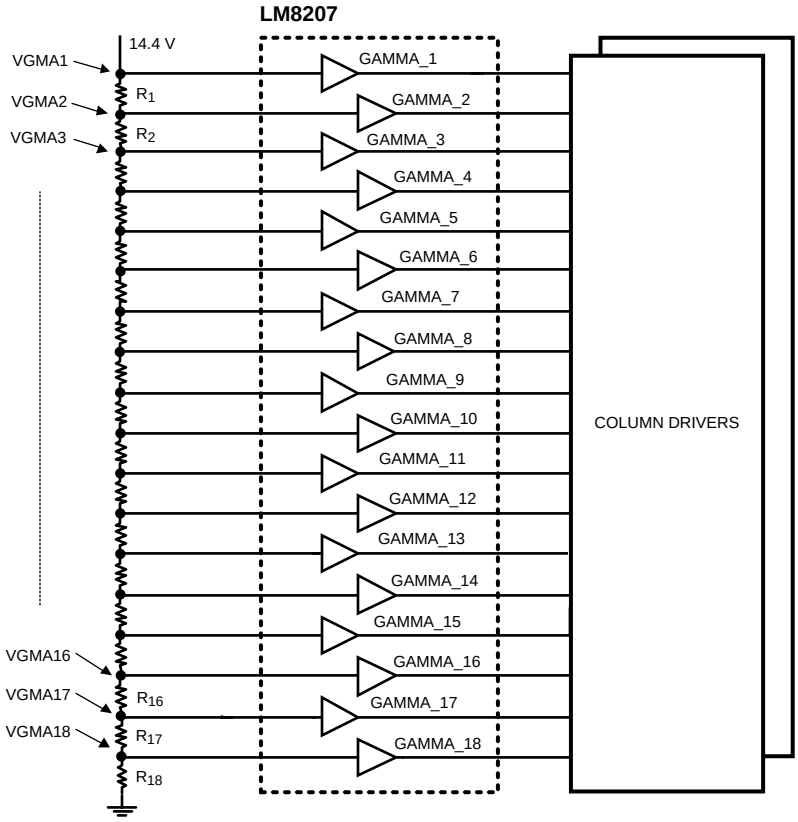


Figure 38. Typical TFT Display Application Diagram Using the LM8207

The values of the resistors in the gamma correction curve are calculated such that a current of 1 mA flows in the resistor chain.

$$R_{18} = \left(\frac{VGMA18}{I} \right) \text{ and } R_X = \left(\frac{VGMAx}{I} \right) - \sum_{y=x+1}^{18} R_y$$

where

- x is the index for the corresponding gamma voltage and has a range of 1 to 18 (3)

Using these formulas the resistor values in Table 1 are calculated. High accuracy resistors values can be realized using 0.1% resistors. A method for fine-tuning the resistor value is to combine two resistors in series.

Table 1. Resistor Values for Defining the Gamma Correction Curve

Gamma Curve Definition		
VGMA Node	VGMA Voltage	Calculated Resistance (Ω)
1	11.59	210
2	11.38	2200
3	9.18	670
4	8.51	670
5	7.84	430
6	7.41	280
7	7.13	980
8	6.15	80
9	6.07	170
10	5.90	80
11	5.82	980
12	4.84	280
13	4.56	430
14	4.13	670
15	3.46	730
16	2.73	2190
17	0.54	210
18	0.33	330

Changing the gamma correction curve, in combination with the load of the column drivers can impact the behavior of the gamma buffers. Gamma buffers 1 and 2 are designed for operating voltages near V_{DD}, and will source the current into the column drivers. Gamma buffers 17 and 18 are designed for operating voltages near V_{SS} and will sink this current. Buffers 3 to 16 are designed to operate in the mid-voltage range and can sink or source current. Under special circumstances, by increasing the voltage gap between gamma buffer 1 and gamma buffer 2, in combination with a low impedance load of the column driver between these outputs, the output of buffer 2 has to sink more current than possible, and can saturate. This will result in a setting error of the inputs of the column driver.

For buffer 17 and 18 an identical situation can occur, by increasing the operating voltage range of buffer 17 with respect to buffer 18.

A simple and cost effective solution is to lower the resistance between buffer 2 and 3 or buffer 16 and 17, using an additional by-pass resistor R_S. This method is presented in Figure 39. This will not affect the desired voltage levels, and buffer 3 which has a larger linear output current spec will sink the current instead of buffer 2. The resistor value R_S can be calculated by the voltage drop divided by the current. The resistor value should be low enough to sink this current, otherwise buffer 2 and/or buffer 17 will still saturate.

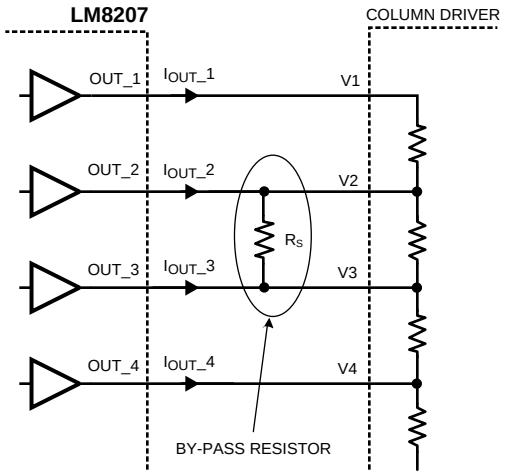


Figure 39. Using additional by-pass resistor to increase current sinking capability

GAMMA VOLTAGE ACCURACY

Adding buffers to the tabs of the gamma correction resistor chain will make the values more independent of the load variations. Unfortunately, there are some other effects that will influence the gamma values. The following effects determine the accuracy of each gamma voltage.

Major effects are:

- Variation of the internal voltage reference. This can be found in the 16V Electrical Characteristics table. This is the maximum variation between parts.
- Variation of the feedback resistors used for setting the output voltage of the voltage reference (OUT_V_{REF}). Using high accuracy resistors will result in a small variation of the output voltage between different boards
- The accuracy of the resistors obtained from the gamma correction voltage curve. The gamma correction curve will be affected by the accuracy of the resistors. This will vary over different boards. Temperature variations will not affect this curve.
- Output offset voltage (V_{OS}) of the buffers. Variations of V_{OS} (output offset voltage) of the buffers, will affect the gamma correction curve. The contribution of V_{OS} is higher for the buffers driving the lower gamma voltages.

Minor effects are:

- Input current (I_{BIAS}) of the gamma buffers. Variations of the input current (I_{BIAS}) of the gamma buffers caused by temperature changes, will affect the gamma correction voltages.

V_{COM} BUFFER

The V_{COM} buffer supplies a common voltage to the back plate of all the pixels in a TFT panel. When column drivers write to the pixels, current pulses will occur onto the V_{COM} line. These pulses are the result of charging the capacitance between V_{COM} and the column lines. This capacitance is a combination of stray capacitance and pixel capacitance. This stray capacitance varies between panel sizes but typically ranges from 16 pF to 33 pF per column. Pixel capacitance is in the order of 0.5 pF and contributes very little to these pulses because only one pixel at a time is connected to a column. Charging this capacitance can result in short positive or negative current pulses of 100 mA or more, depending on the panel size. The V_{COM} buffer is designed to handle these pulses. A V_{COM} buffer is basically a voltage regulator that can sink or source current in large capacitive loads. The V_{COM} buffer should recover very fast from these disturbances. The operating voltage of the V_{COM} buffer is in the middle of the gamma voltage range.

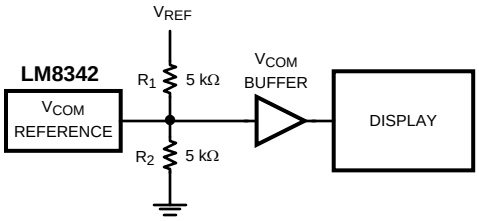


Figure 40. VCOM Buffer

The typical application in Figure 40 shows the V_{COM} buffer supplying a common voltage to the back plate of the display. This level can be adjusted by changing the value of the resistors. Increasing the value of R_1 or decreasing the value of R_2 will decrease the V_{COM} level. Increasing the value of R_2 or decreasing the value of R_1 will increase the V_{COM} level.

Another, more flexible, solution is to use Texas Instruments' programmable V_{COM} calibrator, the LM8342. The V_{COM} level can be adjusted using an I^2C interface. See the *LM8342 Programmable TFT V COM Calibrator with Non-Volatile Memory* datasheet (literature number: snosam0) for more detailed information about this part.

LM8207 CONFIGURATION

A complete configured typical application of the LM8207 is given in Figure 41. All three basic functions of the LM8207 are discussed in the previous sections. Details for setting the Voltage Reference are given in the "Voltage Reference" section. Calculations for defining a gamma correction curve are given in the section entitled "Gamma Buffers." Defining and adjusting the V_{COM} level is discussed in the "V_{COM} Buffer" section. The LM8207 is an 18 channel gamma buffer plus a V_{COM} buffer. In certain applications some of the gamma buffers or the V_{COM} buffer may not be used. In such cases it is recommended that the unused buffer input pins be tied to the input voltage range value.

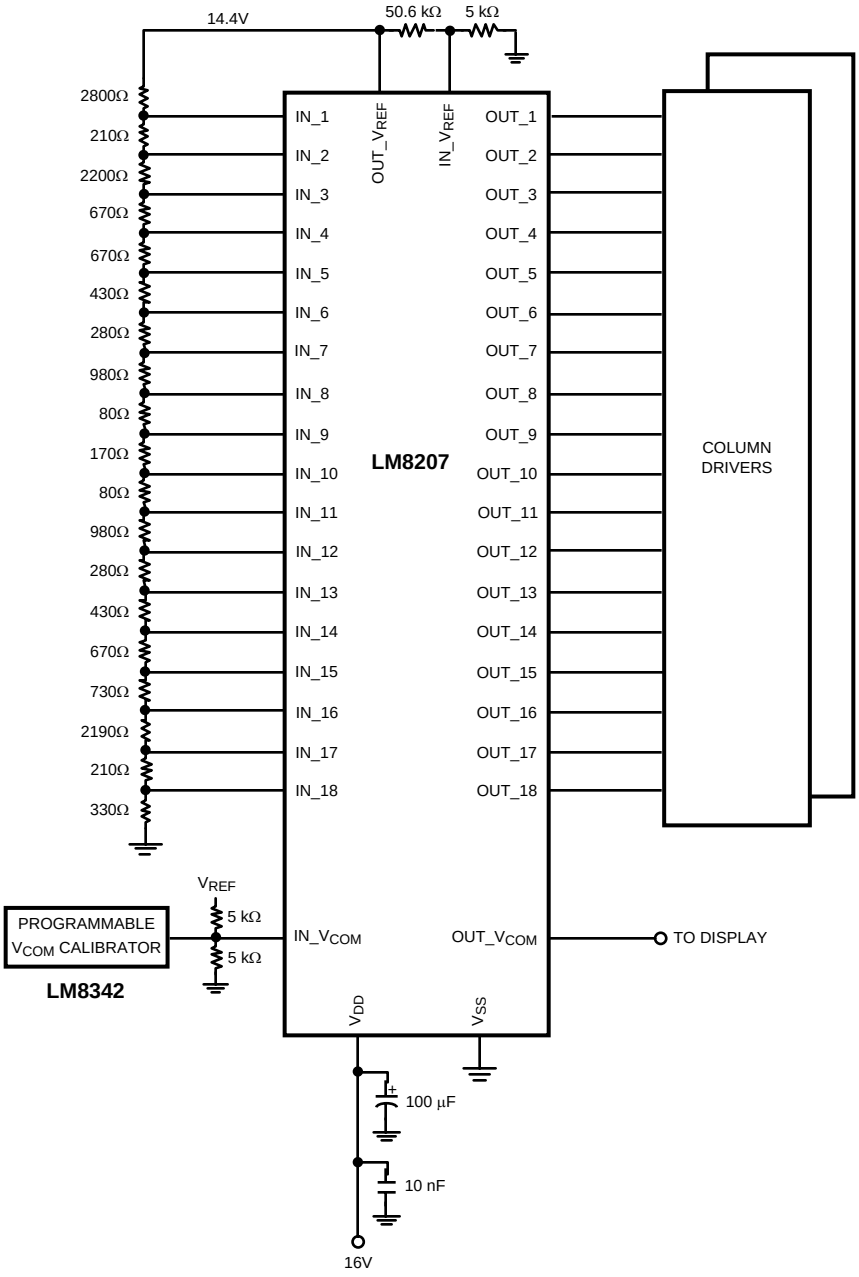


Figure 41. LM8207 Configuration

MAXIMUM POWER DISSIPATION

The maximum power dissipation in the LM8207 TSSOP package depends on the ambient temperature and the increase of the junction temperature of the die. Exceeding the maximum temperature will damage the part. (See the Absolute Maximum Ratings table.) The V_{COM} buffer of the LM8207 is designed for use in pulsed conditions. Driving a continuous current of several hundred mA to a load will damage the part due to the high power consumption of the output stage of the V_{COM} buffer.

The maximum operating temperature can be calculated using this formula:

$$T_J = T_A + \theta_{JA} \times P_{DISSIPATION} \quad (4)$$

where

- T_A = Ambient temperature
- θ_{JA} = Thermal resistance of package (See Operating Ratings table) (84°C/W)
- $P_{DISSIPATION}$ = Total power dissipation of the LM8207

Examples:

The estimated power consumption of the LM8207 in a steady state situation with no load is:

V_{DD}	= 16V
I_{DD}	= 6 mA (all buffers within normal operating range)
OUT_V_{REF}	= 14.4V
I_{LOAD}	= 3 mA
$V_{DD} \times I_{DD}$	= 16 V x 6 mA
(V_{DD} - OUT_V_{REF}) x I_{LOAD} = (16 V – 14.4 V) x 3 mA	= 4.8 mW
Total steady state power dissipation	= 100.8 mW

For an ambient temperature T_A of 40°C and a dissipated power of 100.8 mW, the junction temperature T_J will be 49°C. This will not exceed the maximum operating temperature.

Two issues are not considered in the calculation:

- Continuous power dissipation of the gamma buffers. This is load dependent, and can be calculated using the voltage drop over the output stage times the output current:
  - $P = (V_{DD}\text{-}V_{GMAx}) \times I_{OUT}$ for current sourcing
  - $P = (V_{GMAx}) \times I_{OUT}$ for current sinking
- Pulsed power dissipation of the buffers. The RMS value of this pulsed current depends on the magnitude of the current fluctuations and the duty cycle. This can majorly contribute to the total power dissipation.

When the LM8207 is in steady state biasing, the V buffer is considered at three various load conditions:

I_{OUTRMS} (mA)	V_{COM} Level (V)	Dissipation (mW)	Temp Rise	T_J
10	8	80	7	56
50	8	400	35	83
100 (1)	8	800	67	107

(1) When I_{OUTRMS} = 100 mA, the package (T_J) will exceed the Operating Temperature

EVALUATION BOARD

For testing purposes an evaluation board is available. It is intended to evaluate the following functions:

- The Voltage Reference is fully adjustable within the operating range. For optimal output voltage ranges, user defined resistors can be trimmed by using two resistors in series.
- The Gamma correction curve is user defined using external resistors. Each optimal value can be achieved by using two series resistors for fine-tuning.
- The V_{COM} node input voltage can be achieved using Texas Instruments' LM8342 programmable V_{COM} calibrator, or using an external supply.
- For testing, an additional dummy load can be connected to all outputs of the gamma buffers.

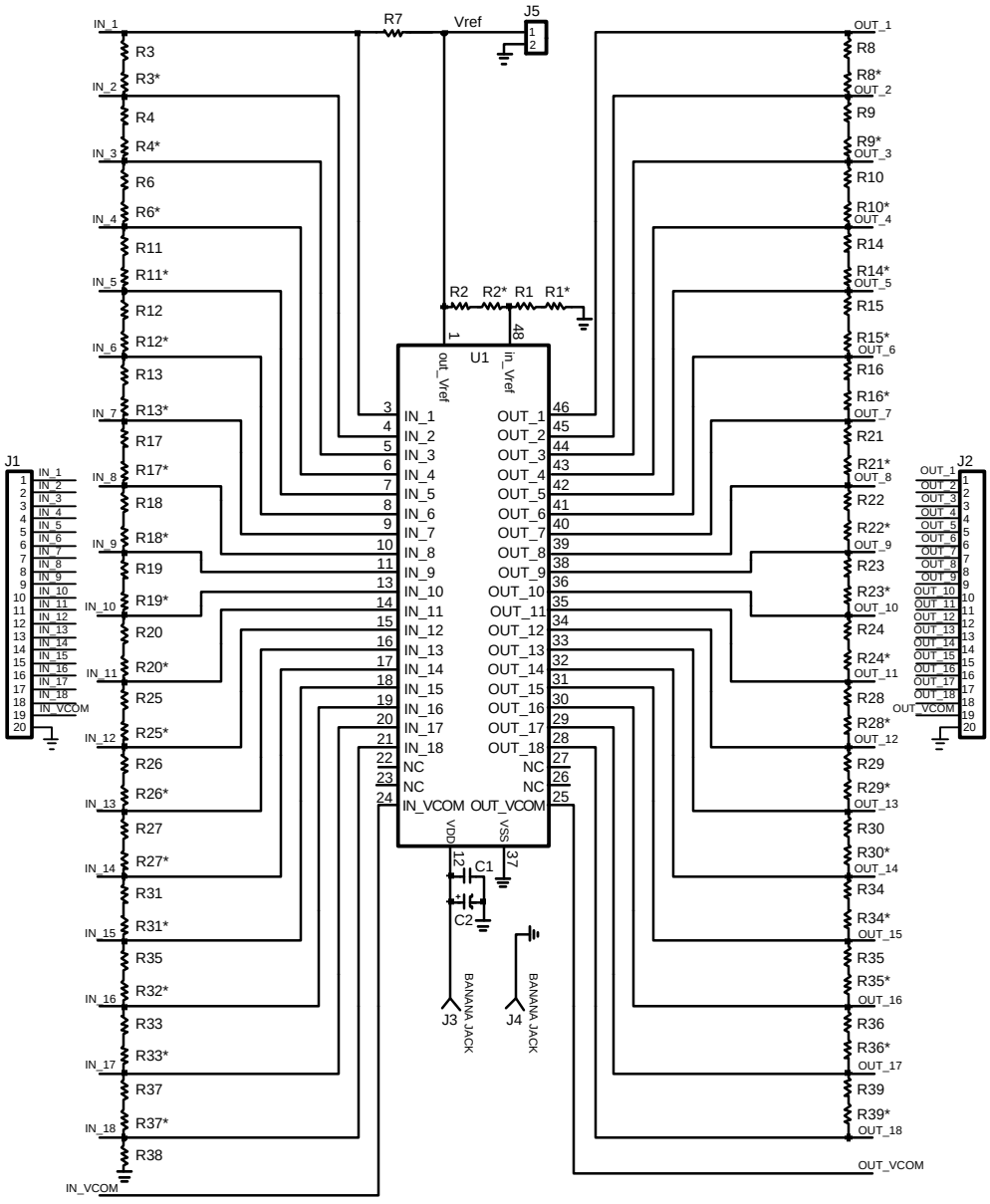


Figure 42. Schematic LM8207 Evaluation Board

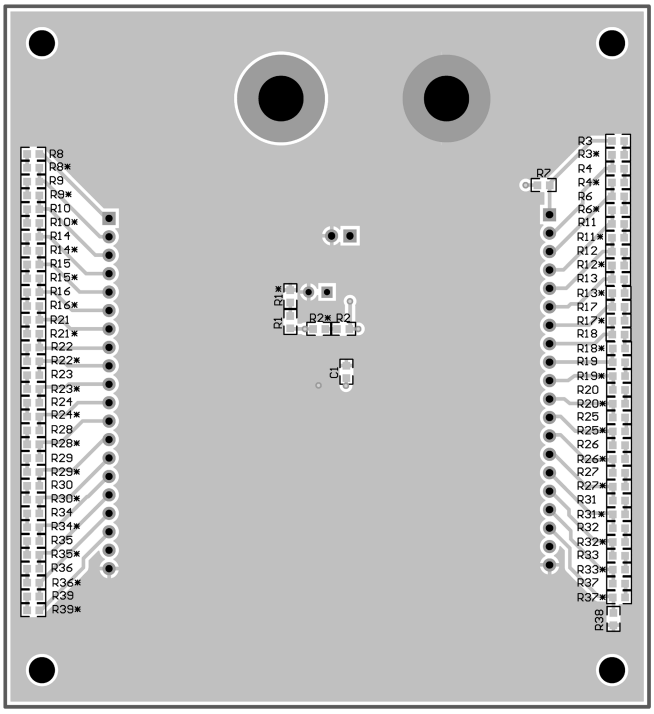


Figure 43. Layout of LM8207 Evaluation Board (Actual Size) — Bottom View

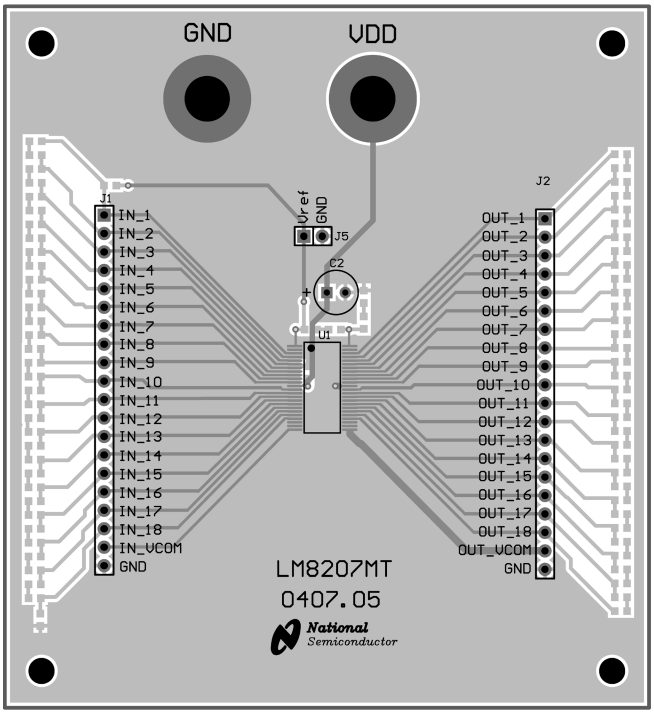


Figure 44. Layout of LM8207 Evaluation Board (Actual Size) — Top View

LAYOUT RECOMMENDATIONS

A proper layout is necessary for optimum performance of the LM8207. A low impedance and clean ground plane is recommended. The traces from the V_{SS} pin to the ground plane should be as short as possible. Decoupling capacitors should be placed very close to the V_{DD} pin. Connections of these decoupling capacitors to the ground plane should be very short. An additional decoupling capacitor for OUT_V_{REF} is recommended.

Due to the heavy current peaks and short transitions at the V_{COM} node, traces from the output of the V_{COM} buffer should be low impedance and as short as possible, to minimize both voltage drops over the trace and unwanted EM disturbances.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM8207MTX/NOPB	NRND	Production	TSSOP (DGG) | 48	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	LM8207MT
LM8207MTX/NOPB.A	NRND	Production	TSSOP (DGG) | 48	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	LM8207MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

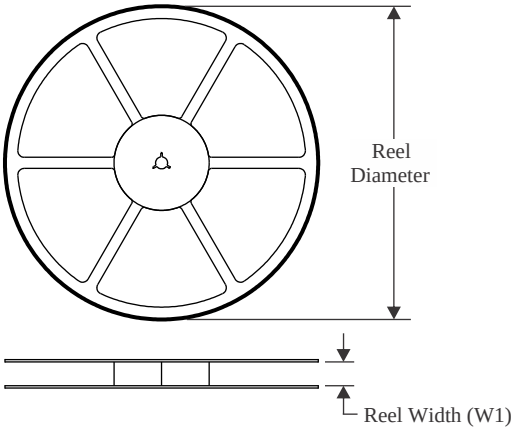
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

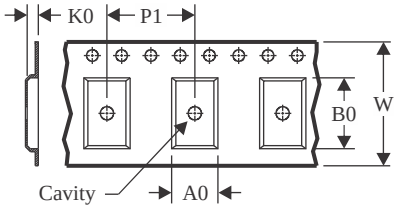
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

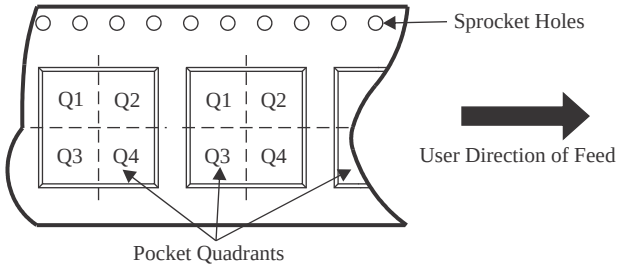


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

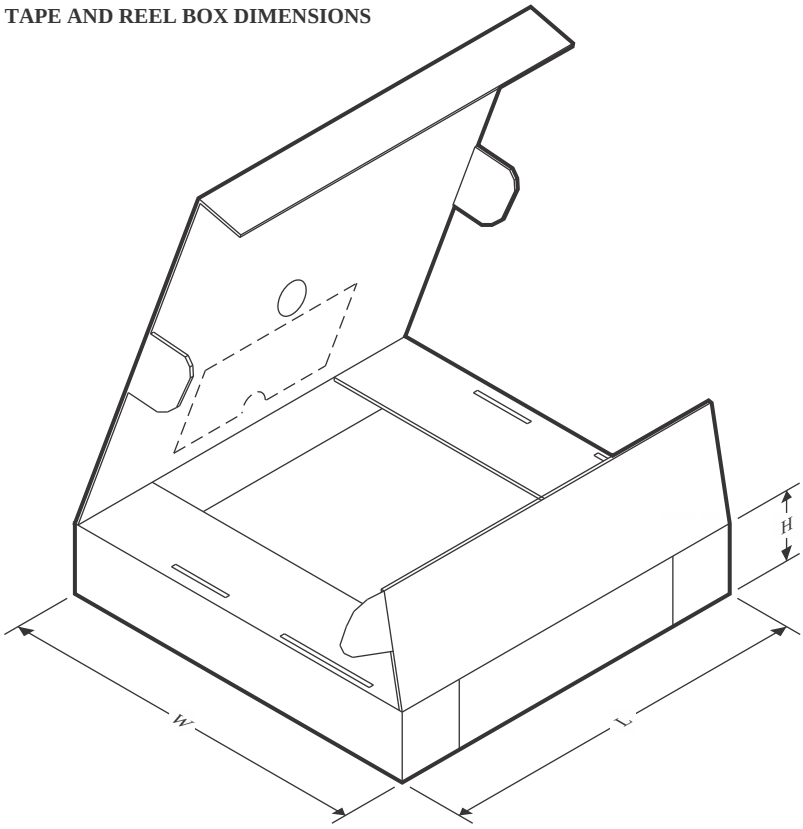
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

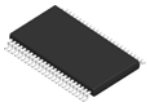
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8207MTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8207MTX/NOPB	TSSOP	DGG	48	1000	356.0	356.0	45.0

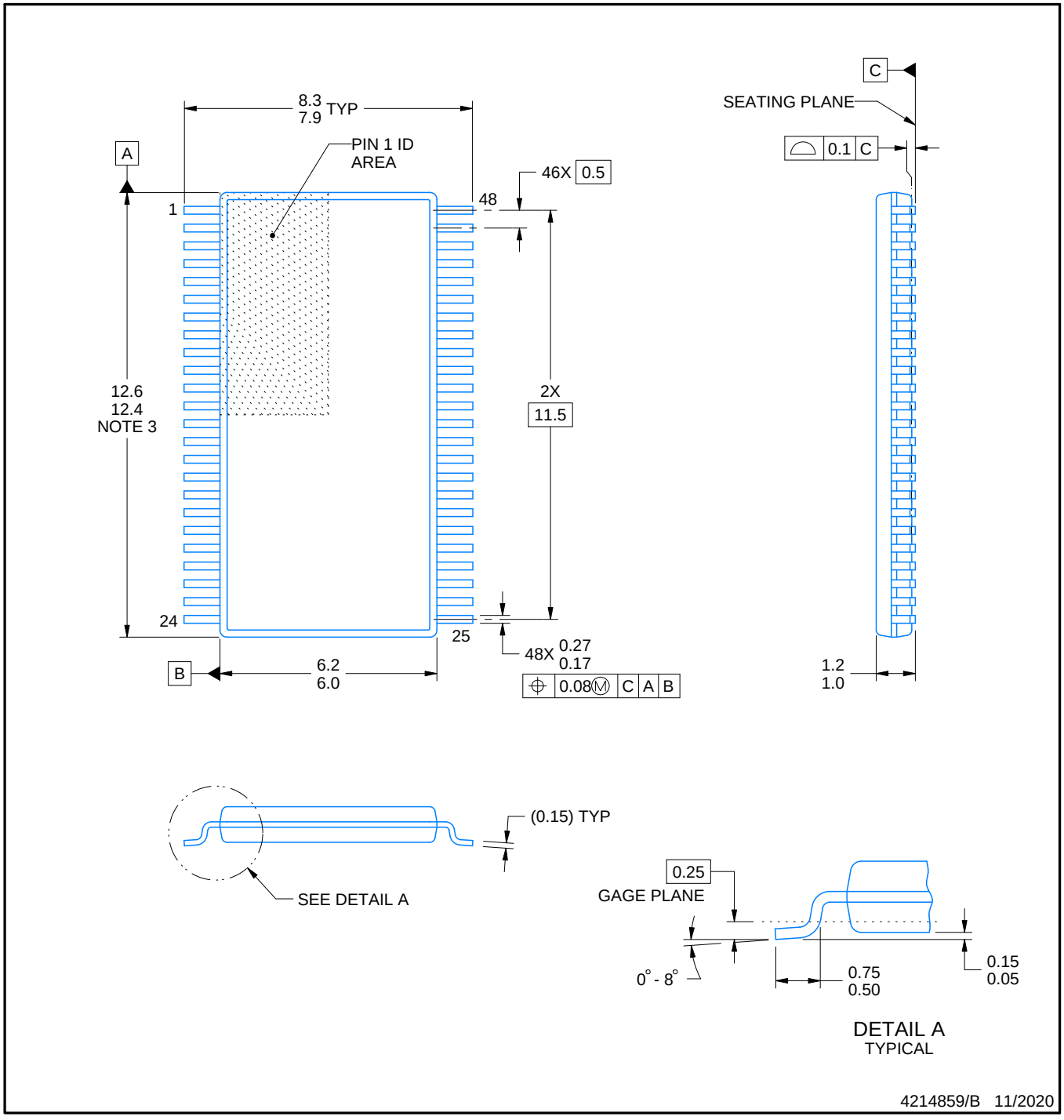


PACKAGE OUTLINE

DGG0048A

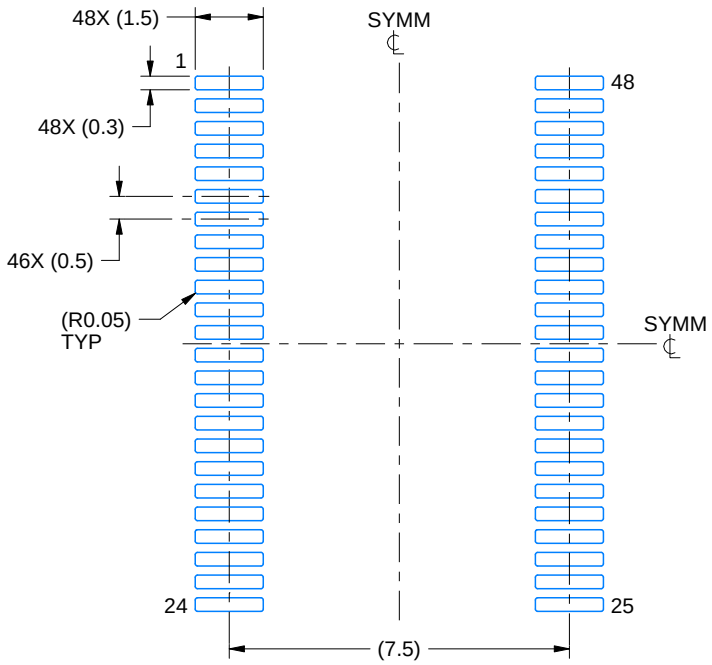
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

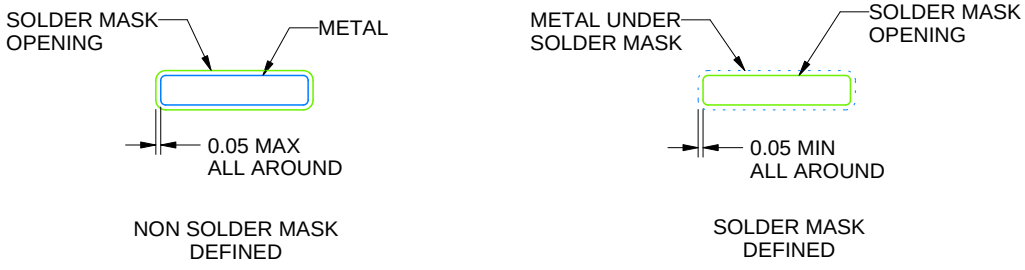


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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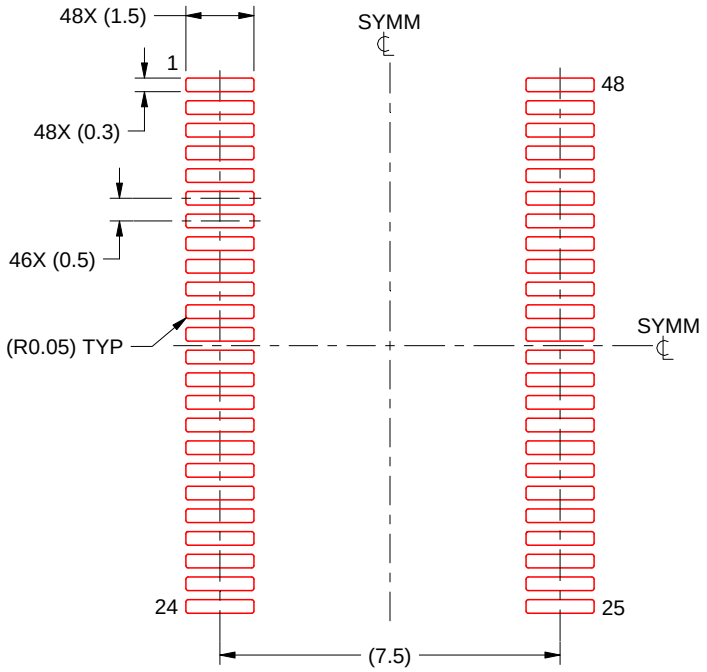
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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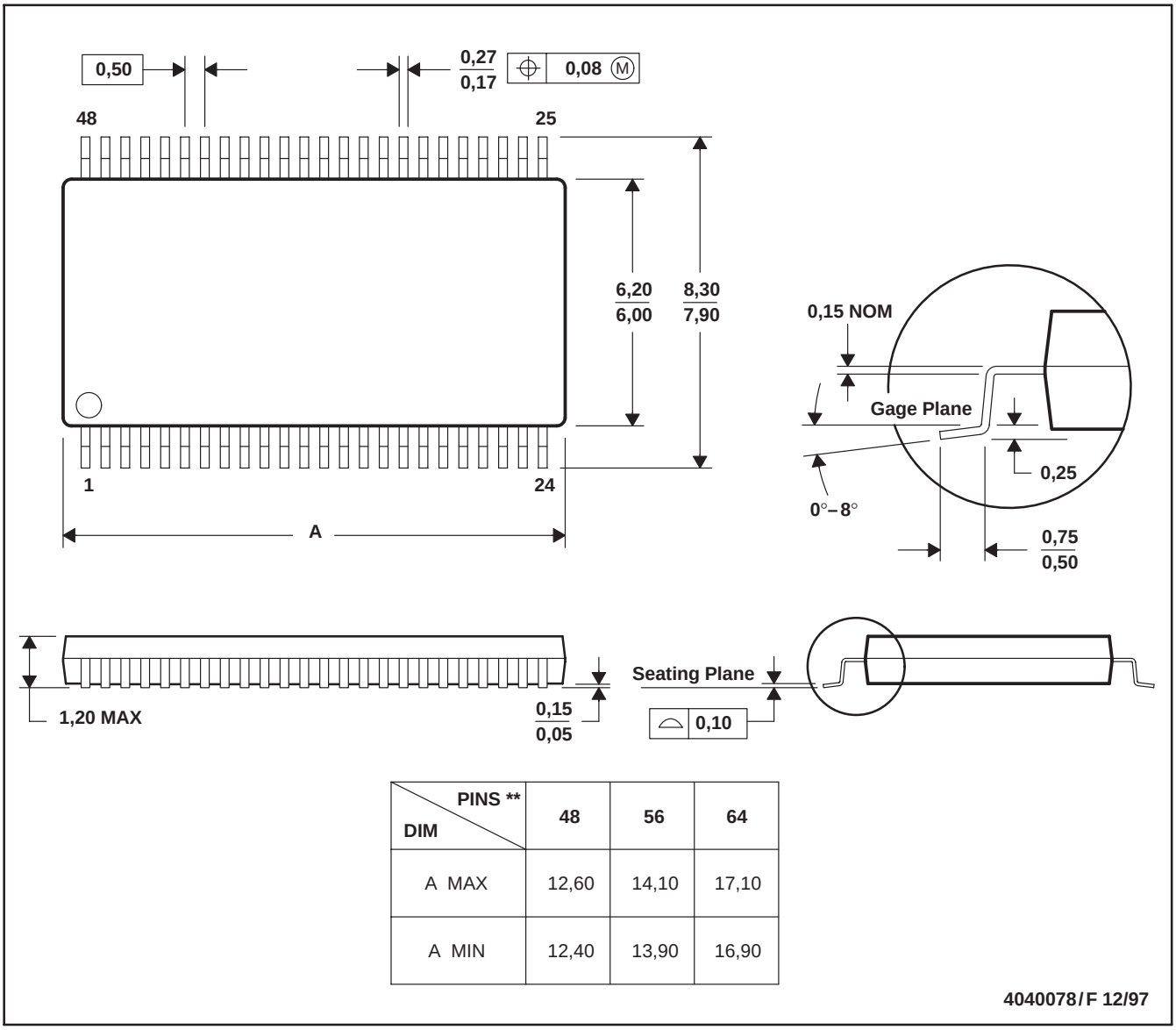
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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