LMC6035/LMC6035-Q1/LMC6036 Low Power 2.7V Single Supply CMOS Operational Amplifiers

Check for Samples: LMC6035, LMC6036

FEATURES

- (Typical Unless Otherwise Noted)
- LMC6035 in DSBGA Package
- Ensured 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20fA
- Rail-to-Rail Output Swing
  - @ 600Ω: 200mV from Either Rail at 2.7V
  - @ 100kΩ: 5mV from Either Rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  - -0.1V to 2.3V at $V_S = 2.7V$
- Low Distortion: 0.01% at 10kHz
- LMC6035 Dual LMC6036 Quad
- See AN-1112 (Literature Number SNVA009) for DSBGA Considerations
- AEC-Q100 Grade 3 Qualified (LMC6035-Q1)

APPLICATIONS

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation
- Automotive Applications

DESCRIPTION

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump DSBGA) using micro SMD package technology. Both allow for single supply operation and are ensured for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its ensured 2.7V operation. This provides a “comfort zone” for adequate operation at voltages significantly below 2.7V. Its ultra low input currents ($I_{IN}$) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

Connection Diagram

Figure 1. 8-Bump DSBGA Package
(Bump Side Down)
See Package Number YZR0008

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### Table 1. DSBGA Connection Table

<table>
<thead>
<tr>
<th>Bump Number</th>
<th>LM6035IBP</th>
<th>LM6035IBPX</th>
<th>LM6035ITL</th>
<th>LM6035ITLX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>OUTPUT A</td>
<td></td>
<td>OUTPUT B</td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>IN A⁻</td>
<td>V⁺</td>
<td>IN A⁺</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>IN A⁺</td>
<td></td>
<td>OUTPUT A</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>V⁻</td>
<td></td>
<td>IN A⁻</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>IN B⁺</td>
<td></td>
<td>IN A⁺</td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>IN B⁻</td>
<td></td>
<td>V⁻</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>OUTPUT B</td>
<td></td>
<td>IN B⁺</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>V⁺</td>
<td></td>
<td>IN B⁻</td>
<td></td>
</tr>
</tbody>
</table>

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>ESD Tolerance (^{(3)})</th>
<th>Human Body Model (LMC6035, LMC6036)</th>
<th>3000V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model (LMC6035-Q1)</td>
<td>2000V</td>
<td></td>
</tr>
<tr>
<td>Machine Model</td>
<td>300V</td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>± Supply Voltage</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (V⁺ – V⁻)</td>
<td>16V</td>
<td></td>
</tr>
<tr>
<td>Output Short Circuit to V⁺</td>
<td>See (^{(4)})</td>
<td></td>
</tr>
<tr>
<td>Output Short Circuit to V⁻</td>
<td>See (^{(5)})</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10 sec.)</td>
<td>260°C</td>
<td></td>
</tr>
<tr>
<td>Current at Output Pin</td>
<td>±18mA</td>
<td></td>
</tr>
<tr>
<td>Current at Input Pin</td>
<td>±5mA</td>
<td></td>
</tr>
<tr>
<td>Current at Power Supply Pin</td>
<td>35mA</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature (^{(6)})</td>
<td>150°C</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

\(^{(2)}\) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

\(^{(3)}\) Human body model, 1.5kΩ in series with 100pF.

\(^{(4)}\) Do not short circuit output to V⁺ when V⁺ is greater than 13V or reliability will be adversely affected.

\(^{(5)}\) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30mA over long term may adversely affect reliability.

\(^{(6)}\) The maximum power dissipation is a function of T\(_{\text{JMAX}}\), \(\theta\_<\text{JA}\), and \(T\_<\text{A}\). The maximum allowable power dissipation at any ambient temperature is \(P_D = (T_{\text{JMAX}} - T_{\text{A}})\theta_{JA}\). All numbers apply for packages soldered directly onto a PC board with no air flow.

### Operating Ratings

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>2.0V to 15.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Range</td>
<td>LMC6035I and LMC6036I</td>
</tr>
<tr>
<td>(\theta_{JA})</td>
<td>(-40°C ≤ T_J ≤ +85°C)</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>8-pin VSSOP</td>
</tr>
<tr>
<td></td>
<td>230°C/W</td>
</tr>
<tr>
<td></td>
<td>8-pin SOIC</td>
</tr>
<tr>
<td></td>
<td>175°C/W</td>
</tr>
<tr>
<td></td>
<td>14-pin SOIC</td>
</tr>
<tr>
<td></td>
<td>127°C/W</td>
</tr>
<tr>
<td></td>
<td>14-pin TSSOP</td>
</tr>
<tr>
<td></td>
<td>137°C/W</td>
</tr>
<tr>
<td></td>
<td>8-Bump (6 mil) DSBGA</td>
</tr>
<tr>
<td></td>
<td>220°C/W</td>
</tr>
<tr>
<td></td>
<td>8-Bump (12 mil) Thin DSBGA</td>
</tr>
<tr>
<td></td>
<td>220°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
## DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.35V$ and $R_L > 1M\Omega$.

**Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>LMC6035I/LMC6036I</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>Min(1)</td>
<td>Typ(2)</td>
</tr>
<tr>
<td>$TCV_{OS}$</td>
<td>Input Offset Voltage Average Drift</td>
<td>2.3</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current</td>
<td>See(3)</td>
<td>0.02</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>See(3)</td>
<td>0.01</td>
</tr>
<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td>&gt; 10</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>63</td>
<td>96</td>
</tr>
<tr>
<td>+PSRR</td>
<td>Positive Power Supply Rejection Ratio</td>
<td>63</td>
<td>93</td>
</tr>
<tr>
<td>−PSRR</td>
<td>Negative Power Supply Rejection Ratio</td>
<td>74</td>
<td>97</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input Common-Mode Voltage Range</td>
<td>$V^+ = 2.7V$ For CMRR $\geq 40dB$</td>
<td>−0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 3V$ For CMRR $\geq 40dB$</td>
<td>−0.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 5V$ For CMRR $\geq 50dB$</td>
<td>−0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 15V$ For CMRR $\geq 50dB$</td>
<td>−0.5</td>
</tr>
<tr>
<td>$A_V$</td>
<td>Large Signal Voltage Gain$^{(4)}$</td>
<td>$R_L = 600\Omega$</td>
<td>Sourcing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2k\Omega$</td>
<td>Sourcing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>500</td>
</tr>
</tbody>
</table>

---

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm or one sigma value.
(3) Ensured by design.
(4) $V^+ = 15V$, $V_{CM} = 7.5V$ and $R_L$ connected to $7.5V$. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $3.5V \leq V_O \leq 7.5V$. 

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DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for \( T_J = 25\, ^\circ\, C \), \( V^+ = 2.7V \), \( V^- = 0V \), \( V_{CM} = 1.0V \), \( V_O = 1.35V \) and \( R_L > 1\, \Omega \).

**Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>LMC6035I/LMC6036I</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_O )</td>
<td>Output Swing</td>
<td>( V^+=2.7V ) ( R_L=600, \Omega ) to 1.35V</td>
<td>Min((1))</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+=2.7V ) ( R_L=2k, \Omega ) to 1.35V</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ =15V ) ( R_L=600, \Omega ) to 7.5V</td>
<td>13.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ =15V ) ( R_L=2k, \Omega ) to 7.5V</td>
<td>14.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>LMC6035I/LMC6036I</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_O )</td>
<td>Output Current</td>
<td>( V_O=0V )</td>
<td>Sourcing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O=2.7V )</td>
<td>Sinking</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>LMC6035 for Both Amplifiers</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>( V_O=1.35V )</td>
<td>0.65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LMC6036 for All Four Amplifiers</td>
<td>1.3</td>
</tr>
</tbody>
</table>

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25\, ^\circ\, C \), \( V^+ = 2.7V \), \( V^- = 0V \), \( V_{CM} = 1.0V \), \( V_O = 1.35V \) and \( R_L > 1\, \Omega \).

**Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Typ((1))</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>See((2))</td>
<td>1.5</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth Product</td>
<td>( V^+ =15V )</td>
<td>1.4</td>
</tr>
<tr>
<td>( \Theta_m )</td>
<td>Phase Margin</td>
<td></td>
<td>48</td>
</tr>
<tr>
<td>( G_m )</td>
<td>Gain Margin</td>
<td></td>
<td>17</td>
</tr>
<tr>
<td>( A_{\text{amp}} )</td>
<td>Amp-to-Amp Isolation</td>
<td>See((3))</td>
<td>130</td>
</tr>
<tr>
<td>( e_n )</td>
<td>Input-Reflected Voltage Noise</td>
<td>( f = 1kHz ) ( V_{CM} = 1V )</td>
<td>27</td>
</tr>
<tr>
<td>( I_n )</td>
<td>Input Referred Current Noise</td>
<td>( f = 1kHz )</td>
<td>0.2</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>( f = 1kHz ); ( A_V = -10 ) ( R_L = 2k, \Omega ); ( V_O = 8 , V_{PP} ); ( V^+ = 10V )</td>
<td>0.01</td>
</tr>
</tbody>
</table>

\((1)\) Typical Values represent the most likely parametric norm or one sigma value.

\((2)\) \( V^+ = 15V \). Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

\((3)\) Input referred, \( V^+ = 15V \) and \( R_L = 100k\, \Omega \) connected to 7.5V. Each amp excited in turn with 1kHz to produce \( V_O = 12 \, V_{PP} \).
Typical Performance Characteristics

Unless otherwise specified, $V_S = 2.7V$, single supply, $T_A = 25°C$

**Supply Current vs. Supply Voltage (Per Amplifier)**

**Input Current vs. Temperature**

**Sourcing Current vs. Output Voltage**

**Sinking Current vs. Output Voltage**

**Figure 2.**

**Figure 3.**

**Figure 4.**

**Figure 5.**

**Figure 6.**

**Figure 7.**
Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 2.7V$, single supply, $T_A = 25°C$

**Output Voltage Swing vs. Supply Voltage**

![Figure 8.](image)

**Input Noise vs. Supply Voltage**

![Figure 9.](image)

**Input Noise vs. Frequency**

![Figure 10.](image)

**Amp to Amp Isolation vs. Frequency**

![Figure 11.](image)

**Amp to Amp Isolation vs. Frequency**

![Figure 12.](image)

**+PSRR vs. Frequency**

![Figure 13.](image)
Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 2.7V$, single supply, $T_A = 25^\circ C$

- **PSRR vs. Frequency**
- **CMRR vs. Frequency**
- **CMRR vs. Input Voltage**
- **Input Voltage vs. Output Voltage**
Typical Performance Characteristics (continued)

Unless otherwise specified, \( V_S = 2.7V \), single supply, \( T_A = 25^\circ C \)

**Frequency Response vs. Temperature**

![Frequency Response vs. Temperature](image)

**Gain and Phase vs. Capacitive Load**

![Gain and Phase vs. Capacitive Load](image)

**Slew Rate vs. Supply Voltage**

![Slew Rate vs. Supply Voltage](image)

**Non-Inverting Large Signal Response**

![Non-Inverting Large Signal Response](image)
Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 2.7\text{V}$, single supply, $T_A = 25\text{°C}$

**Non-Inverting Large Signal Response**

![Non-Inverting Large Signal Response](image1)

**Non-Inverting Small Signal Response**

![Non-Inverting Small Signal Response](image2)

**Non-Inverting Large Signal Response**

![Non-Inverting Large Signal Response](image3)

**Inverting Large Signal Response**

![Inverting Large Signal Response](image4)
Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 2.7V$, single supply, $T_A = 25°C$

**Inverting Large Signal Response**

- Figure 32.
- $T_A = +25°C$
- $R_I = 2 \, k\Omega$
- Figure 33.
- $T_A = -40°C$
- $R_I = 2 \, k\Omega$

**Inverting Small Signal Response**

- Figure 34.
- $T_A = +85°C$
- $R_I = 2 \, k\Omega$
- Figure 35.
- $T_A = +25°C$
- $R_I = 2 \, k\Omega$

**Inverting Small Signal Response**

- Figure 36.
- $T_A = -40°C$
- $R_I = 2 \, k\Omega$

**Stability vs. Capacitive Load**

- Figure 37.
- $A_V = +1$
- $V_S = \pm 1.35V$
- $R_I = 6000 \, \Omega$
- 25% Overshoot
Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 2.7V$, single supply, $T_A = 25°C$

Stability vs. Capacitive Load

Figure 38.

Stability vs. Capacitive Load

Figure 39.

Stability vs. Capacitive Load

Figure 40.

Stability vs. Capacitive Load

Figure 41.

Stability vs. Capacitive Load

Figure 42.
Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability—a hallmark for TI's CMOS amplifiers. The circuit of Figure 43 illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about $600 \Omega$ of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance ($X_c$) is negligible compared to inductive reactance ($X_I$) of T1.

![Figure 43. Differential Driver](image)

The circuit in Figure 43 consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of $-2$, while the U1B amplifies the input with a non-inverting gain of $+2$. Since the two outputs are $180^\circ$ out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6—like many op amps—sources and sinks output current through two complementary transistors in series. This “totem pole” arrangement translates to a channel resistance ($R_{\text{ds}}$) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails—except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of Figure 44 and Figure 45 represent measurements taken directly at the output (relative to GND) of U1A, in Figure 43. Figure 44 illustrates the output swing capability of the LMC6035, while Figure 45 provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)
Notice the superior drive capability of LMC6035 when compared with the benchmark measurement—even though the benchmark op amp uses twice the supply current.
Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain \( (A_{\text{VOL}}) \) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of Figure 43. The graph of Figure 46 shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of \( R_L \) (600Ω) and T1’s winding resistances—a performance deficiency of the transformer.)

![Figure 46. THD+Noise Performance of LMC6035 and “Benchmark” per Circuit of Figure 43](image)

Figure 46 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the \( A_{\text{VOL}} \) of the benchmark part to drop significantly which causes increased distortion.

**APPLICATION CIRCUITS**

**Low-Pass Active Filter**

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents \( (I_{\text{IN}}) \) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 47 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency \( (f_c) \). The bold component values of Figure 47 provide a cutoff frequency of 3kHz. An example of the scaling procedure follows Figure 47.

![Figure 47. 2-Pole, 3kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response](image)
Low-Pass Frequency Scaling Procedure
The actual component values represented in bold of Figure 47 were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing \( f_c \) at 3kHz, provides the following FSF computation:
   \[
   \text{FSF} = \frac{2\pi \times 3\text{kHz}}{ \text{desired cutoff freq.} } = 18.84 \times 10^3
   \]

2. Then divide all of the normalized capacitor values by the FSF as follows:
   \[
   C_1' = \frac{0.707}{18.84 \times 10^3} = 37.93 \times 10^{-6} \quad C_2' = \frac{1.414}{18.84 \times 10^3} = 75.05 \times 10^{-6}
   \]
   (C1' and C2': prior to impedance scaling)

3. Lastly, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2.
   \[
   Z = \frac{C_2'}{C_2 \text{ (chosen)}} = \frac{75.05 \times 10^{-6}}{6.8\text{nF}} = 8.4k
   \]
   (Standard capacitor value chosen for C1 is 4.7nF
   (Standard value chosen for R1 and R2 is 8.45kΩ)

High-Pass Active Filter
The previous low-pass filter circuit of Figure 47 converts to a high-pass active filter per Figure 48.

High-Pass Frequency Scaling Procedure
Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300Hz) as follows:

\[
Z = \frac{C}{C \text{ (chosen)}} = \frac{1}{6.8\text{nF}} = \frac{1}{2\pi \times 300\text{Hz}} = 78.05k
\]

\[
R_1 = Z \times R_1 \text{ (normalized)} = 78.05k \times \frac{1}{0.707} = 110.4kΩ
\]
(Standard value chosen for R1 is 110kΩ)

\[
R_2 = Z \times R_2 \text{ (normalized)} = 78.05k \times \frac{1}{1.414} = 55.2kΩ
\]
(Standard value chosen for R2 is 54.9kΩ)

Dual Amplifier Bandpass Filter
The dual amplifier bandpass (DABP) filter features the ability to independently adjust \( f_c \) and Q. In most other bandpass topologies, the \( f_c \) and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of Figure 49, provides a 1kHz center frequency and a Q of 100.
DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency \( f_c \). Figure 49 represents component values that were obtained from the following computation for a center frequency of 1kHz. \( R_2 = R_3 = 1/(2\pi f_c C) \) \( \text{Given: } f_c = 1\text{kHz and } C = 6.8\text{nF} \quad R_2 = R_3 = 1/(2\pi \times 3\text{kHz} \times 6.8\text{nF}) = 23.4\Omega \)
   
   - (Chosen standard value is 23.7\( \Omega \))

2. Then compute \( R_1 \) for a desired \( Q \left( f_c / BW \right) \) as follows: \( R_1 = Q \times R_2 \). Choosing a \( Q \) of 100, \( R_1 = 100 \times 23.7\Omega = 2.37\text{M}\Omega \).

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with < 1000pA of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically < 0.04pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 50. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of \( 10^{12}\Omega \), which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of \( 10^{11}\Omega \) would cause only 0.05pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 51(a) through Figure 51(c) for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 51(d).
Figure 50. Example, using the LMC6036 of Guard Ring in PC Board Layout

(a) Inverting Amplifier (Guard Ring Connections)

(b) Non-Inverting Amplifier (Guard Ring Connections)

(c) Follower (Guard Ring Connections)

(d) Howland Current Pump

Figure 51. Guard Ring Connections

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 52, the addition of a small resistor (50Ω–100Ω) in series with the op amp's output, and a capacitor (5pF–10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

**DSBGA Considerations**

Contrary to what might be guessed, the DSBGA package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in DSBGA has thermal resistance of 220°C/W compared to 230°C/W in VSSOP. Even when driving a 600Ω load and operating from ±7.5V supplies, the maximum temperature rise will be under 4.5°C. For application information specific to DSBGA, see Application note AN-1112 (Literature Number SNVA009).

![Figure 52. Rx, Cx Improve Capacitive Load Tolerance](image)

Capacitive load driving capability is enhanced by using a pull up resistor to V+ (Figure 53). Typically a pull up resistor conducting 500μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

![Figure 53. Compensating for Large Capacitive Loads with a Pull Up Resistor](image)

**Connection Diagrams**

![Figure 54. 8-Pin SOIC or VSSOP Package](image)

See Package Number D0008A or DGK0008A

![Figure 55. 14-Pin SOIC or TSSOP Package](image)

See Package Number D0014A or PW0014A
## PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LMC6035, LMC6035-Q1:**

- **Catalog:** LMC6035
- **Automotive:** LMC6035-Q1

**NOTE:** Qualified Version Definitions:

- **Catalog:** TI's standard catalog product

- **Automotive:** Q100 devices qualified for high-reliability automotive applications targeting zero defects
**TAPE AND REEL INFORMATION**

---

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

---

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

---

*All dimensions are nominal*

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### TAPE AND REEL BOX DIMENSIONS

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TUBE

- **T** - Tube length
- **L** - Tube length
- **W** - Tube width
- **T** - Tube height
- **B** - Alignment groove width

*All dimensions are nominal*

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

D: Max = 1.921 mm, Min = 1.86 mm
E: Max = 1.768 mm, Min = 1.708 mm
NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.  
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.  
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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