# LMC66x CMOS Dual Operational Amplifiers

## 1 Features

- Rail-to-rail output swing
- Specified for 2kΩ and 600Ω loads
- High voltage gain: 126dB
- Low input offset voltage: 3mV
- Low offset voltage drift: 1.3µV/°C
- Ultra low input bias current: 2fA
- Low voltage noise: 22nV/√Hz
- Input common-mode range includes V−
- Operating range from 4.75V to 15.5V supply
- $I_{SS}$ = 400µA/amplifier; Independent of V+
- Slew rate: 1.1V/µs

## 2 Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

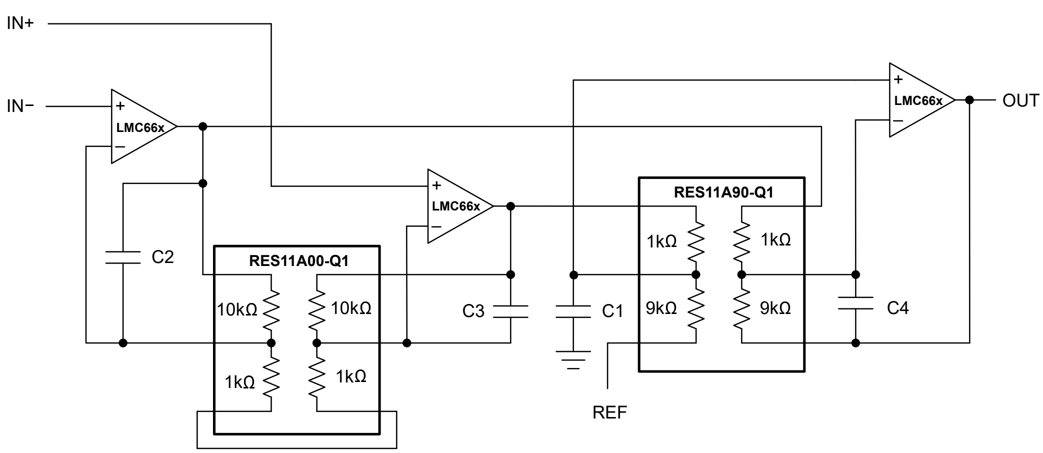
## 3 Description

The dual LMC662 and quad LMC660 (LMC66x) are CMOS operational amplifiers designed for operation from a single supply, and built with TI's advanced CMOS process. The device operates from 5V to 15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input offset voltage ($V_{OS}$), offset drift, and broadband noise as well as voltage gain into realistic loads (2kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

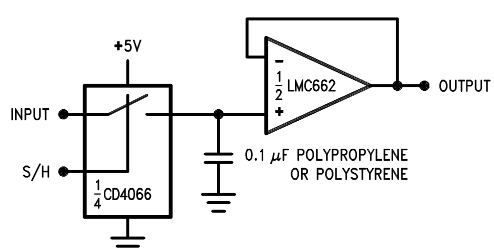
**Device Information**

| PART NUMBER | CHANNEL COUNT | PACKAGE(1) |
|---|---|---|
| LMC662 | Dual | D (SOIC, 8) |
| | | P (PDIP, 8) |
| LMC660 | Quad | D (SOIC, 8) |
| | | P (PDIP, 8) |

(1) For all available packages, see Section 9.




**Typical Application: Instrumentation Amplifier With RES11A**




**Typical Application: Low Leakage Sample and Hold**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

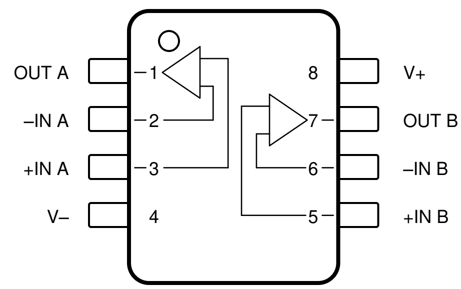



**Figure 4-1. LMC662 D Package, 8-Pin SOIC, and P package, 8-Pin PDIP (Top View)**

**Table 4-1. LMC662 Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN A | 3 | Input | Noninverting input, channel A |
| –IN A | 2 | Input | Inverting input, channel A |
| +IN B | 5 | Input | Noninverting input, channel B |
| –IN B | 6 | Input | Inverting input, channel B |
| OUT A | 1 | Output | Output, channel A |
| OUT B | 7 | Output | Output, channel B |
| V+ | 8 | Power | Positive (highest) power supply |
| V– | 4 | Power | Negative (lowest) power supply |

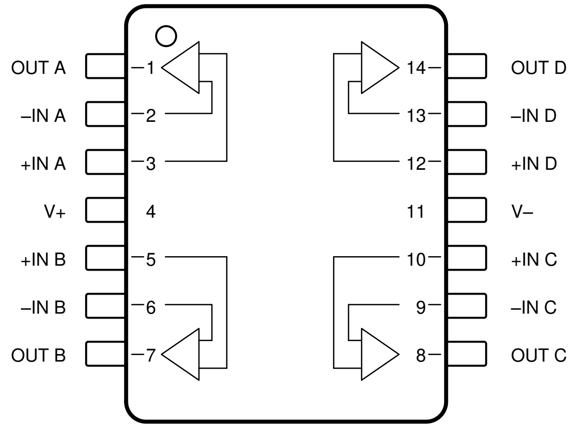



**Figure 4-2. LMC660 D Package, 14-Pin SOIC, and P package, 14-Pin PDIP (Top View)**

**Table 4-2. LMC660 Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| +IN A | 3 | Input | Noninverting input, channel A |
| +IN B | 5 | Input | Noninverting input, channel B |
| +IN C | 10 | Input | Noninverting input, channel C |
| +IN D | 12 | Input | Noninverting input, channel D |
| –IN A | 2 | Input | Inverting input, channel A |
| –IN B | 6 | Input | Inverting input, channel B |
| –IN C | 9 | Input | Inverting input, channel C |
| –IN D | 13 | Input | Inverting input, channel D |
| OUT A | 1 | Output | Output, channel A |
| OUT B | 7 | Output | Output, channel B |
| OUT C | 8 | Output | Output, channel C |
| OUT D | 14 | Output | Output, channel D |
| V+ | 4 | — | Positive (highest) power supply |
| V– | 11 | — | Negative (lowest) power supply |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Differential input voltage | | | ±Supply Voltage | V |
| Supply voltage, $V_S$ = (V+) – (V–) | Single supply | 0 | 16 | V |
| | Dual supply | | ±8 | |
| Signal input pins | Voltage | (V–) – 0.3 | (V+) + 0.3 | V |
| | Current | | ±5 | mA |
| Output pin current | | | ±18 | mA |
| Output short circuit | To V+ | See[(3)] | | |
| | To V– | See[(4)] | | |
| Power supply pin | Current | | 35 | mA |
| Power dissipation | | See[(5)] | | |
| Temperature | Operating, $T_A$ | –40 | 150 | °C |
| | Junction, $T_J$ | | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |
| | Lead (soldering, 10 sec.) | | 260 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Do not connect output to V+ when V+ is greater than 13V or reliability will be adversely affected.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(max)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±1000 | V |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | Single supply | 4.75 | | 15.5 | V |
| | Dual supply | ±2.375 | | ±7.75 | |
| Temperature range, $T_J$ | LMC66xAI | –40 | | 85 | °C |
| | LMC66xC | 0 | | 70 | |
| Power dissipation | | | | See[(1)] | |

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance $\theta_{JA}$ with $P_D = (T_J – T_A) / \theta_{JA}$.

## 5.4 Thermal Information LMC662

| THERMAL METRIC[(1)] | | LMC662 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | P (PDIP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 165 | 101 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Thermal Information LMC660

| THERMAL METRIC[(1)] | | LMC660 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | P(PDIP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 115 | 85 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.6 Electrical Characteristics

at $T_A$ = +25°C, $V_S$ = 5V (V– = 0V), $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 1MΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LMC66xAI | | | ±1 | ±3 | mV |
| | | | $T_A$ = –40°C to +85°C | | | ±3.3 | |
| | | LMC66xC | | | ±1 | ±6 | |
| | | | $T_A$ = 0°C to 70°C | | | ±6.3 | |
| $dV_{OS}/dT$ | Input offset voltage drift | LMC66xAI | $T_A$ = –40°C to +85°C | | ±1.3 | | µV/°C |
| | | LMC66xC | $T_A$ = 0°C to 70°C | | ±1.3 | | |
| PSRR | Power-supply rejection ratio | Positive, 5V ≤ $V_S$ ≤ 15V | LMC66xAI | 75 | 85 | | dB |
| | | | LMC66xAI $T_A$ = –40°C to +85°C | 72 | | | |
| | | | LMC66xC | 66 | 85 | | |
| | | | LMC66xC $T_A$ = 0°C to 70°C | 63 | | | |
| | | Negative, –10V ≤ $V_S$ ≤ 0V | LMC66xAI | 84 | 94 | | |
| | | | LMC66xAI $T_A$ = –40°C to +85°C | 81 | | | |
| | | | LMC66xC | 74 | 94 | | |
| | | | LMC66xC $T_A$ = 0°C to 70°C | 71 | | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±2 | | fA |
| | | LMC66xAI | $T_A$ = –40°C to +85°C | | | ±4 | pA |
| | | LMC66xC | $T_A$ = 0°C to 70°C | | | ±2 | |
| $I_{OS}$ | Input offset current | | | | ±1 | | fA |
| | | LMC66xAI | $T_A$ = –40°C to +85°C | | | ±2 | pA |
| | | LMC66xC | $T_A$ = 0°C to 70°C | | | ±1 | |
| **NOISE** | | | | | | | |
| $e_n$ | Input voltage noise density | f = 1kHz | | | 22 | | nV/√Hz |
| $i_n$ | Input current noise density | f = 1kHz | | | 4 | | fA/√Hz |
| THD | Total harmonic distortion | f = 10kHz, G = – 10V/V, $R_L$ = 2kΩ, $V_{OUT}$ = $8V_{pp}$, $V_S$ = 15V | | | 0.2 | | % |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | To positive rail, 5V ≤ $V_S$ ≤ 15V, CMRR > 60dB | | | (V+) – 1.9 | (V+) – 2.3 | V |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | | | (V+) – 2.5 | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | | | (V+) – 2.6 | |
| | | To negative rail, 5V ≤ $V_S$ ≤ 15V, CMRR > 60dB | | (V–) – 0.1 | (V–) – 0.4 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | (V–) | | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | (V–) | | | |
| CMRR | Common-mode rejection ratio | $V_S$ = 15V, 0V < $V_{CM}$ < 12V | LMC66xAI | 75 | 85 | | dB |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 72 | | | |
| | | | LMC66xC | 66 | 85 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 63 | | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Input resistance | | | | >1 | | TΩ |

## 5.6 Electrical Characteristics (continued)

at $T_A$ = +25°C, $V_S$ = 5V (V– = 0V), $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 1MΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | Sourcing, $V_S$ = 15V, $V_{CM}$ = 7.5V, 7.5V < $V_O$ < 11.5V, $R_L$ = 2kΩ | LMC66xAI | 440 | 2000 | | V/mV |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 400 | | | |
| | | | LMC66xC | 300 | 2000 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 200 | | | |
| | | Sinking, $V_S$ = 15V, $V_{CM}$ = 7.5V, 2.5V < $V_O$ < 7.5V, $R_L$ = 2kΩ | LMC66xAI | 180 | 500 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 120 | | | |
| | | | LMC66xC | 90 | 500 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 80 | | | |
| | | Sourcing, $V_S$ = 15V, $V_{CM}$ = 7.5V, 7.5V < $V_O$ < 11.5V, $R_L$ = 600Ω | LMC66xAI | 220 | 1000 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 200 | | | |
| | | | LMC66xC | 150 | 1000 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 100 | | | |
| | | Sinking, $V_S$ = 15V, $V_{CM}$ = 7.5V, 2.5V < $V_O$ < 7.5V, $R_L$ = 600Ω | LMC66xAI | 100 | 250 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 60 | | | |
| | | | LMC66xC | 50 | 250 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 40 | | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain bandwidth product | | | | 1.4 | | MHz |
| SR | Slew rate[2] | $V_S$ = 15V, 10V step | | | 1.1 | | V/µs |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 0.6 | | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 0.7 | | | |
| $θ_m$ | Phase margin | | | | 50 | | ° |
| | Crosstalk | Dual and quad channel, $V_S$ = 15V, $R_L$ = 100kΩ to 7.5V, f = 1kHz, $V_{OUT}$ = $12V_{pp}$ | | | 130 | | dB |

## 5.6 Electrical Characteristics (continued)

at $T_A$ = +25°C, $V_S$ = 5V (V– = 0V), $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 1MΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | Positive rail, $V_S$ = 5V, $R_L$ = 2kΩ | LMC66xAI | 4.82 | 4.87 | | V |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 4.79 | | | |
| | | | LMC66xC | 4.78 | 4.87 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 4.76 | | | |
| | | Negative rail, $V_S$ = 5V, $R_L$ = 2kΩ | LMC66xAI | | 0.10 | 0.15 | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | | | 0.17 | |
| | | | LMC66xC | | 0.10 | 0.19 | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | | | 0.21 | |
| | | Positive rail, $V_S$ = 5V, $R_L$ = 600Ω | LMC66xAI | 4.41 | 4.61 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 4.31 | | | |
| | | | LMC66xC | 4.27 | 4.61 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 4.21 | | | |
| | | Negative rail, $V_S$ = 5V, $R_L$ = 600Ω | LMC66xAI | | 0.30 | 0.50 | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | | | 0.56 | |
| | | | LMC66xC | | 0.30 | 0.63 | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | | | 0.69 | |
| | | Positive rail, $V_S$ = 15V, $R_L$ = 2kΩ | LMC66xAI | 14.50 | 14.63 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 14.44 | | | |
| | | | LMC66xC | 14.37 | 14.63 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 14.32 | | | |
| | | Negative rail, $V_S$ = 15V, $R_L$ = 2kΩ | LMC66xAI | | 0.26 | 0.35 | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | | | 0.40 | |
| | | | LMC66xC | | 0.26 | 0.44 | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | | | 0.48 | |
| | | Positive rail, $V_S$ = 15V, $R_L$ = 600Ω | LMC66xAI | 13.35 | 13.90 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 13.15 | | | |
| | | | LMC66xC | 12.92 | 13.90 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 12.76 | | | |
| | | Negative rail, $V_S$ = 15V, $R_L$ = 600Ω | LMC66xAI | | 0.79 | 1.16 | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | | | 1.32 | |
| | | | LMC66xC | | 0.79 | 1.45 | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | | | 1.58 | |

## 5.6 Electrical Characteristics (continued)

at $T_A$ = +25°C, $V_S$ = 5V (V– = 0V), $V_{CM}$ = 1.5V, $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 1MΩ connected to $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{SC}$ | Short-circuit current | Sourcing, $V_S$ = 5V, $V_{OUT}$ = 0V | LMC66xAI | 16 | 22 | | mA |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 14 | | | |
| | | | LMC66xC | 13 | 22 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 11 | | | |
| | | Sinking, $V_S$ = 5V, $V_{OUT}$ = 13V | LMC66xAI | 16 | 21 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 14 | | | |
| | | | LMC66xC | 13 | 21 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 11 | | | |
| | | Sourcing, $V_S$ = 15V, $V_{OUT}$ = 0V | LMC66xAI | 28 | 40 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 25 | | | |
| | | | LMC66xC | 23 | 40 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 21 | | | |
| | | Sinking, $V_S$ = 15V, $V_{OUT}$ = 13V(1) | LMC66xAI | 28 | 39 | | |
| | | | LMC66xAI, $T_A$ = –40°C to +85°C | 24 | | | |
| | | | LMC66xC | 23 | 39 | | |
| | | | LMC66xC, $T_A$ = 0°C to 70°C | 20 | | | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | LMC662 $V_{OUT}$ = 7.5V, $V_S$ = 15V | LMC662AI | | 375 | 650 | µA |
| | | | LMC662AI, $T_A$ = –40°C to +85°C | | | 750 | |
| | | | LMC662C | | 375 | 800 | |
| | | | LMC662C, $T_A$ = 0°C to 70°C | | | 900 | |
| | | LMC660 $V_{OUT}$ = 7.5V, $V_S$ = 15V | LMC660AI | | 375 | 550 | |
| | | | LMC660AI, $T_A$ = –40°C to +85°C | | | 650 | |
| | | | LMC660C | | 375 | 675 | |
| | | | LMC660C, $T_A$ = 0°C to 70°C | | | 725 | |

(1) Do not connect output to V+ when V+ is greater than 13V or reliability can be adversely affected.
(2) Specification limit established from device population bench system measurements across multiple lots. Number specified is the slower of the positive and negative slew rates.

## 5.7 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±7.5V, $V_{OUT}$ = mid-supply, $R_L$≥ 1MΩ (unless otherwise specified)

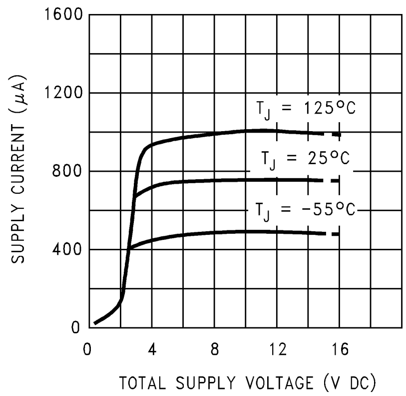



Figure 5-1. Supply Current vs Supply Voltage

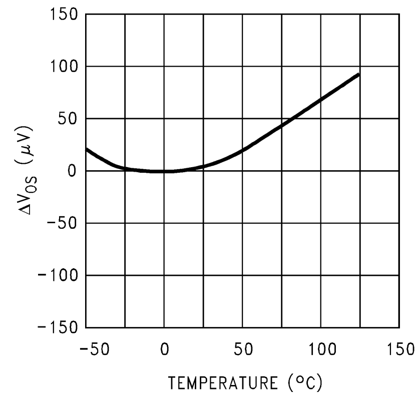



Figure 5-2. Offset Voltage

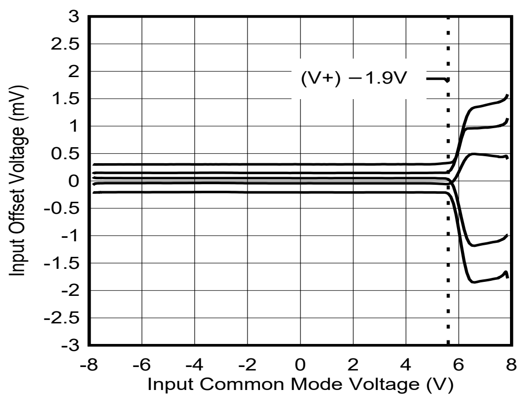



Figure 5-3. Offset Voltage vs Common-Mode Voltage

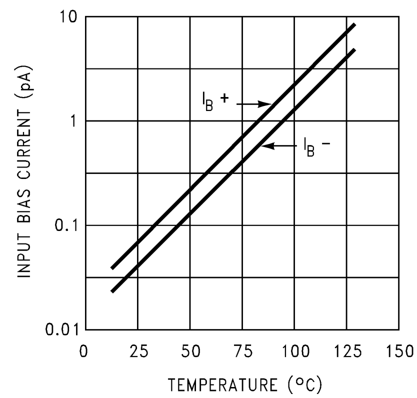



Figure 5-4. Input Bias Current

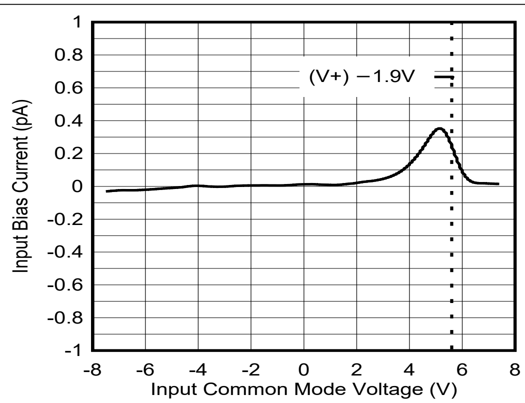
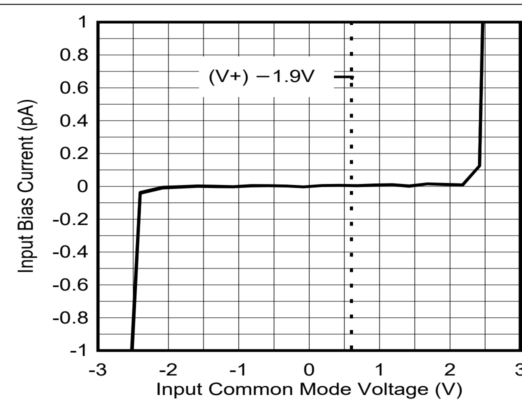



Figure 5-5. Input Bias Current vs Input Common-Mode Voltage




$V_S$ = ±2.5V

Figure 5-6. Input Bias Current vs Input Common-Mode Voltage

## 5.7 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±7.5V, $V_{OUT}$ = mid-supply, $R_L$≥ 1MΩ (unless otherwise specified)

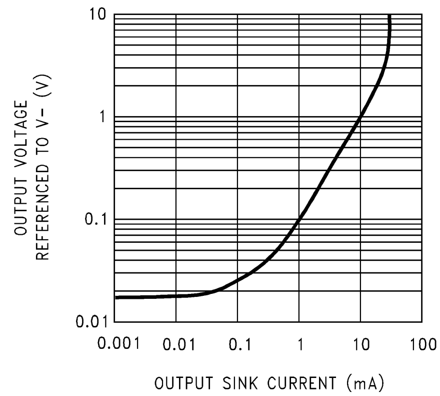



**Figure 5-7. Output Characteristics Current Sinking**

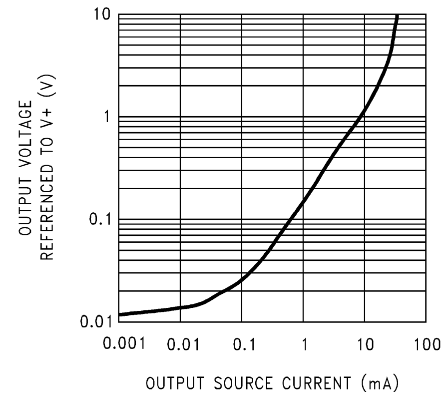



**Figure 5-8. Output Characteristics Current Sourcing**

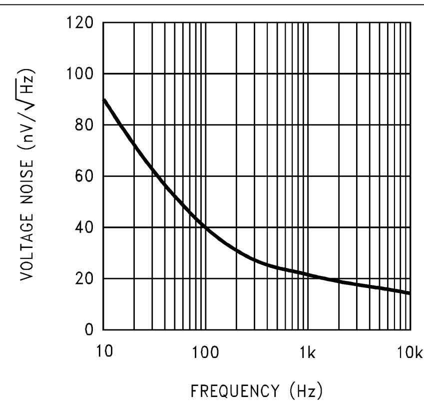



**Figure 5-9. Input Voltage Noise vs Frequency**

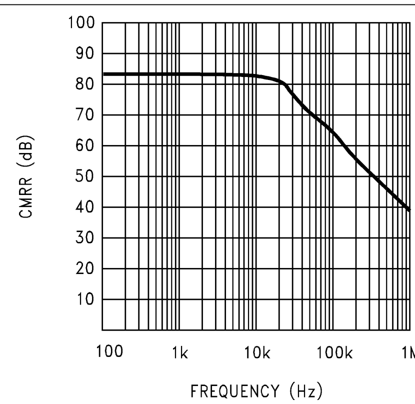



**Figure 5-10. CMRR vs Frequency**

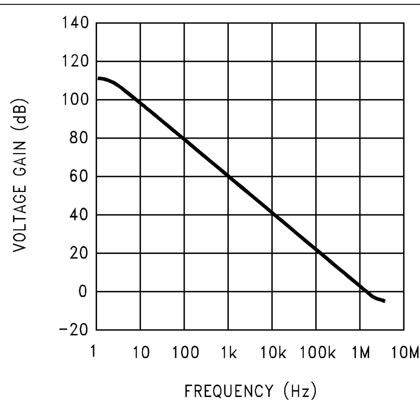



**Figure 5-11. Open-Loop Frequency Response**

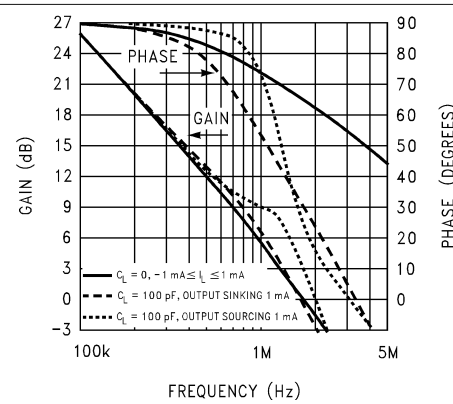



**Figure 5-12. Frequency Response vs Capacitive Load**

## 5.7 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±7.5V, $V_{OUT}$ = mid-supply, $R_L$≥ 1MΩ (unless otherwise specified)

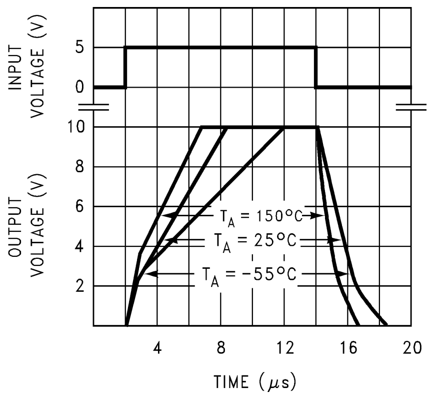
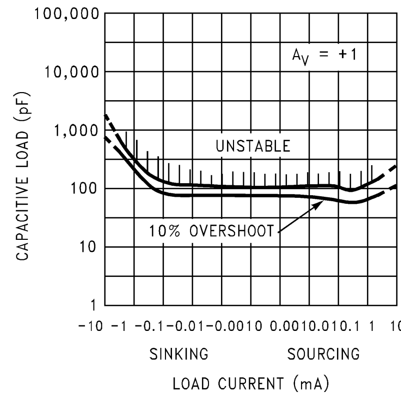
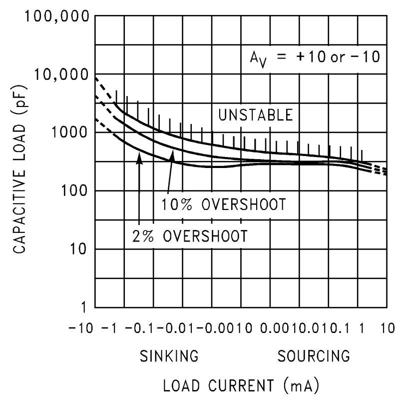



**Figure 5-13. Noninverting Large-Signal Pulse Response**




Avoid resistive loads < 500Ω because of possible instability

**Figure 5-14. Stability vs Capacitive Load**




Avoid resistive loads < 500Ω because of possible instability

**Figure 5-15. Stability vs Capacitive Load**

# 6 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 6.1 Application Information

### 6.1.1 Amplifier Topology

The topology chosen for the LMC66x, shown in Figure 6-1, is unconventional compared to general-purpose op amps. The LMC66x incorporates novel op amp design that enables a wide input common-mode range and rail to rail output swing even when driving a large load. The input common-mode range includes ground, making the LMC66x an excellent choice for single supply applications. While the LMC66x supports both a wide supply and common-mode voltage range, large input common-mode voltage can cause an increase in input bias current.

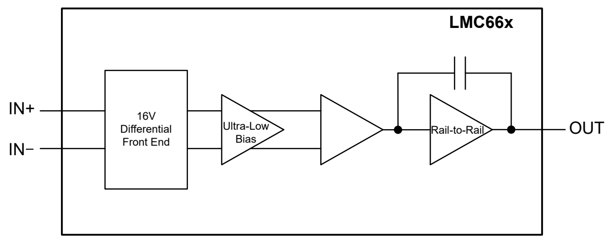



**Figure 6-1. LMC66x Circuit Topology (Each Amplifier)**

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain is reduced as indicated in the *Electrical Characteristics*.

### 6.1.2 Compensating Input Capacitance

The high input resistance of the LMC66x op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit can be especially sensitive to the layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and ac ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, and so on) and the feedback resistors create a pole in the feedback path. In Figure 6-2, the frequency of this pole is:

$$f_P = \frac{1}{2\pi R_P C_S} \quad (1)$$

where

- $C_S$ is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, and so on.
- $R_P$ is the parallel combination of $R_F$ and $R_{IN}$.

This formula, as well as the next formula, apply to inverting and noninverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole can be quite high, because $C_S$ is generally less than 10pF. If the frequency of the feedback pole is much greater than the *ideal* closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of $C_S$), the pole can have a negligible effect on stability, as only a small amount of phase shift is added.

However, if the feedback pole is less than approximately 6 to 10 times the *ideal* −3dB frequency, connect a feedback capacitor, $C_F$, between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier low-frequency noise gain. To maintain stability, a feedback capacitor is probably be needed if:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \le \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \quad (2)$$

where

$\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier low-frequency noise gain and GBW is the amplifier gain bandwidth product. An amplifier low-frequency noise gain is represented by the following formula, regardless of whether the amplifier is being used in an inverting or noninverting mode:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \quad (3)$$

A feedback capacitor is more likely to be needed when the noise gain is low, the feedback resistor is large, or both.

If the previous condition is met (indicating that a feedback capacitor is probably needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \le 2\sqrt{GBW \times R_F \times C_S} \quad (4)$$

the following value of feedback capacitor is recommended:

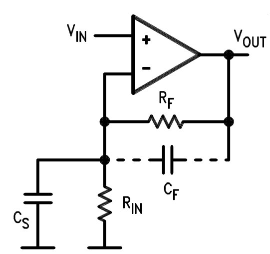
$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)} \quad (5)$$

If $\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$ , then set the feedback capacitor to:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \quad (6)$$

These capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \quad (7)$$




$C_S$ consists of the amplifier input capacitance plus any stray capacitance from the circuit board and socket. $C_F$ compensates for the pole caused by $C_S$ and the feedback resistor.

**Figure 6-2. General Operational Amplifier Circuit**

Using the smaller capacitors provides much higher bandwidth with little degradation of transient response. In any of the previous cases, the use a somewhat larger feedback capacitor can be necessary to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board (PCB) stray capacitance can be larger or smaller than the breadboard stray capacitance, so the actual preferred value for $C_F$ can be different from the one estimated using the breadboard. In most cases, check the value of $C_F$ on the actual circuit, starting with the computed value.

### 6.1.3 Capacitive Load Tolerance

Like many other op amps, the LMC66x can oscillate when the applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See also Section 5.7.

The load capacitance interacts with the op amp output resistance to create an additional pole. If this pole frequency is sufficiently low, the pole can degrade the op amp phase margin so that the amplifier is no longer stable at low gains. Figure 6-3 shows that the addition of a small resistor (50Ω to 100Ω) in series with the op amp output, and a capacitor (5pF to 10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. In all cases, the output can ring heavily when the load capacitance is near the threshold for oscillation.

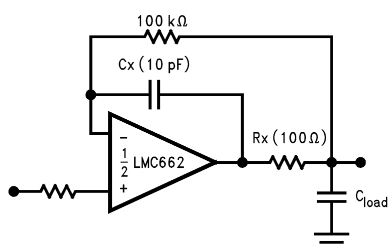



**Figure 6-3. Rx, Cx Improve Capacitive Load Tolerance**

Capacitive load driving capability is enhanced by using a pullup resistor to V+, as in Figure 6-4. Typically, a pullup resistor conducting 500µA or more significantly improves capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see the *Electrical Characteristics*).

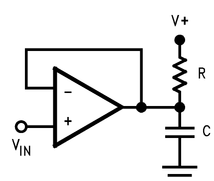



**Figure 6-4. Compensating for Large Capacitive Loads With a Pullup Resistor**

### 6.1.4 Bias Current Testing

The test method of Figure 6-5 is appropriate for bench-testing bias current with reasonable accuracy. To understand the circuit operation, first close switch S2 momentarily. When S2 is opened, then:

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C_2 \tag{8}$$

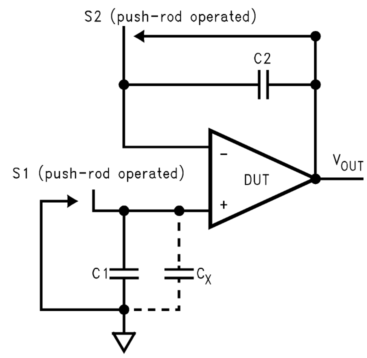



**Figure 6-5. Simple Input Bias Current Test Circuit**

A recommended capacitor for $C_2$ is a 5pF or 10pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of $I_b$−, take into account the leakage of the capacitor and socket. Leave switch S2 shorted most of the time, or else the dielectric absorption of the capacitor $C_2$ can cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted):

$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C_1 + C_x) \tag{9}$$

where $C_x$ is the stray capacitance at the noninverting input.

## 6.2 Typical Applications

Additional single-supply applications ideas can be found in the LM358 data sheet. The LMC66x is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features can improve the performance of many existing single-supply applications. Be aware, however, that the supply voltage range of the LM662 is smaller than that of the LM358.

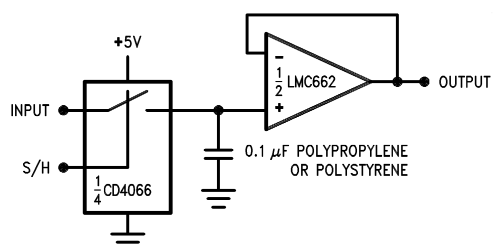
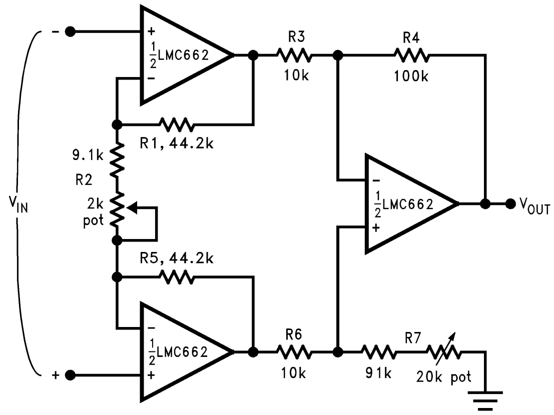



**Figure 6-6. Low Leakage Sample and Hold**




If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

**Figure 6-7. Instrumentation Amplifier**

Use low drift resistors for good CMRR performance over temperature. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain can be adjusted through R2. CMRR can be adjusted through R7. An improved circuit can be designed using the RES11A-Q1, low drift, precision matched resistor pairs. A precise gain of 99 is easily implemented as shown in Figure 6-8.

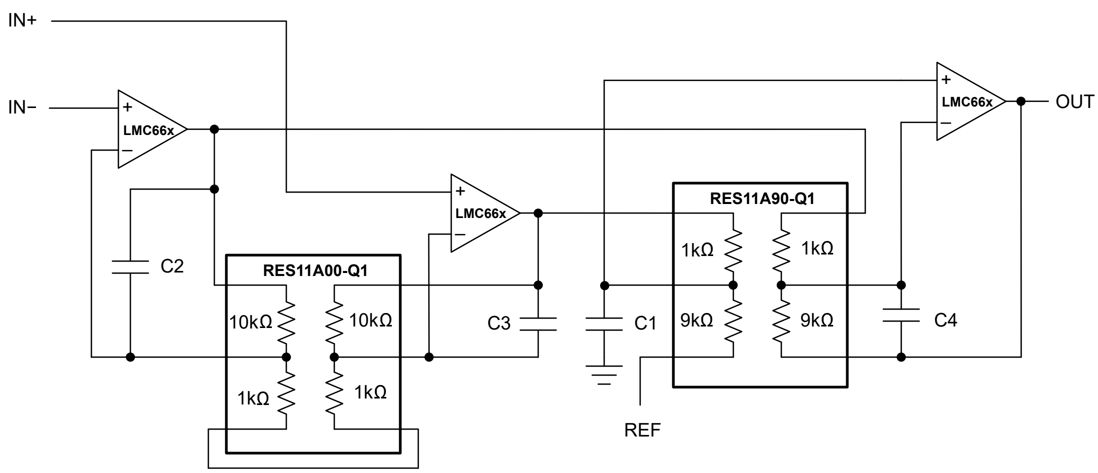
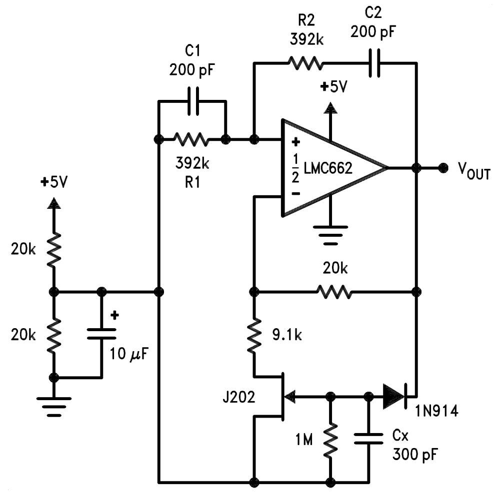



**Figure 6-8. Improved Instrumentation Amplifier With the RES11A**




Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

**Figure 6-9. Sine-Wave Oscillator**

This circuit, as shown, oscillates at 2.0kHz with a peak-to-peak output swing of 4.5V.

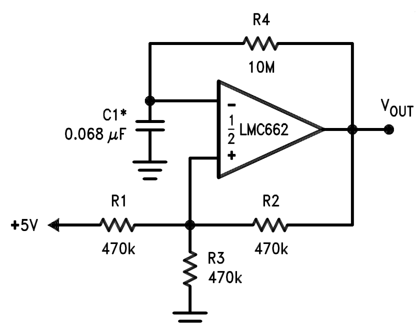



**Figure 6-10. 1Hz Square-Wave Oscillator**

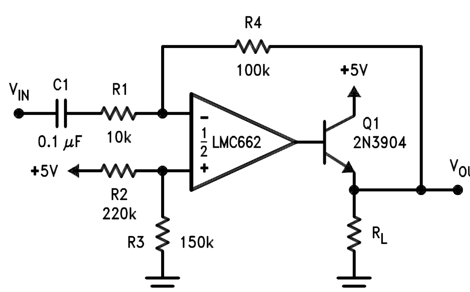
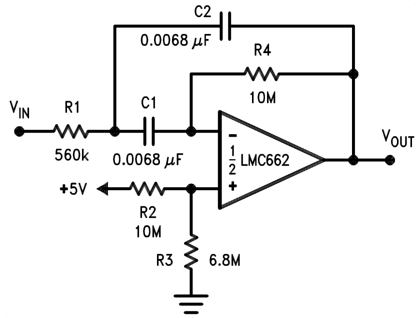
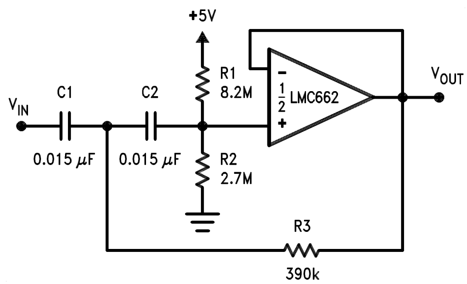



**Figure 6-11. Power Amplifier**




$f_O$ = 10Hz, Q = 2.1, gain = −8.8

**Figure 6-12. 10Hz Band-Pass Filter**




$f_c$ = 10Hz, d = 0.895, gain = 1, 2dB pass-band ripple

**Figure 6-13. 10Hz High-Pass Filter**

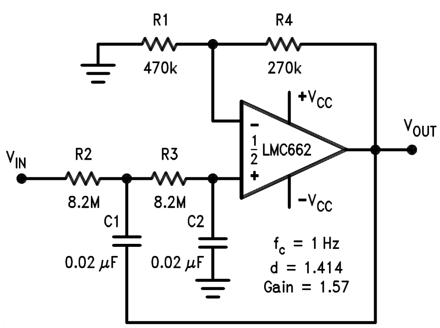
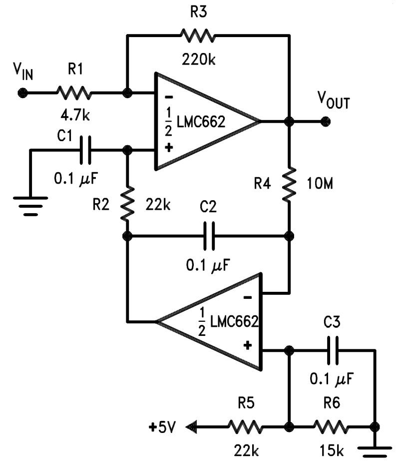



**Figure 6-14. 1Hz Low Pass Filter (Maximally Flat, Dual Supply Only)**




Gain = −46.8 Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1mV).

**Figure 6-15. High Gain Amplifier with Offset Voltage Reduction**

## 6.3 Layout

### 6.3.1 Layout Guidelines

#### *6.3.1.1 Printed Circuit Board Layout for High-Impedance Work*

Generally, any circuit that operates with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC66x, typically less than 40fA, an excellent layout is essential. Fortunately, the techniques for obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though the leakage can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC66x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op amp inputs. See Figure 6-16. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PCB foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of an input. The leakage causes a 100 times degradation from the LMC66x actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 50fA of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See Figure 6-17, Figure 6-18, and Figure 6-19 for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 6-20.

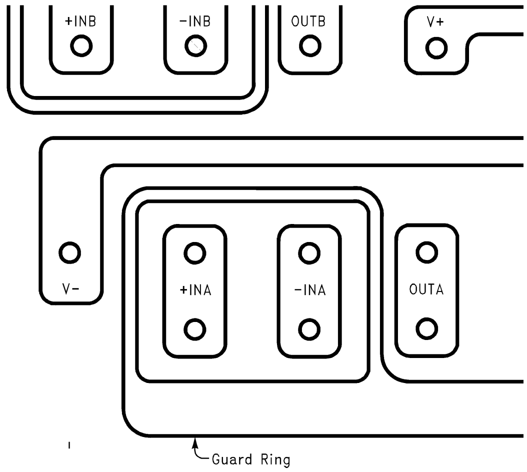



**Figure 6-16. Example, Using the LMC660, of Guard Ring in PCB Layout**

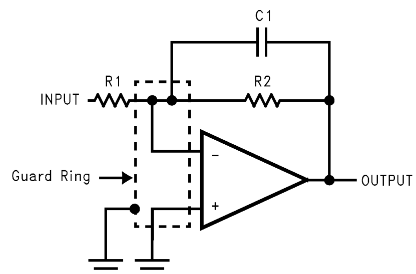



**Figure 6-17. Guard Ring Connections: Inverting Amplifier**

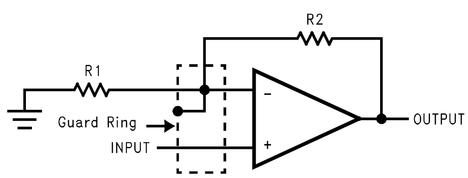



**Figure 6-18. Guard Ring Connections: Non-Inverting Amplifier**

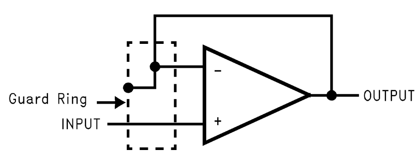



**Figure 6-19. Guard Ring Connections: Follower**

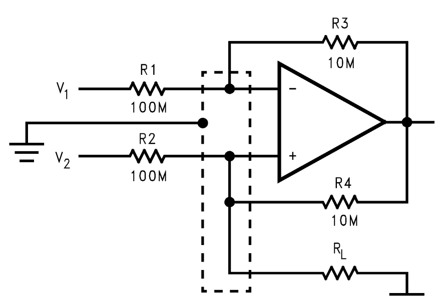
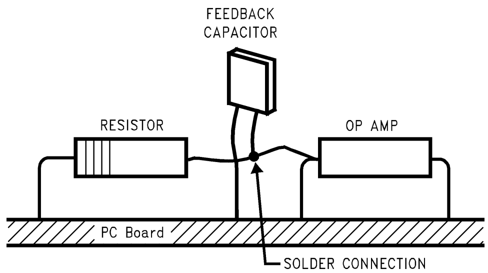



**Figure 6-20. Guard Ring Connections: Howland Current Pump**

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, there is another technique that is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all; instead, bend the pin up in the air and use only air as an insulator because air is an excellent insulator. In this case, some of the advantages of PCB construction are lost, but the advantages of air are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See also Figure 6-21.




Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.

**Figure 6-21. Air Wiring**

# 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.4 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (March 2013) to Revision D (February 2024)** — **Page**

- Added quad channel LMC660 device and associated content....................1
- Deleted low distortion and added low noise to *Features* ....................1
- Updated description text in *Description* ....................1
- Updated pin configuration diagram and added pin functions table....................2
- Added *Thermal Information* ....................5
- Changed separate DC and AC *Electrical Characteristics* into single *Electrical Characteristics* ....................6
- Changed parameter names to conform to new standards in *Electrical Characteristics* ....................6
- Changed input current noise density from 0.0002pA/√Hz to 4fA/√Hz to align with modern noise test setup.....6
- Changed total harmonic distortion specification from 0.01% to 0.2% in *Electrical Characteristics* ....................6
- Added footnote detailing how slew rate minimum specification is specified in *Electrical Characteristics* ......... 6
- Added *Offset Voltage vs Input Common-Mode Voltage* and *Input Bias vs Common-Mode Voltage* curves ... 10
- Updated section text and circuit topology diagram in *Amplifier Topology* .................... 13
- Added instrumentation amplifier circuit with RES11A in *Typical Single Supply Applications* .................... 16

**Changes from Revision B (March 2013) to Revision C (March 2013)** — **Page**

- Changed layout of National Data Sheet to TI format....................16

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC660AIM/NOPB | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 85 | LMC660AIM | |
| LMC660AIMX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | LMC660AIM | Samples |
| LMC660AIN/NOPB | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | -40 to 85 | LMC660AIN | |
| LMC660CM/NOPB | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | 0 to 70 | LMC660CM | |
| LMC660CMX/NOPB | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | 0 to 70 | LMC660CM | Samples |
| LMC660CN/NOPB | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI | 0 to 70 | LMC660CN | |
| LMC662AIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LMC66<br>2AIM | Samples |
| LMC662AIN/NOPB | ACTIVE | PDIP | P | 8 | 40 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LMC<br>662AIN | Samples |
| LMC662CM/NOPB | OBSOLETE | SOIC | D | 8 | | TBD | Call TI | Call TI | 0 to 70 | LMC66<br>2CM | |
| LMC662CMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | 0 to 70 | LMC66<br>2CM | Samples |
| LMC662CN/NOPB | ACTIVE | PDIP | P | 8 | 40 | RoHS & Green | NIPDAU | Level-1-NA-UNLIM | 0 to 70 | LMC<br>662CN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

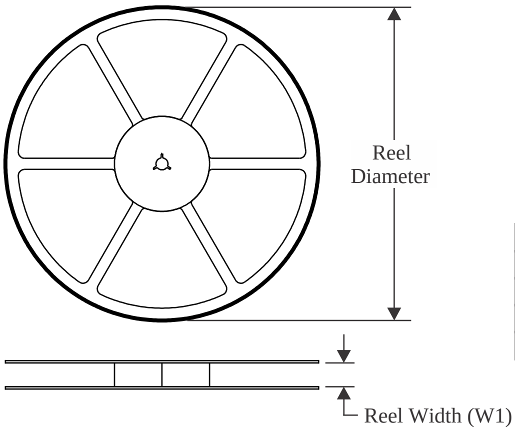
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

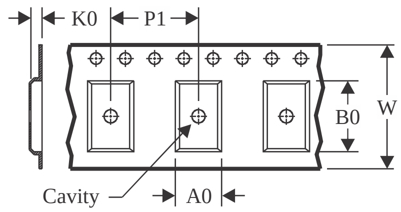
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

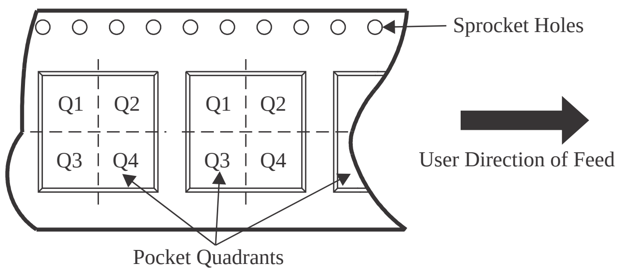



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

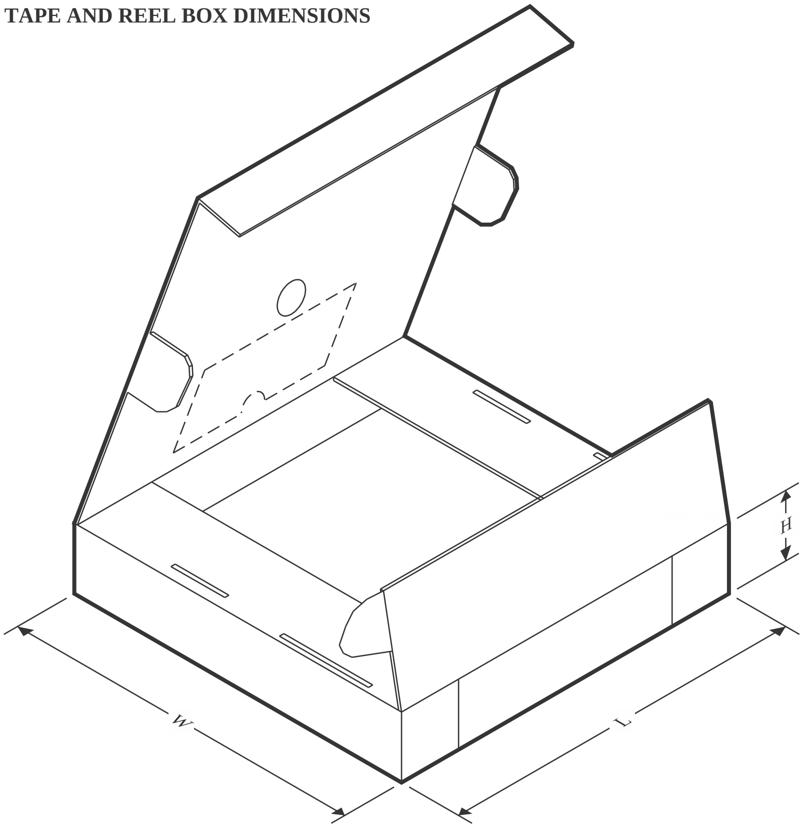
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC660AIMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LMC660CMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LMC662AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMC662CMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC662CMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

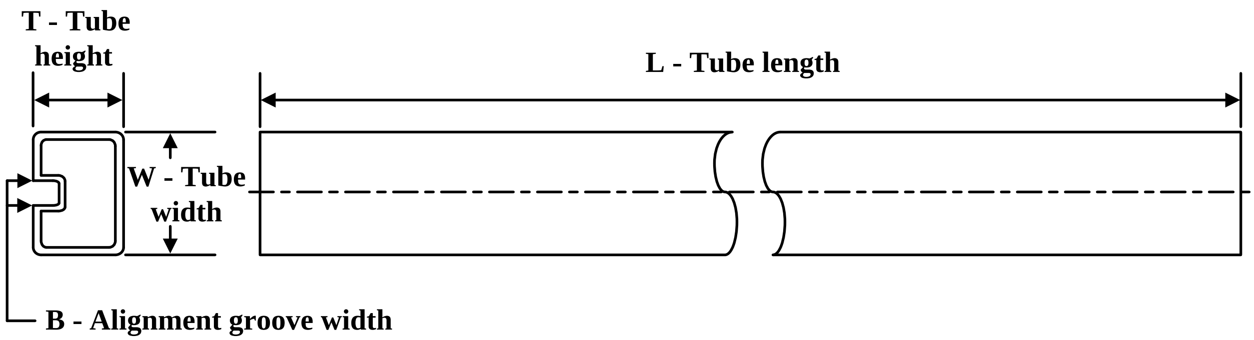
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

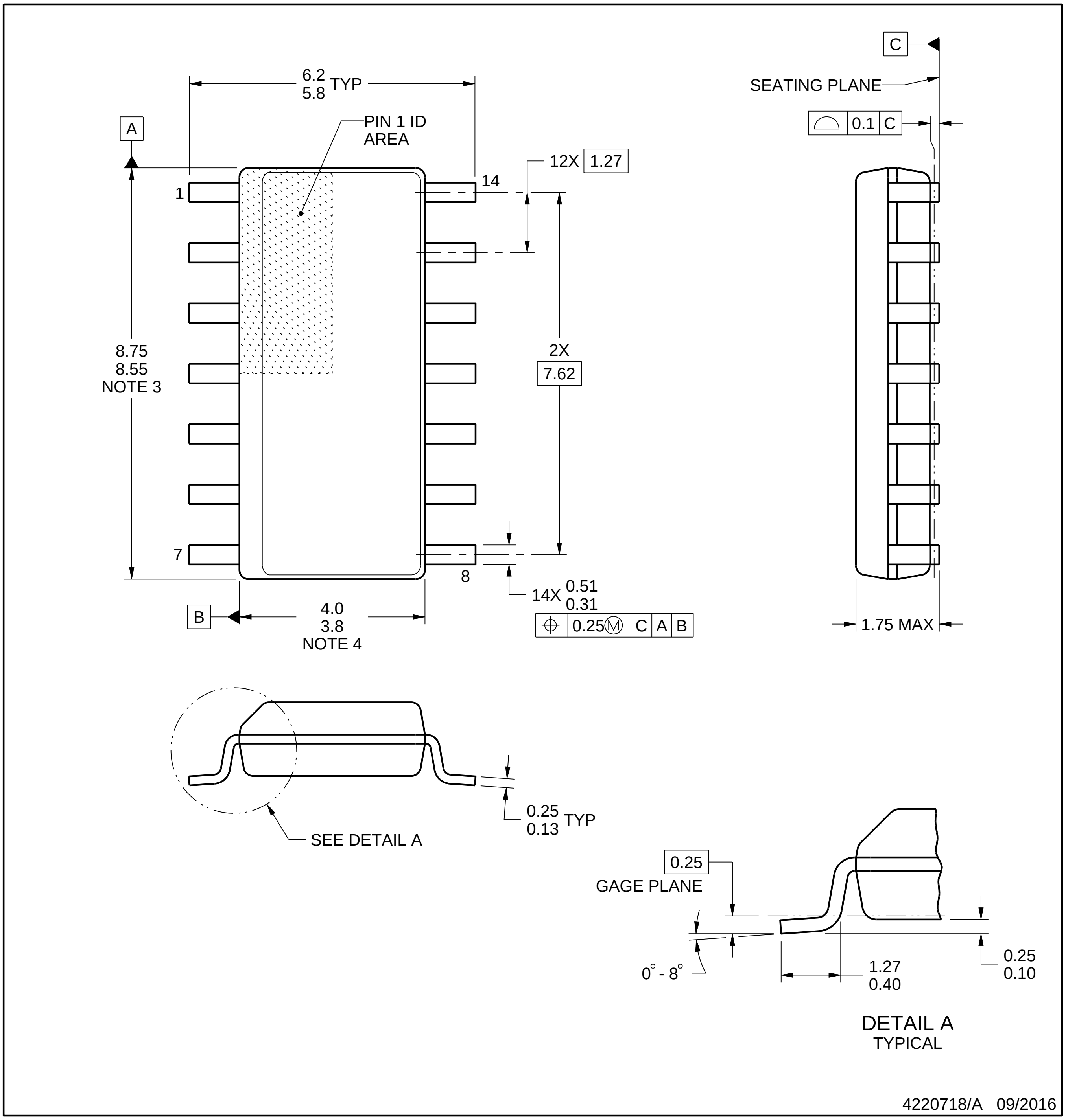
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC660AIMX/NOPB | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| LMC660CMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC662AIMX/NOPB | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| LMC662CMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC662CMX/NOPB | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE



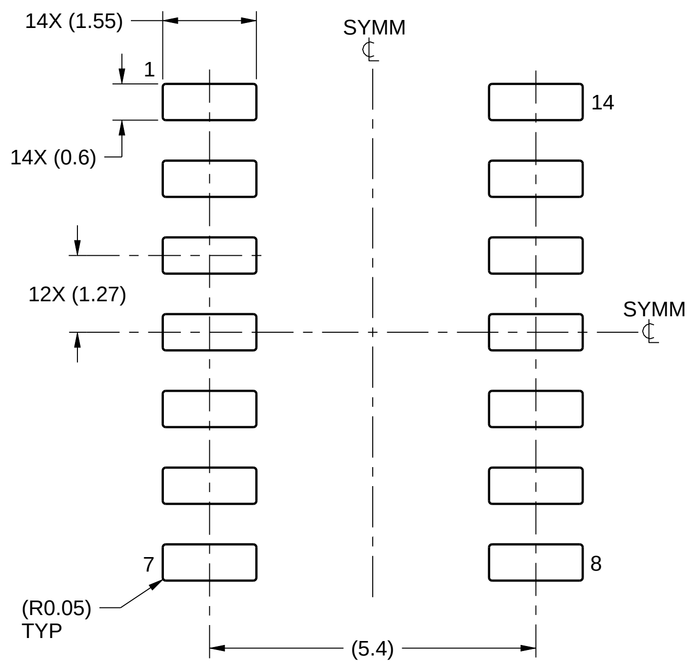

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LMC662AIN/NOPB | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LMC662CN/NOPB | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |

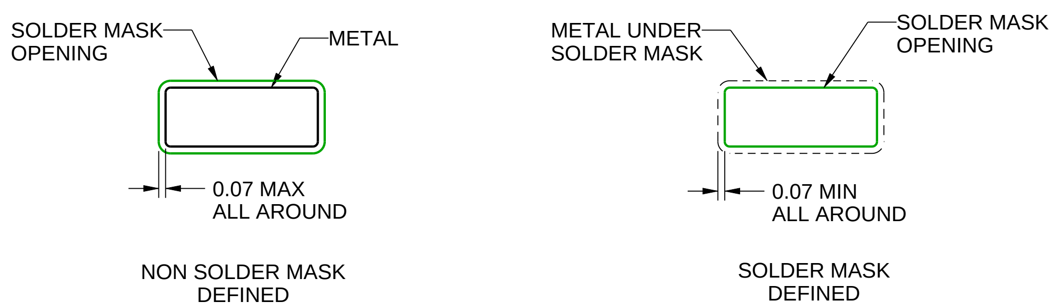



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X

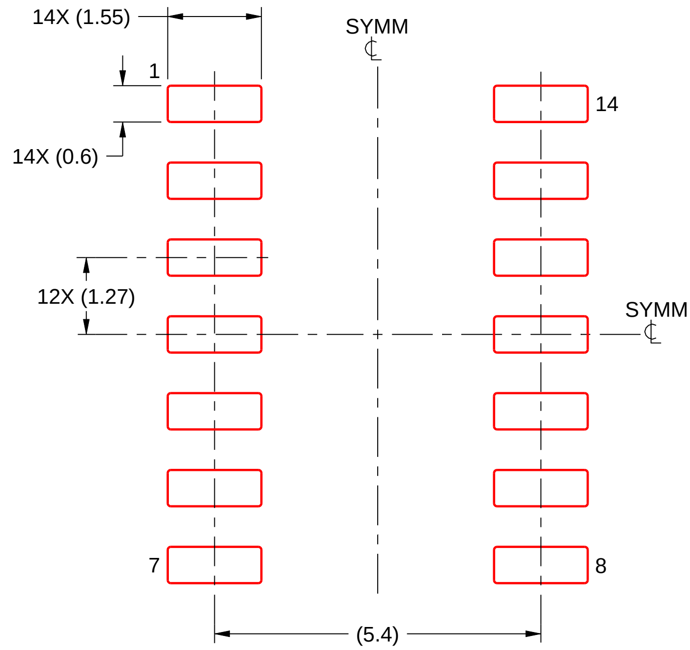



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

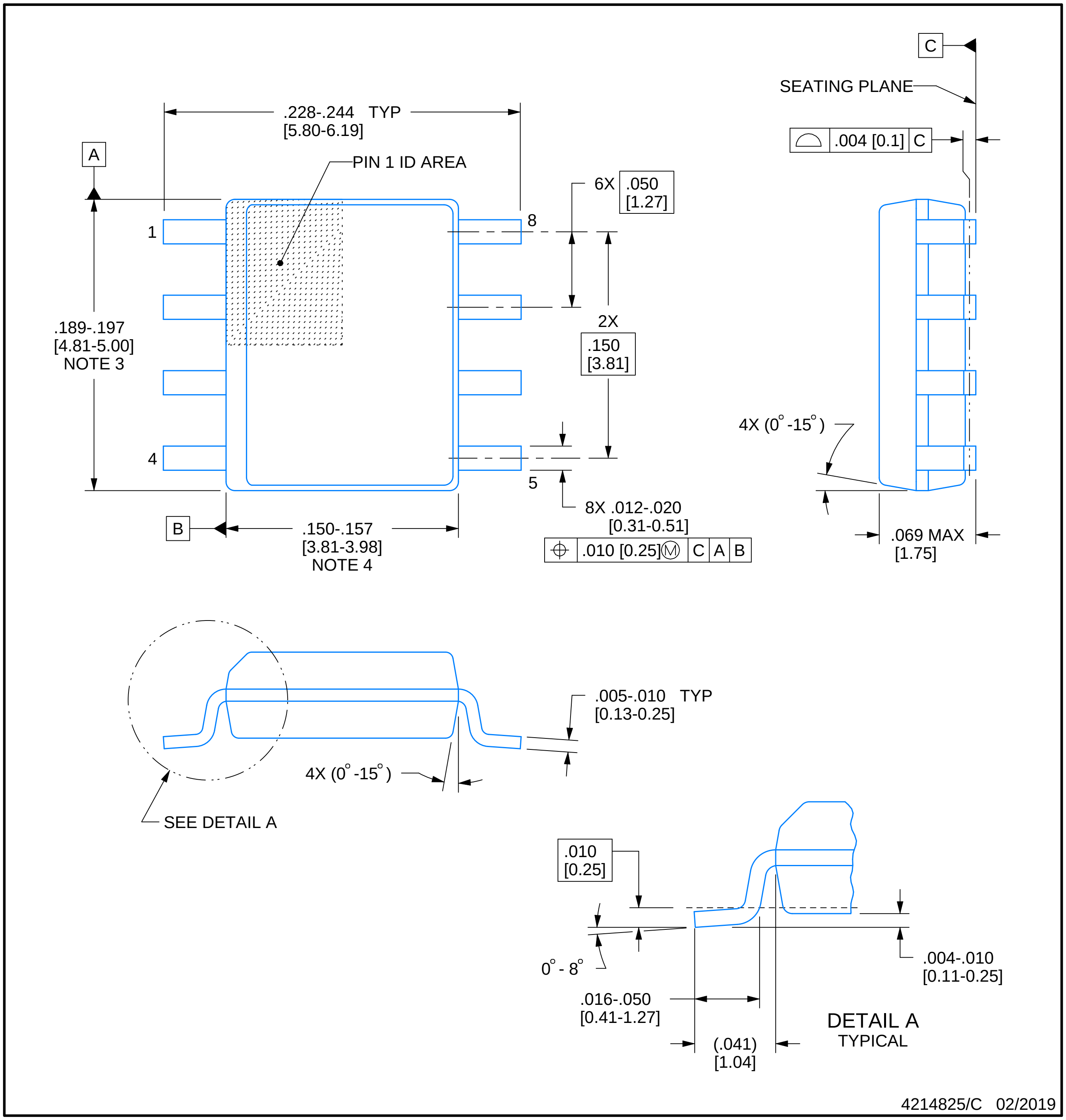



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

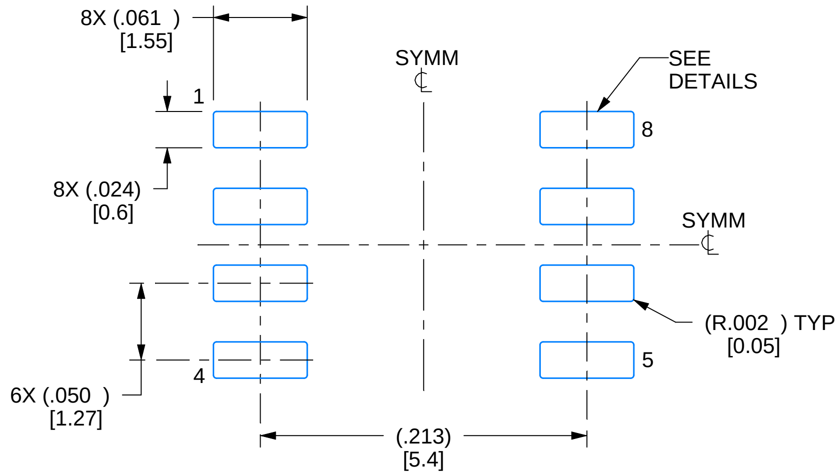
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

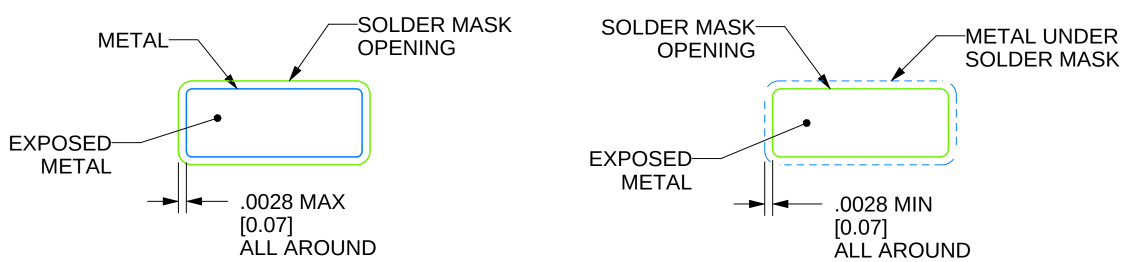



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




NON SOLDER MASK DEFINED

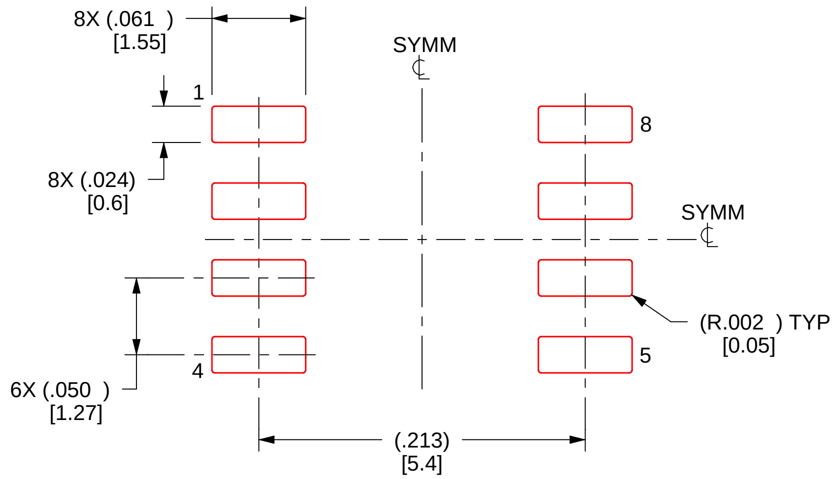
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



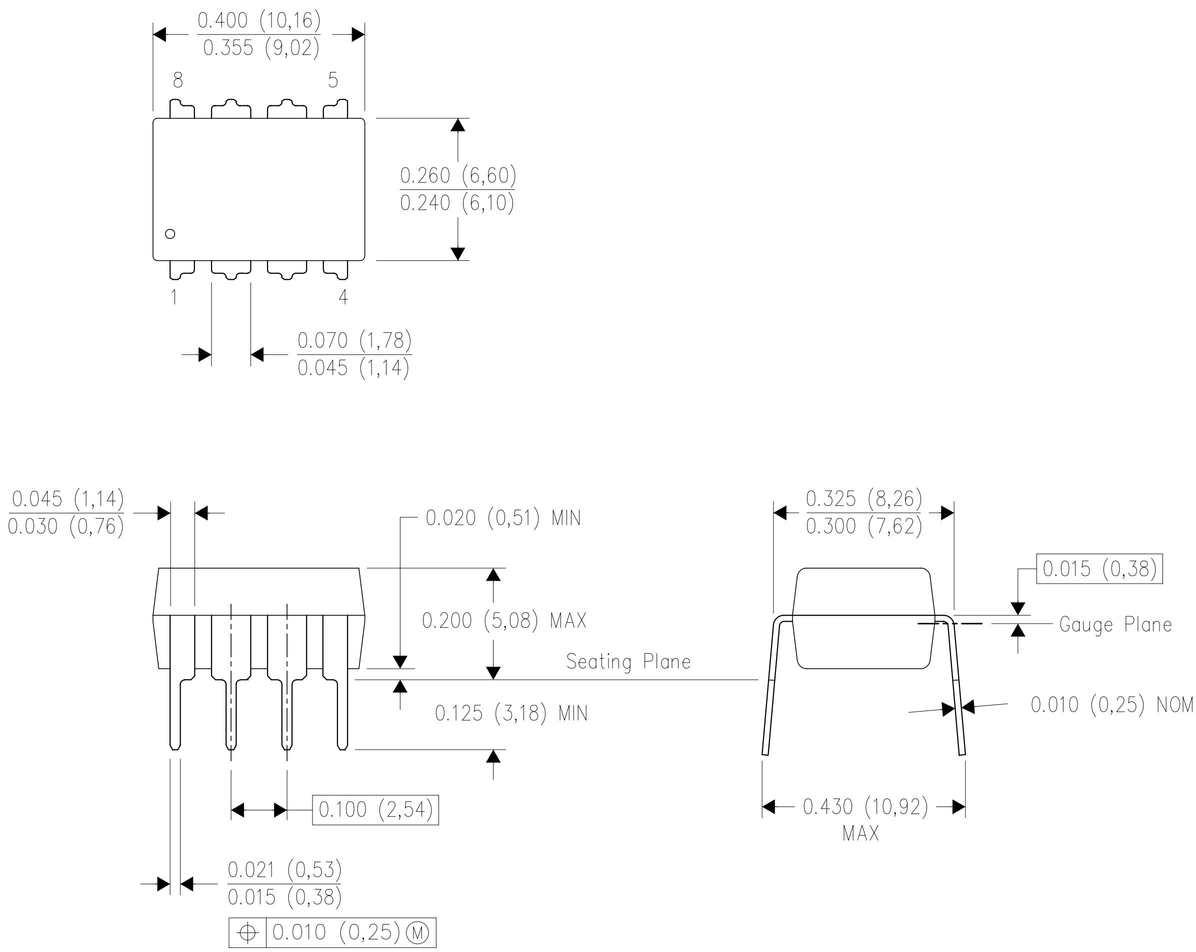

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

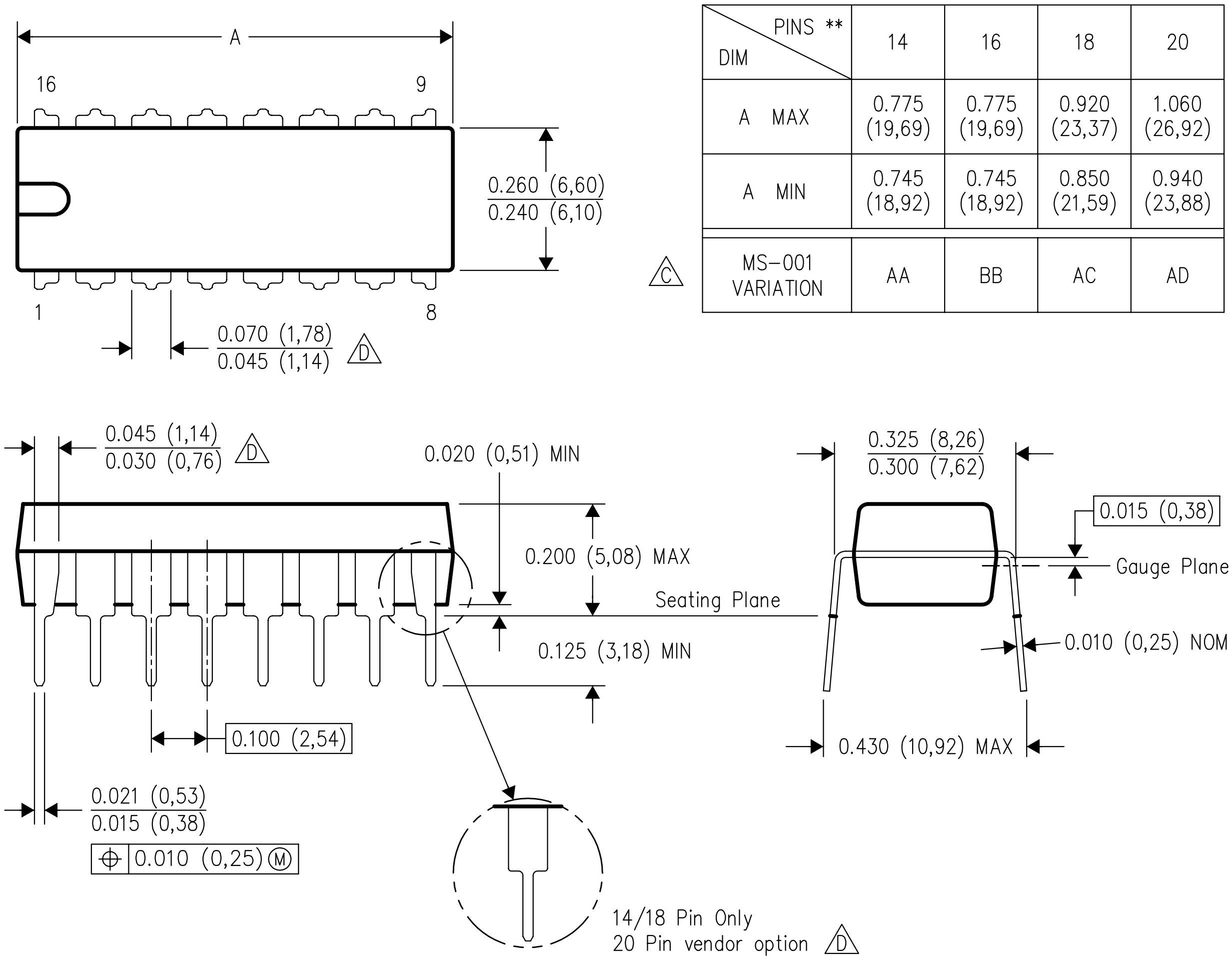



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

# N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION | AA | BB | AC | AD |

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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