LME49723 Dual High Fidelity Audio Operational Amplifier

Check for Samples: LME49723

FEATURES
• Easily Drives 600Ω Loads
• Optimized for Superior Audio Signal Fidelity
• Output Short Circuit Protection
• PSRR and CMRR Exceed 100dB (typ)
• SOIC Package

APPLICATIONS
• High Quality Audio Amplification
• High Fidelity Preamplifiers
• High Fidelity Multimedia
• Phono Pre Amps
• High Performance Professional Audio
• High Fidelity Equalization and Crossover Networks
• High Performance Line Drivers
• High Performance Line Receivers
• High Fidelity Active Filters

KEY SPECIFICATIONS
• Power Supply Voltage Range: ±2.5 to ±17 V
• THD+N (Aᵥ = 1, Vₒᵤᵤ = 3VRMS, fᵢᵢᵢ = 1kHz)
  - Rₐ = 2kΩ: 0.0002 % (typ)
  - Rₐ = 600Ω: 0.0002 % (typ)
• Input Noise Density: 3.6 nV/√Hz (typ)
• Slew Rate: ±8 V/μs (typ)
• Gain Bandwidth Product: 17 MHz (typ)
• Open Loop Gain (Rₐ = 600Ω): 105 dB (typ)
• Input Bias Current: 200 nA (typ)
• Input Offset Voltage: 0.3 mV (typ)

DESCRIPTION
The LME49723 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49723 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49723 combines extremely low voltage noise density (3.6nV/√Hz) with vanishingly low THD+N (0.0002%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49723 has a high slew rate of ±20V/μs and an output current capability of ±26mA. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

The LME49723’s outstanding CMRR (100dB), PSRR (100dB), and Vₒᵤ (0.3mV) give the amplifier excellent operational amplifier DC performance.

The LME49723 has a wide supply range of ±2.5V to ±17V. Over this supply range the LME49723’s input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49723 is unity gain stable.

The LME49723 is available in an 8-lead narrow body SOIC package. Demonstration boards are available for each package.
TYPICAL APPLICATION

Figure 1. Passively Equalized RIAA Phono Preamplifier

CONNECTION DIAGRAM

Figure 2. SOIC Package
See Package Number D0008A

Note: 1% metal film resistors, 5% polypropylene capacitors

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($V_S = V^+ - V^-$) 36V
Storage Temperature $-65^\circ C$ to $150^\circ C$
Input Voltage $V^-(V^-) - 0.7V$ to $(V^+) + 0.7V$
Output Short Circuit (4) Continuous
Power Dissipation Internally Limited
ESD Susceptibility (5) 800V
ESD Susceptibility (6) 180V
Junction Temperature 150°C
Thermal Resistance $\theta_{JA}$ (SO) 145°C/W
Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$ $-40^\circ C \leq T_A \leq 85^\circ C$
Supply Voltage Range $\pm 2.5V \leq V_S \leq \pm 17V$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Amplifier output connected to GND, any number of amplifiers within a package.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage and then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

ELECTRICAL CHARACTERISTICS FOR THE LME49723

The specifications apply for $V_S = \pm 15V$, $R_L = 2k\Omega$, $f_{IN} = 1kHz$, $T_A = 25^\circ C$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LME49723</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typical</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3)</td>
<td>(4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Units (Limits)</td>
<td></td>
</tr>
<tr>
<td>VOS</td>
<td>Offset Voltage</td>
<td>$\pm 0.3$</td>
<td>1 mV (max)</td>
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<tr>
<td>FPBW</td>
<td>Full Power Bandwidth</td>
<td>$V_{OUT} = 1V_{PP-P}$, $-3$dB referenced to output magnitude at $f = 1kHz$</td>
<td>4 MHz</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Equivalent Input Noise Voltage</td>
<td>$f_{BW} = 20Hz$ to 20kHz</td>
<td>$0.45$</td>
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<tr>
<td></td>
<td>Equivalent Input Noise Density</td>
<td>$f = 1kHz$</td>
<td>$3.2$</td>
</tr>
<tr>
<td>$I_n$</td>
<td>Current Noise Density</td>
<td>$f = 1kHz$</td>
<td>$0.7$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td>$V_{CH} = 0V$</td>
<td>$200$</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) Typical specifications are specified at $+25^\circ C$ and represent the most likely parametric norm.
(4) Tested limits are specified to AOQL (Average Outgoing Quality Level).
(5) PSRR is measured as follows: $V_{OS}$ is measured at two supply voltages, $\pm 5V$ and $\pm 15V$. $PSRR = |20\log(\Delta V_{OS}/\Delta V_S)|$. 

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The specifications apply for $V_S = \pm 15\,\text{V}$, $R_L = 2\,\Omega$, $f_{IN} = 1\,\text{kHz}$, $T_A = 25\,\degree\,\text{C}$, unless otherwise specified.

<table>
<thead>
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<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LME49723</th>
<th>Units (Limits)</th>
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<tr>
<td>$\Delta I_O S/\Delta T_e$</td>
<td>Input Bias Current Drift vs Temperature</td>
<td>$-40\degree,\text{C} \leq T_A \leq 85\degree,\text{C}$</td>
<td>0.1</td>
<td>nA/$\degree,\text{C}$</td>
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<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>$V_{CM} = 0,\text{V}$</td>
<td>7</td>
<td>100</td>
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<tr>
<td>$V_{IN-CM}$</td>
<td>Common-Mode Input Voltage Range</td>
<td>$\pm 14,\text{V}$</td>
<td>(V+) − 2.0 (V−) + 2.0</td>
<td>V (min)</td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection</td>
<td>$-10,\text{V} &lt; V_{cm} &lt; 10,\text{V}$</td>
<td>100</td>
<td>90</td>
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<td>$Z_{IN}$</td>
<td>Differential Input Impedance</td>
<td>$-10,\text{V} &lt; V_{cm} &lt; 10,\text{V}$</td>
<td>30</td>
<td>90</td>
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<tr>
<td>$A_{VOL}$</td>
<td>Open Loop Voltage Gain</td>
<td>$-10,\text{V} &lt; V_{out} &lt; 10,\text{V}$, $R_L = 600,\Omega$</td>
<td>100</td>
<td>98</td>
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<td>$</td>
<td>V_{OUTMAX}</td>
<td>$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 600,\Omega$</td>
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<tr>
<td>$</td>
<td>V_{OUTMAX}</td>
<td>$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 2,\Omega$</td>
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<tr>
<td>$</td>
<td>V_{OUTMAX}</td>
<td>$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 10,\Omega$</td>
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<tr>
<td>$I_{OUT}$</td>
<td>Output Current</td>
<td>$R_L = 600,\Omega$, $V_S = \pm 17,\text{V}$</td>
<td>±25</td>
<td>±21</td>
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<td>$I_{OUT-CC}$</td>
<td>Instantaneous Short Circuit Current</td>
<td>$I_{IN} = 10,\text{kHz}$</td>
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<tr>
<td>$R_{OUT}$</td>
<td>Output Impedance</td>
<td>$I_{IN} = 10,\text{kHz}$</td>
<td>0.01</td>
<td>13</td>
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<tr>
<td>$C_{LOAD}$</td>
<td>Capacitive Load Drive Overshoot</td>
<td>100pF</td>
<td>16</td>
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<tr>
<td>$I_S$</td>
<td>Total Quiescent Current</td>
<td>$I_{OUT} = 0,\text{mA}$</td>
<td>6.7</td>
<td>7.5</td>
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</table>
TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Output Voltage
$V_s = \pm 5V, R_L = 2k\Omega$

Figure 3.

THD+N vs Output Voltage
$V_s = \pm 5V, R_L = 10k\Omega$

Figure 4.

THD+N vs Output Voltage
$V_s = \pm 5V, R_L = 600$Ω

Figure 5.

THD+N vs Output Voltage
$V_s = \pm 15V, R_L = 2k\Omega$

Figure 6.

THD+N vs Output Voltage
$V_s = \pm 15V, R_L = 10k\Omega$

Figure 7.

THD+N vs Output Voltage
$V_s = \pm 15V, R_L = 600$Ω

Figure 8.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

THD+N vs Frequency
V\textsubscript{S} = ±15V, V\textsubscript{OUT} = 3V\textsubscript{RMS}, R\textsubscript{L} = 2kΩ

Figure 9.

THD+N vs Frequency
V\textsubscript{S} = ±15V, V\textsubscript{OUT} = 3V\textsubscript{RMS}, R\textsubscript{L} = 600Ω

Figure 11.

THD+N vs Frequency
V\textsubscript{S} = ±15V, V\textsubscript{OUT} = 3V\textsubscript{RMS}, R\textsubscript{L} = 10kΩ

Figure 10.

THD+N vs Frequency
V\textsubscript{S} = ±5V, R\textsubscript{L} = 10kΩ, V\textsubscript{RIPPLE} = 200mV\textsubscript{PP}

Figure 13.

THD+N vs Frequency
V\textsubscript{S} = ±5V, R\textsubscript{L} = 600Ω, V\textsubscript{RIPPLE} = 200mV\textsubscript{PP}

Figure 14.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**PSRR+ vs Frequency**

$V_S = \pm 15V$, $R_L = 2k\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 15.

$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 16.

$V_S = \pm 15V$, $R_L = 600\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 17.

$V_S = \pm 5V$, $R_L = 2k\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 18.

$V_S = \pm 5V$, $R_L = 600\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 19.

$V_S = \pm 5V$, $R_L = 10k\Omega$, $V_{RIPPLE} = 200mV_{PP}$

FREQUENCY (Hz)

Figure 20.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR- vs Frequency

Figure 21.

PSRR- vs Frequency

Figure 22.

CMRR vs Frequency

Figure 23.

CMRR vs Frequency

Figure 24.

CMRR vs Frequency

Figure 25.

CMRR vs Frequency

Figure 26.
Crosstalk vs Frequency

\( V_S = \pm 15V, \ V_{OUT} = 3V_{RMS}, \ R_L = 2k\Omega, \)

Figure 27.

Crosstalk vs Frequency

\( V_S = \pm 15V, \ V_{OUT} = 3V_{RMS}, \ R_L = 10k\Omega, \)

Figure 28.

Crosstalk vs Frequency

\( V_S = \pm 15V, \ V_{OUT} = 3V_{RMS}, \ R_L = 600\Omega, \)

Figure 29.

IMD vs Output Voltage

\( V_S = \pm 5V, \ R_L = 2k\Omega, \)

Figure 30.

IMD vs Output Voltage

\( V_S = \pm 5V, \ R_L = 10k\Omega, \)

Figure 31.

IMD vs Output Voltage

\( V_S = \pm 5V, \ R_L = 600\Omega, \)

Figure 32.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Voltage vs Load Resistance

Output Voltage vs Supply Voltage

Supply Current vs Supply Voltage

Figure 33.

Figure 34.

Figure 35.

Figure 36.

Figure 37.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Supply Current vs Supply Voltage

\[ R_L = 10k\Omega \]

**Figure 39.**

Supply Current vs Supply Voltage

\[ R_L = 600\Omega \]

**Figure 40.**

Noninverting Amp

\[ \text{IN} \]

**Figure 41.**

Inverting Amp

\[ \text{OUT} \]

**Figure 42.**

Voltage Gain & Phase vs Frequency

\[ V_S = \pm 15V \]
\[ R_L = 2k\Omega \]

**Figure 43.**

**Figure 44.**
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Figure 45.

Power Bandwidth

Figure 46.

Equivalent Input Noise vs Frequency

Voltage (nV/ Hz)

FREQUENCY (Hz)

V_S = ±15V
R_L = 2 kΩ
THD ≤ 1%
APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49723 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier’s inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49723’s low residual distortion is an input referred internal error. As shown in Figure 47, adding the 10Ω resistor connected between the amplifier’s inverting and non-inverting inputs changes the amplifier’s noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier’s closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 47.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment’s capabilities. This datasheet’s THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

![Figure 47. THD+N and IMD Distortion Test Circuit](image)

The LME49723 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

**Figure 48. Noise Measurement Circuit**
Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: $e_n = \frac{V_0}{560,000}$ (V)

**Figure 49. RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency**

**Figure 50. Flat Amp Voltage Gain vs Frequency**

**TYPICAL APPLICATIONS**

**Figure 51. Balanced to Single Ended Converter**

$V_O = V_1 - V_2$
\[ V_O = V_1 + V_2 - V_3 - V_4 \]

**Figure 52. Adder/Subtracter**

\[ f_0 = \frac{1}{2\pi RC} \]

**Figure 53. Sine Wave Oscillator**

If \( C_1 = C_2 = C \)

\[ R_1 = \frac{3}{2\pi f_0 C} \]

\[ R_2 = 2R_1 \]

Illustration is \( f_0 = 1 \text{ kHz} \)

**Figure 54. Second Order High Pass Filter (Butterworth)**
Illustration is $f_0 = 1$ kHz

**Figure 55. Second Order Low Pass Filter (Butterworth)**

$t_0 = \frac{1}{2\pi C_1 R_1}, Q = \frac{1}{2} \left( 1 + \frac{R_2}{R_0} \right), A_{BP} = A_{LP} = A_{H} = \frac{R_2}{R_0}$

Illustration is $f_0 = 1$ kHz, $Q = 10$, $A_{BP} = 1$

**Figure 56. State Variable Filter**

**Figure 57. AC/DC Converter**
Figure 58. 2 Channel Panning Circuit (Pan Pot)

Figure 59. Line Driver

Illustration is:

\[ f_L = 32 \text{ Hz}, \quad f_{LB} = 320 \text{ Hz} \]

\[ f_H = 11 \text{ kHz}, \quad f_{HB} = 1.1 \text{ kHz} \]
Figure 60. Tone Control

- $A_v = 35 \text{ dB}$
- $E_n = 0.33 \mu V$
- $S/N = 90 \text{ dB}$
- $f = 1 \text{ kHz}$
- A Weighted
- A Weighted, $V_{IN} = 10 \text{ mV}$
- @$f = 1 \text{ kHz}$

Figure 61. RIAA Preamp

\[ V_0 = 101(V_2 - V_1) \]

Illustration is:
\[ V_0 = 101(V_2 - V_1) \]

Figure 62. Balanced Input Mic Amp
Figure 63. Band Graphic Equalizer

<table>
<thead>
<tr>
<th>$f_0$ (Hz)</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>$R_1$</th>
<th>$R_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>0.12μF</td>
<td>4.7μF</td>
<td>75kΩ</td>
<td>500Ω</td>
</tr>
<tr>
<td>64</td>
<td>0.056μF</td>
<td>3.3μF</td>
<td>68kΩ</td>
<td>510Ω</td>
</tr>
<tr>
<td>125</td>
<td>0.033μF</td>
<td>1.5μF</td>
<td>62kΩ</td>
<td>510Ω</td>
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<td>250</td>
<td>0.015μF</td>
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<td>16k</td>
<td>330pF</td>
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## REVISION HISTORY

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<th>Description</th>
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<td>01/07/08</td>
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<td>1.01</td>
<td>02/11/08</td>
<td>Text edits.</td>
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<tr>
<td>B</td>
<td>04/04/13</td>
<td>Changed layout of National Data Sheet to TI format.</td>
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## PACKAGING INFORMATION

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<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>LME49723MA/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L49723 MA</td>
<td>Samples</td>
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<td>D</td>
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<td>2500</td>
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<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>L49723 MA</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LME49723MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LME49723MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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