LMG1025-Q1 Automotive Low Side GaN and MOSFET Driver For High Frequency and Narrow Pulse Applications

1 Features

- AEC-Q100 grade 1 qualified
- 1.25ns typical minimum input pulse width
- 2.6ns typical rising propagation delay
- 2.9ns typical falling propagation delay
- 300ps typical pulse distortion
- Independent 7A pull-up and 5A pull-down current
- 650ps typical rise time (220pF load)
- 850ps typical fall time (220pF load)
- 2mm x 2mm QFN package
- Inverting and non-inverting inputs
- UVLO and over-temperature protection
- Single 5V supply voltage

2 Applications

- Automotive LIDAR
- Driver monitoring
- Vehicle occupant detection sensor
- DC/DC converter

3 Description

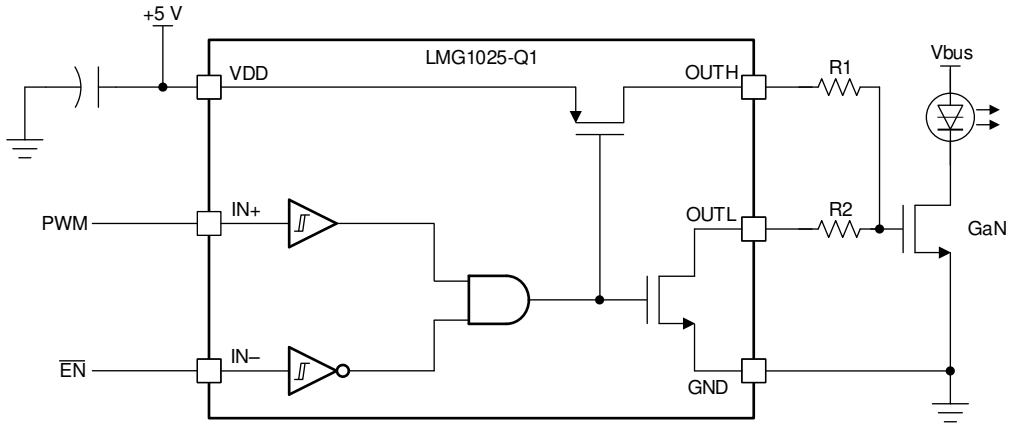
The LMG1025-Q1 is a single channel low-side enhancement-mode GaN FET and logic-level MOSFET driver for high switching frequency automotive applications. Narrow pulse width capability, fast switching specification, and small pulse distortion combine to significantly enhance LiDAR, ToF, and Power Converter performance. 1.25ns output pulse width enables more powerful, eye-safe diode pulses. This, combined with 300ns distortion, leads to longer-range, precise LiDAR/ToF systems. 2.9ns propagation delay significantly improves the control loop response time and thus overall performance of the power converters. Split output allows the drive strength and timing to be independently adjusted through external resistors between OUTH, OUTL, and the FET gate.

The driver features undervoltage lockout (UVLO) and over-temperature protection (OTP) to ensure the device is not damaged in overload or fault conditions. LMG1025-Q1 is available in a compact, leadless, AEC-Q100 automotive qualified package to meet the size and gate loop inductance requirements of high switching frequency automotive applications.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LMG1025QDRVRQ1	DRV (WSON 6)	2mm x 2mm
LMG1025QDEERQ1	DEE (WSON 6)	2mm x 2mm

(1) For all available packages, see Section 12.



Typical (Simplified) System Diagram

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4 Pin Configuration and Functions

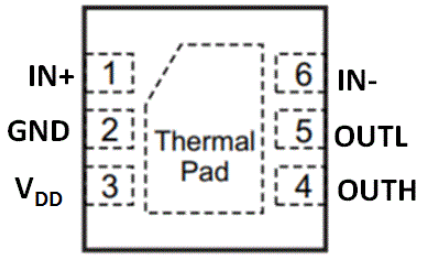


Figure 4-1. DEE 6-Pin WSON Top View

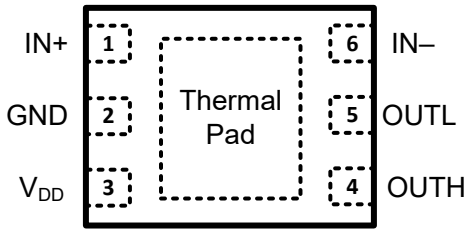


Figure 4-2. DRV 6-Pin WSON Top View

Table 4-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GND	2	G	Power supply and source return. Connect with a direct path to the transistor's source.
IN+	1	I	Positive logic-level input.
IN–	6	I	Negative logic-level input.
OUTL	5	O	Pull-down gate drive output. Connect through an optional resistor to the target transistor's gate.
OUTH	4	O	Pull-up gate drive output. Connect through a resistor to the target transistor's gate.
VDD	3	P	Input voltage supply. Decouple through a compact capacitor to GND.
Thermal Pad	-	-	Internally connected to GND through substrate. Connect this pad to large copper area, generally a ground plane.

(1) I=Input, O=Output, P=Power, G=Ground

5 Specifications

5.1 Absolute Maximum Ratings

All voltages are with respect to GND pin.(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	5.75	V
V_{IN}	IN+, IN- pin voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	OUTH, OUTL pin voltage	-0.3	5.75	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Operating Temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stessing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{INx}	IN+ or IN- input voltage	0		V_{DD}	V
V_{OUTx}	OUTH, OUTL pin voltage	0		5.25	V
T_J	Operating Temperature	-40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		LMG1025-Q1		UNIT
		DRV (WSON)	DEE (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.4	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.1	87.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.8	30.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.1	2.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	35.8	30.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

VDD = 5V, good feed-through bypass capacitor from VDD to GND pin, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
$I_{VDD, Q}$	VDD Quiescent Current	IN_+ = IN_- = 0 V			75	µA
$I_{VDD, op}$	VDD Operating Current	fsw = 30 MHz, no load, 2Ω as R_{OUTH} and R_{OUTL}		40		mA
		fsw = 30 MHz, 100-pF load, 2Ω as R_{OUTH} and R_{OUTL}		51		mA
$V_{DD, UVLO}$	Under-voltage Lockout	V_{DD} rising	4.0		4.35	V
$\Delta V_{DD, UVLO}$	UVLO Hysteresis			85		mV
T_{OTP}	Over temperature shutdown, turn-off threshold			170		°C
ΔT_{OTP}	Over temperature hysteresis			20		°C
Input DC Characteristics						
V_{IH}	IN+, IN- high threshold		1.7		2.6	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.38		1	V
R_{IN+}	Positive input pull-down resistance	To GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to V_{DD}	100	150	250	kΩ
C_{IN+}	Positive input pin capacitance	To GND		1.45		pF
C_{IN-}	Negative input pin capacitance	To GND		1.45		pF
Output DC Characteristics						
V_{OL}	OUTL voltage	I_{OUTL} = 100 mA, IN+= IN- = 0 V			45	mV
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH} = 100 mA, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V			52	mV
I_{OH}	Peak source current	V_{OUTH} = 0 V, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V		7		A
I_{OL}	Peak sink current	V_{OUTL} = 5 V, IN+= IN- = 0 V, V_{DD} = 5 V		5		A

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{start}	Startup Time, V_{DD} rising above UVLO	IN- = GND, IN+ = V_{DD} , V_{DD} rising above 4.4 V to OUTH rising		40	78	µs
$t_{shut-off}$	ULVO falling	IN- = GND, IN+ = VDD , VDD falling below 3.9 V to OUTH falling	0.7	2.5	3.5	µs
$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100-pF load	1.5	2.6	4.1	ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100-pF load	1.8	2.9	4.4	ns
Δt_{pd}	Pulse positive distrortion, ($t_{pd, f}$ - $t_{pd, r}$)		0	300	610	ps
t_{rise}	Output rise time	0Ω series 220 pF load(1)		650		ps
t_{fall}	Output fall time	0Ω series 220 pF load(1)		850		ps
t_{min}	Minimum input pulse width that changes output state	0Ω series 220 pF load(1)		1.25		ns

(1) Rise and fall time calcuated as time from 20% of the gate voltage to 80% of the gate voltage of the GaN FET.

5.7 Typical Characteristics

VDD = 5 V

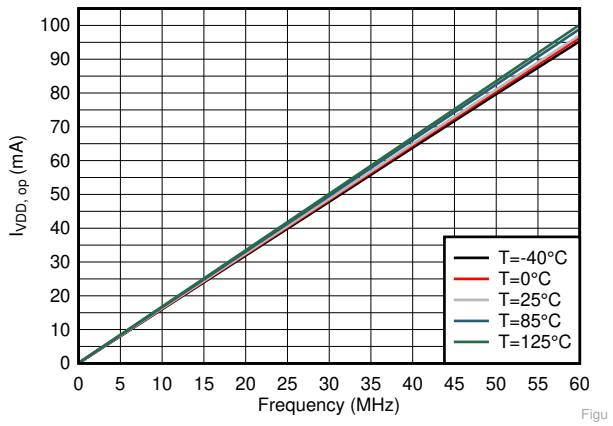


Figure 5-1. $I_{VDD,op}$ with 2 Ω in Series with 100pF Load

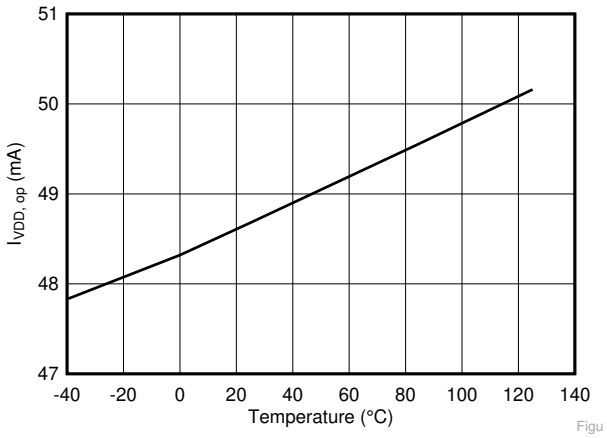


Figure 5-2. $I_{VDD,op}$ with 2 Ω in Series with 100pF Load

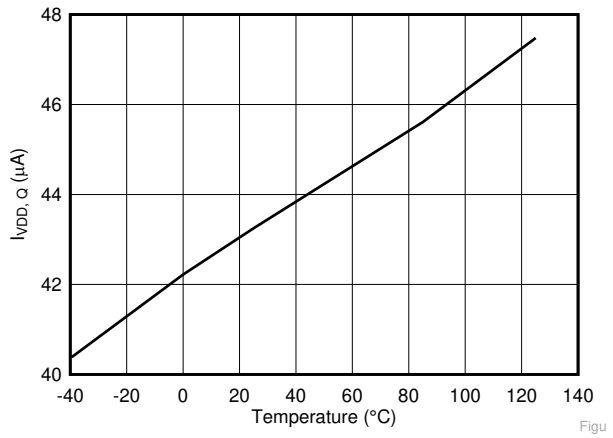


Figure 5-3. Quiescent Current

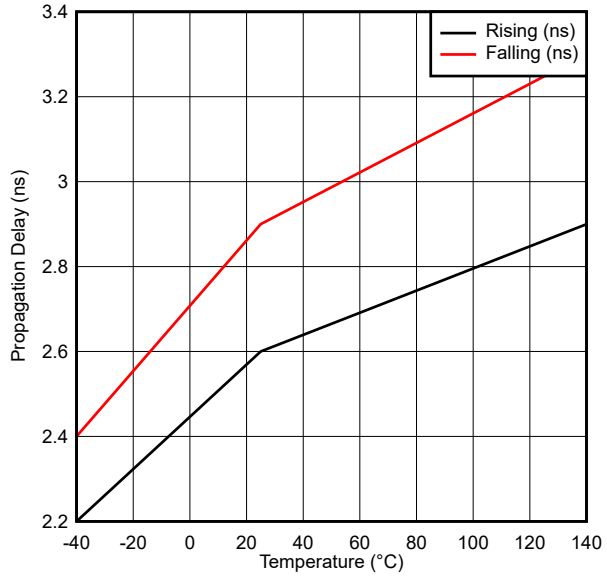


Figure 5-4. Propagation Delay with 100pF Load

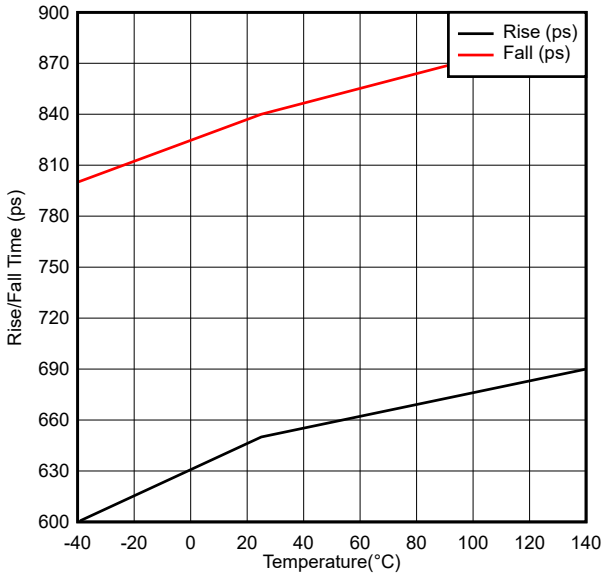


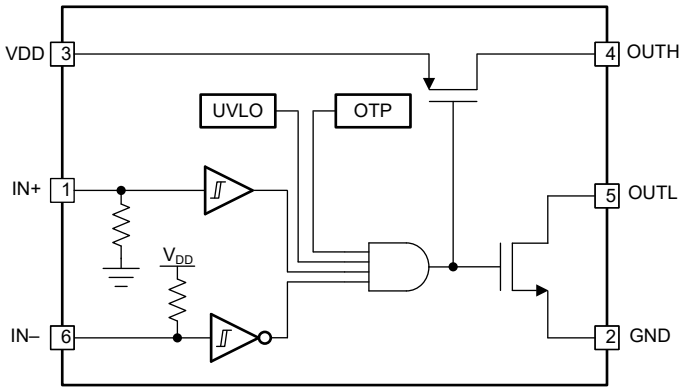
Figure 5-5. Rise and Fall Time with 100pF Load

6 Detailed Description

6.1 Overview

LMG1025-Q1 is a high-performance low-side 5-V gate driver for GaN and logic-level MOSFETs. While it is designed to function well in high-speed applications, such as wireless power transmission and LiDAR/ToF, it can be used in any application where a low-side gate driver is required. The LMG1025-Q1 is optimized to provide the lowest propagation delay through the driver to the power transistor. LMG1025-Q1 is in a small 2mm×2mm QFN package with wettable flanks, in order to minimize its parasitic inductance. This low inductance design is necessary to achieve high current, low ringing performance in very high frequency operation when driving power FETs. The same holds true for when designing with LMG1025-Q1. QFN package with wettable flanks is also needed to improve system robustness in many automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Stage

The input stage features two Schmitt-triggers at the pins IN+ and IN– to reduce sensitivity to noise on the inputs. IN+ signal and the inverted IN– signal are both sent to an AND gate. IN+ is connected with a pull-down resistor while IN– is connected with a pull-up resistor to prevent unintended turn-on. The output of the driver will be high when input voltage goes above input thresholds and output goes low when input voltage is below input threshold mentioned in the electrical characteristics table. Both IN+ and IN– are single ended inputs, and these two pins cannot be used as a differential input pair. Parasitic elements become extremely important in high frequency designs and extreme care should be taken while laying out the printed circuit board to minimize these parasitic elements. The performance of the LMG1025-Q1 and the performance of the overall system gets affected by the layout and components being selected.

6.3.2 Output Stage

LMG1025-Q1 provides 7-A source, 5-A sink (asymmetrical drive) peak-drive current capability, and features a split output configuration. The OUTH and OUTL outputs of the LMG1025-Q1 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turn-on and turn-off drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver. The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device Ciss, and thus preventing false turn-on. This ringing heavily depends on the layout as switching frequency increases and as rise and fall time gets shorter. The distance between the gate driver and power device need to be as minimum as possible. Gate loop should be as minimum as possible. If ringing is un-avoidable then the gate resistor should be selected in such a way that the ringing is minimized. Bypass capacitor type, value, and position also significantly affects this ringing.

6.3.3 Bias Supply and Under Voltage Lockout

LMG1025-Q1 features nominal 5 V and maximum 5.25 V of supply voltage, and its absolute maximum supply voltage is 5.75 V. In the design, it is recommended to limit the variability of the power supply to be within 5%

(0.25 V), and the overshoot voltage during switching transient not to exceed the absolute maximum voltage. Refer to Section VDD and Overshoot for more on the detailed design guide. LMG1025-Q1 also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.0 V and 4.35 V with a hysteresis of 85mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low $R_{DS(ON)}$ region. During UVLO condition, the OUTL pin is pulled down to ground.

6.3.4 Overtemperature Protection (OTP)

LMG1025-Q1 features overtemperature protection (OTP) function by having a rising edge trigger point at around 170°C of junction temperature. With a hysteresis of 20°C, the device can restart to operate when junction temperature is below 150°C.

6.4 Device Functional Modes

The device will operate in following mode when not in UVLO state.

Table 6-1. Truth Table

IN-	IN+	OUTH	OUTL
L	L	Open	L
L	H	H	Open
H	L	Open	L
H	H	Open	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

To operate GaN FET or MOSFET at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gate of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 5 V) in order to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1025-Q1 is a high frequency low-side gate driver for enhancement mode GaN FETs and Si FETs in a single ended configuration. The split-gate outputs with strong source and sink capability provides flexibility to adjust the turn-on and turn-off strength independently. As a low side driver, LMG1025-Q1 can be used in a variety of applications, including different power converters, LiDAR, time-of-flight (ToF) laser drivers, class-E wireless chargers, synchronous rectifiers, and augmented reality devices. LMG1025-Q1 can also be used as a high frequency low current laser diode driver, or as a signal buffer with very fast rise/fall time.

7.2 Typical Application

The LMG1025-Q1 is designed to be used with a single low-side, ground-referenced GaN or logic-level FET, as shown in Figure 7-1. Independent gate drive resistors, R1 and R2, are used to independently control the turnon and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor. The care should be taken that the ringing on the gate of the power device or ringing on any of the gate driver pin does not exceed the recommended rating. Resistors play an important role in damping these ringing. The layout and type of gate resistor with respect to gate driver and power device is also very important.

It is strongly recommended to use at least a 2-Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing has to be ensured to be below V_{DD}+0.3 V.

For applications requiring smaller resistance, please contact the factory for guidance.

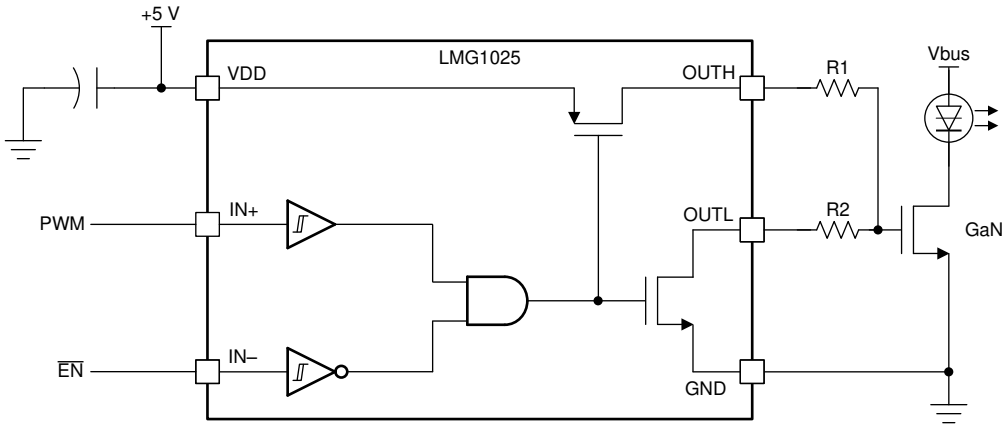


Figure 7-1. Typical Implementation of a Circuit

7.2.1 Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates the LMG1025-Q1 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

7.2.2 Detailed Design Procedure

7.2.2.1 Handling Ground Bounce

For the best switching performance and gate loop with lowest parasitics, it is recommended to connect the ground return pin of LMG1025-Q1 as close as possible to the source of the low-side FET in a low inductance manner. However, doing so can cause the ground of LMG1025-Q1 to bounce relative to the system or controller ground and lead to erroneous switching logic on the input so as mis-turn on/off on the output.

First of all, LMG1025-Q1 has input hysteresis built into the input buffers to help counteract this effect. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by Equation 1

$$\frac{di_s}{dt} = \frac{V_{HYST}}{L_{RS}} \tag{1}$$

where

- L_{RS} is the inductance of the sense resistor,
- V_{HYST} is the hysteresis of the input pin,
- and dis/dt is the maximum allowed current slew rate.

For an assumed shunt resistor parasitic inductance of 0.5 nH and a minimum hysteresis of 0.5 V, the maximum slew rate is 1 A/ns. Many applications would exhibit higher current slew rates, up to the 10 A/ns range, which would make this approach impractical. The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to the LMG1025-Q1. A current-limiting, 100 Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

Secondly, for moderate ground-bounce cases, a simple R-C filter can be built with a simple resistor in series with the inputs. By utilizing the input capacitance of LMG1025-Q1, the resistor could be close to its input pin. The addition of a small capacitor on the input as supplement can also be helpful. A small time constant of the R-C filter may be enough to filter out high frequency noise. This solution is acceptable for moderate cases in applications where extra delay is acceptable and the pulse width is not extremely short such as in 1ns range.

For more extreme cases, or where no delay is tolerable while pulse width is extremely short, using a commonmode choke provides the best results.

One example application where ground-bounce is particularly challenging is when using a current sense resistor. In Figure 7-2 LMG1025-Q1 ground is connected to the source of GaN FET, while the controller ground is connected to the other side of the current sense resistor as shown in Figure 7-2. Due to the fast switching and very fast current slew rates, the high ground potential bounce induced by inductance of the sense resistor can disrupt the operation of the circuit or even damage the part. To prevent this, a common-mode choke can be used for IN+ and IN–, respectively. Resistors can also added to the signal output line before LMG1025-Q1 depending on the input signal pulse width to provide additional RC filtering. Figure 7-4 presents the schematic using approach A with the preferred filtering method. Approach B as shown in Figure 7-3 places the current sense resistor within the gate drive loop path. In this case, the LMG1025-Q1 GND pin is connected to the signal ground, and with good ground plane connection, the ground bounce issue can be less severe than approach A. However, the inductance of the current sense resistor adds common-source inductance to the gate drive loop. The voltage generated across this parasitic inductance will subtract from the gate-drive voltage of the FET, slowing down the turnon and turnoff di/dt of the FET, or even cause mis-turn on and off. Additional gate resistance will have to be added to ensure the loop is stable and ring-free. The slower rise may negate the advantage of the fast switching of the GaN FET and may cause additional losses in the circuit. Therefore, this approach is not recommended.

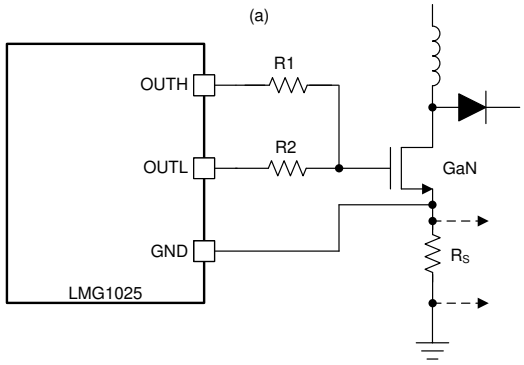


Figure 7-2. Source Resistor Current Sense A Configuration

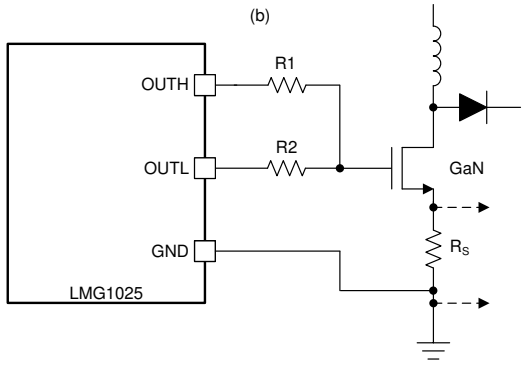


Figure 7-3. Source Resistor Current Sense B Configuration

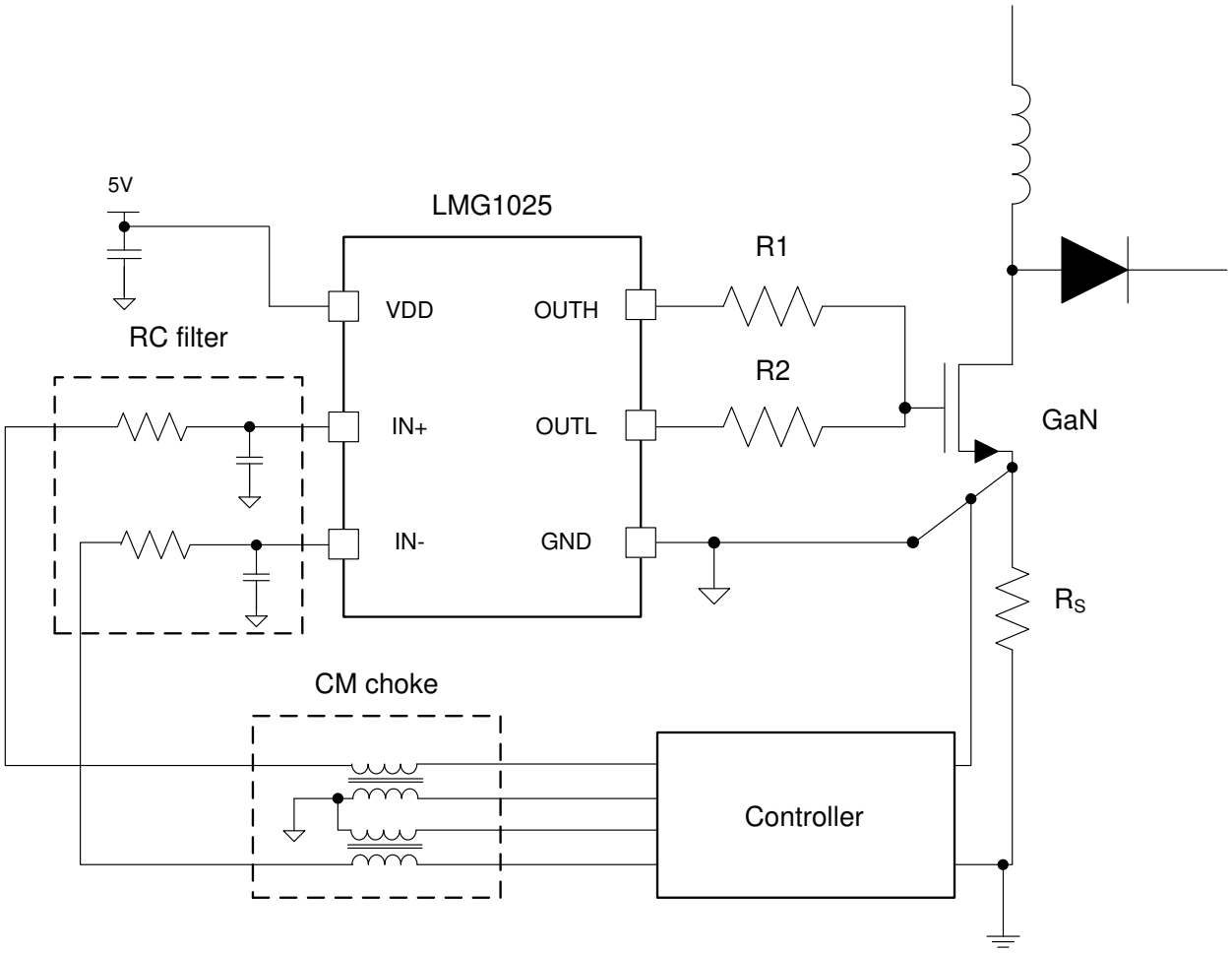


Figure 7-4. Filtering For Ground Bounce Noise Handling When Using LMG1025-Q1

7.2.2.2 Creating Nanosecond Pulse

LMG1025-Q1 can be used to drive pulses of nano seconds duration on to a capacitive load. LMG1025-Q1 can be driven with a equivalently short pulse on one input pin. However, this takes a sufficiently strong digital driver and careful consideration of the routing parasitics from digital output to input of LMG1025-Q1. Two inputs and included AND gate in LMG1025-Q1 provide an alternate method to create a short pulse at the LMG1025-Q1 output. Starting with both IN+ and IN– at low, taking IN+ high will cause the output to go high. Now if IN– is taken high as well, output will be pulled low. So a digital signal and its delayed version can be applied to IN+ and IN– respectively to create a pulse at the output with width corresponding to the delay between the signals, as shown in Figure 7-5. The delay can be digitally controlled in the nanosecond range. This method alleviates the requirements for driving the input of LMG1025-Q1. If a separate delayed version of the digital signal is not available, an RC delay followed by a buffer can be used to derive the second signal. Optionally, if LMG1025-Q1 must be driven with a single short duration pulse, that pulse can itself be generated using another LMG1025-Q1 by the above method to meet drive requirements.

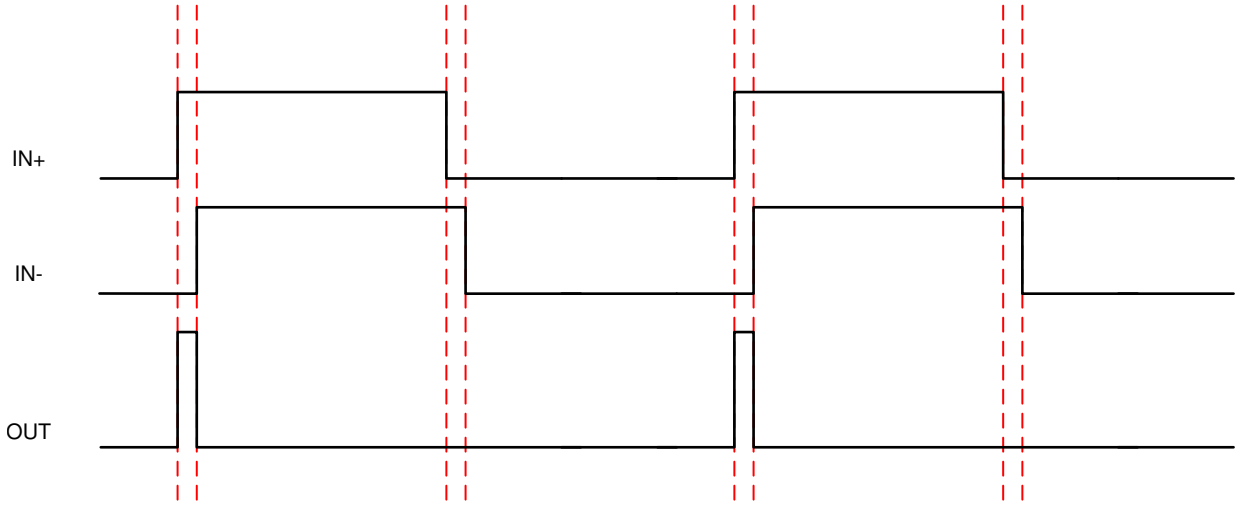


Figure 7-5. Timing Diagram To Create Short Pulses

7.2.2.3 VDD and Overshoot

Fast switching with high current is prone to ringing with parasitic inductances, including those on PCB traces. Overshoot associated with such ringing transients need to be evaluated and controlled as a part of the PCB design process to limit device stress. The parameters affecting stress are how high the overshoot is above the absolute maximum specification and the ratio of overshoot duration to the switching time period. Recommended design practice is to limit the overshoots to the absolute maximum pin voltages. This is accomplished with carful PCB layout to minimize parasitic inductances, choice of components with low ESL and addition of series resistance to limit rise times. For large overshoots, limiting the variability of the power supply may be required. For example, 0.5V of overshoot will be permissible with a maximum recommended supply of 5.25 V (5% variability); however, for larger overshoots, a supply with lower variability will be preferred.

7.2.2.4 Operating at Higher Frequency

With fast rise/fall time, and capability of achieving nano-second pulse width, depending on the capacitive load condition, the operating frequency of LMG1025-Q1 can be increased in a burst manner. In conditions which requires very high frequency pulsing, a pulse train with certain period of pause between each burst can be adopted to avoid overheat of the device. This will help maintain the RMS output current similar as lower frequency operation but boost the transient frequency to very high. In addition, higher decoupling capacitance will be needed to supply high frequency charging of the capacitive load.

7.2.3 Application Curves

LMG1025-Q1 EVM is used to take application waveforms. This EVM has LDO, input buffer, GaN FET, and load resistor. It shows the switching performance of the LMG1025-Q1 when equivalent laser diode current is switched. Figure 7-6 and Figure 7-7 show VDD turn-on and turn-off delay in an application-like set-up. System designer need to make sure that these delays are acceptable in their designs. LIDAR design needs to pulse the laser diode for very short duration. Figure 7-8 shows how LMG1025-Q1 can not only handle nano-second pulse at its input but also can produce a nano-second pulse at the output while driving a reasonably sized GaN FET that has 3.2nC of typical total gate charge. Figure 7-8 also shows very small, e.g. less than 3 ns, rising and falling propagation delay of LMG1025-Q1. Figure 7-9 shows drive strength of LMG1025-Q1. It shows how LMG1025-Q1 can achieve sub-nano second rise and fall time, which is very important for LIDAR applicatoins.

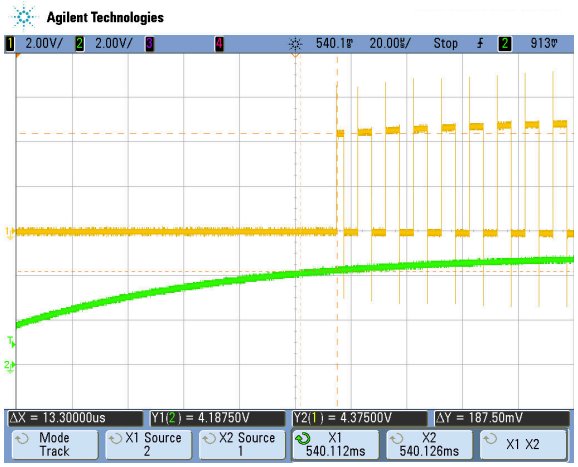


Figure 7-6. Startup Time

Figure 7-7. Shutdown Time

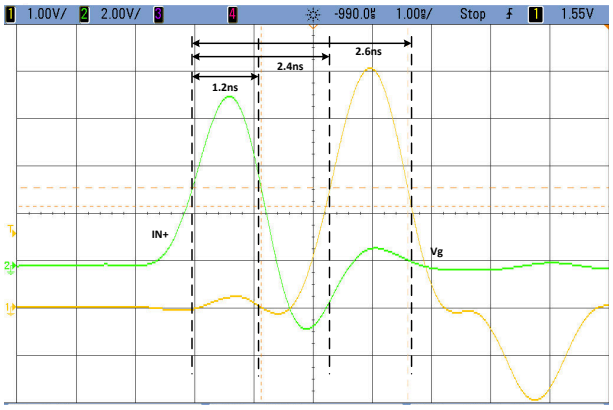


Figure 7-8. Input Pulse Width and Propagation Delays

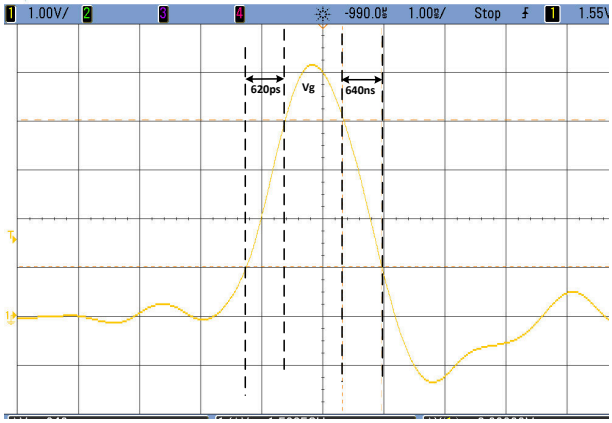


Figure 7-9. Rise and Fall Time

8 Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and GND pins to support the high peak current being drawn from VDD during turnon of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

TI recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to the IC, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1 µF of 0402 or feed-through capacitor (closest to LMG1025-Q1) and a 1 µF 0603 capacitor is recommended.

9 Layout

9.1 Layout Guidelines

The layout of the LMG1025-Q1 is critical to its performance and functionality. The LMG1025-Q1 is available in a 2x2 DFN, which allows a low inductance connection to a FET. Figure 9-1shows the recommended layout of the LMG1025-Q1 with a ball-grid GaN FET.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package should be used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

9.1.1 Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the LMG1025-Q1. The LMG1025-Q1 should be placed as close to the GaN FET as possible, with gate drive resistors immediately connecting OUTH and OUTL to the FET gate. Large traces need to be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the LMG1025-Q1 GND pin connect to this plane with minimal impedance. Finally, care must be taken to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

9.1.2 Bypass Capacitor

The VDD power terminal of the LMG1025-Q1 must by bypassed to ground immediately adjacent to the IC. The placement and value of the bypass capacitor is very critical because of the fast gate drive of the IC, . The bypass capacitor must be located on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF, up to 1 µF, with temperature coeffient X7R or better. Recommended body types are LICC, IDC, Feed-though, and LGA. Finally, an additional 1µF capacitor should be placed as close to the IC as practical.

9.2 Layout Example

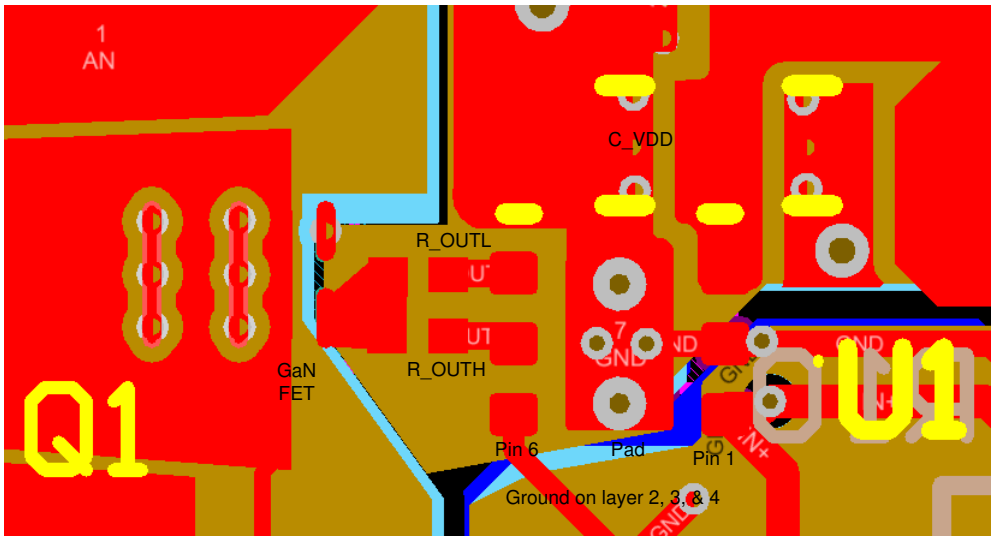


Figure 9-1. Typical LMG1025-Q1 Layout With Ball-Grid GaN FET

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Trademarks

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10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2020) to Revision C (December 2024)	Page
• Add the DRV package information	3
• Added the Y- axis title to Figure 5-4 and Figure 5-5	6
• Changed functional block diagram pin numbers	8

Changes from Revision A (August 2019) to Revision B (January 2020)	Page
• Changed marketing status from Advance Information to Production Data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG1025QDEERQ1	Active	Production	WSON (DEE) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG
LMG1025QDEETQ1	Active	Production	WSON (DEE) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG
LMG1025QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LQ25

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

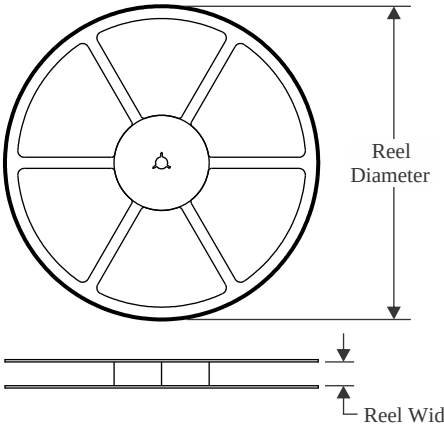
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

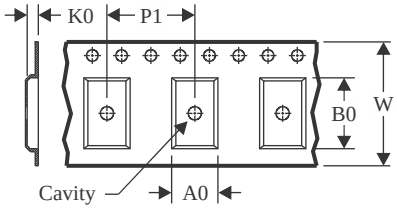
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

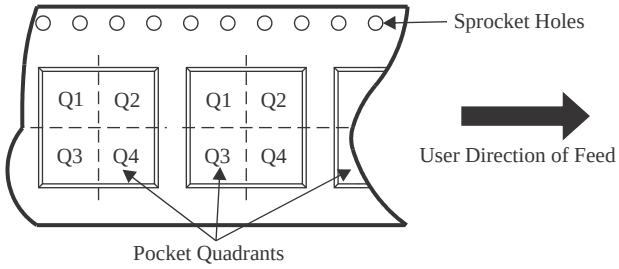


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

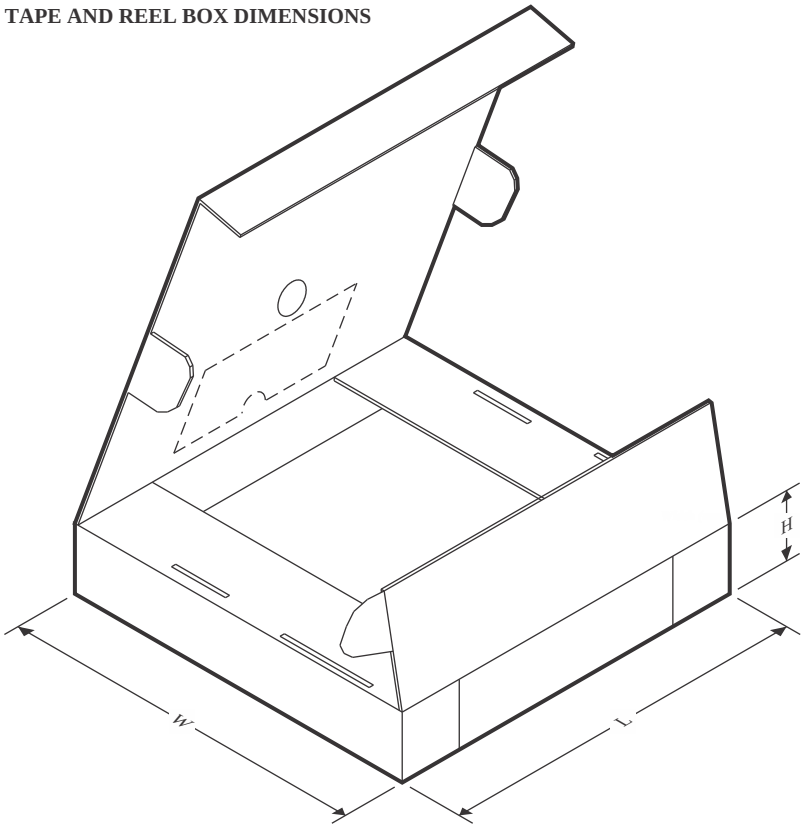
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1025QDEERQ1	WSON	DEE	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMG1025QDEETQ1	WSON	DEE	6	250	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMG1025QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

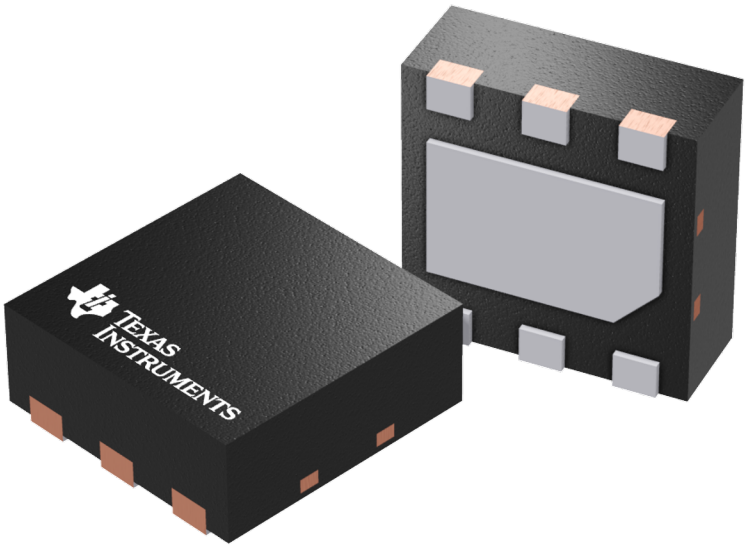


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1025QDEERQ1	WSON	DEE	6	3000	213.0	191.0	35.0
LMG1025QDEETQ1	WSON	DEE	6	250	213.0	191.0	35.0
LMG1025QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



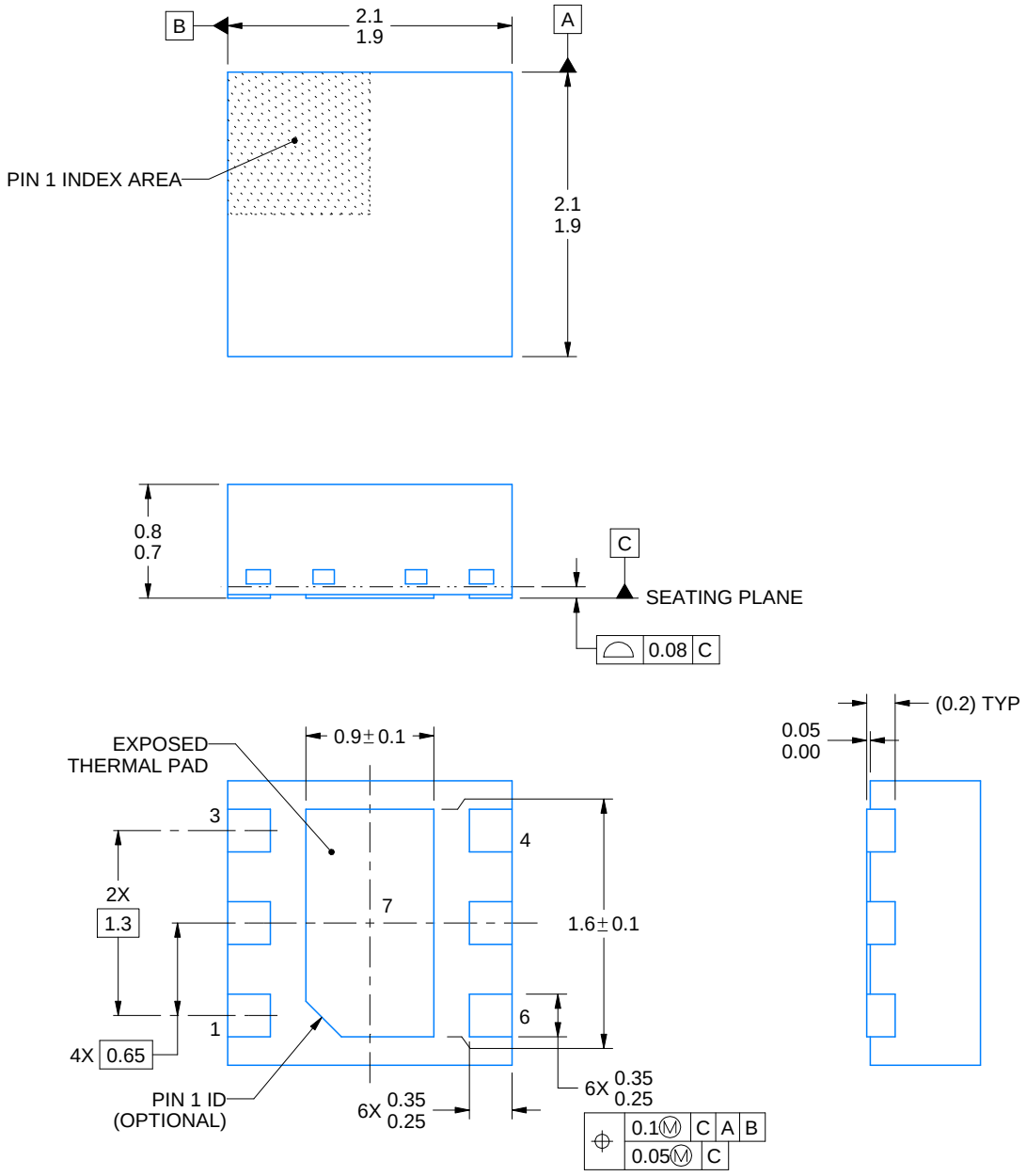
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006E

PACKAGE OUTLINE

WSON - 0.8 mm max height

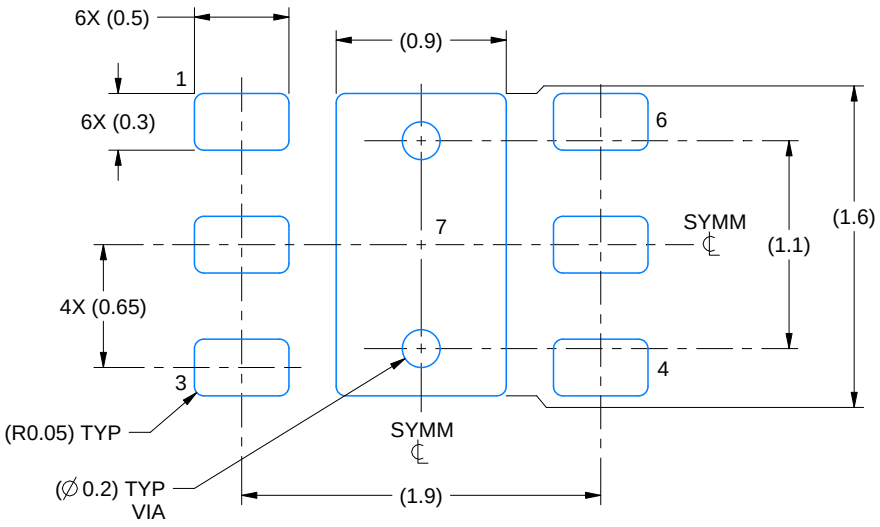
PLASTIC SMALL OUTLINE - NO LEAD



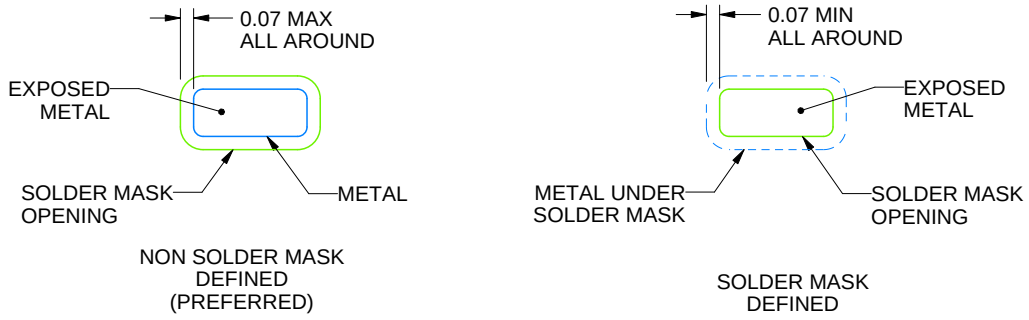
4230187/A 11/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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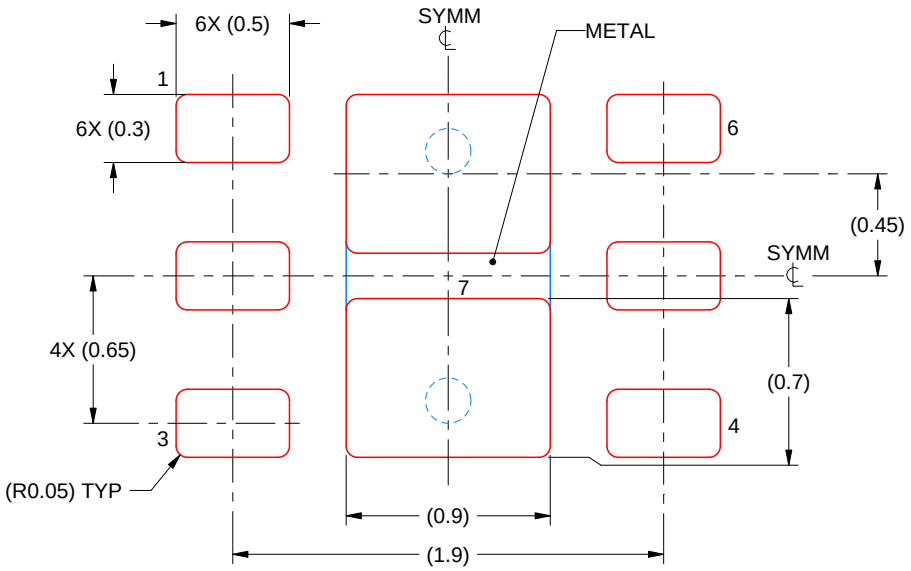
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4230187/A 11/2023

NOTES: (continued)

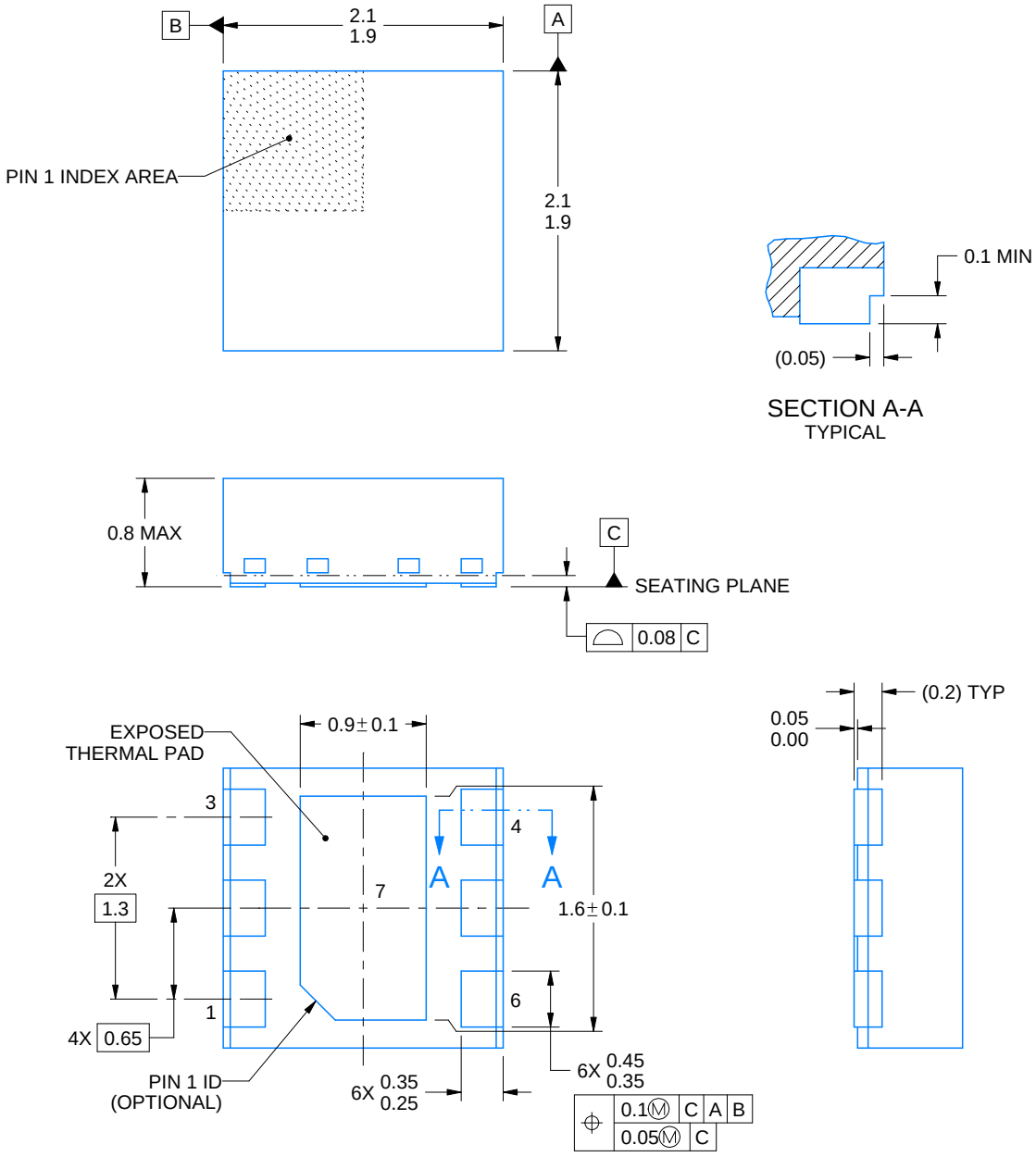
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DEE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4219364/A 01/2019

NOTES:

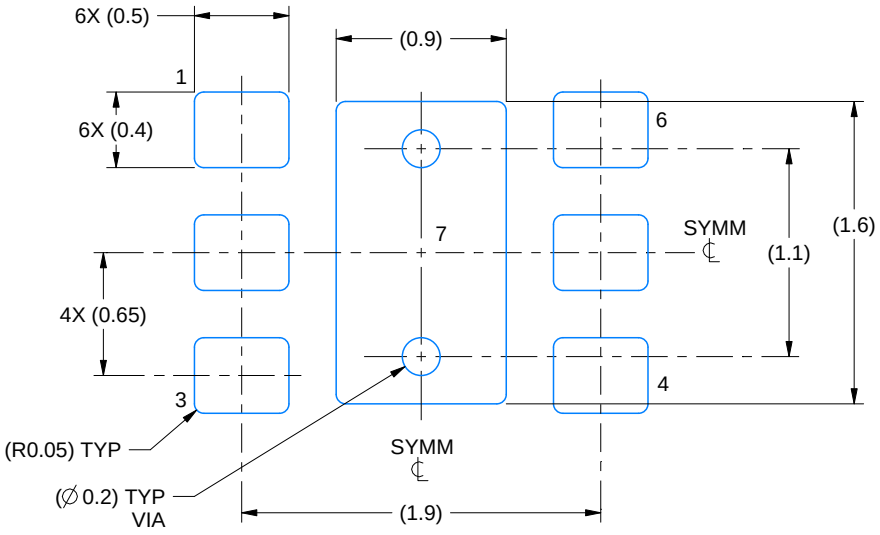
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

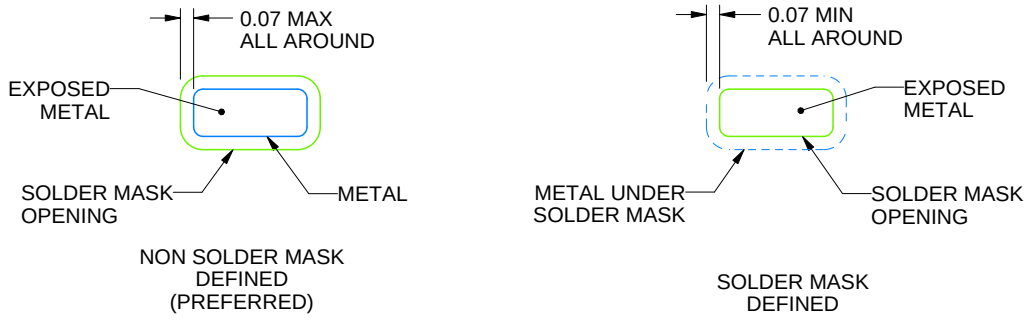
DEE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

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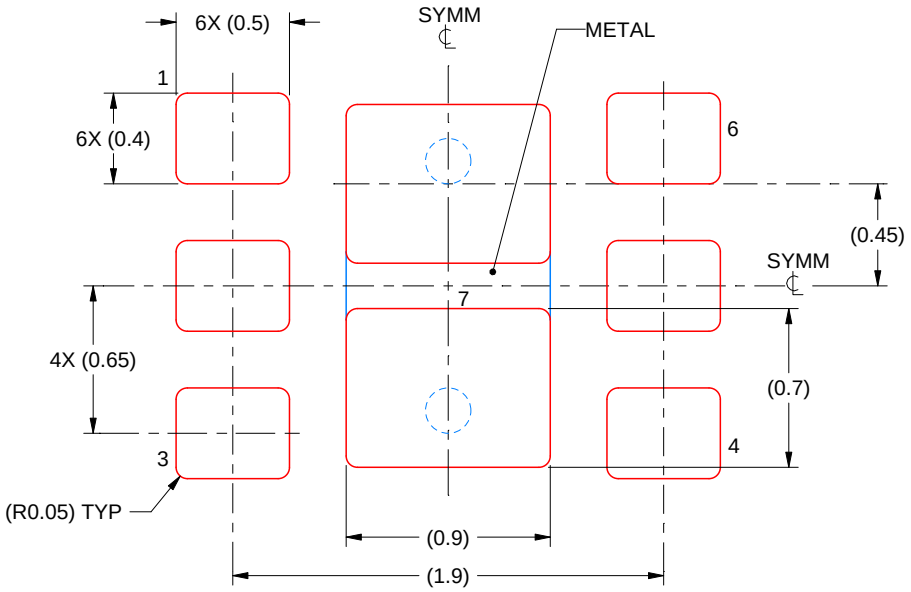

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

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