LMH0302 3-Gbps HD/SD SDI Cable Driver

1 Features
- Supports ST 424 (3G), 292 (HD), and 259 (SD)
- Data Rates up to 2.97 Gbps
- Supports DVB-ASI at 270 Mbps
- 100-Ω Differential Input
- 75-Ω Single-Ended Outputs
- Selectable Slew Rate
- Output Driver Power-Down Control
- Single 3.3-V Supply Operation
- Industrial Temperature Range: −40°C to 85°C
- Typical Power Consumption: 125 mW in SD Mode and 165 mW in HD Mode
- 16-Pin WQFN Package
- Footprint Compatible With the LMH0002SQ
- Replaces the Gennum GS2978

2 Applications
- ST 424, ST 292, ST 344, and ST 259 Serial Digital Interfaces
- Digital Video Routers and Switches
- Distribution Amplifiers

3 Description
The LMH0302 3-Gbps HD/SD SDI cable driver is designed for use in ST 424, ST 292, ST 344, and ST 259 serial digital video applications. The LMH0302 drives 75-Ω transmission lines (Belden 1694A, Belden 8281, or equivalent) at data rates up to 2.97 Gbps.

The LMH0302 provides two selectable slew rates for ST 259 and ST 424 or 292 compliance. The output driver may be powered down through the output driver enable pin.

The LMH0302 is powered from a single 3.3-V supply. Power consumption is typically 125 mW in SD mode and 165 mW in HD mode. The LMH0302 is available in a 16-pin WQFN package.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH0302</td>
<td>WQFN (16)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

![Typical Application Diagram](image)
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................ 1
3 Description .............................................................. 1
4 Revision History ...................................................... 2
5 Pin Configuration and Functions ................................. 3
6 Specifications .......................................................... 4
   6.1 Absolute Maximum Ratings ................................. 4
   6.2 ESD Ratings ..................................................... 4
   6.3 Recommended Operating Conditions ....................... 4
   6.4 Thermal Information .......................................... 4
   6.5 Electrical Characteristics – DC ............................ 4
   6.6 Electrical Characteristics – AC .............................. 5
   6.7 Typical Characteristics ........................................ 5
7 Detailed Description ................................................ 6
   7.1 Overview ........................................................ 6
   7.2 Functional Block Diagram .................................... 6
8 Application and Implementation ................................ 8
   8.1 Application Information ....................................... 8
   8.2 Typical Application .......................................... 8
9 Power Supply Recommendations .............................. 10
10 Layout ................................................................. 10
   10.1 Layout Guidelines ............................................ 10
   10.2 Layout Example .............................................. 11
11 Device and Documentation Support ......................... 12
   11.1 Community Resources ...................................... 12
   11.2 Trademarks .................................................. 12
   11.3 Electrostatic Discharge Caution ......................... 12
   11.4 Glossary ...................................................... 12
12 Mechanical, Packaging, and Orderable Information ....... 12

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H .............................. 1
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section

Changes from Revision F (April 2013) to Revision G .............................. 1
• Changed layout of National Data Sheet to TI format
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENABLE</td>
<td>6</td>
<td>Output driver enable. When low, the SDO/SDO output driver is powered off. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off.</td>
</tr>
<tr>
<td>EP</td>
<td>—</td>
<td>EP is the exposed pad at the bottom of the WQFN package. The exposed pad must be connected to the ground plane through a via array. See Figure 6 for details.</td>
</tr>
<tr>
<td>NC</td>
<td>5, 7, 8, 13, 14, 15, 16</td>
<td>No connect. Not bonded internally.</td>
</tr>
<tr>
<td>RREF</td>
<td>4</td>
<td>Output driver level control. Connect a resistor to VCC to set output voltage swing.</td>
</tr>
<tr>
<td>SD/HD</td>
<td>10</td>
<td>Output slew rate control. Output rise/fall time complies with ST 424 or 292 when low and ST 259 when high.</td>
</tr>
<tr>
<td>SDI</td>
<td>1</td>
<td>Serial data true input.</td>
</tr>
<tr>
<td>SDI</td>
<td>2</td>
<td>Serial data complement input.</td>
</tr>
<tr>
<td>SDO</td>
<td>12</td>
<td>Serial data true output.</td>
</tr>
<tr>
<td>SDO</td>
<td>11</td>
<td>Serial data complement output.</td>
</tr>
<tr>
<td>VCC</td>
<td>9</td>
<td>Positive power supply (3.3 V).</td>
</tr>
<tr>
<td>VEE</td>
<td>3</td>
<td>Negative power supply (ground).</td>
</tr>
</tbody>
</table>

(1)  G = Ground, I = Input, O = Output, and P = Power
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>–0.5</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage (all inputs)</td>
<td>–0.3</td>
<td>(V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Output current</td>
<td>28</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Lead temperature, soldering (4 s)</td>
<td>260</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction temperature, (T_J)</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±4500</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Machine model (MM)</td>
<td>±250</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ((V_{CC} – V_{EE}))</td>
<td>3.13</td>
<td>3.3</td>
<td>3.46</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature</td>
<td>100</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating free air temperature, (T_A)</td>
<td>–40</td>
<td>25</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LMH0302</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>47.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>47.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>25.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>1.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>25.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>14.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics – DC

Over supply voltage and operating free-air temperature range (unless otherwise noted) \(^{(1)}\)(2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CMIN})</td>
<td>Input common mode voltage</td>
<td>SDI, SDI</td>
<td>1.1 + (V_{SDI}/2)</td>
<td>(V_{CC} – V_{SDI}/2)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{SDI})</td>
<td>Input voltage swing</td>
<td>Differential, SDI, SDI</td>
<td>100</td>
<td>2200</td>
<td>mV_{p-p}</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to \(V_{EE} = 0\) V.
\(^{(2)}\) Typical values are stated for \(V_{CC} = 3.3\) V and \(T_A = 25\)°C.
Electrical Characteristics – DC (continued)

Over supply voltage and operating free-air temperature range (unless otherwise noted) \(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CMOUT})</td>
<td>Output common mode voltage</td>
<td>SDI, SDO</td>
<td>(V_{CC} - V_{SDO})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{SDD})</td>
<td>Output voltage swing</td>
<td>Single-ended, 75-Ω load, (R_{REF} = 750 , \Omega, 1%)</td>
<td>720</td>
<td>800</td>
<td>880</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input voltage high level</td>
<td>SD/HD, ENABLE</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input voltage low level</td>
<td>SD/HD, ENABLE</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Supply current</td>
<td>SD/HD = 0, SDO/SDO enabled</td>
<td>50</td>
<td>59</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SD/HD = 0, SDO/SDO disabled</td>
<td>26</td>
<td>33</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SD/HD = 1, SDO/SDO enabled</td>
<td>38</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SD/HD = 1, SDO/SDO disabled</td>
<td>15</td>
<td>22</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Typical values are stated for \(V_{CC} = 3.3 \, V\) and \(T_A = 25^\circ C\).

\(^{(2)}\) Specification is ensured by characterization.

\(^{(3)}\) Output return loss is dependent on board design. The LMH0302 meets this specification on the SD302 evaluation board.

6.6 Electrical Characteristics – AC

Over supply voltage and operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(DR_{SDI})</td>
<td>Input data rate</td>
<td>SDI, SDI</td>
<td>2970</td>
<td>Mbps</td>
<td></td>
</tr>
<tr>
<td>(T_{JR})</td>
<td>Additive jitter</td>
<td>2.97 Gbps, SDO, SDO</td>
<td>20</td>
<td>psp</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.485 Gbps, SDO, SDO</td>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>270 Mbps, SDO, SDO</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{r,tf})</td>
<td>Output rise time, fall time</td>
<td>(SD/HD = 0, 20% - 80%, SDO, SDO)</td>
<td>90</td>
<td>130</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SD/HD = 1, 20% - 80%, SDO, SDO)</td>
<td>400</td>
<td>800</td>
<td></td>
</tr>
<tr>
<td>(T_{MATCH})</td>
<td>Mismatch in rise time, fall time</td>
<td>(SD/HD = 0, SDO, SDO)</td>
<td>30</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SD/HD = 1, SDO, SDO)</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{DCD})</td>
<td>Duty cycle distortion</td>
<td>(SD/HD = 0, 2.97 Gbps, SDO, SDO)</td>
<td>27</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SD/HD = 0, 1.485 Gbps, SDO, SDO)</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SD/HD = 1, SDO, SDO)</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{OS})</td>
<td>Output overshoot</td>
<td>(SD/HD = 0, SDO, SDO)</td>
<td>10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SD/HD = 1, SDO, SDO)</td>
<td>8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(RL_{SDD})</td>
<td>Output return loss</td>
<td>5 MHz to 1.5 GHz, SDO, SDO</td>
<td>15</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5 GHz to 3.0 GHz, SDO, SDO</td>
<td>10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Typical values are stated for \(V_{CC} = 3.3 \, V\) and \(T_A = 25^\circ C\).

\(^{(2)}\) Specification is ensured by characterization.

\(^{(3)}\) Output return loss is dependent on board design. The LMH0302 meets this specification on the SD302 evaluation board.

6.7 Typical Characteristics

Typical device characteristics at \(T_A = 25^\circ C\) and \(V_{CC} = 3.3 \, V\) (unless otherwise noted)

---

Figure 1. SDO PRBS10 at 2.97 Gbps

Figure 2. SDO PRBS10 at 1.485 Gbps
7 Detailed Description

7.1 Overview
The LMH0302 ST 424, ST292, ST259 serial digital cable driver is a monolithic, high-speed cable driver designed for use in serial digital video data transmission applications. The LMH0302 drives 75-Ω transmission lines (Belden 8281, 1694A, Canare L-5CFB, or equivalent) at data rates up to 2.97 Gbps.

The LMH0302 provides two selectable slew rates for ST 259 and ST 292/424 compliance. The output voltage swing is adjustable through a single external resistor (R_{REF}).

The LMH0302 is powered from a single 3.3-V supply. Power consumption is typically 125 mW in SD mode and 165 mW in HD mode. The LMH0302 is available in a 16-pin WQFN package.

7.2 Functional Block Diagram

7.3 Feature Description
The LMH0302 data path consists of several key blocks:

- Input interfacing
- Output interfacing
- Output slew rate control
- Output enable

7.3.1 Input Interfacing
The LMH0302 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range.

7.3.2 Output Interfacing
The LMH0302 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75-Ω AC-coupled coaxial cable with an R_{REF} resistor of 750 Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}.
Feature Description (continued)

The $R_{\text{REF}}$ resistor must be placed as close as possible to the $R_{\text{REF}}$ pin. In addition, the copper in the plane layers below the $R_{\text{REF}}$ network must be removed to minimize parasitic capacitance.

7.3.3 Output Slew Rate Control

The LMH0302 output rise and fall times are selectable for either ST 259, ST 424, or 292 compliance through the SD/HD pin. For slower rise and fall times, or ST 259 compliance, SD/HD is set high. For faster rise and fall times, ST 424 and ST 292 compliance, SD/HD is set low.

7.3.4 Output Enable

The SDO/SDO output driver are enabled or disabled with the ENABLE pin. When set low, the output driver is powered off. ENABLE has an internal pullup.

7.4 Device Functional Modes

The LMH0302 features are programmed using pin mode only.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LMH0302 is a single-channel SDI cable driver that supports different application spaces. The following sections describe the typical use cases and common implementation practices.

8.1.1 General Guidance for All Applications
The SMPTE specifications define the use of AC-coupling capacitors for transporting uncompressed serial data streams with heavy low-frequency content. This specification requires the use of a 4.7-µF AC-coupling capacitor to avoid low frequency DC wander. The 75-Ω signal is also required to meet certain rise and fall timing to facilitate highest eye opening for the receiving device.

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, 3 Gbps, and higher data rates over coaxial cables. One of the requirements is meeting the required return loss. This requirement specifies how closely the port resembles 75-Ω impedance across a specified frequency band. Output return loss is dependent on board design. The LMH0302 supports these requirements.

8.2 Typical Application

Figure 3. Application Circuit

Copyright © 2016, Texas Instruments Incorporated
Typical Application (continued)

8.2.1 Design Requirements

For the LMH0302 design example, Table 1 lists the design parameters.

Table 1. LMH0302 Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>REQUIREMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input termination</td>
<td>Required; 49.9 Ω are recommended (see Figure 3).</td>
</tr>
<tr>
<td>Output AC-coupling capacitors</td>
<td>Required; both SDO and SDO require AC-coupling capacitors. SDO AC-coupling capacitors are expected to be 4.7 µF to comply with SMPTE wander requirement.</td>
</tr>
<tr>
<td>DC power supply coupling capacitors</td>
<td>To minimize power supply noise, place 0.1-µF capacitor as close to the device V_CC pin as possible.</td>
</tr>
<tr>
<td>Distance from device to BNC</td>
<td>Keep this distance as short as possible.</td>
</tr>
<tr>
<td>High speed SDI and SDI trace impedance</td>
<td>Design differential trace impedance of SDI and SDI with 100 Ω.</td>
</tr>
<tr>
<td>High speed SDO and SDO trace impedance</td>
<td>Single-ended trace impedance for SDO and SDO with 75 Ω.</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

The following design procedure is recommended:

1. Select a suitable power supply voltage for the LMH0302. It can be powered from a single 3.3-V supply.
2. Check that the power supply meets the DC requirements in Electrical Characteristics – DC.
3. Select the proper pull-high or pull-low for SD/HD to set the slew rate.
4. Select proper pull-high or pull-low for ENABLE to enable or disable the output driver.
5. Choose a high-quality 75-Ω BNC that is capable to support 2.97-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended BNC footprint for meeting SMPTE return loss requirements.
6. Choose small 0402 surface-mount ceramic capacitors for the AC-coupling and bypass capacitors.
7. Use proper footprint for BNC and AC-coupling capacitors. Anti-pads are commonly used in power and ground planes under these landing pads to achieve optimum return loss.

8.2.3 Application Curves

![Figure 4. SDO PRBS10 at 270 Mbps](image1)

![Figure 5. SDO Amplitude vs R_REF Resistance](image2)
9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the recommended operating conditions (see Recommended Operating Conditions).
2. The maximum current draw for the LMH0302 is provided in Electrical Characteristics – DC. This figure can be used to calculate the maximum current the supply must provide.
3. The LMH0302 does not require any special power supply filtering, provided the recommended operating conditions are met. Only standard supply coupling is required.

10 Layout

10.1 Layout Guidelines

TI recommends the following layout guidelines for the LMH0302:

1. The $R_{REF}$ 1% tolerance resistor must be placed as close as possible to the $R_{REF}$ pin. In addition, the copper in the plane layers below the $R_{REF}$ network must be removed to minimize parasitic capacitance.
2. Choose a suitable board stackup that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer 2 ground plane reference for the 100-Ω differential traces and a second ground plane at Layer 3 reference for the 75-Ω single-ended traces.
3. Use single-ended uncoupled trace designed with 75-Ω impedance for signal routing to SDO and $\overline{SDO}$. The trace width is typically 8-10 mil reference to a ground plane at Layer 3.
4. Use coupled differential traces with 100-Ω impedance for signal routing to SDI and $\overline{SDI}$. They are usually 5-mil to 8-mil trace width reference to a ground plane at Layer 2.
5. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-μF AC-coupling capacitor, return loss network, and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stackup and can be determined by a 3-dimension electromagnetic simulation tool.
6. Use a well-designed BNC footprint to ensure the BNC’s signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
7. Keep trace length short between the BNC and SDO. The trace routing for SDO and $\overline{SDO}$ must be symmetrical, approximately equal lengths, and equal loading.
8. The exposed pad EP of the package must be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flow into the plated-through holes during the board manufacturing process.
9. Connect each supply pin ($V_{CC}$ and $V_{EE}$) to the power or ground planes with a short via. The via is usually placed tangent to the landing pads of the supply pins with the shortest trace possible.
10. Power-supply bypass capacitors must be placed close to the supply pins.
10.2 Layout Example

Figure 6 shows an example of proper layout requirements for the LMH0302.

![Diagram of LMH0302 High-Speed Traces Layout Example](image)

**Figure 6.** LMH0302 High-Speed Traces Layout Example
11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH0302SQ/NOPB</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>L0302</td>
<td></td>
</tr>
<tr>
<td>LMH0302SQE/NOPB</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>L0302</td>
<td></td>
</tr>
<tr>
<td>LMH0302SQX/NOPB</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>4500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>L0302</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **Reel Diameter**

#### TAPE DIMENSIONS

- **A0** Dimension designed to accommodate the component width
- **B0** Dimension designed to accommodate the component length
- **K0** Dimension designed to accommodate the component thickness
- **W** Overall width of the carrier tape
- **P1** Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

---

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH0302SQ/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.3</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LMH0302SQE/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>178.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.3</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LMH0302SQX/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>4500</td>
<td>330.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.3</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

---

www.ti.com 6-Nov-2021
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH0302SQ/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>1000</td>
<td>208.0</td>
<td>191.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMH0302SQE/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>208.0</td>
<td>191.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMH0302SQX/NOPB</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>4500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated