**FEATURES**

- $V_s = \pm 5V$, $T_A = 25^\circ C$, $R_F = 1k\Omega$, $R_G = 174\Omega$, $R_L = 100\Omega$, $A_V = A_{V(MAX)} = 10$ Typical Values Unless Specified.
- -3dB BW: 130MHz
- Gain Control BW: 100MHz
- Adjustment Range (Typical Over Temp): 70dB
- Gain Matching (Limit): $\pm 0.6$dB
- Slew Rate: 1800V/µs
- Supply Current (No Load): 27mA
- Linear Output Current: $\pm 75$mA
- Output Voltage ($R_L = 100\Omega$, $V_O = 2V_{PP}$): $-53$dBc
- Replacement for CLC520

**DESCRIPTION**

The **LMH™6502** is a wideband DC coupled differential input voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is more than 70dB for up to 10MHz.

Maximum gain is set by external components and the gain can be reduced all the way to cut-off. Power consumption is 300mW with a speed of 130MHz. Output referred DC offset voltage is less than 350mV over the entire gain control voltage range. Device-to-device Gain matching is within $\pm 0.6$dB at maximum gain. Furthermore, gain at any $V_G$ is tested and the tolerance is ensured. The output current feedback Op Amp allows high frequency large signals (Slew Rate = 1800V/µs) and can also drive heavy load current (75mA). Differential inputs allow common mode rejection in low level amplification or in applications where signals are carried over relatively long wires. For single ended operation, the unused input can easily be tied to ground (or to a virtual half-supply in single supply application). Inverting or non-inverting gains could be obtained by choosing one input polarity or the other.

To provide ease of use when working with a single supply, $V_G$ range is set to be from 0V to $+2V$ relative to pin 11 potential (ground pin). In single supply operation, this ground pin is tied to a “virtual” half supply.

**APPLICATIONS**

- Variable Attenuator
- AGC
- Voltage Controller Filter
- Video Imaging Processing

LMH6502 gain control is linear in dB for a large portion of the total gain control range. This makes the device suitable for AGC circuits among other applications. For linear gain control applications, see the LMH6503 datasheet. The LMH6502 is available in the SOIC and TSSOP package.
**Typical Application**

![Gain vs. Vg for Various Temperature](image)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>ESD Tolerance(3)</th>
<th>Human Body</th>
<th>2KV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Machine Model</td>
<td></td>
<td>200V</td>
</tr>
<tr>
<td>Input Current</td>
<td>±10mA</td>
<td></td>
</tr>
<tr>
<td>V_in Differential</td>
<td>±(V^+ - V^-)</td>
<td></td>
</tr>
<tr>
<td>Output Current</td>
<td>120mA(4)</td>
<td></td>
</tr>
<tr>
<td>Supply Voltages (V^+ - V^-)</td>
<td>12.6V</td>
<td></td>
</tr>
<tr>
<td>Voltage at Input/Output pins</td>
<td>V^+ +0.8V, V^- -0.8V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
<td></td>
</tr>
<tr>
<td>Soldering Information:</td>
<td>Infrared or Convection (20 sec)</td>
<td>235°C</td>
</tr>
<tr>
<td>Wave Soldering (10 sec)</td>
<td>260°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

(4) The maximum output current (I_OUT) is determined by device power dissipation limitations or value specified, whichever is lower.

**Operating Ratings**

| Supply Voltages (V^+ - V^-) | 5V to 12V |
| Temperature Range           | -40°C to +85°C |

<table>
<thead>
<tr>
<th>Thermal Resistance:</th>
<th>(θJC)</th>
<th>45°C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-Pin SOIC</td>
<td>(θJA)</td>
<td>138°C/W</td>
</tr>
<tr>
<td>(θJC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14-Pin TSSOP</td>
<td>(θJA)</td>
<td>51°C/W</td>
</tr>
<tr>
<td>(θJC)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specific specifications, see the Electrical Characteristics tables.
### Electrical Characteristics (1)

Unless otherwise specified, all limits specified for $T_J = 25^\circ C$, $V_S = \pm 5V$, $A_{V(MAX)} = 10$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, $V_{IN\_DIFF} = \pm 0.1V$, $R_L = 100\Omega$, $V_G = +2V$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(2)</th>
<th>Typ(2)</th>
<th>Max(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Domain Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>-3dB Bandwidth</td>
<td>$V_{OUT} &lt; 0.5PP$</td>
<td>130</td>
<td></td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{OUT} &lt; 0.5PP, A_{V(MAX)} = 100$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GF</td>
<td>Gain Flatness</td>
<td>$V_{OUT} &lt; 0.5VPP$</td>
<td>30</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0.6V \leq V_G \leq 2V, \pm 0.3dB$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Att Range</td>
<td>Flat Band (Relative to Max Gain)</td>
<td>$\pm 0.2dB, f &lt; 30MHz$</td>
<td>16</td>
<td></td>
<td>7.5</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Attenuation Range</td>
<td>$\pm 0.1dB, f &lt; 30MHz$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW Control</td>
<td>Gain control Bandwidth</td>
<td>$V_G = 1V$</td>
<td>100</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>PL</td>
<td>Linear Phase Deviation</td>
<td>DC to 60MHz</td>
<td>1.5</td>
<td></td>
<td></td>
<td>deg</td>
</tr>
<tr>
<td>G Delay</td>
<td>Group Delay</td>
<td>DC to 130MHz</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CT (dB)</td>
<td>Feed-through</td>
<td>$V_G = 0V, 30MHz$ (Output Referred)</td>
<td>-47</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>GR</td>
<td>Gain Adjustment Range</td>
<td>$f &lt; 10MHz$</td>
<td>72</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f &lt; 30MHz$</td>
<td>67</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Time Domain Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Rise and Fall Time</td>
<td>0.5V Step</td>
<td>2.2</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>OS %</td>
<td>Overshoot</td>
<td>0.5V Step</td>
<td>10</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>4V Step</td>
<td>1800</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>ΔG Rate</td>
<td>Gain Change Rate</td>
<td>$V_{IN} = 0.3V, 10%-90%$ of Final Output</td>
<td>4.8</td>
<td></td>
<td></td>
<td>dB/ns</td>
</tr>
<tr>
<td><strong>Distortion &amp; Noise Performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD2</td>
<td>2nd Harmonic Distortion</td>
<td>$2VPP, 20MHz$</td>
<td>-55</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>HD3</td>
<td>3rd Harmonic Distortion</td>
<td>$2VPP, 20MHz$</td>
<td>-57</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>$2VPP, 20MHz$</td>
<td>-53</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>En tot</td>
<td>Total Equivalent Input Noise</td>
<td>1MHz to 150MHz</td>
<td>7.7</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>I$_N$</td>
<td>Input Noise Current</td>
<td>1MHz to 150MHz</td>
<td>2.4</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>DG</td>
<td>Differential Gain</td>
<td>$f = 4.43MHz$, $R_L = 150\Omega$, Neg. Sync</td>
<td>0.34</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

(2) Typical values represent the most likely parametric norm. Bold numbers refer to over temperature limits.

(3) Flat Band Attenuation (Relative to Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either $\pm 0.2dB$ or $\pm 0.1dB$) relative to $A_{VMAX}$ gain. For example, for $f < 30MHz$, here are the Flat Band Attenuation ranges:
- $\pm 0.2dB$: 20dB down to 4dB = 16dB range
- $\pm 0.1dB$: 20dB down to 12.5 dB = 7.5dB range

(4) Gain Control Frequency Response Schematic:
### Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for $T_J = 25^\circ C$, $V_S = \pm 5V$, $A_{IN(MAX)} = 10$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, $V_{IN\_DIFF} = \pm 0.1V$, $R_L = 100\Omega$, $V_G = +2V$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(2)</th>
<th>Typ(2)</th>
<th>Max(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP</td>
<td>Differential Phase</td>
<td>$f = 4.43MHz$, $R_L = 150\Omega$, Neg. Sync</td>
<td>0.10</td>
<td></td>
<td></td>
<td>deg</td>
</tr>
</tbody>
</table>

### DC & Miscellaneous Performance

#### GACCU
Gain Accuracy (See Application Information)

- $V_G = 2.0V$
- $1V < V_G < 2V$: $+0.6/–0.3$ dB
- $1 < V_G < 2V$: $+2.8/–3.9$ dB

#### G Match
Gain Matching (See Application Information)

- $V_G = 2.0V$
- $1 < V_G < 2V$: $±0.6$ dB

#### K
Gain Multiplier (See Application Information)

- $V_G = 2.0V$

#### $V_{CM}$
Input Voltage Range

- Pin 3 & 6 Common Mode, $|CMRR| > 55dB$ (5)
- $±2.0/±2.2$ V

#### $V_{IN\_DIFF}$
Differential Input Voltage Between pins 3 & 6

- $±0.3/±0.39$ V
- $±0.12$ V

#### $I_{RG\_MAX}$
$R_G$ Current

- Pins 4 & 5: $±1.70/±1.56$ mA
- $±2.22$ mA

#### $I_{BIAS}$
Bias Current

- Pins 3 & 6: $2.5/5$ µA

#### $TC\_I_{BIAS}$
Bias Current Drift

- Pin 3 & 6: $100$ nA/°C

#### $I_{OFF}$
Offset Current

- Pin 3 & 6: $0.01/2.0$ µA
- $3.6$ µA

#### $TC\_I_{OFF}$
Offset Current Drift

- See (7)
- $5$ nA/°C

#### $R_N$
Input Resistance

- Pin 3 & 6: $750$ kΩ

#### $C_N$
Input Capacitance

- Pin 3 & 6: $5$ pF

#### $I_{VG}$
$V_G$ Bias Current

- Pin 2, $V_G = 0V$: $–300$ µA

#### $TC\_I_{VG}$
$V_G$ Bias Drift

- Pin 2: $20$ nA/°C

#### $R_{VG}$
$V_G$ Input Resistance

- Pin 2: $10$ kΩ

#### $C_{VG}$
$V_G$ Input Capacitance

- Pin 2: $1.3$ pF

#### $V_{OUT}$
Output Voltage Range

- $R_L = 100\Omega$: $±3.00/±2.95$ V
- $R_L = Open$: $±3.95/±3.82$ V

#### $R_{OUT}$
Output Impedance

- DC: $0.1$ Ω

#### $I_{OUT}$
Output Current

- $V_{OUT} = ±4V$ from Rails: $±80/±75$ mA
- $±90$ mA

#### $V_{D\_OFFSET}$
Output Offset Voltage

- $0V < V_G < 2V$: $±80/±300$ mV
- $±380$ mV

#### +PSRR
+Power Supply Rejection Ratio (6)

- Input Referred, 1V change, $V_G = 2.2V$: $–69/–47$ dB
- $–45$ dB

#### –PSRR
–Power Supply Rejection Ratio (6)

- Input Referred, 1V change, $V_G = 2.2V$: $–58/–41$ dB
- $–40$ dB

#### CMRR
Common Mode Rejection Ratio (5)

- Input Referred, $V_G = 2V$,
  $–1.8V < V_{CM} < 1.8V$: $–72$ dB

#### $I_S$
Supply Current

- No Load: $27/38/41$ mA
- $V_G = ±2.5V$, $R_L = Open$: $9.3/16/19$ mA

(5) CMRR definition: $|\Delta V_{OUT}/\Delta V_{CM}| / A_V$ with 0.1V differential input voltage.

(6) Positive current corresponds to current flowing in the device.

(7) Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change.

(8) +PSRR definition: $|\Delta V_{OUT}/|\Delta V_{IN}| / A_V$, –PSRR definition: $|\Delta V_{OUT}/\Delta V_{CM}| / A_V$ with 0.1V differential input voltage.
Connection Diagram

14-Pin SOIC/TSSOP (Top View)
See Package Numbers D (R-PDSO-G14) and PW (R-PDSO-G14)
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, 25°C, $V_G = V_{G\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in 50Ω, $R_L = 100\Omega$, Typical values, results referred to device output.

**Figure 3.** Small Signal Frequency for Various $V_G$

**Figure 4.** Large Signal Frequency for Various $V_G$

**Figure 5.** Frequency Response Over Temperature ($A_{V\text{MAX}} = 10$)

**Figure 6.** Frequency Response for Various $V_G$ ($A_{V\text{MAX}} = 10$)

**Figure 7.** Frequency Response for Various $V_G$ ($A_{V\text{MAX}} = 10$) ($\pm 2.5V$)

**Figure 8.** Small Signal Frequency Response for Various $A_{V\text{MAX}}$
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_S = \pm 5V$, 25°C, $V_G = V_{G\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in 50Ω, $R_L = 100\Omega$, Typical values, results referred to device output.

**Large Signal Frequency Response for Various $A_{V\text{MAX}}$**

**Frequency Response for Various $V_G$ ($A_{V\text{MAX}} = 105$)**

**Input Bias Current vs. $V_S$**

---

Figure 9.

Figure 10.

Figure 11.

Figure 12.

Figure 13.

Figure 14.
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_S = \pm 5V, \) \( 25^\circ C, V_G = V_{G\text{MAX}}, V_{CM} = 0V, R_F = 1k\Omega, R_G = 174\Omega, \) both inputs terminated in 50\( \Omega, R_L = 100\Omega, \) Typical values, results referred to device output.

\[ A_{V\text{MAX}} \text{ vs. } V_{CM} \]

Figure 15.

\[ A_{V\text{MAX}} \text{ vs. } V_{CM} \]

Figure 16.

\[ \text{PSRR } \pm 5V \]

Figure 17.

\[ \text{PSRR } \pm 2.5V \]

Figure 18.

\[ \text{CMRR } \pm 5V \]

Figure 19.

\[ \text{CMRR } \pm 2.5V \]

Figure 20.
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_S = \pm 5V, 25^\circ C, V_G = V_{G\text{MAX}}, V_{CM} = 0V, R_F = 1k\Omega, R_G = 174\Omega \), both inputs terminated in 50\( \Omega \), \( R_L = 100\Omega \), Typical values, results referred to device output.

\[ A_{V\text{MAX}} \text{ vs. Supply Voltage} \]

\[ \text{Supply Current vs. } V_{CM} \]

\[ \text{Output Offset Voltage vs. } V_{CM} \text{ (Typical Unit #1)} \]

\[ \text{Output Offset Voltage vs. } V_{CM} \text{ (Typical Unit #2)} \]

\[ \text{Output Offset Voltage vs. } V_{CM} \text{ (Typical Unit #3)} \]
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$. Typical values, results referred to device output.

**Feed through Isolation**

[Graph showing gain and phase characteristics]

---

**Gain Flatness and Linear Phase Deviation vs. $V_G$**

[Graph showing gain and phase deviation]

---

**Group Delay vs. Frequency**

[Graph showing group delay]

---

**K Factor vs. $R_G$**

[Graph showing K factor variation]

---

**Gain vs. $V_G$ Including Limits**

[Graph showing gain variation]

---

(1) Flat Band Attenuation (Relative to Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB) relative to $A_{V\text{MAX}}$ gain. For example, for $f < 30MHz$, here are the Flat Band Attenuation ranges:

- ±0.2dB: 20dB down to 4dB = 16dB range
- ±0.1dB: 20dB down to 12.5 dB = 7.5dB range
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_S = \pm 5V, 25^\circ C, V_G = V_{G\text{MAX}}, V_{CM} = 0V, R_F = 1k\Omega, R_G = 174\Omega, \) both inputs terminated in 50\( \Omega \), \( R_L = 100\Omega \), Typical values, results referred to device output.

![BW vs. \( R_F \)](image1)

![Gain vs. \( V_G (\pm 5V) \)](image2)

![Output Offset Voltage vs. \( V_G \) (Typical Unit #1)](image3)

![Output Offset Voltage vs. \( V_G \) (Typical Unit #2)](image4)

![Output Offset Voltage vs. \( V_G \) (Typical Unit #3)](image5)
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{GMAX}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$. Typical values, results referred to device output.

Output Offset Voltage vs. $\pm V_S$ for various $V_G$

(Typical Units# 1)

![Graph](image1)

**Figure 39.**

Output Offset Voltage vs. $\pm V_S$ for various $V_G$

(Typical Units# 2)

![Graph](image2)

**Figure 40.**

Output Offset Voltage vs. $\pm V_S$ for various $V_G$

(Typical Units# 3)

![Graph](image3)

**Figure 41.**

Noise vs. Frequency ($A_{VMAX} = 2$)

![Graph](image4)

**Figure 42.**

Noise vs. Frequency ($A_{VMAX} = 10$)

![Graph](image5)

**Figure 43.**

Noise vs. Frequency ($A_{VMAX} = 105$)

![Graph](image6)

**Figure 44.**
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_S = \pm 5V, \) 25°C, \( V_G = V_{\text{GMAX}}, V_{\text{CM}} = 0V, \) \( R_F = 1k\Omega, R_G = 174\Omega, \) both inputs terminated in 50Ω, \( R_L = 100\Omega, \) Typical values, results referred to device output.

![Graph](Figure 45.)

-1dB Compression

-10 -5 0 5 10 15 20
0 10 20 30 40 50 60 70 80 90 100
<table>
<thead>
<tr>
<th>THD (dBc)</th>
</tr>
</thead>
</table>
P OUT (dBm)
20MHz
1MHz

![Graph](Figure 46.)

Output Voltage vs. Output Current

0 20 40 60 80 100
0 0.5 1 1.5 2 2.5 3 3.5 4
V OUT FROM SUPPLY (V)
I OUT (mA)
SOURCE
SINK
V IN_DIFF = ±0.5V

![Graph](Figure 47.)

HD2 & HD3 vs. P OUT

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
</table>
|0|1|2|3
|1|2|3|4
|2|3|4|5
|3|4|5|6
|4|5|6|7
|5|6|7|8
|6|7|8|9
|7|8|9|10

![Graph](Figure 48.)

THD vs. P OUT

-10 -5 0 5 10 15 20
0 10 20 30 40 50 60 70 80 90 100
<table>
<thead>
<tr>
<th>THD (dB)</th>
</tr>
</thead>
</table>
P OUT (dBm)
HD2, 20MHz
HD3, 20MHz
HD2, 1MHz
HD3, 1MHz

![Graph](Figure 49.)

THD vs. P OUT

-10 -5 0 5 10 15 20
0 10 20 30 40 50 60 70 80 90 100
<table>
<thead>
<tr>
<th>THD (dB)</th>
</tr>
</thead>
</table>
P OUT (dBm)
1MHz
20MHz
V G = V GMAX = 2.0V

![Graph](Figure 50.)

HD2 & HD3 vs. V G

0 0.5 1 1.5 2
0.6 0.8 1 1.2 1.4 1.6 1.8 2
<table>
<thead>
<tr>
<th>HD2 OR HD3 (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V G (V)</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G_{\text{MAX}}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output.

**THD vs. $V_G$**

![THD vs. $V_G$](image)

Figure 51.

**THD vs. $V_G$**

![THD vs. $V_G$](image)

Figure 52.

**$V_G$ Bias Current vs. $V_G$**

![$V_G$ Bias Current vs. $V_G$](image)

Figure 53.

**Step Response Plot**

![Step Response Plot](image)

Figure 54.

**Step Response Plot**

![Step Response Plot](image)

Figure 55.

**Gain vs. $V_G$ Step**

![Gain vs. $V_G$ Step](image)

Figure 56.
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_S = \pm 5\, \text{V}, \, 25^\circ\, \text{C}, \, V_G = V_{G\text{MAX}}, \, V_{CM} = 0\, \text{V}, \, R_F = 1\, \text{k}\, \Omega, \, R_G = 174\, \Omega, \) both inputs terminated in 50\, \Omega, \( R_L = 100\, \Omega, \) Typical values, results referred to device output.

Feedthrough from \( V_G \)

Figure 57.
**THEORY OF OPERATION**

A simplified schematic is shown in Figure 58. $+V_{IN}$ and $-V_{IN}$ are buffered with closed loop voltage followers inducing a signal current in Rg proportional to $(+V_{IN}) - (-V_{IN})$, the differential input voltage. This current controls a current source which supplies two well-matched transistors, Q1 and Q2.

The current flowing through Q2 is converted to the final output voltage using $R_F$ and the output amplifier, U1. By changing the fraction of the signal current "I" which flows through Q2, the gain is changed. This is done by changing the voltage applied differentially to the bases of Q1 and Q2. For example, with $V_G = 0V$, Q1 conducts heavily and Q2 is off. With none of "I" flowing through $R_F$, the LMH6502's input to output gain is strongly attenuated. With $V_G = +2V$, Q1 is off and the entire signal current flows through Q2 to $R_F$ producing maximum gain. With $V_G$ set to 1V, the bases of Q1 and Q2 are set to approximately the same voltage, Q1 and Q2 have the same collector currents - equal to one half of the signal current "I", thus the gain is approximately one half the maximum gain.

![Figure 58. LMH6502 Block Diagram](image)

**CHOOSING $R_F$ & $R_G$**

Maximum input amplitude and maximum gain are the two key specifications that determine component values in a LMH6502 application.

The output stage op amp is a current-feedback type amplifier optimized for $R_F = 1k\Omega$. $R_G$ can then be computed as:

$$R_G = \frac{R_F \times 1.72}{A_{VMAX} - 3\Omega} \text{ WITH } R_F = 1k\Omega$$

(1)

To determine whether the maximum input amplitude will overdrive the LMH6502, compute:

$$V_{DMAX} = (R_G + 3.0\Omega) \times 1.70mA$$

(2)

the maximum differential input voltage for linear operation. If the maximum input amplitude exceeds the above $V_{DMAX}$ limit, then LMH6502 should either be moved to a location in the signal chain where input amplitudes are reduced, or the LMH6502 gain $A_{VMAX}$ should be reduced or the values for $R_G$ and $R_F$ should be increased. The overall system performance impact is different based on the choice made. If the input amplitude is reduced, recompute the impact on signal-to-noise ratio. If $A_{VMAX}$ is reduced, post LMH6502 amplifier gain, should be increased, or another gain stage added to make up for reduced system gain. To increase $R_G$ and $R_F$, compute the lowest acceptable value for $R_G$:

$$R_G > 590 \times V_{DMAX} - 3\Omega$$

(3)

Operating with $R_G$ larger than this value insures linear operation of the input buffers.

$R_F$ may be computed from selected $R_G$ and $A_{VMAX}$: $R_F$ should be $> 1k\Omega$ for overall best performance, however $R_F < 1k\Omega$ can be implemented if necessary using a loop gain reducing resistor to ground on the inverting summing node of the output amplifier (see application note OA-13 (SNOA366) for details).
ADJUSTING OFFSET

Offset can be broken into two parts; an input-referred term and an output-referred term. The input-referred offset shows up as a variation in output voltage as \( V_G \) is changed. This can be trimmed using the circuit in Figure 59 by placing a low frequency square wave (\( V_{\text{LOW}} = 0V, V_{\text{HIGH}} = 2V \)) into \( V_G \) with \( V_{\text{IN}} = 0V \), the input referred \( V_{\text{OS}} \) term shows up as a small square wave riding a DC value. Adjust \( R_{10} \) to null the \( V_{\text{OS}} \) square wave term to zero. After adjusting the input-referred offset, adjust \( R_{14} \) (with \( V_{\text{IN}} = 0, V_G = 0 \)) until \( V_{\text{OUT}} \) is zero. Finally, for inverting applications \( V_{\text{IN}} \) may be applied to pin 6 and the offset adjustment to pin 3. These steps will minimize the output offset voltage. However, since the offset term itself varies with the gain setting, the correction is not perfect and some residual output offset will remain at in-between \( V_G \)'s. Also, this offset trim does not improve output offset temperature coefficient.

![Figure 59. Nulling the output offset voltage](image)

GAIN ACCURACY

Defined as the actual gain compared against the theoretical gain at a certain \( V_G \) (results expressed in dB).

Theoretical gain is given by:

\[
A(V/V) = K \times \frac{R_F}{R_G} \times \frac{1}{1 + \frac{V_G}{V_C}}
\]

(4)

Where \( K = 1.72 \) (nominal) & \( V_C = 90mV \) @ room temperature.

For a \( V_G \) range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case difference between the "Typical Gain" and the "Theoretical gain". The "Max" value would be the worst case difference between the max/min gain limit and the "Theoretical gain".

GAIN MATCHING

Defined as the limit on gain variation at a certain \( V_G \) (expressed in dB). Specified as "Max" only (no "Typical"). For a \( V_G \) range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case difference between the max/min gain limit and the typical gain.

NOISE

Figure 60 describes the LMH6502’s output-referred spot noise density as a function of frequency with \( A_{\text{VMAX}} = 10V/V \). The plot includes all the noise contributing terms. However, with both inputs terminated in \( 50\Omega \), the input noise contribution is minimal. At \( A_{\text{VMAX}} = 10V/V \), the LMH6502 has a typical input-referred spot noise density (\( e_{\text{in}} \)) of 7.7nV/\( \sqrt{\text{Hz}} \) flat-band. For applications extending well into the flat-band region, the input RMS voltage noise can be determined from the following single-pole model:
\[ V_{\text{RMS}} = e_{\text{in}} \times 1.57 \times (-3\text{dB BANDWIDTH}) \]  

(5)

**Figure 60. Output Referred Voltage Noise vs. Frequency**

**CIRCUIT LAYOUT CONSIDERATIONS & EVALUATION BOARD**

A good high frequency PCB layout including ground plane construction and power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the in input (pin 12); keep node trace area small. Shunt capacitance across the feedback resistor should not be used to compensate for this effect. For best performance at low maximum gains \(A_{\text{VMAX}} < 10\) \(+R_G\) and \(-R_G\) connections should be treated in a similar fashion. Capacitance to ground should be minimized by removing the ground plane from under the body of \(R_G\). Parasitic or load capacitance directly on the output (pin 10) degrades phase margin leading to frequency response peaking.

The LMH6502 is fully stable when driving a 100Ω load. With reduced load (e.g. 1kΩ) there is a possibility of instability at very high frequencies beyond 400MHz especially with a capacitive load. When the LMH6502 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100Ω and 39pF in series tied between the LMH6502 output and ground). \(C_L\) can also be isolated from the output by placing a small resistor in series with the output (pin 10).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Evaluation Board Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6502MA</td>
<td>SOIC</td>
<td>LMH730033</td>
</tr>
</tbody>
</table>
SINGLE SUPPLY OPERATION

It is possible to operate the LMH6502 with a single supply. To do so, tie pin 11 (GND) to a potential about mid point between V+ and V−. Two examples are shown in Figure 61 & Figure 62.

Figure 61. AC Coupled Single Supply VGA

Figure 62. Transformer Coupled Single Supply VGA
OPERATING AT LOWER SUPPLY VOLTAGES

The LMH6502 is rated for operation down to 5V supplies ($V^+ - V^-$). There are some specifications shown for operation at ±2.5V within the data sheet (i.e. Frequency Response, CMRR, PSRR, Gain vs. $V_G$, etc.). Compared to ±5V operation, at lower supplies:

a) $V_G$ range shifts lower.

Here are the approximate expressions for various $V_G$ voltages as a function of $V^+$:

<table>
<thead>
<tr>
<th>$V_G$</th>
<th>Definition</th>
<th>Expression (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{G_{MIN}}$</td>
<td>Gain Cut-off</td>
<td>$0.2 \times V^+ - 1$</td>
</tr>
<tr>
<td>$V_{G_{MID}}$</td>
<td>$A_{V_{MAX}}/2$</td>
<td>$0.2 \times V^+$</td>
</tr>
<tr>
<td>$V_{G_{MAX}}$</td>
<td>$A_{V_{MAX}}$</td>
<td>$0.2 \times V^+ + 1$</td>
</tr>
</tbody>
</table>

b) $V_{G_{LIMIT}}$ (maximum permissible voltage on $V_G$) is reduced. This is due to limitations within the device arising from transistor headroom. Beyond this limit, device performance will be affected (non-destructive). This could reveal itself as premature high frequency response roll-off. With ±2.5V supplies, $V_{G_{LIMIT}}$ is below 1.1V whereas $V_G = 1.5V$ is needed to get maximum gain. This means that operating under these conditions has reduced the maximum permissible voltage on $V_G$ to a level below what is needed to get Max gain. If supply voltages are asymmetrical with $V^+$ being lower, further "pinching" of $V_G$ range could result; for example, with $V^+ = 2V$, and $V^- = -3V$, $V_{G_{LIMIT}} = 0.40V$ which results in maximum gain being 2.5dB less than what would be expected when $V_S$ is higher.

c) "Max_gain" reduces. There is an intrinsic reduction in max gain when the total supply voltage is reduced (see Typical Performance Characteristics plots for Gain vs. $V_G$ ($V_S = \pm 2.5V$). In addition, there is the more drastic mechanism described in "b" above. Beyond $V_{G_{LIMIT}}$, high frequency response is also effected.

Application Circuits

AGC LOOP

Figure 63 shows a typical AGC circuit. The LMH6502 is followed up with a LMH6714 for higher overall gain. The output of the LMH6714 is rectified and fed to an inverting integrator using a LMH6657 (wideband voltage feedback op amp). When the output voltage, $V_{OUT}$, is too large the integrator output voltage ramps down reducing the net gain of the LMH6502 and $V_{OUT}$. If the output voltage is too small, the integrator ramps up increasing the net gain and the output voltage. Actual output level is set with $R_1$. To prevent shifts in DC output voltage with DC changes in input signal level, trim pot $R_2$ is provided. AGC circuits are always limited in the range of input signals over which constant output level can be maintained. In this circuit, we would expect that reasonable AGC action could be maintained for at least 40dB. In practice, rectifier dynamic range limits reduce this slightly.
FREQUENCY SHAPING

Frequency Shaping Frequency shaping and bandwidth extension of the LMH6502 can be accomplished using parallel networks connected across the $R_G$ ports. The network shown in the Figure 64 schematic will effectively extend the LMH6502’s bandwidth.
# REVISION HISTORY

Changes from Revision C (March 2013) to Revision D                                                                                               Page

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>21</td>
</tr>
</tbody>
</table>

Submit Documentation Feedback

Copyright © 2003–2013, Texas Instruments Incorporated

Product Folder Links: LMH6502
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6502MA/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>55</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LMH6502MA</td>
<td>Samples</td>
</tr>
<tr>
<td>LMH6502MAX/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LMH6502MA</td>
<td>Samples</td>
</tr>
<tr>
<td>LMH6502MT/NOPB</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>94</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LMH6502MT</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer**: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1
- Q2
- Q3
- Q4

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6502MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.35</td>
<td>2.3</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------------</td>
<td>--------------</td>
<td>-----------------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
<td>------------</td>
<td>-------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LMH6502MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
**TUBE**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6502MA/NOPB</td>
<td>D</td>
<td>SOIC</td>
<td>14</td>
<td>55</td>
<td>495</td>
<td>8</td>
<td>4064</td>
<td>3.05</td>
</tr>
<tr>
<td>LMH6502MT/NOPB</td>
<td>PW</td>
<td>TSSOP</td>
<td>14</td>
<td>94</td>
<td>495</td>
<td>8</td>
<td>2514.6</td>
<td>4.06</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated