LMH6515 600 MHz, Digital Controlled, Variable Gain Amplifier

Check for Samples: LMH6515

FEATURES

- **Adjustable Gain with a 31 dB Range**
- **Precise 1 dB Gain Steps**
- **Parallel 5-bit Gain Control**
- **On Chip Register Stores Gain Setting**
- **Fully Differential Signal Path**
- **Single Ended to Differential Capable**
- **200Ω Input Impedance**
- **Small Footprint (4 mm x 4 mm) WQFN Package**

APPLICATIONS

- **Cellular Base Stations**
- **IF Sampling Receivers**
- **Instrumentation**
- **Modems**
- **Imaging**
- **Differential Line Receiver**

KEY SPECIFICATIONS

- **600 MHz bandwidth @ 100Ω load**
- **40 dBm OIP3 @ 75 MHz, 200Ω load**
- **20 dB to 30 dB maximum gain**
- **Selectable output impedance of 200Ω or 400Ω**
- **8.3 dB noise figure**
- **5 ns gain step switching time**
- **100 mA supply current**

DESCRIPTION

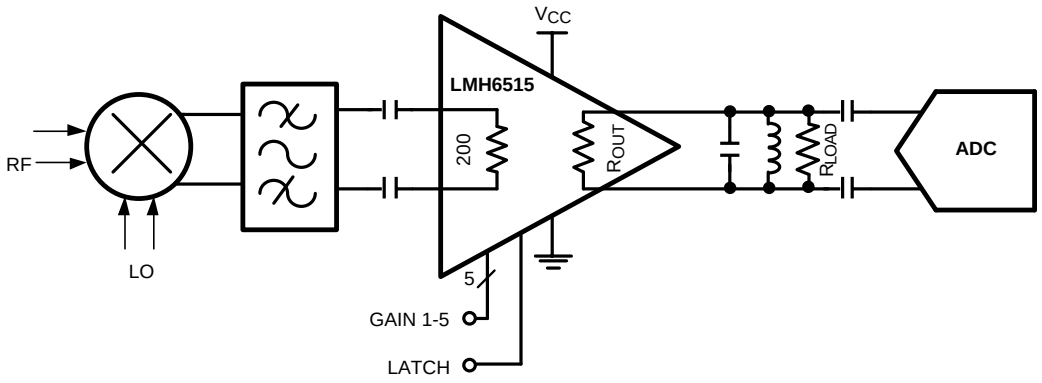
The LMH6515 is a high performance, digitally controlled variable gain amplifier (DVGA). It combines precision gain control with a low noise, ultra-linear, differential amplifier. Typically, the LMH6515 drives a high performance ADC in a broad range of mixed signal and digital communication applications such as mobile radio and cellular base stations where automatic gain control (AGC) is required to increase system dynamic range. When used in conjunction with a high speed ADC, system dynamic range can be extended by up to 32 dB.

The LMH6515 has a differential input and output allowing large signal swings on a single 5V supply. It is designed to accept signals from RF elements and maintain a terminated impedance environment. The input impedance is 200Ω resistive. The output impedance is either 200Ω or 400Ω and is user selectable. A unique internal architecture allows use with both single ended and differential input signals.

Input signals to the LMH6515 are scaled by a highly linear, digitally controlled attenuator with 31 accurate 1 dB steps. The attenuator output provides the input signal for a high gain, ultra linear differential transconductor. The transconductor differential output current can be converted into a voltage by using the on-chip 200Ω or 400Ω loads. The transconductance gain is 0.1 Amp/Volt resulting in a maximum voltage gain of +26 dB when driving a 200Ω load, or 32 dB when driving the 400Ω load. On chip digital latches are provided for local storage of the gain setting. The gain step settling time is 5 ns and care has been taken to reduce the sensitivity of bandwidth and phase to gain setting.

The LMH6515 operates over the industrial temperature range of −40°C to +85°C. The LMH6515 is available in a 16-Pin, thermally enhanced, WQFN package.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

ESD Tolerance(3)	Human Body Model	2 kV
	Machine Model	150V
Positive Supply Voltage (Pin 3)		−0.6V to 5.5V
Output Voltage (pin 14,15)		−0.6V to 6.8V
Differential Voltage Between Any Two Grounds		<200 mV
Analog Input Voltage Range		−0.6V to V_{CC}
Digital Input Voltage Range		−0.6V to 3.6V
Output Short Circuit Duration (one pin to ground)		Infinite
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

OPERATING RATINGS(1)

Supply Voltage (Pin 3)	4V to 5.25V
Output Voltage Range (Pin 14, 15)	1.4V to 6.4V
Differential Voltage Between Any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	±1.4V
Temperature Range(2)	−40°C to +85°C
Package Thermal Resistance (θ_{JA}) 16-Pin WQFN	47°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

5V ELECTRICAL CHARACTERISTICS(1)

The following specifications apply for single supply with V_{CC} = 5V, Maximum Gain , R_L = 100Ω (200Ω external || 200Ω internal), V_{OUT} = 2 V_{PP}, fin = 150 MHz. Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
Dynamic Performance						
SSBW	−3 dB Bandwidth	Average of all Gain Settings		600		MHz
Noise and Distortion						
	Third Order Intermodulation Products	f = 75 MHz, V_{OUT} = 2 V_{PP}		−76		dBc
		f = 150 MHz, V_{OUT} = 2 V_{PP}		−72		
		f = 250 MHz, V_{OUT} = 2 V_{PP}		−66		
		f = 450 MHz, V_{OUT} = 2 V_{PP}		−58		
OIP3	Output 3rd Order Intercept Point	f = 75 MHz, V_{OUT} = 2 V_{PP}, Tone Spacing = 0.5 MHz		39		dBm
		f = 150 MHz, V_{OUT} = 2 V_{PP}, Tone Spacing = 2 MHz		37		
		f = 250 MHz, V_{OUT} = 2 V_{PP}, Tone Spacing = 2 MHz		34		
		f = 75 MHz, R_L = 200Ω, V_{OUT} = 2 V_{PP}, Tone Spacing = 0.5 MHz		40		
		f = 150 MHz, R_L = 200Ω, V_{OUT}= 2 V_{PP}, Tone Spacing = 2 MHz		37		
		f = 250 MHz, R_L = 200Ω, V_{OUT} = 2 V_{PP}, Tone Spacing = 2 MHz		34		
P1 dB	Output Level for 1 dB Gain Compression	f = 75 MHz, R_L = 200Ω		16.7		dBm
		f = 250 MHz, R_L = 200Ω		14.7		
		f = 75 MHz		14.5		
		f = 450 MHz		13.2		
VNI	Input Noise Voltage	Maximum Gain, f = 40 MHz		1.8		nV/√Hz
VNO	Output Noise Voltage	Maximum Gain, f = 40 MHz		18		nV/√Hz
NF	Noise Figure	Maximum Gain		8.3		dB
Analog I/O						
	Differential Input Resistance		165 **160**	186	210 **220**	Ω
	Input Common Mode Resistance		825 **785**	971	1120 **1160**	Ω
	Differential Output Impedance	Low Gain Option		187		Ω
		High Gain Option	330 **325**	370	410 **415**	
	Internal Load Resistors	Between Pins 13, 14 and Pins 15, 16	165 **160**	187	210 **235**	Ω
	Input Signal Level (AC Coupled)	Max Gain, V_O = 2 V_{PP}, R_L = 1 kΩ		126		mV_{PP}
	Maximum Differential Input Signal	AC Coupled		5.6		V_{PP}
	Input Common Mode Voltage	Self Biased	1.3 **1.1**	1.4	1.5 **1.7**	V
	Input Common Mode Voltage Range	Driven Externally		0.9 to 2.0		V
	Minimum Input Voltage	DC		0		V
	Maximum Input Voltage	DC		3.3		V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specified parametric performance is indicated in the electrical tables under conditions different than those tested

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

5V ELECTRICAL CHARACTERISTICS[1] (continued)

The following specifications apply for single supply with V_{CC} = 5V, Maximum Gain , R_L = 100Ω (200Ω external || 200Ω internal), V_{OUT} = 2 V_{PP}, fin = 150 MHz. Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
	Maximum Differential Output Voltage Swing	V_{CC} = 5V, Output Common Mode = 5V		5.5		V_{PP}
V_{OS}	Output Offset Voltage	All Gain Settings		30		mV
CMRR	Common Mode Rejection Ratio			85		dB
PSRR	Power Supply Rejection Ratio		63 **61**	83		dB
Gain Parameters						
	Maximum Gain	DC, Internal R_L = 200Ω, External R_L = 1280Ω	23.9 **23.4**	24.2	24.6 **24.8**	dB
	Minimum Gain	DC, Internal R_L = 200Ω, External R_L = 1280Ω	−7.2 **−7.7**	−6.9	−6.5 **−6.4**	dB
	Gain Step Size	DC		1.0		dB
	Gain Step Error	DC		0.02		dB
		f = 150 MHz		0.07		
	Cumulative Gain Step Error	DC, Gain Step 31 to Gain Step 0	−0.1 **−0.2**	0.05	0.3 **0.4**	dB
	Gain Step Switching Time			5		ns
Digital Inputs/Timing						
	Logic Compatibility	CMOS Logic		3.3		V
VIL	Logic Input Low Voltage				0.8	V
VIH	Logic Input High Voltage		2.0			V
IIH	Logic Input High Input Current[4]			32	40	µA
TSU	Setup Time			3		ns
THOLD	Hold Time			3		ns
TPW	Minimum Latch Pulse Width			10		ns
Power Requirements						
ICC	Total Supply Current	V_{OUT} = 0V Differential, V_{OUT} Common Mode = 5V		107	124 **134**	mA
	Amplifier Supply Current	Pin 3 Only		56	66 **74**	mA
	Output Stage Bias Currents	Pins 13, 14 and Pins 15, 16; V_{OUT} Common Mode = 5 V		48	58 **60**	mA

(4) Negative input current implies current flowing out of the device.

CONNECTION DIAGRAM

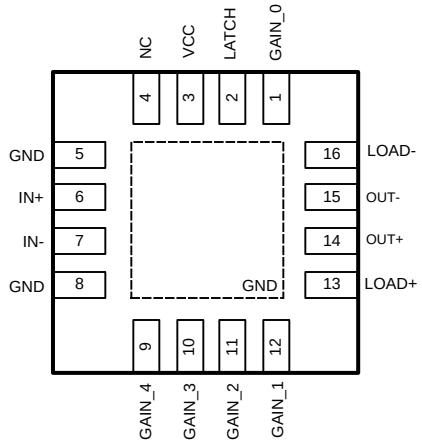


Figure 1. 16-Pin WQFN (Top View)

Gain Control Pins

Pin Number	Pin Name	Gain Step Size
1	GAIN_0	1 dB
12	GAIN_1	2 dB
11	GAIN_2	4 dB
10	GAIN_3	8 dB
9	GAIN_4	16 dB

PIN DESCRIPTIONS

Pin Number	Symbol	Description
Analog I/O		
6	IN+	Non-inverting analog input. Internally biased to 1.4V. Input voltage should not exceed V_{CC} or go below GND by more than 0.5V.
7	IN−	Inverting analog input. Internally biased to 1.4V. Input voltage should not exceed V_{CC} or go below GND by more than 0.5V. If using amplifier single ended this input should be capacitively coupled to ground.
15	OUT−	Open collector inverting output. This pin is an output that also requires a power source. This pin should be connected to 5V through either an RF choke or an appropriately sized inductor that can form part of a filter. See APPLICATION INFORMATION section for details.
14	OUT+	Open collector non-inverting output. This pin is an output that also requires a power source. This pin should be connected to 5V through either an RF choke or an appropriately sized inductor that can form part of a filter. See APPLICATION INFORMATION section for details.
16	LOAD−	Internal 200Ω resistor connection to pin 15. This pin can be left floating for higher gain or shorted to pin 13 for lower gain and lower effective output impedance. See APPLICATION INFORMATION section for details.
13	LOAD+	Internal 200Ω resistor connection to pin 14. This pin can be left floating for higher gain or shorted to pin 16 for lower gain and lower effective output impedance. See APPLICATION INFORMATION section for details.
Power		
3	V_{CC}	5V power supply pin. Use ceramic, low ESR bypass capacitors. This pin powers everything except the output stage.
5,8	GND	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is also a ground connection.

PIN DESCRIPTIONS (continued)

Pin Number	Symbol	Description
Digital Inputs		
1,12,11, 10,9	GAIN_0 to GAIN_4	Gain setting pins. See above table for gain step sizes for each pin. These pins are 3.3V CMOS logic compatible. 5V inputs may cause damage.
2	LATCH	This pin controls the function of the gain setting pins mentioned above. With LATCH in the logic HIGH state the gain is fixed and will not change. With the LATCH in the logic LOW state the gain is set by the state of the gain control pins. Any changes in gain made with the LATCH pin in the LOW state will take effect immediately. This pin is 3.3V CMOS logic compatible. 5V inputs may cause damage.
4	NC	This pin is not connected. It can be grounded or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V

Frequency Response All Gain Settings

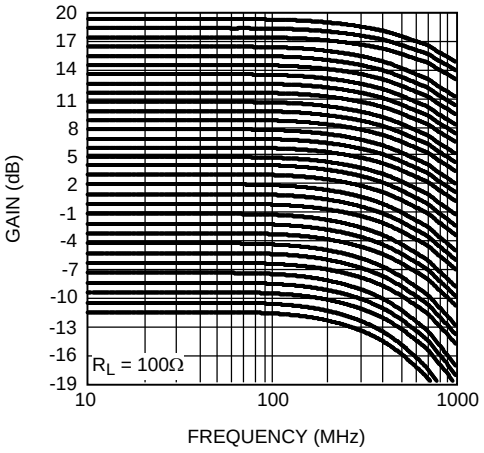


Figure 2.

Frequency Response with Capacitive Load

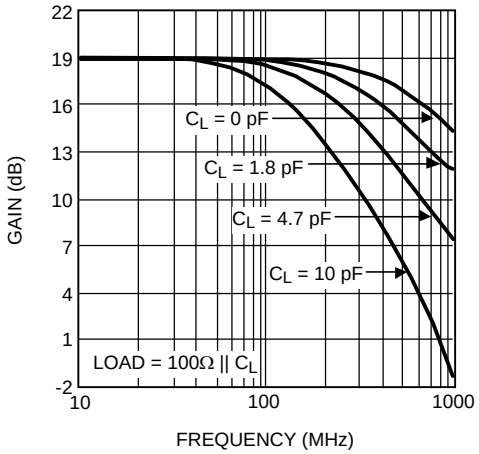


Figure 3.

Frequency Response Over Temperature, Maximum Gain

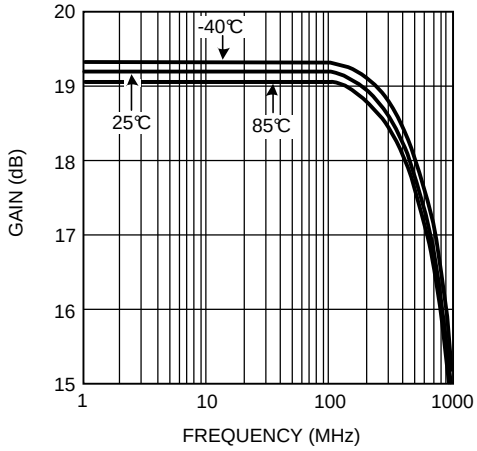


Figure 4.

Frequency Response Over Temperature, Minimum Gain

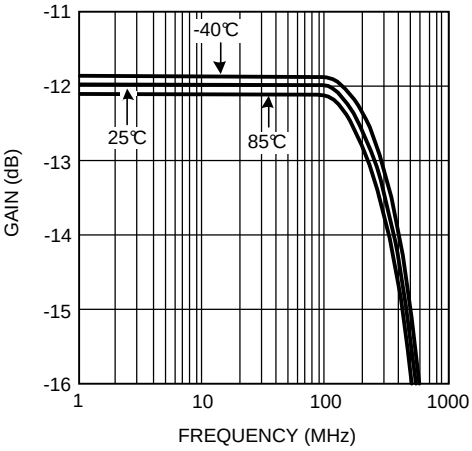


Figure 5.

OIP3 High Gain Mode

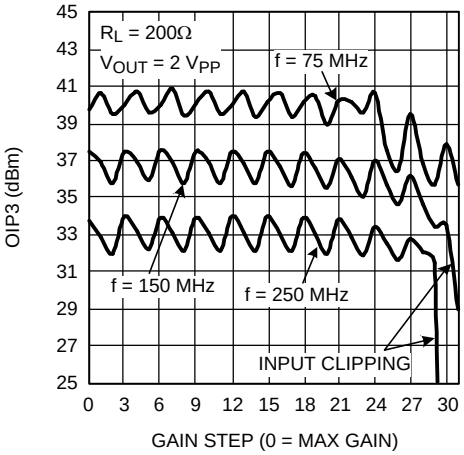


Figure 6.

OIP3 Low Gain Mode

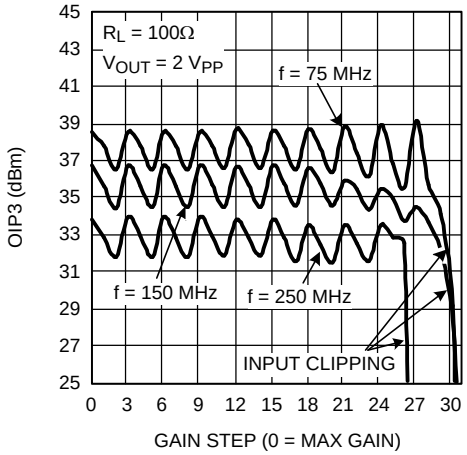


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V (continued)

OIP3 Over Temperature

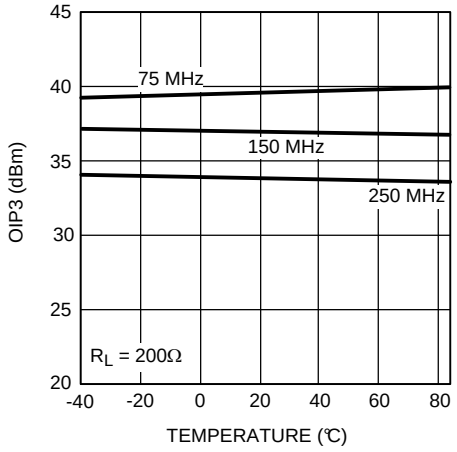


Figure 8.

OIP3 High Gain Mode

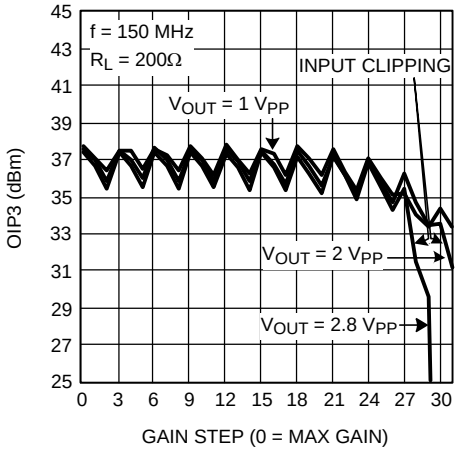


Figure 9.

IMD3 Low Gain Mode

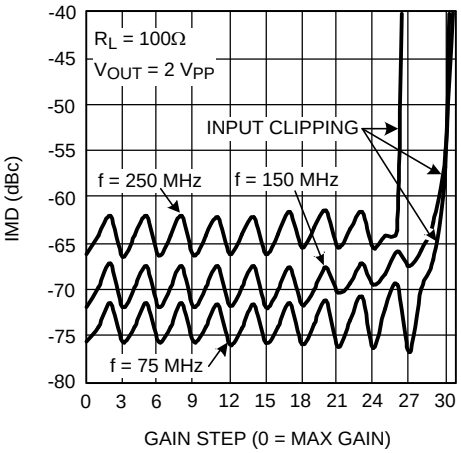


Figure 10.

IMD3 High Gain Mode

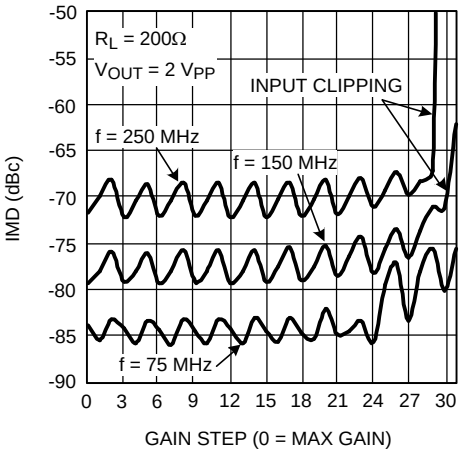


Figure 11.

IMD3 High Gain Mode

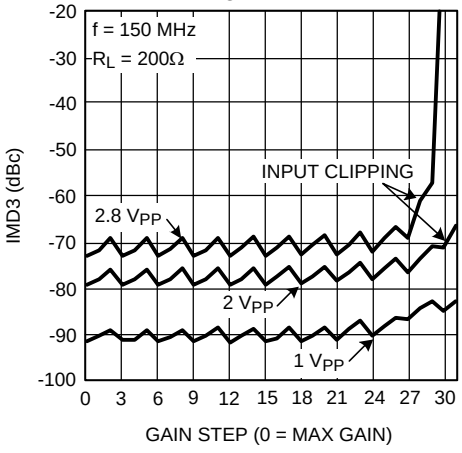


Figure 12.

HD2 vs. Frequency

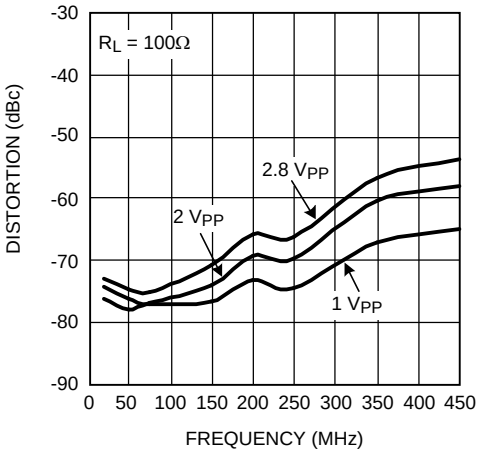


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V (continued)

HD3 vs. Frequency

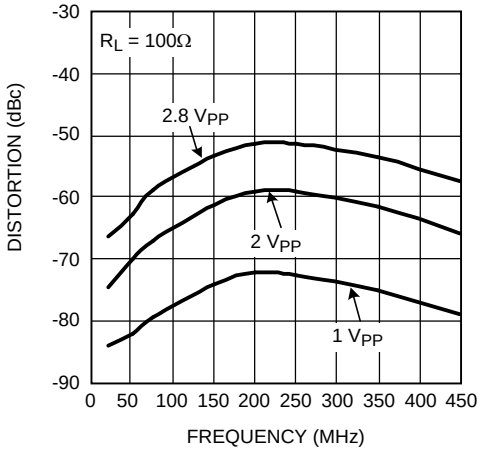


Figure 14.

HD2 vs. Frequency

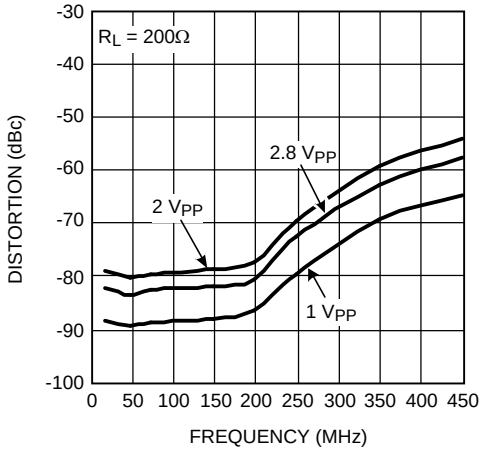


Figure 15.

HD3 vs. Frequency

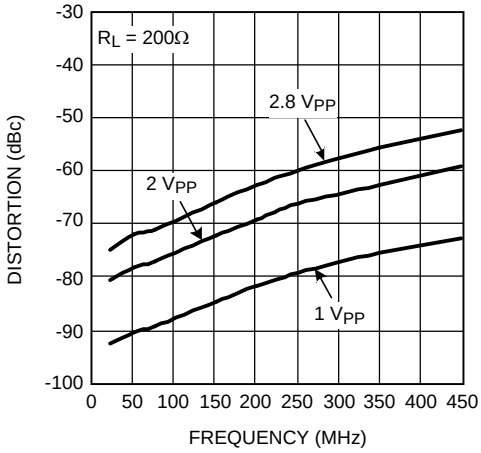


Figure 16.

Noise Figure for All Gain Settings

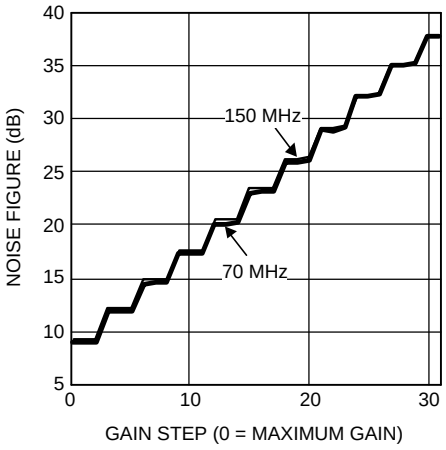


Figure 17.

Noise Figure vs. Frequency

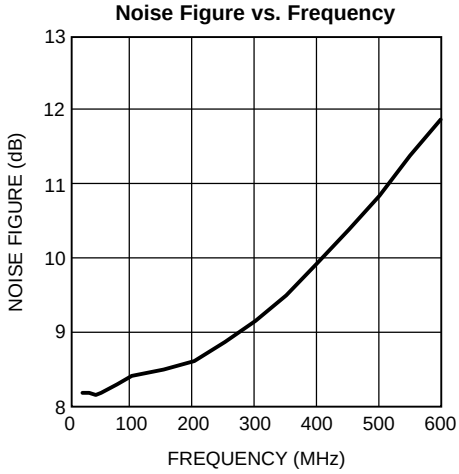


Figure 18.

Differential Output Noise

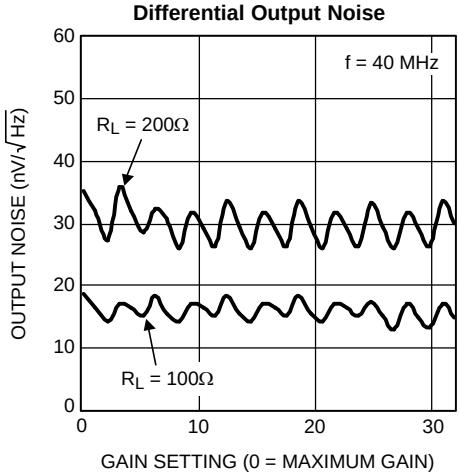


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V (continued)

Maximum Gain vs. Supply Voltage

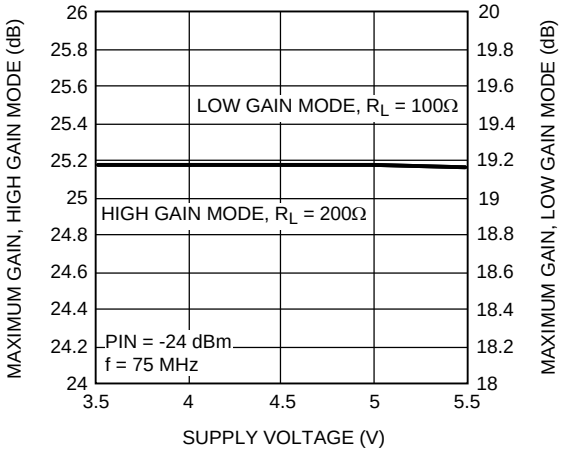


Figure 20.

Gain vs. External Load

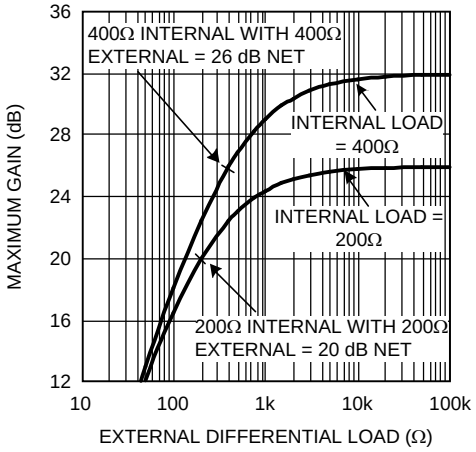


Figure 21.

Maximum Gain Over Temperature

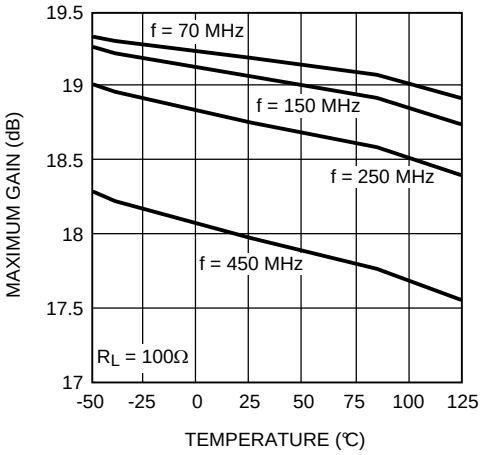


Figure 22.

Worst Case Gain Step Error vs. Frequency

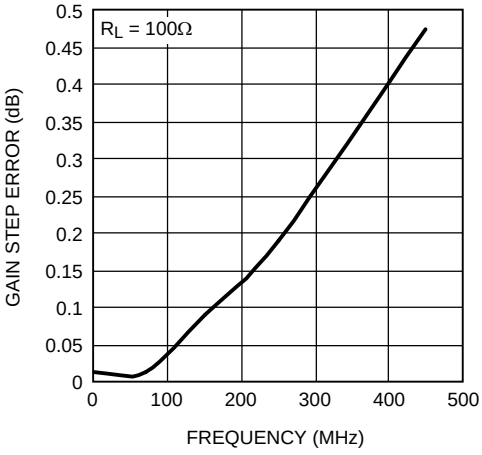


Figure 23.

Worst Case Gain Step Error vs. Frequency

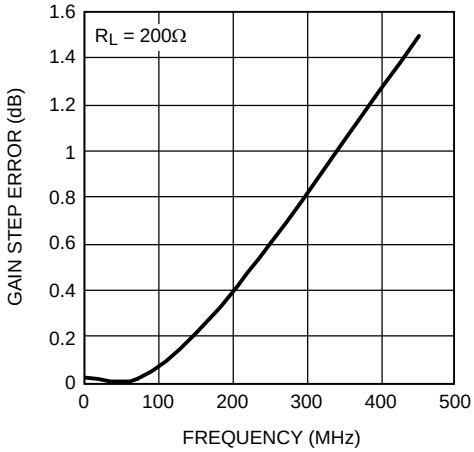


Figure 24.

Worst Case Gain Step Error Over Temperature

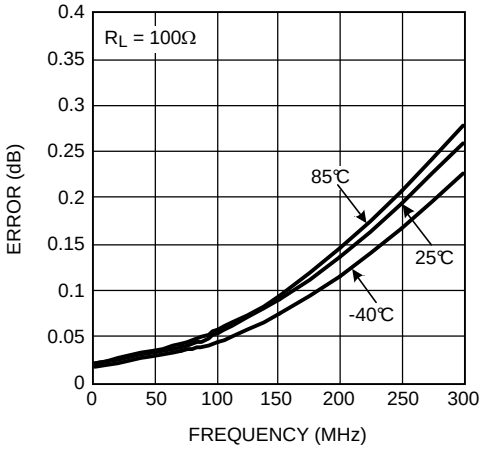


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V (continued)

Digital Crosstalk

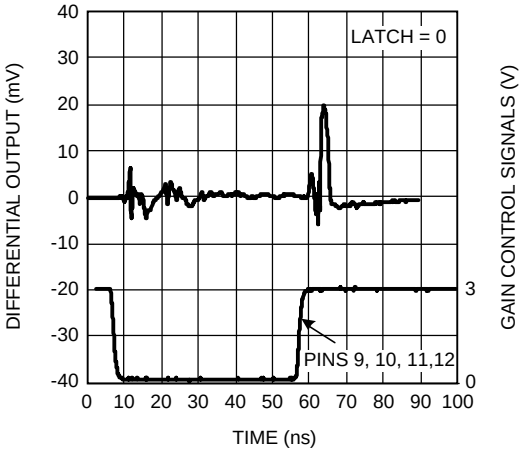


Figure 26.

Digital Crosstalk

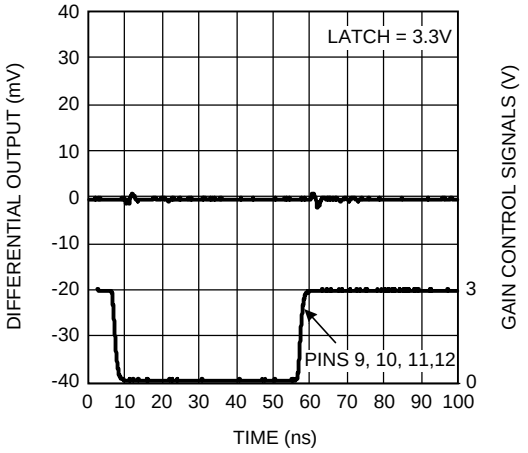


Figure 27.

Digital Pin to Output Isolation

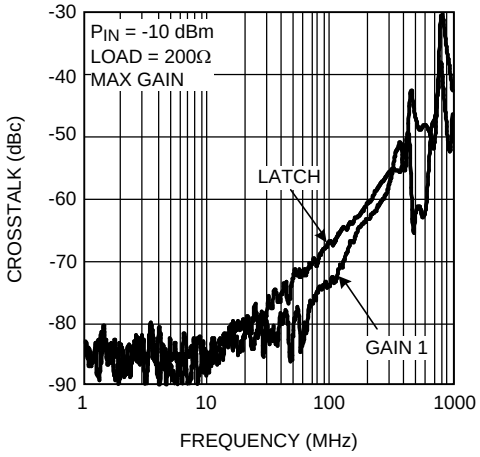


Figure 28.

Minimum Gain to Maximum Gain Switching Using Latch Pin

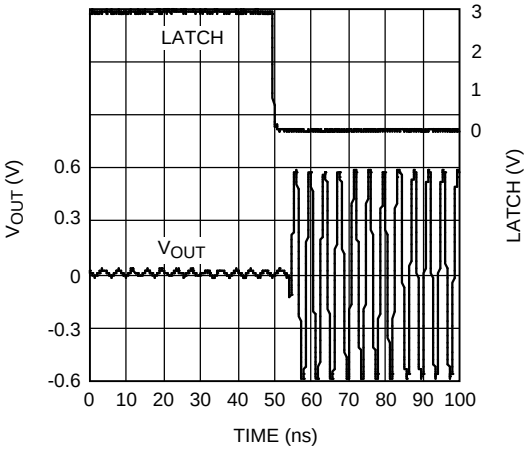


Figure 29.

Maximum Gain to Minimum Gain Switching Using Latch Pin

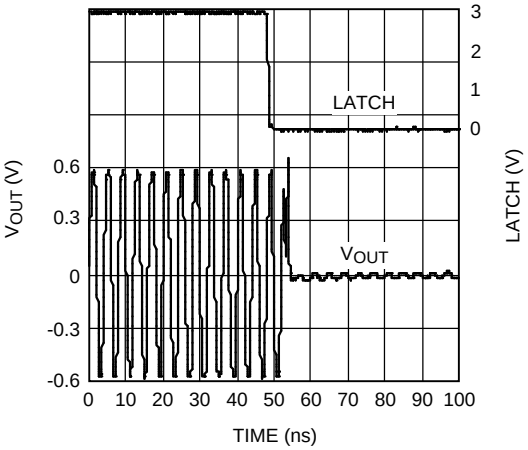


Figure 30.

16 dB Gain Step Using Latch Pin

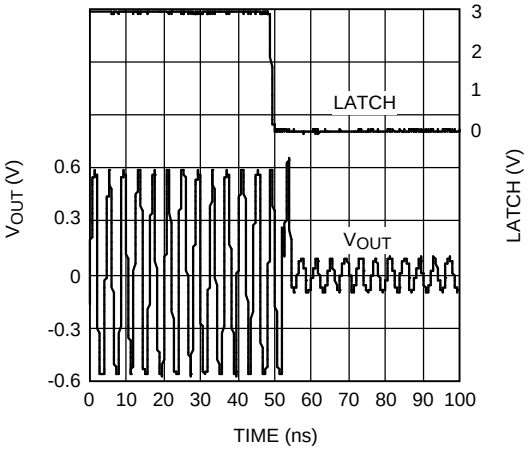


Figure 31.

TYPICAL PERFORMANCE CHARACTERISTICS
V_{CC} = 5V (continued)

16 dB Gain Step with Latch Pin Low Switching Gain Pin 4

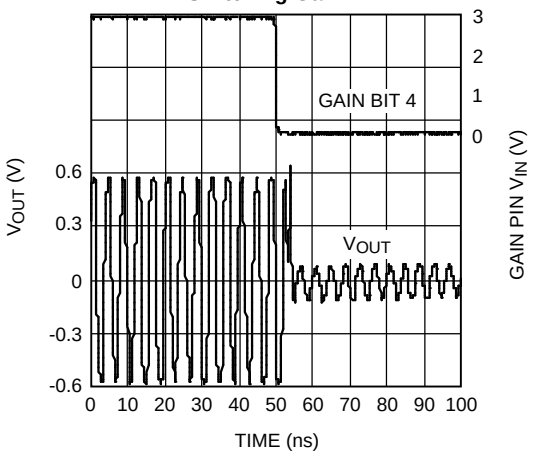


Figure 32.

8 dB Gain Step with Latch Pin Low Switching Gain Pin 3

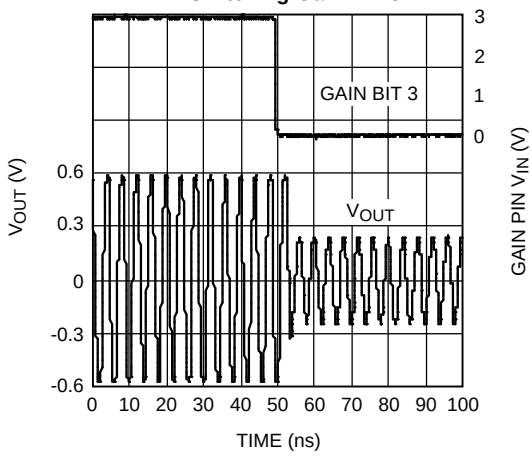


Figure 33.

4 dB Gain Step Using Latch Pin

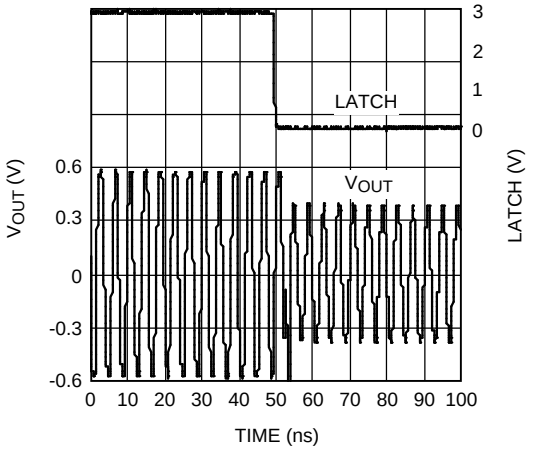


Figure 34.

Power On Timing, Maximum Gain

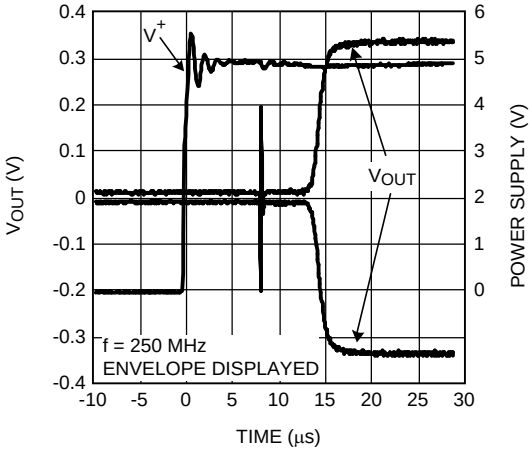


Figure 35.

Power On Timing, Minimum Gain

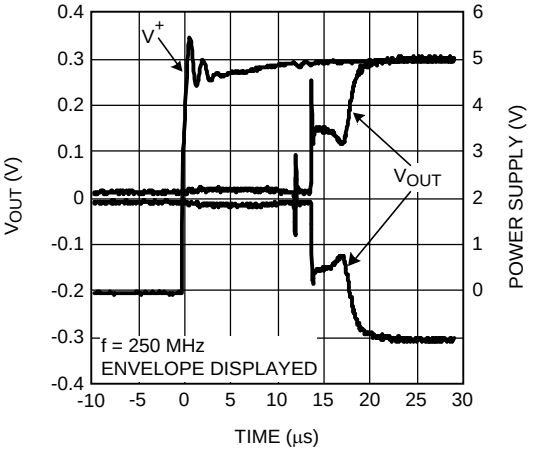


Figure 36.

Power Off Timing, Maximum Gain

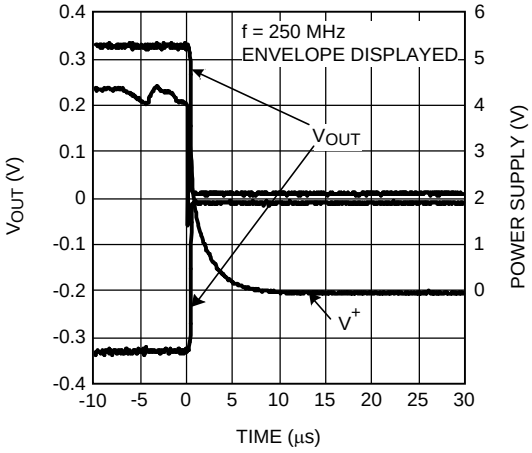


Figure 37.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V (continued)

Power Off Timing, Minimum Gain

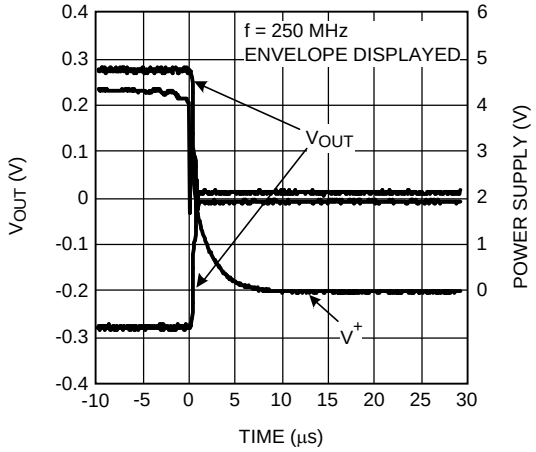


Figure 38.

APPLICATION INFORMATION

The LMH6515 is a fully differential amplifier optimized for signal path applications up to 400 MHz. The LMH6515 has a 200Ω input. The absolute gain is load dependent, however the gain steps are always 1 dB. The LMH6515 output stage is a class A amplifier. This class A operation results in excellent distortion and linearity characteristics. This makes the LMH6515 ideal for voltage amplification and an ideal ADC driver where high linearity is necessary.

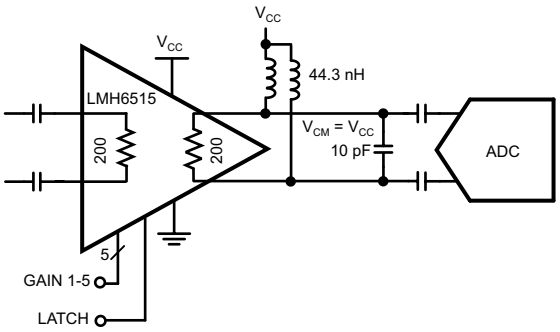


Figure 39. LMH6515 Typical Application

The LMH6515 output common mode should be set carefully. Using inductors to set the output common mode is one preferred method and will give maximum output swing. AC coupling of the output is recommended. The inductors mentioned above will shift the idling output common mode to the positive supply. Also, with the inductors, the output voltage can exceed the supply voltage. Other options for setting the output common mode require supply voltages above 5V. If using a supply higher than 5V care should be taken to make sure the output common mode does not exceed the 5.25V supply rating.

It is also important to note the maximum voltage limits for the OUT+ and OUT− pins, which is 6.4V. When using inductors these pins will experience voltage swings beyond the supply voltage. With a 5V output common mode operating point this makes the effective maximum swing 5.6 V_{PP} differential. System calibration and automatic gain control algorithms should be tailored to avoid exceeding this limit.

In order to help with system design TI offers the ADC14V155KDRB High IF Receiver reference design board. This board combines the LMH6515 DVGA with the ADC14V155 ADC and provides a ready made solution for many IF receiver applications. Using an IF frequency of 169 MHz it achieves a small signal SNR of 72 dBFS and an SFDR of greater than 90 DBFS. Large signal measurements show an SNR of 68 dBFS and an SFDR of 77 dBFS. The High IF Receiver board also features the LMK03000 low-jitter precision clock conditioner.

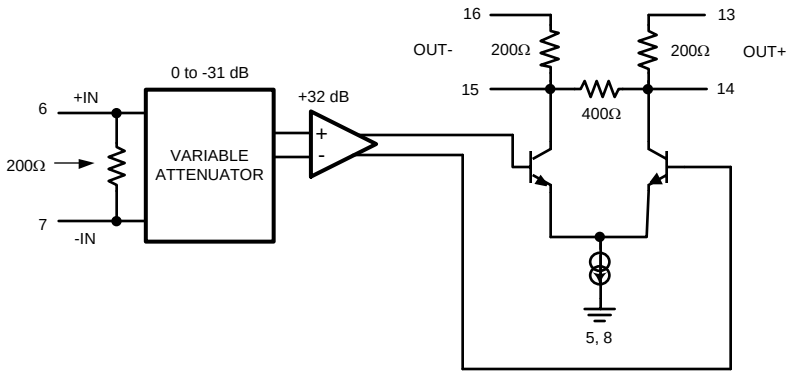
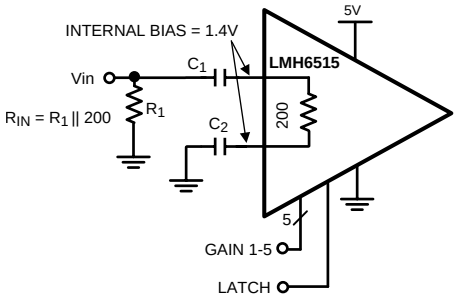


Figure 40. LMH6515 Block Diagram

INPUT CHARACTERISTICS

The LMH6515 input impedance is set by internal resistors to a nominal 200Ω. Process variations will result in a range of values as shown in the 5V Electrical Characteristics table. At higher frequencies parasitics will start to impact the impedance. This characteristic will also depend on board layout and should be verified on the customer's system board.

At maximum gain the digital attenuator is set to 0 dB and the input signal will be much smaller than the output. At minimum gain the output is 12 dB or more smaller than the input. In this configuration the input signal size may limit the amplifier output amplitude, depending on the output configuration and the desired output signal voltage. The input signal cannot swing more than 0.5V below the negative supply voltage (normally 0V) nor should it exceed the positive supply voltage. The input signal will clip and cause severe distortion if it is too large. Because the input stage self biases to approximately 1.4V the lower supply voltage will impose the limit for input voltage swing. To drive larger input signals the input common mode can be forced higher than 1.4V to allow for more swing. An input common mode of 2.0V will allow an 8 V_{PP} maximum input signal. The trade off for input signal swing is that as the input common mode is shifted away from the 1.4V internal bias point the distortion performance will suffer slightly.



(Note capacitor on grounded input)

Figure 41. Single Ended Input

OUTPUT CHARACTERISTICS

The LMH6515 has the option of two different output configurations. The LMH6515 is an open collector topology. As shown in Figure 46 each output has an on chip 200Ω pull up resistor. In addition there is an internal 400Ω resistor between the two outputs. This results in a 200Ω or a 400Ω differential load in parallel with the external load. The 400Ω option is the high gain option and the 200Ω provides for less gain. The 200Ω configuration is recommended unless more gain is required.

The output common mode of the LMH6515 must be set by external components. Most applications will benefit from the use of inductors on the output stage. In particular, the 400Ω option, as shown in Figure 47, will require inductors in order to be able to develop an output voltage. The 200Ω option as shown in Figure 48 or Figure 49 will also require inductors since the voltage drop due to the on chip 200Ω resistors will saturate the output transistors. It is also possible to use resistors and high voltage power supplies to set the output common mode. This operation is not recommended, unless it is necessary to DC couple the output. If DC coupling is required the input common mode and output common mode voltages must be taken into account.

Maximum bandwidth with the LMH6515 is achieved by using the low gain, low impedance output option and using a low load resistance. With an effective load of 67Ω a bandwidth of nearly 1 GHz can be realized. As the effective resistance on the output stage goes up the capacitance of the board traces and amplifier output stage limit bandwidth in a roughly linear fashion. At an output impedance of 100Ω the bandwidth is down to 600 MHz, and at 200Ω the bandwidth is 260 MHz. For this reason driving very high impedance loads is not recommended.

Although bandwidth goes down with higher values of load resistance, the distortion performance improves and gain increases. The LMH6515 has a common emitter Class A output stage and minimizing the amount of current swing in the output devices improves distortion substantially.

The LMH6515 output stage is powered through the collectors of the output transistors. Power for the output stage is fed through inductors and the reactance of the inductors allows the output voltage to develop. In Figure 39 the inductors are shown with a value of 44.4 nH. The value of the inductors used will be different for different applications. In Figure 39 the inductors have been chosen to resonate with the ADC and the load capacitor to provide a weak band pass filter effect. For broad band applications higher value inductors will allow for better low frequency operation. However, large valued inductors will reduce high frequency performance, particularly inductors of small physical sizes like 0603 or smaller. Larger inductors will tend to perform better than smaller ones of the same value even for narrow band applications. This is because the larger inductors will have a lower DC resistance and less inter-winding capacitance and hence a higher Q and a higher self resonance frequency. The self resonance frequency should be higher than any desired signal content by at least a factor of two. Another consideration is that the power inductors and the filter inductors need to be placed on the circuit board such that their magnetic fields do not cause coupling. Mutual coupling of inductors can compromise filter characteristics and lead to unwanted distortion products.

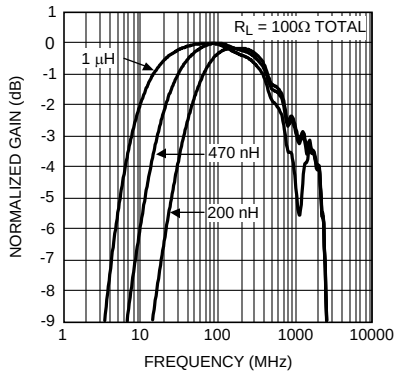


Figure 42. Bandwidth Changes Due to Different Inductor Values

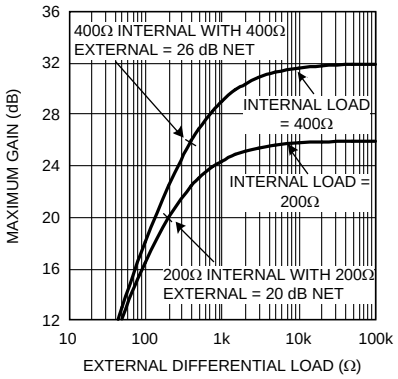


Figure 43. Gain vs. External Load

DIGITAL CONTROL

The LMH6515 has 32 gain settings covering a range of 31 dB. To avoid undesirable signal transients the LMH6515 should be powered on at the minimum gain state (all logic input pins at 0V). The LMH6515 has a 5-bit gain control bus as well as a latch pin. When the latch pin is low, data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). When the latch pin transitions high the current gain state is held and subsequent changes to the gain set pins are ignored. To minimize gain change glitches multiple gain control pins should not change while the latch pin is low. In order to achieve the very fast gain step switching time of 5 ns the internal gain change circuit is very fast. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If continuous gain control is desired the latch pin can be tied to ground. This state is called transparent mode and the gain pins are always active. In this state the timing of the gain pin logic transitions should be planned carefully to avoid undesirable transients.

The LMH6515 was designed to interface with 3.3V CMOS logic circuits. If operation with 5V logic is required a simple voltage divider at each logic pin will allow for this. To properly terminate 100Ω transmission lines a divider with a 66.5Ω resistor to ground and a 33.2Ω series resistor will properly terminate the line as well as give the 3.3V logic levels. Care should be taken not to exceed the 3.6V absolute maximum voltage rating of the logic pins.

EXPOSED PAD WQFN PACKAGE

The LMH6515 is in a thermally enhanced package. The exposed pad is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of this pad. The exposed pad should be attached to as much copper on the circuit board as possible, preferably external copper. However, it is also very important to maintain good high speed layout practices when designing a system board. Please refer to the LMH6515 evaluation board for suggested layout techniques.

Package information is available on the TI Web site.www.ti.com/packaging

INTERFACING TO ADC

The LMH6515 was designed to be used with high speed ADCs such as the ADC14155. As shown in the Typical Application schematic, AC coupling provides the best flexibility especially for IF sub-sampling applications. Any resistive networks on the output will also cause a gain loss because the output signal is developed across the output resistors. The chart Maximum Gain vs. External Load shows the change in gain when an external load is added.

The inputs of the LMH6515 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately 1.4V. In most applications the LMH6515 input will need to be AC coupled.

The output common mode voltage is not self biasing, it needs to be pulled up to the positive supply rail with external inductors as shown in Figure 39. This gives the LMH6515 the capability for large signal swings with very low distortion on a single 5V supply. The internal load resistors provide the LMH6515 with very consistent gain.

A unique internal architecture allows the LMH6515 to be driven by either a differential or single ended source. If driving the LMH6515 single ended, the unused input should be terminated to ground with a 0.01 µF capacitor. Directly shorting the unused input to ground will disrupt the internal bias circuitry and will result in poor performance.

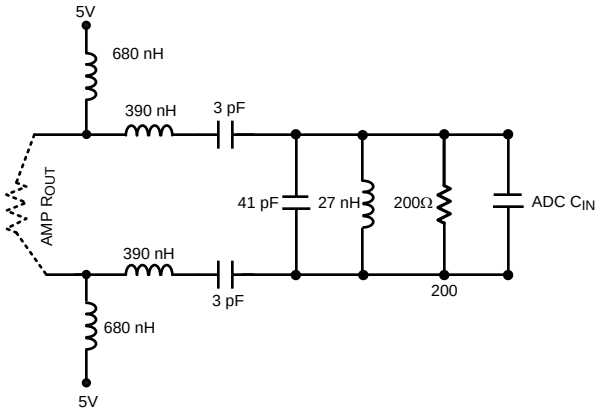


Figure 44. Bandpass Filter
Center Frequency is 140 MHz with a 20 MHz Bandwidth
Designed for 200Ω Impedance

ADC Noise Filter

Figure 44 shows a filter schematic and the following table of values are for some common IF frequencies. The filter shown offers a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology works best with the 12 and 14-bit sub-sampling analog to digital converters shown in the Table 2 table.

Table 1. Filter Component Values

Filter Component Values					
	Fc	75 MHz	140 MHz	170 MHz	250 MHz
	BW	40 MHz	20 MHz	25 MHz	Narrow Band
Components	L1, L2	10 µH	10 µH	10 µH	10 µH
	L3, L4	390 nH	390 nH	560 nH	—
	C1, C2	10 pF	3 pF	1.4 pF	47 pF
	C3	22 pF	41 pF	32 pF	11 pF
	L5	220 nH	27 nH	30 nH	22 nH
	R1, R2	100	200	100	499

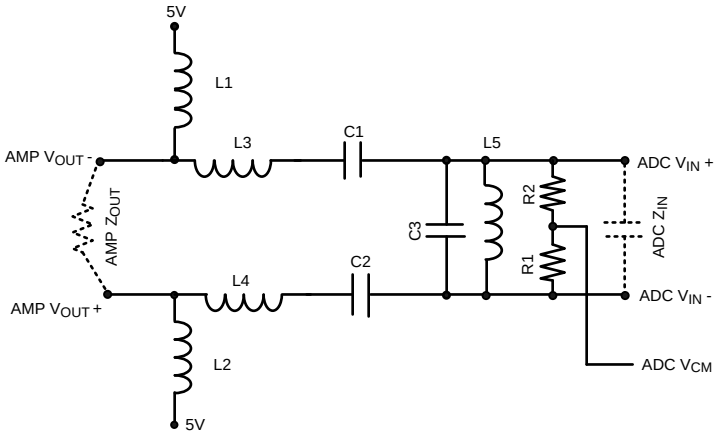


Figure 45. Sample Filter

POWER SUPPLIES

As shown in Figure 46, the LMH6515 has a number of options for power supply connections on the output pins. Pin 3 (V_{CC}) is always connected. The output stage can be connected as shown in Figure 47, Figure 48, or Figure 49. The supply voltage range for V_{CC} is 4V to 5.25V. A 5V supply provides the best performance while lower supplies will result in less power consumption. Power supply regulation of 2.5% or better is advised.

Of special note is that the digital circuits are powered from an internal supply voltage of 3.3V. The logic pins should not be driven above the absolute maximum value of 3.6V. See the DIGITAL CONTROL section for details.

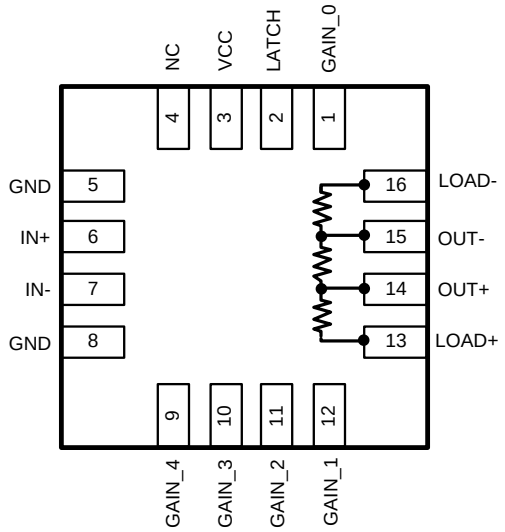


Figure 46. Internal Load Resistors

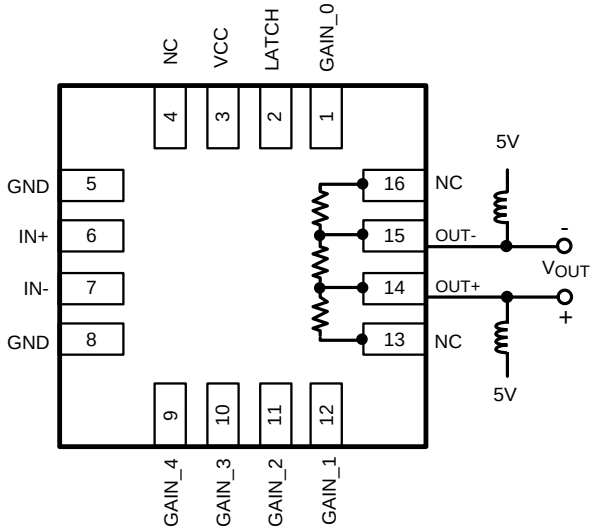


Figure 47. Using High Gain Mode (400Ω Load)

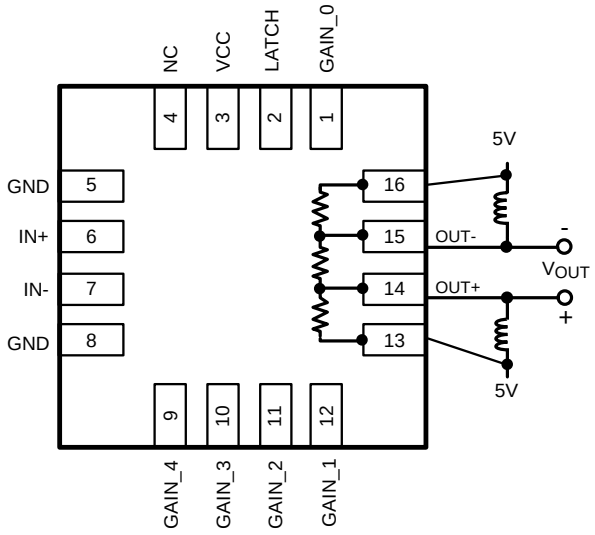


Figure 48. Using Low Gain Mode (200Ω Load)

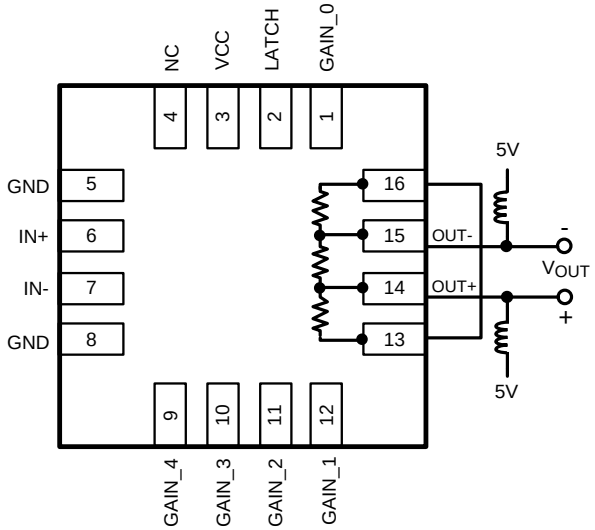


Figure 49. Alternate Connection for Low Gain Mode (200Ω Load)

Table 2. Compatible High Speed Analog to Digital Converters

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC12L063	62	12	SINGLE
ADC12DL065	65	12	DUAL
ADC12L066	66	12	SINGLE
ADC12DL066	66	12	DUAL
CLC5957	70	12	SINGLE
ADC12L080	80	12	SINGLE
ADC12DL080	80	12	DUAL
ADC12C080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C080	80	14	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08060	60	8	SINGLE
ADC10DL065	65	10	DUAL
ADC10065	65	10	SINGLE
ADC10080	80	10	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6515SQ/NOPB	ACTIVE	WQFN	RGH	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6515SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

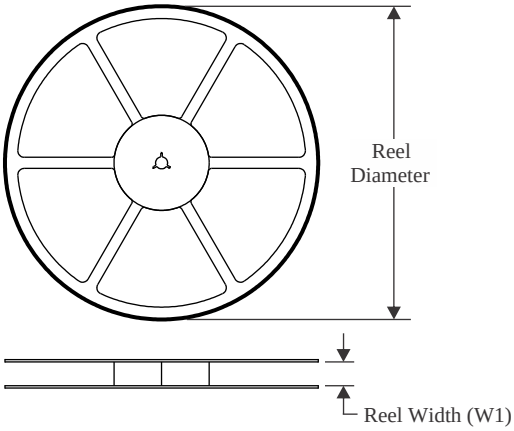
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

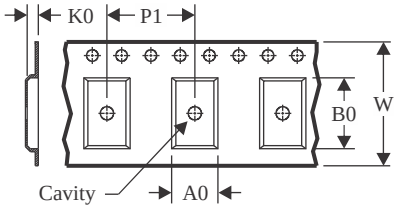
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

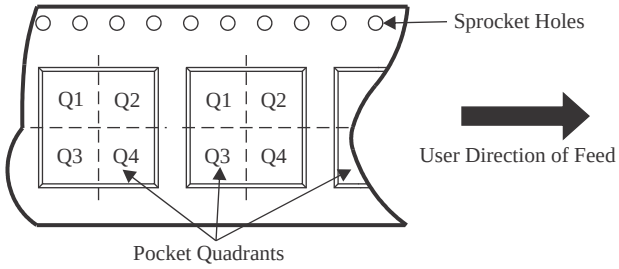


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

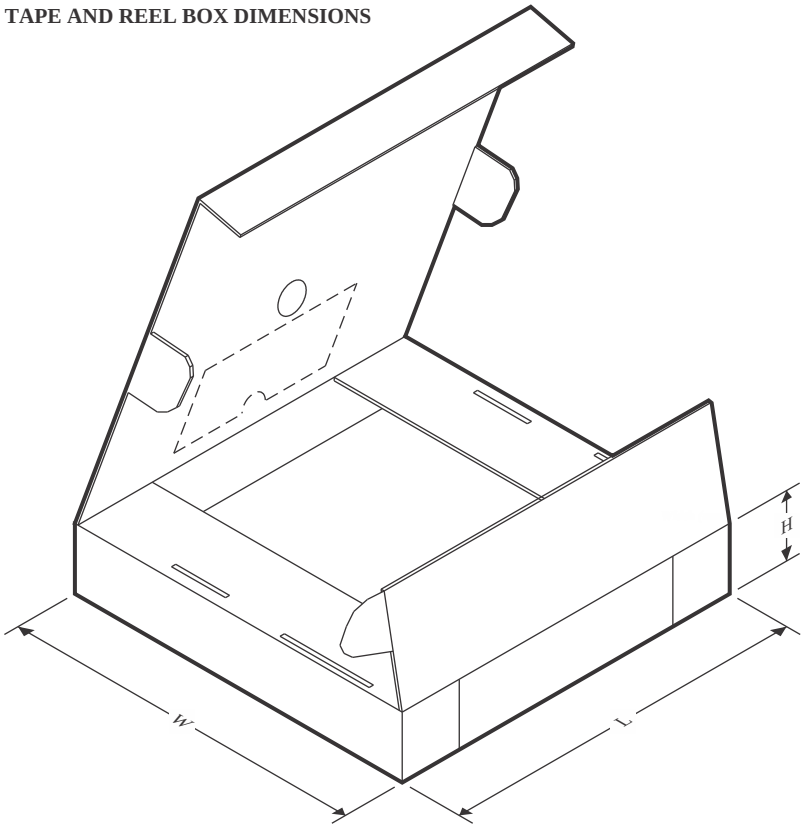
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6515SQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

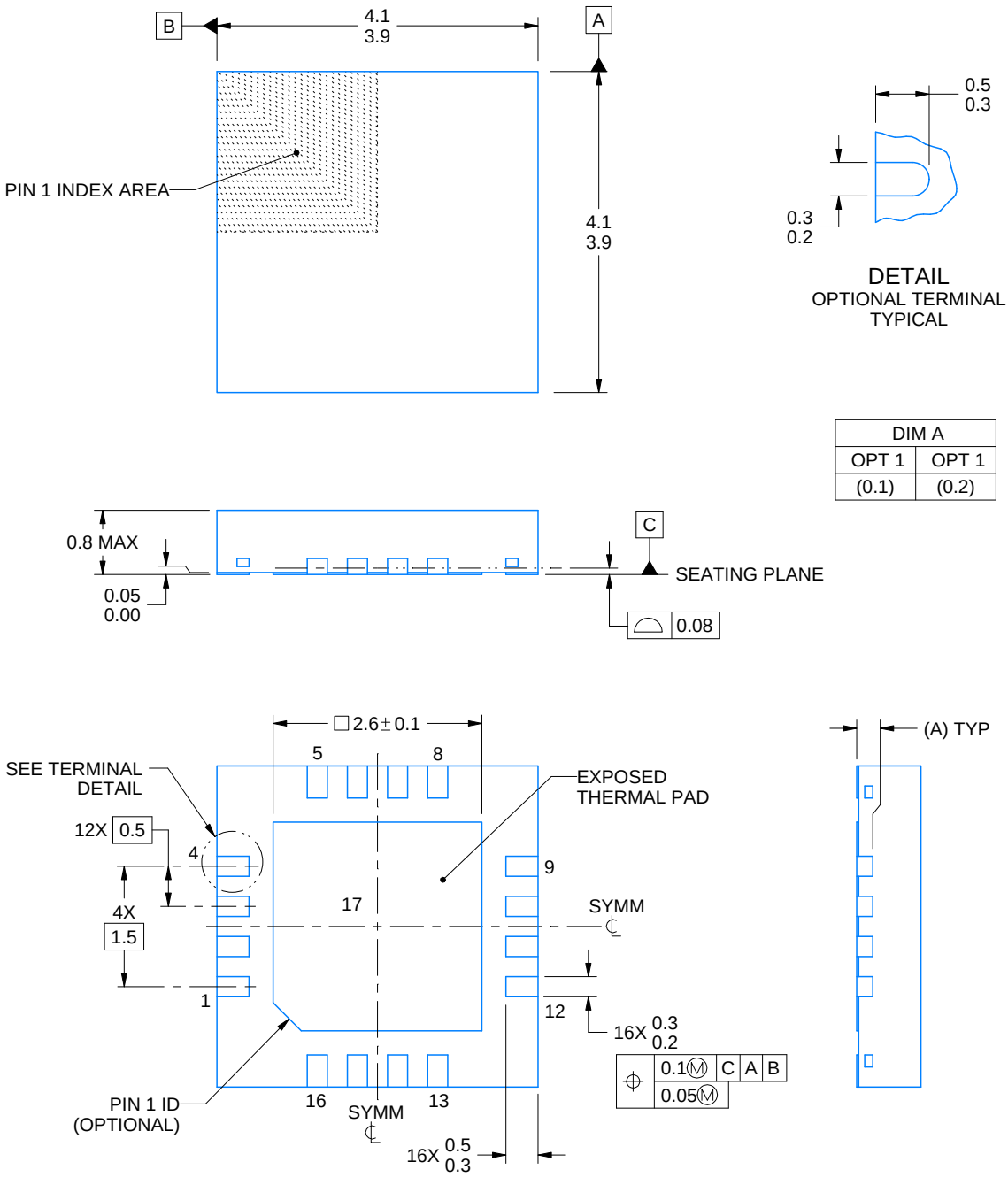
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6515SQ/NOPB	WQFN	RGH	16	1000	208.0	191.0	35.0

PACKAGE OUTLINE

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

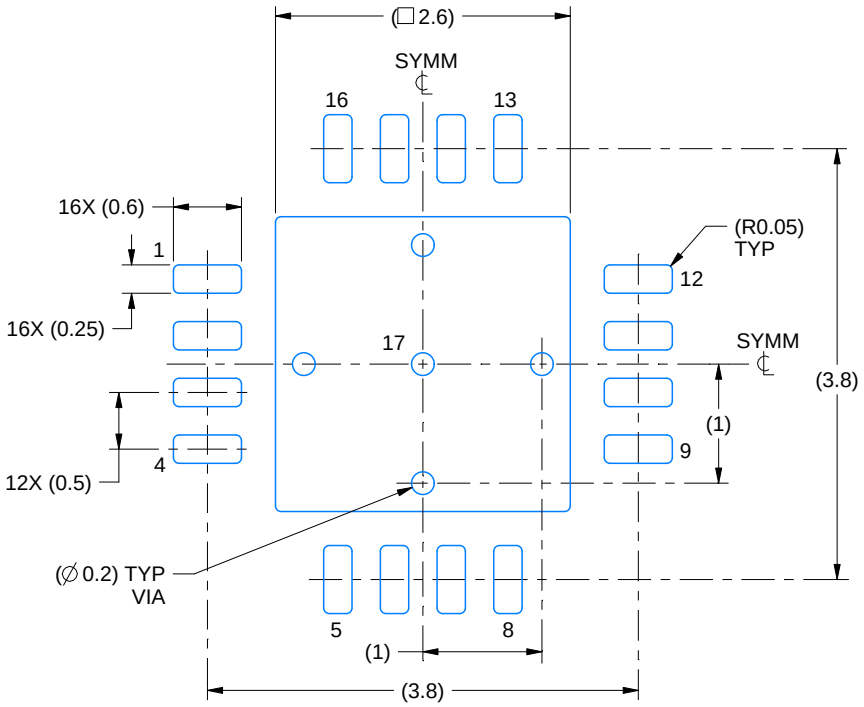
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

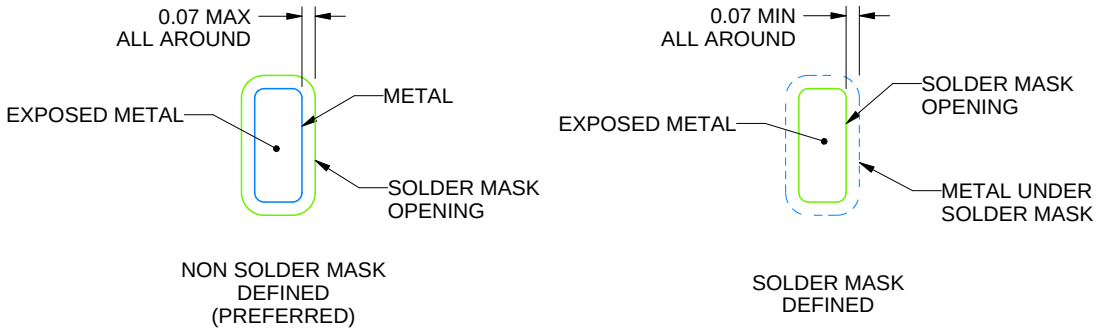
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

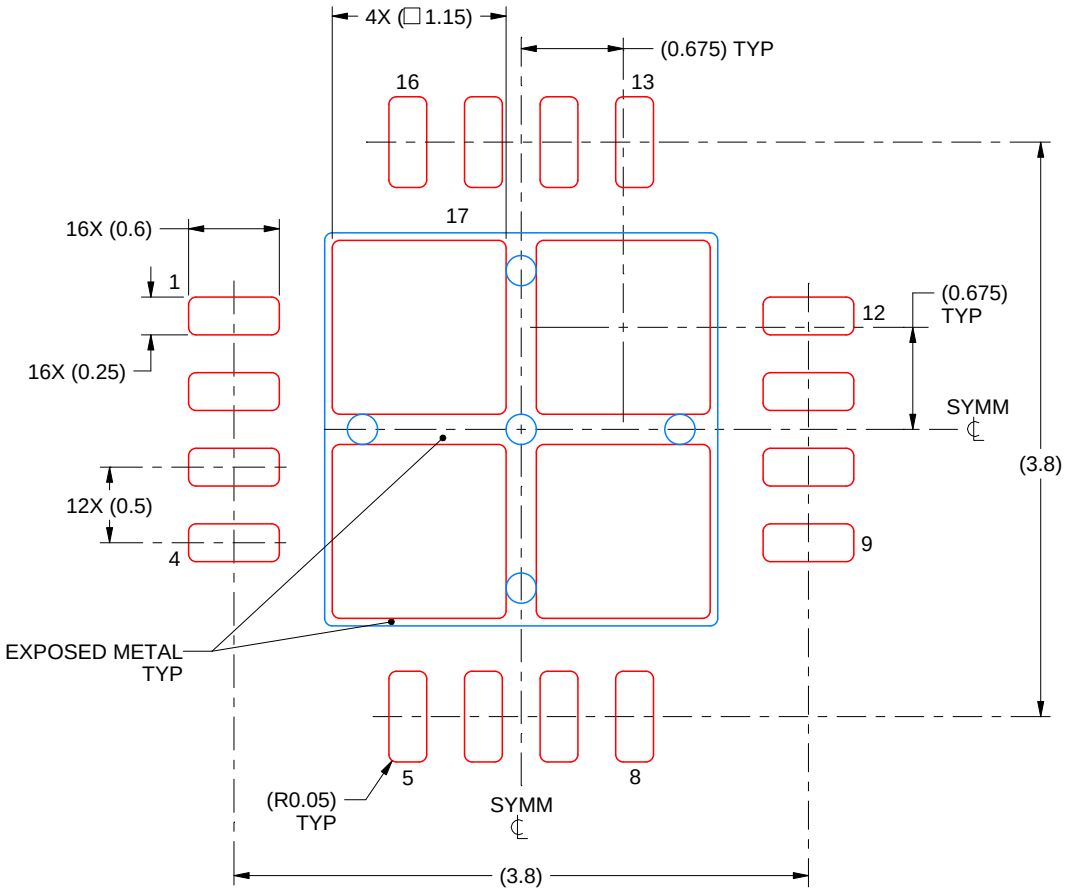


SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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