LMH6628 Dual Wideband, Low Noise, Voltage Feedback Op Amp

Check for Samples: LMH6628

FEATURES
- Wide Unity Gain Bandwidth: 300MHz
- Low Noise: 2nV/√Hz
- Low Distortion: −65/−74dBc (10MHz)
- Settling Time: 12ns to 0.1%
- Wide Supply Voltage Range: ±2.5V to ±6V
- High Output Current: ±85mA
- Improved Replacement for CLC428

APPLICATIONS
- High Speed Dual Op Amp
- Low Noise Integrators
- Low Noise Active Filters
- Driver/receiver for Transmission Systems
- High Speed Detectors
- I/Q Channel Amplifiers

DESCRIPTION
The Texas Instruments LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628’s low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual (±5V) power supply.

Each of the LMH6628’s closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/√Hz). Low 2nd/3rd harmonic distortion (−65/−74dBc at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of high resolution analog-to-digital converters. Combining the LMH6628’s two tightly matched amplifiers in a single 8-pin SOIC package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using TI’s VIP10™ complementary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (CLC730036).

Connection Diagram

![Connection Diagram](image)

Figure 1. 8-Pin SOIC, Top View

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All other trademarks are the property of their respective owners.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tr>
<td>Human Body Model ESD Tolerance (2-kV)</td>
<td>2kV</td>
</tr>
<tr>
<td>Machine Model ESD Tolerance</td>
<td>200V</td>
</tr>
<tr>
<td>Supply Voltage</td>
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<tr>
<td>Short Circuit Current</td>
<td>150°C</td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>V⁺ - V⁻</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>V⁺ - V⁻</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
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<td>Storage Temperature Range</td>
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<tr>
<td>Lead Temperature (soldering 10 sec)</td>
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</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.

(4) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

**Operating Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
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<td>Thermal Resistance (θJC)</td>
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<tr>
<td>(θJA)</td>
<td>145°C/W</td>
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<tr>
<td>Temperature Range</td>
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</tr>
<tr>
<td>Nominal Supply Voltage</td>
<td>±2.5V to ±6V</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

(2) The maximum power dissipation is a function of T(J(MAX)), θ JA and TA. The maximum allowable power dissipation at any ambient temperature is PD = (T(J(MAX)) - TA) / θ JA. All numbers apply for packages soldered directly onto a PC board.
Electrical Characteristics(1)

V_{CC} = ±5V, A_{V} = +2V/V, R_{F} = 100Ω, R_{S} = 100Ω, R_{L} = 100Ω; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Typ</th>
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<td>dB</td>
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<td>ns</td>
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<td>3rd Harmonic Distortion</td>
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<td>G_{OL}</td>
<td>Open-Loop Gain</td>
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<td></td>
<td>dB</td>
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<td>V_{IO}</td>
<td>Input Offset Voltage</td>
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<td>±2/6</td>
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<td>mV</td>
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<td>µV/°C</td>
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<td>I_{BN}</td>
<td>Input Bias Current</td>
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<td>±20</td>
<td>±30</td>
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<td>µA</td>
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<td>D_{IBN}</td>
<td>Average Drift</td>
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<td>I_{OS}</td>
<td>Input Offset Current</td>
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<td>±6</td>
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<td></td>
<td>µA</td>
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<tr>
<td>D_{OSD}</td>
<td>Average Drift</td>
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<td></td>
<td></td>
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<td>nA/°C</td>
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<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>60/46</td>
<td>70</td>
<td></td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>57/54</td>
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<td></td>
<td>dB</td>
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<td>I_{CC}</td>
<td>Supply Current</td>
<td>Per Channel, R_{L} = ∞</td>
<td>7.5</td>
<td>9</td>
<td>12.5</td>
<td>mA</td>
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<td>R_{IN}</td>
<td>Input Resistance</td>
<td>Common-Mode</td>
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<td>C_{IN}</td>
<td>Input Capacitance</td>
<td>Common-Mode</td>
<td>200</td>
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<td>kΩ</td>
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<td>R_{OUT}</td>
<td>Output Resistance</td>
<td>Closed-Loop</td>
<td>.1</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_{J} = T_{A}. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_{J} > T_{A}. See Note 6 for information on temperature de-rating of this device.* Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.


Electrical Characteristics\(^{(1)}\) (continued)

\(V_{CC} = \pm 5\text{V}, A_V = \pm 2\text{V/V}, R_F = 100\Omega, R_O = 100\Omega, R_L = 100\Omega;\) unless otherwise specified. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
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<td>(V_O)</td>
<td>Output Voltage Range</td>
<td>(R_L = \infty)</td>
<td>±3.8</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>(V_{OL})</td>
<td></td>
<td>(R_L = 100\Omega)</td>
<td>±3.2</td>
<td>±3.1</td>
<td>±3.5</td>
<td>V</td>
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<td>CMIR</td>
<td>Input Voltage Range</td>
<td>Common- Mode</td>
<td>±3.7</td>
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<td></td>
<td>V</td>
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<tr>
<td>(I_O)</td>
<td>Output Current</td>
<td></td>
<td>±50</td>
<td>±85</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics

\[ T_A = +25^\circ, \quad A_V = +2, \quad V_{CC} = \pm 5V, \quad R_I = 100\Omega, \quad R_L = 100\Omega, \text{ unless specified} \]

Non-Inverting Frequency Response

Inverting Frequency Response

Frequency Response vs. Load Resistance

Frequency Response vs. Capacitive Load

Gain Flatness & Linear Phase

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Product Folder Links: LMH6628
Typical Performance Characteristics (continued)

$(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_i = 100\Omega, R_L = 100\Omega, \text{unless specified})$

![Channel Matching](image)

![Channel to Channel Crosstalk](image)

Pulse Response ($V_O = 2V$)

Pulse Response ($V_O = 100mV$)

2nd Harmonic Distortion vs. Output Voltage

3rd Harmonic Distortion vs. Output Voltage

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Typical Performance Characteristics (continued)

(T_A = +25°C, A_V = +2, V_CC = ±5V, R_i = 100Ω, R_L = 100Ω, unless specified)

2nd & 3rd Harmonic Distortion vs. Frequency

Figure 15.

PSRR and CMRR (±5V)

Figure 16.

PSRR and CMRR (±2.5V)

Figure 17.

Closed Loop Output Resistance (±2.5V)

Figure 18.

Closed Loop Output Resistance (±5V)

Figure 19.

Open Loop Gain & Phase (±2.5V)

Figure 20.
Typical Performance Characteristics (continued)

\( T_A = +25^\circ, \ A_V = +2, \ V_{CC} = \pm 5V, \ R_f = 100\Omega, \ R_L = 100\Omega, \) unless specified

---

**Figure 21.**
Open Loop Gain & Phase (±5V)

**Figure 22.**
Recommended \( R_S \) vs. \( C_L \)

**Figure 23.**
DC Errors vs. Temperature

**Figure 24.**
Maximum \( V_O \) vs. \( R_L \)
Typical Performance Characteristics (continued)

$(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_i = 100\Omega, R_L = 100\Omega, \text{unless specified})$

2-Tone, 3rd Order Intermodulation Intercept

Figure 25.

Voltage & Current Noise vs. Frequency

Figure 26.

Settling Time vs. Accuracy

Figure 27.
APPLICATION SECTION

LOW NOISE DESIGN
Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for $R_F$ and $R_G$, amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of $2nV/\sqrt{Hz}$ multiplied by the desired gain ($A_V$).

DC BIAS CURRENTS AND OFFSET VOLTAGES
Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage ($V_{OS}$) multiplied by the desired gain ($A_V$). Application Note OA-7 (SNOA365) offers several solutions to further reduce the output offset.

OUTPUT AND SUPPLY CONSIDERATIONS
With ±5V supplies, the LMH6628 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See Figure 22.

LAYOUT
Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1μF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 (SNOA367) for more information. Texas Instruments suggests the CLC730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)
The circuit in Figure 28 implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in Figure 29, the circuit provides a 13.1ns delay (with $R = 40.2Ω$, $C = 47pF$). $R_F$ and $R_G$ should be of equal and low value for parasitic insensitive operation.

![Figure 28. Circuit That Implements an All-pass Network Using the LMH6628](image-url)
The circuit gain is +1 and the delay is determined by the following equations.

\[ T_{\text{delay}} = 2(2RC + T_d) \]  
\[ T_d = \frac{1}{360} \frac{d\phi}{df} \]  

where \( T_d \) is the delay of the op amp at \( A_V = +1 \).

The LMH6628 provides a typical delay of 2.8ns at its -3dB point.

**FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION**

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 30, one of the LMH6628's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier \( A_2 \) (\( B_2 \)) is connected across R and forms differential amplifier for the signals transmitted by driver \( A_1 \) (\( B_1 \)). If \( R_F = R_G \), receiver \( A_2 \) (\( B_1 \)) will then reject the signals from driver \( A_1 \) (\( B_1 \)) and pass the signals from driver \( B_1 \) (\( A_1 \)).

The output of the receiver amplifier will be:

\[ V_{\text{out}} = \frac{1}{2} V_{I_{\text{out}}(A(B)}} \left[ 1 - \frac{R_f}{R_g} \right] + \frac{1}{2} V_{I_{\text{out}}(B(A)}} \left[ 1 + \frac{R_f}{R_g} \right] \]  

Figure 30. Full Duplex Transmit and Receive Using the LMH6628
Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 31 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

![Figure 31. Simultaneous Reception of Signals Transmitted at 1MHz and 10MHz](image)

**POSITIVE PEAK DETECTOR**

The LMH6628’s dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 32.

![Figure 32. LMH6628’s Dual Amplifiers Used to Implement a Unity-Gain Peak Detector Circuit](image)

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging $C_{\text{hold}}$. A plot of the circuit’s performance is shown in Figure 33 with a 1MHz sinusoidal input.

![Figure 33. Circuit's Performance With a 1MHz Sinusoidal Input](image)
A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when $V_{IN}$ is less than $V_C$. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

**ADJUSTABLE OR BANDPASS EQUALIZER**

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in Figure 34.

![Figure 34. "Boost" Equalizer Made With the LMH6628 by Summing a Bandpass Response With the Input Signal](image)

The overall transfer function is shown in Equation 4.

$$\frac{V_{out}}{V_{in}} = \left[ \frac{R_b}{K(R_a + R_b)} \right] \frac{s2\omega_o}{s^2 + s\omega_o/Q + \omega_o^2} - 1$$

(Equation 4)

To build a boost circuit, use the design equations Equation 5 and Equation 6.

$$\frac{R_aC}{2} = \frac{Q}{\omega_o}$$

(Equation 5)

$$2C(R_a || R_b) = \frac{1}{Q\omega_o}$$

(Equation 6)

Select $R_2$ and $C$ using Equation 5. Use reasonable values for high frequency circuits - $R_2$ between 10Ω and 5kΩ, $C$ between 10pF and 2000pF. Use Equation 6 to determine the parallel combination of $R_a$ and $R_b$. Select $R_a$ and $R_b$ by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance $V_{in}$ is capable of driving.

Finish the design by determining the value of $K$ from Equation 7.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}} \frac{(\omega_o)}{2KR_a} = \frac{R_2}{2KR_a} - 1$$

(Equation 7)

Figure 35 shows an example of the response of the circuit of Figure 34, where $f_o$ is 2.3MHz. The component values are as follows: $R_a = 2.1k\Omega$, $R_b = 68.5\Omega$, $R_2 = 4.22k\Omega$, $R = 500\Omega$, $KR = 50\Omega$, $C = 120pF$. 

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Product Folder Links: LMH6628
Figure 35. Example of Response of Circuit of Figure 34, Where $f_0$ is 2.3MHz
## REVISION HISTORY

Changes from Revision C (March 2013) to Revision D | Page
---|---
• Changed layout of National Data Sheet to TI format | 14
## PACKAGING INFORMATION

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<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LMH6628MA</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6628MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Q1, Q2, Q3, Q4: Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)
TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6628MAX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
**TUBE**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6628MA</td>
<td>D</td>
<td>SOIC</td>
<td>8</td>
<td>95</td>
<td>495</td>
<td>8</td>
<td>4064</td>
<td>3.05</td>
</tr>
<tr>
<td>LMH6628MA</td>
<td>D</td>
<td>SOIC</td>
<td>8</td>
<td>95</td>
<td>495</td>
<td>8</td>
<td>4064</td>
<td>3.05</td>
</tr>
<tr>
<td>LMH6628MA/NOPB</td>
<td>D</td>
<td>SOIC</td>
<td>8</td>
<td>95</td>
<td>495</td>
<td>8</td>
<td>4064</td>
<td>3.05</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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