LMH6639 190MHz Rail-to-Rail Output Amplifier with Disable

Check for Samples: LMH6639

FEATURES

- **(V_S = 5V, Typical Values Unless Specified)**
- **Supply Current (No Load) 3.6mA**
- **Supply Current (Off Mode) 400μA**
- **Output Resistance (Closed Loop 1MHz) 0.186Ω**
- **−3dB BW (A_V = 1) 190MHz**
- **Settling Time 33nsec**
- **Input Common Mode Voltage −0.2V to 4V**
- **Output Voltage Swing 40mV from Rails**
- **Linear Output Current 110mA**
- **Total Harmonic Distortion −60dBc**
- **Fully Characterized for 3V, 5V and ±5V**
- **No Output Phase Reversal with CMVR Exceeded**
- **Excellent Overdrive Recovery**
- **Off Isolation 1MHz −70dB**
- **Differential Gain 0.12%**
- **Differential Phase 0.045°**

APPLICATIONS

- **Active Filters**
- **CD/DVD ROM**
- **ADC Buffer Amplifier**
- **Portable Video**
- **Current Sense Buffer**

DESCRIPTION

The LMH6639 is a voltage feedback operational amplifier with a rail-to-rail output drive capability of 110mA. Employing TI's patented VIP10 process, the LMH6639 delivers a bandwidth of 190MHz at a current consumption of only 3.6mA. An input common mode voltage range extending to 0.2V below the V^- and to within 1V of V^+, makes the LMH6639 a true single supply op-amp. The output voltage range extends to within 30mV of either supply rail providing the user with a dynamic range that is especially desirable in low voltage applications.

The LMH6639 offers a slew rate of 172V/μs resulting in a full power bandwidth of approximately 28MHz. The LMH6639 also offers protection for the input transistors by using two anti-parallel diodes and a series resistor connected across the inputs. The T_{ON} value of 83nsec combined with a settling time of 33nsec makes this device ideally suited for multiplexing applications (see application note for details). Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic for any gain setting including +1, and excellent specifications for driving video cables including harmonic distortion of −60dBc, differential gain of 0.12% and differential phase of 0.045°

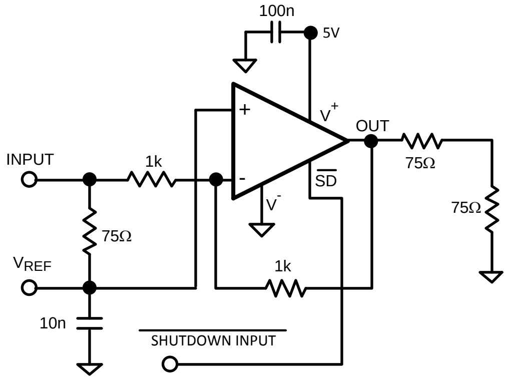

Figure 1. Typical Single Supply Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance		2KV(3)
		200V(4)
V_{IN} Differential		±2.5V
Input Current		±10mA
Supply Voltage (V^+ – V^-)		13.5V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(5)(6)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Operating Ratings(1)

Supply Voltage (V^+ to V^-)		3V to 12V
Operating Temperature Range(2)		−40°C to +85°C
Package Thermal Resistance (θ_{JA})(2)	SOT-23-6	265°C/W
	SOIC-8	190°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3V Electrical Characteristics

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 3V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min(1)	Typ(2)	Max(1)	Units
BW	−3dB BW	A_V = +1		120	170		MHz
		A_V = −1			63		
$BW_{0.1dB}$	0.1dB Gain Flatness	R_F = 2.65kΩ , R_L = 1kΩ,			16.4		MHz
FPBW	Full Power Bandwidth	A_V = +1, V_{OUT} = $2V_{PP}$, −1dB V^+ = 1.8V, V^- = 1.2V			21		MHz
GBW	Gain Bandwidth product	A_V = +1			83		MHz
e_n	Input-Referred Voltage Noise	R_F = 33kΩ	f = 10kHz		19		nV/√Hz
			f = 1MHz		16		
i_n	Input-Referred Current Noise	R_F = 1MΩ	f = 10kHz		1.30		pA/√Hz
			f = 1MHz		0.36		
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = +2, R_L = 1kΩ to $V^+/2$			−50		dBc

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 3V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
T_S	Settling Time	$V_O = 2V_{PP}$, ±0.1%		37		ns
SR	Slew Rate	$A_V = -1$(3)	120	167		V/μs
V_{OS}	Input Offset Voltage			1.01	5 **7**	mV
TC V_{OS}	Input Offset Average Drift	See(4)		8		μV/°C
I_B	Input Bias Current	See(5)		−1.02	−2.6 **−3.5**	μA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	A_V = +1, f = 1kHz, R_S = 1MΩ		6.1		MΩ
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100kΩ		1.35		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.3	−0.2 **−0.1**	V
			1.8 **1.6**	2		
CMRR	Common Mode Rejection Ratio	See(6)	72	93		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 2V_{PP}$, R_L = 2kΩ to $V^+/2$	80 **76**	100		dB
		$V_O = 2V_{PP}$, R_L = 150Ω to $V^+/2$	74 **70**	78		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	2.75	2.93		
		R_L = 50Ω to $V^+/2$, V_{ID} = 200mV	2.6	2.85		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		75	200	
		R_L = 50Ω to $V^+/2$, V_{ID} = −200mV		130	300	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$(7)	50 **35**	120		mA
		Sinking to $V^+/2$(7)	67 **40**	140		
I_{OUT}	Output Current	V_O = 0.5V from either supply		99		mA
PSRR	Power Supply Rejection Ratio	See(6)	72	96		dB
I_S	Supply Current (Enabled)	No Load		3.5	5.6 **7.5**	mA
	Supply Current (Disabled)			0.3	0.5 **0.7**	
TH_SD	Threshold Voltage for Shutdown Mode			V^+−1.59		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connect to 0V(8)		−13		μA
T_{ON}	On Time After Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	R_F = 10kΩ, f = 1kHz, $A_V = -1$		27		mΩ
		R_F = 10kΩ, f = 1MHz, $A_V = -1$		266		

(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) f ≤ 1kHz (see typical performance Characteristics)
(7) Short circuit test is a momentary test.
(8) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics

Unless otherwise specified, all limits ensured for at $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_O = V_{CM} = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min(1)	Typ (2)	Max(1)	Units
BW	−3dB BW	$A_V = +1$		130	190		MHz
		$A_V = -1$			64		
$BW_{0.1dB}$	0.1dB Gain Flatness	$R_F = 2.51k\Omega$, $R_L = 1k\Omega$,			16.4		MHz
FPBW	Full Power Bandwidth	$A_V = +1$, $V_{OUT} = 2V_{PP}$, −1dB			28		MHz
GBW	Gain Bandwidth Product	$A_V = +1$			86		MHz
e_n	Input-Referred Voltage Noise	$R_F = 33k\Omega$	f = 10kHz		19		$nV/\sqrt{Hz}$
			f = 1MHz		16		
i_n	Input-Referred Current Noise	$R_F = 1M\Omega$	f = 10KHz		1.35		$pA/\sqrt{Hz}$
			f = 1MHz		0.35		
THD	Total Harmonic Distortion	f = 5MHz, $V_O = 2V_{PP}$, $A_V = +2$ $R_L = 1k\Omega$ to $V^+/2$			−60		dBc
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$			0.12		%
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$			0.045		deg
T_S	Settling Time	$V_O = 2V_{PP}$, ±0.1%			33		ns
SR	Slew Rate	$A_V = -1$(3)		130	172		V/µs
V_{OS}	Input Offset Voltage				1.02	5 **7**	mV
TC V_{OS}	Input Offset Average Drift	See(4)			8		µV/°C
I_B	Input Bias Current	See(5)			−1.2	−2.6 **−3.25**	µA
I_{OS}	Input Offset Current				20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	$A_V = +1$, f = 1kHz, $R_S = 1M\Omega$			6.88		MΩ
C_{IN}	Common Mode Input Capacitance	$A_V = +1$, $R_S = 100k\Omega$			1.32		pF
CMVR	Common-Mode Input Voltage Range	CMRR ≥ 50dB			−0.3	−0.2 **−0.1**	V
					4	3.8 **3.6**	
CMRR	Common Mode Rejection Ratio	See(6)		72	95		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 4V_{PP}$ $R_L = 2k\Omega$ to $V^+/2$		86 **82**	100		dB
		$V_O = 3.75V_{PP}$ $R_L = 150\Omega$ to $V^+/2$		74 **70**	77		
V_O	Output Swing High	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$		4.90	4.97		V
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$		4.65	4.90		
		$R_L = 50\Omega$ to $V^+/2$, $V_{ID} = 200mV$		4.40	4.77		
	Output Swing Low	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$			25	100	mV
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$			85	200	
		$R_L = 50\Omega$ to $V^+/2$, $V_{ID} = -200mV$			190	400	

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(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) f ≤ 1kHz (see typical performance Characteristics)

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ (7)	100 **79**	160		mA
		Sinking from $V^+/2$ (7)	120 **85**	190		
I_{OUT}	Output Current	V_O = 0.5V from either supply		110		mA
PSRR	Power Supply Rejection Ratio	See (6)	72	96		dB
I_S	Supply Current (Enabled)	No Load		3.6	5.8 **8.0**	mA
	Supply Current (Disabled)			0.40	0.8 **1.0**	
TH_SD	Threshold Voltage for Shutdown Mode			V^+ −1.65		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connected to 0V (5)		−30		μA
T_{ON}	On Time after Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	R_F = 10kΩ, f = 1kHz, A_V = −1		29		mΩ
		R_F = 10kΩ, f = 1MHz, A_V = −1		253		

(7) Short circuit test is a momentary test.

±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for at T_J = 25°C, V_{SUPPLY} = ±5V, V_O = V_{CM} = GND, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1		150	228		MHz
		A_V = −1			65		
$BW_{0.1dB}$	0.1dB Gain Flatness	R_F = 2.26kΩ, R_L = 1kΩ			18		MHz
FPBW	Full Power Bandwidth	A_V = +1, V_{OUT} = $2V_{PP}$, −1dB			29		MHz
GBW	Gain Bandwidth Product	A_V = +1			90		MHz
e_n	Input-Referred Voltage Noise	R_F = 33kΩ	f = 10kHz		19		nV/√Hz
			f = 1MHz		16		
i_n	Input-Referred Current Noise	R_F = 1MΩ	f = 10kHz		1.13		pA/√Hz
			f = 1MHz		0.34		
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = +2, R_L = 1kΩ			−71.2		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L = 150Ω			0.11		%
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω			0.053		deg
T_S	Settling Time	V_O = $2V_{PP}$, ±0.1%			33		ns
SR	Slew Rate	A_V = −1 (3)		140	200		V/μs
V_{OS}	Input Offset Voltage				1.03	5 **7**	mV
TC V_{OS}	Input Offset Voltage Drift	See (4)			8		μV/°C
I_B	Input Bias Current	See (5)			−1.40	−2.6 **−3.25**	μA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V_{SUPPLY} = ±5V, V_O = V_{CM} = GND, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	A_V +1, f = 1kHz, R_S = 1MΩ		7.5		MΩ
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100kΩ		1.28		pF
CMVR	Common Mode Input Voltage Range	CMRR ≥ 50dB		−5.3	−5.2 **−5.1**	V
			3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	See(6)	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 9V_{PP}, R_L = 2kΩ	88 **84**	100		dB
		V_O = 8V_{PP}, R_L = 150Ω	74 **70**	77		
V_O	Output Swing High	R_L = 2kΩ, V_{ID} = 200mV	4.85	4.96		V
		R_L = 150Ω, V_{ID} = 200mV	4.55	4.80		
		R_L = 50Ω, V_{ID} = 200mV	3.60	4.55		
	Output Swing Low	R_L = 2kΩ, V_{ID} = −200mV		−4.97	−4.90	V
		R_L = 150Ω, V_{ID} = −200mV		−4.85	−4.55	
		R_L = 50Ω, V_{ID} = −200mV		−4.65	−4.30	
I_{SC}	Output Short Circuit Current	Sourcing to Ground(7)	100 **80**	168		mA
		Sinking to Ground(7)	110 **85**	190		
I_{OUT}	Output Current	V_O = 0.5V from either supply		112		mA
PSRR	Power Supply Rejection Ratio	See(8)	72	96		dB
I_S	Supply Current (Enabled)	No Load		4.18	6.5 **8.5**	mA
	Supply Current (Disabled)			0.758	1.0 **1.3**	
TH_SD	Threshold Voltage for Shutdown Mode			V^+ − 1.67		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connected to −5V(9)		−84		μA
T_{ON}	On Time after Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	R_F = 10kΩ, f = 1kHz, A_V = −1		32		mΩ
		R_F = 10kΩ, f = 1MHz, A_V = −1		226		

(6) f ≤ 1kHz (see typical performance Characteristics)
(7) Short circuit test is a momentary test.
(8) f ≤ 1kHz (see typical performance Characteristics)
(9) Positive current corresponds to current flowing into the device.

Connection Diagram

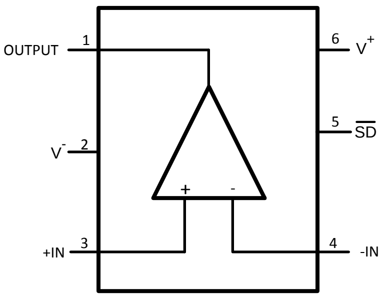


Figure 2. SOT-23-6
Top View

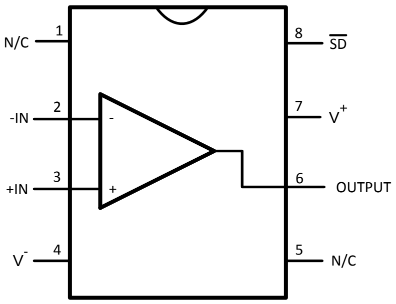


Figure 3. SOIC-8
Top View

Typical Performance Characteristics

At $T_J = 25°C$, $V^+ = +2.5$, $V^- = -2.5V$, $R_F = 330\Omega$ for $A_V = +2$, $R_F = 1k\Omega$ for $A_V = -1$. Unless otherwise specified.

Output Sinking Saturation Voltage vs. I_{OUT} for Various Temperature

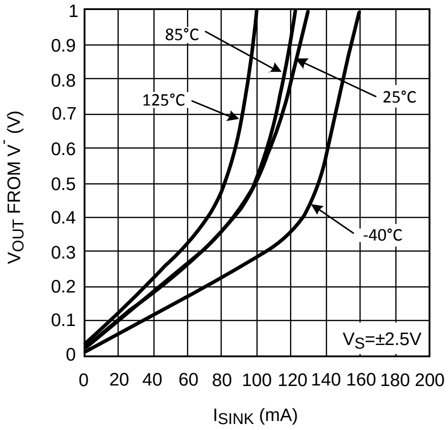


Figure 4.

Output Sourcing Saturation Voltage vs. I_{OUT} for Various Temperature

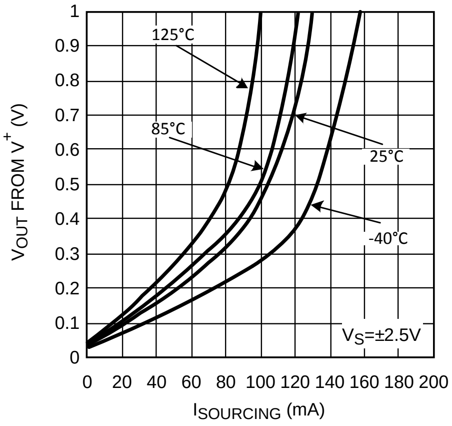


Figure 5.

Positive Output Saturation Voltage vs. V_{SUPPLY} for Various Temperature

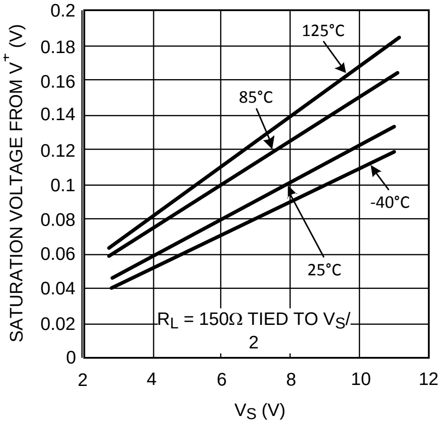


Figure 6.

Negative Output Saturation Voltage vs. V_{SUPPLY} for Various Temperature

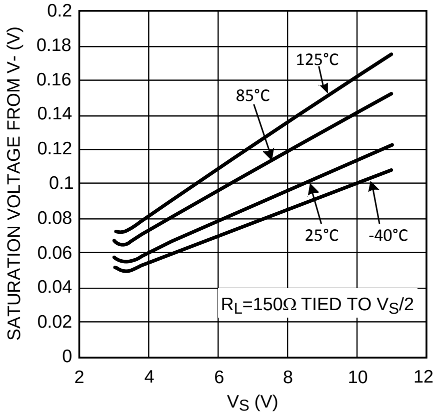


Figure 7.

V_{OUT} from V^+ vs. I_{SOURCE}

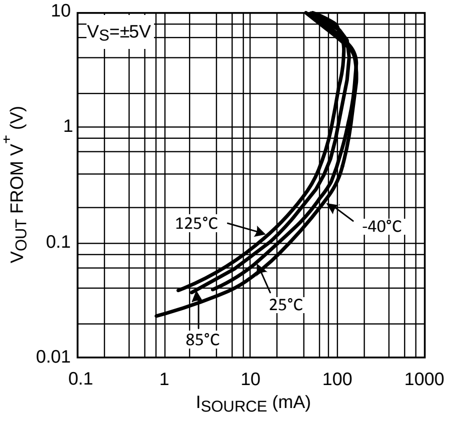


Figure 8.

V_{OUT} from V^- vs. I_{SINK}

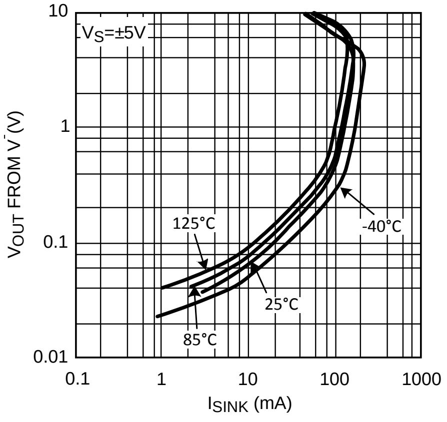


Figure 9.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

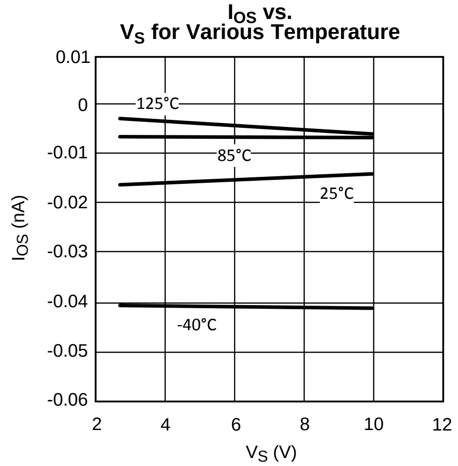

I_{OS} vs. V_S for Various Temperature

Figure 10.

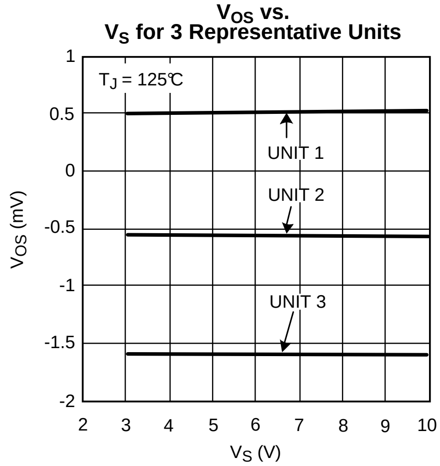

V_{OS} vs. V_S for 3 Representative Units

Figure 11.

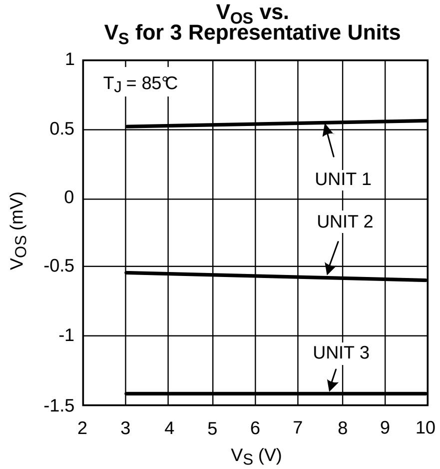

V_{OS} vs. V_S for 3 Representative Units

Figure 12.

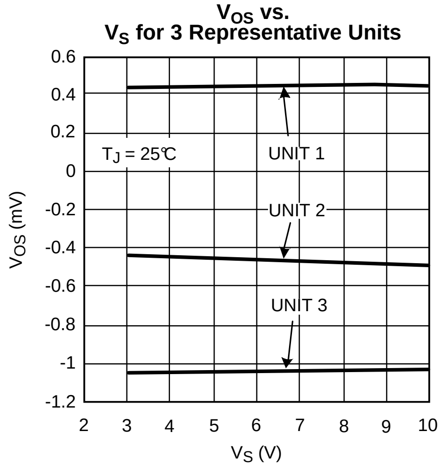

V_{OS} vs. V_S for 3 Representative Units

Figure 13.

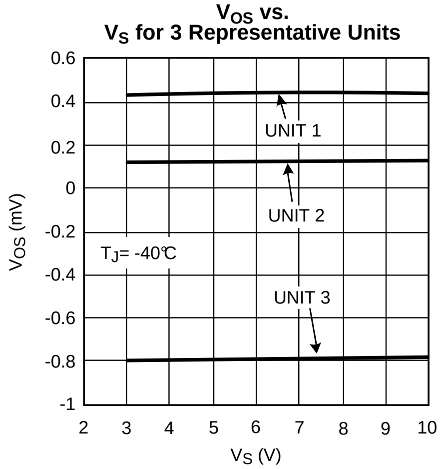

V_{OS} vs. V_S for 3 Representative Units

Figure 14.

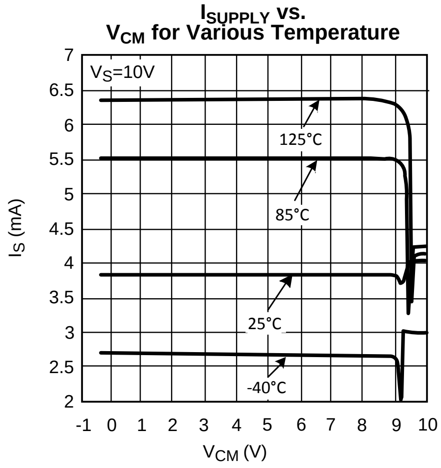
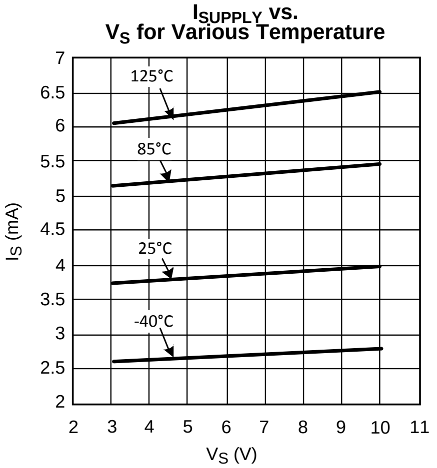

I_{SUPPLY} vs. V_{CM} for Various Temperature

Figure 15.

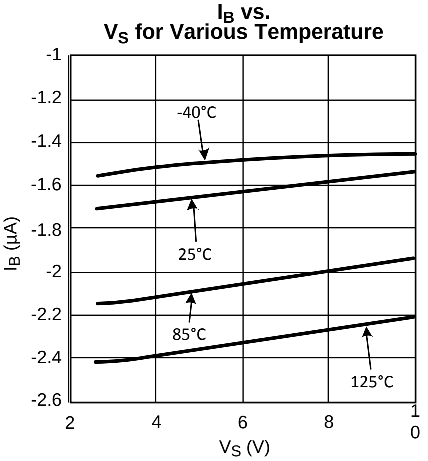
Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.



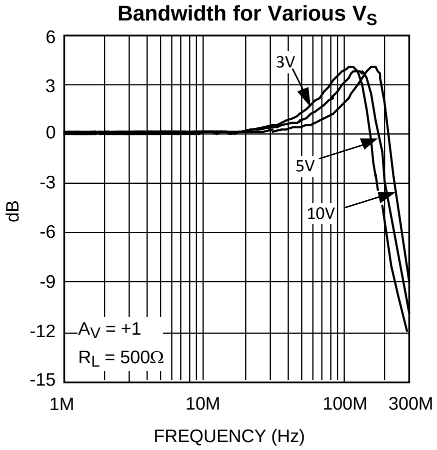
I_{SUPPLY} vs. V_S for Various Temperature

Figure 16.



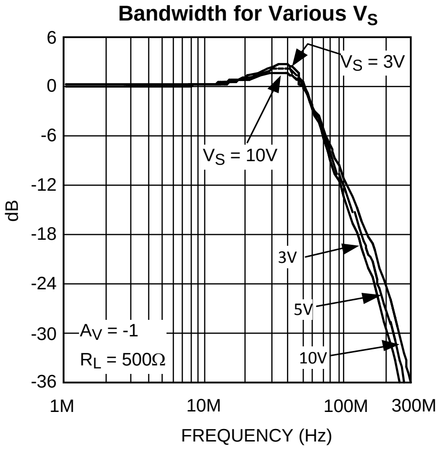
I_B vs. V_S for Various Temperature

Figure 17.



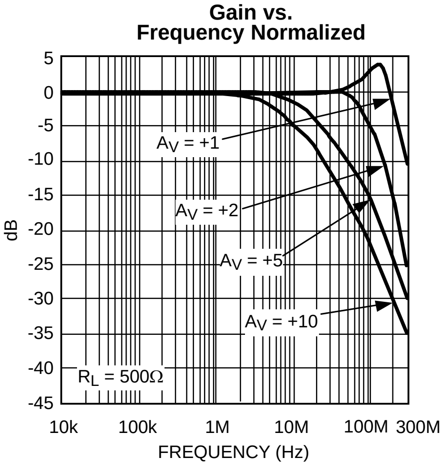
Bandwidth for Various V_S

Figure 18.



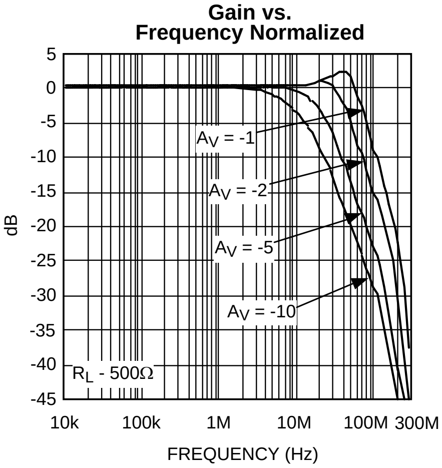
Bandwidth for Various V_S

Figure 19.



Gain vs. Frequency Normalized

Figure 20.



Gain vs. Frequency Normalized

Figure 21.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

0.1dB Gain Flatness

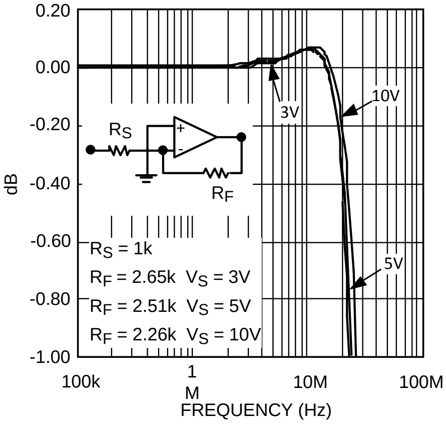


Figure 22.

Gain and phase vs. Frequency for Various Temperature

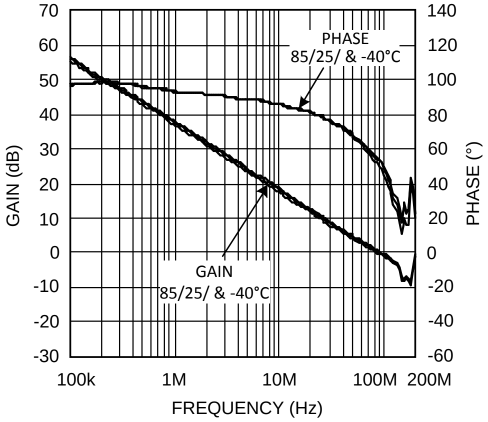


Figure 23.

Frequency Response vs. Temperature

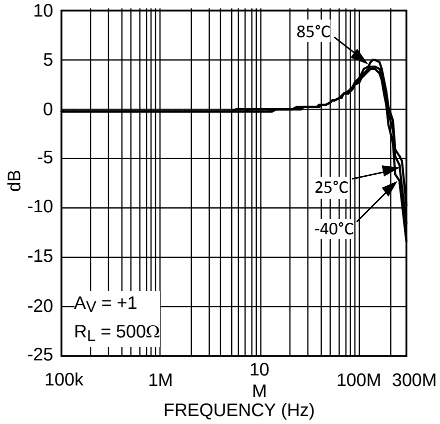


Figure 24.

Harmonic Distortion

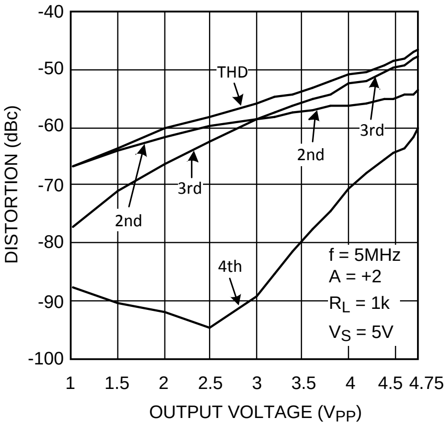


Figure 25.

Differential Gain/Phase

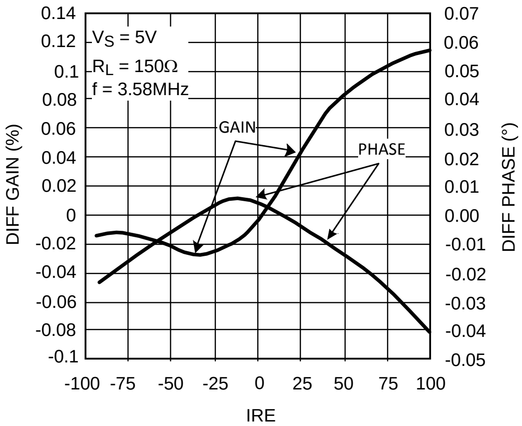


Figure 26.

On-Off Switching DC Voltage

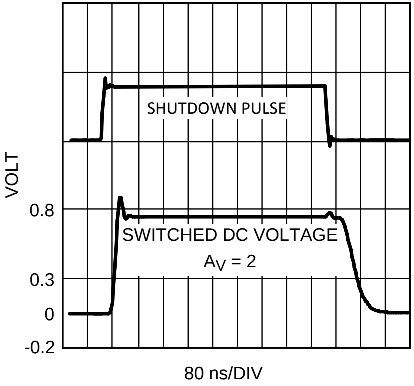


Figure 27.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

On-Off Switching 10MHz

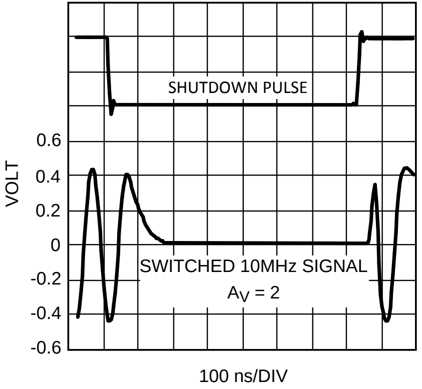


Figure 28.

Slew Rate (Positive)

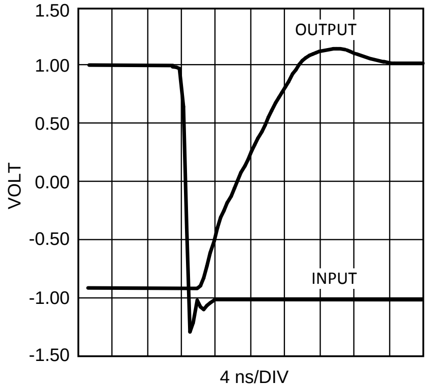


Figure 29.

Slew Rate (Negative)

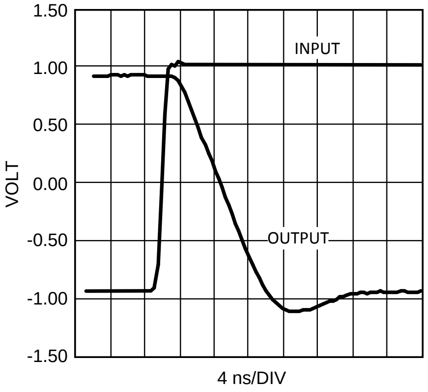


Figure 30.

On-Off Switching of Sinewave

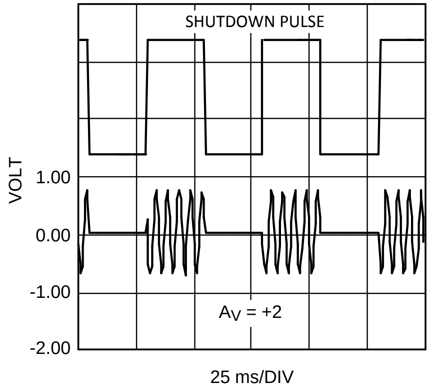


Figure 31.

Power Sweep

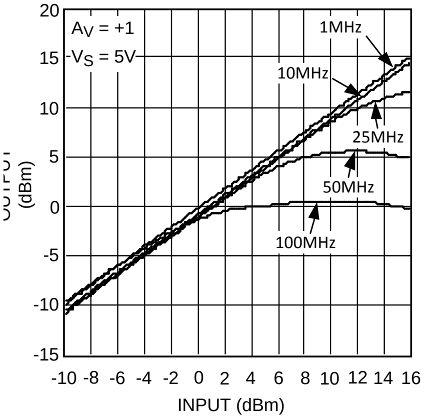


Figure 32.

CMRR vs. Frequency

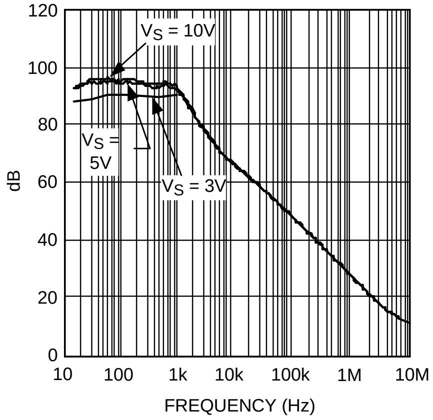


Figure 33.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

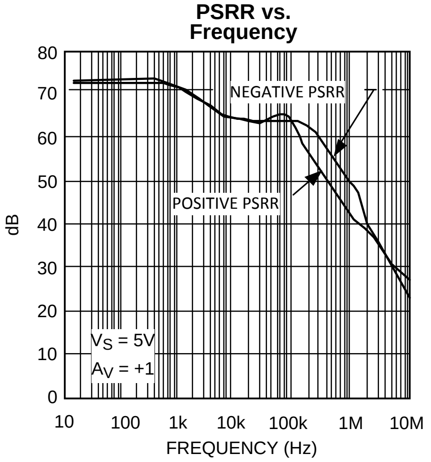

PSRR vs. Frequency

Figure 34.

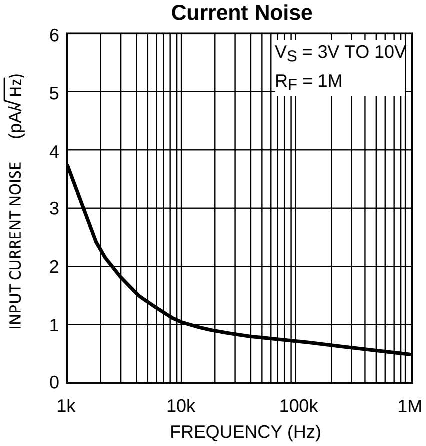

Current Noise

Figure 35.

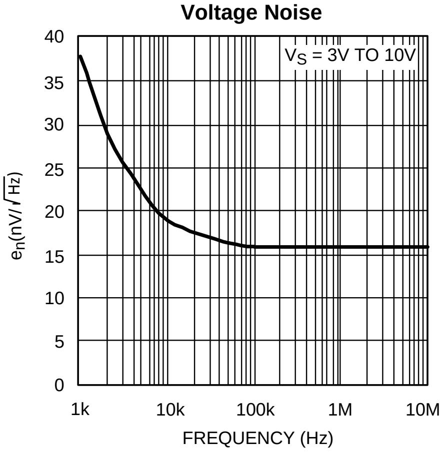

Voltage Noise

Figure 36.

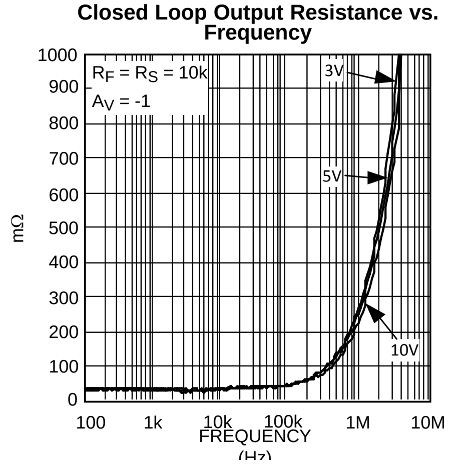

Closed Loop Output Resistance vs. Frequency

Figure 37.

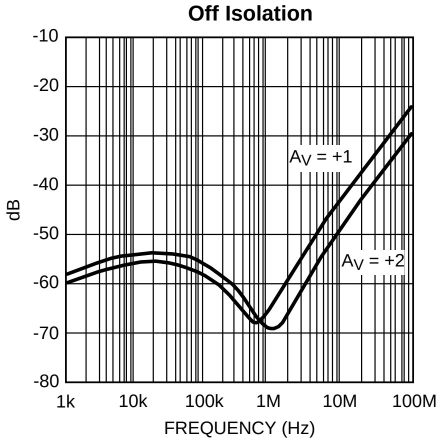

Off Isolation

Figure 38.

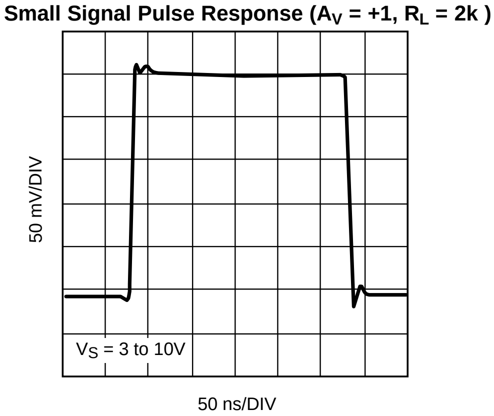

Small Signal Pulse Response (A_V = +1, R_L = 2k)

Figure 39.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

Small Signal Pulse Response (A_V = −1)

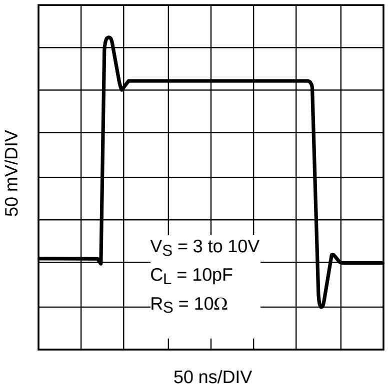


Figure 40.

Large Signal Pulse Response (R_L = 2k)

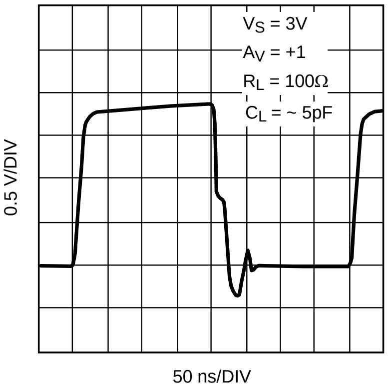


Figure 41.

Large Signal Pulse Response

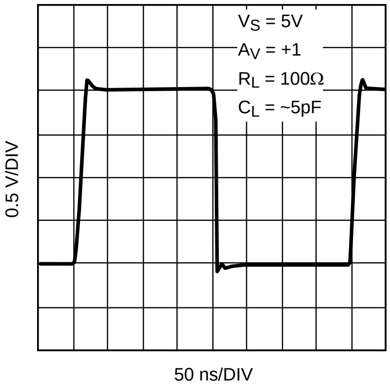


Figure 42.

Large Signal Pulse Response

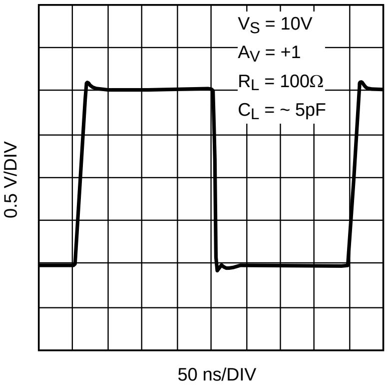


Figure 43.

APPLICATION NOTES

INPUT AND OUTPUT TOPOLOGY

All input / output pins are protected against excessive voltages by ESD diodes connected to V+ and V- rails (see Figure 44). These diodes start conducting when the input / output pin voltage approaches 1V_{be} beyond V+ or V- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in Figure 44), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching 2V_{be}. The most common situation when this occurs is when the device is put in shutdown and the LMH6639's inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases, and a portion of signal may appear at the Hi-Z output. Another possible situation for the conduction of these diodes is when the LMH6639 is used as a comparator (or with little or no feedback). In either case, it is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through the protection circuit extra series resistors can be placed. Together with the build in series resistors of several hundred ohms this extra resistors can limit the input current to a safe number depending on the used application. Be aware of the effect that extra series resistors may impact the switching speed of the device. A special situation occurs when the part is configured for a gain of +1, which means the output is directly connected to the inverting input, see Figure 45. When the part is now placed in shutdown mode the output comes in a high impedance state and is unable to keep the inverting input at the same level as the non-inverting input. In many applications the output is connected to the ground via a low impedance resistor. When this situation occurs and there is a DC voltage offset of more than 2 volt between the non-inverting input and the output, current flows from the non-inverting input through the series resistors R via the bypass diodes to the output. Now the input current becomes much bigger than expected and in many cases the source at the input cannot deliver this current and will drop down. Be sure in this situation that no DC current path is available from the non-inverting input to the output pin, or from the output pin to the load resistor. This DC path is drawn by a curved line and can be broken by placing one of the capacitors C_{IN} or C_{OUT} or both, depending on the used application.

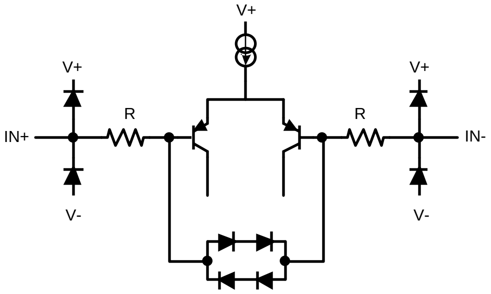


Figure 44.

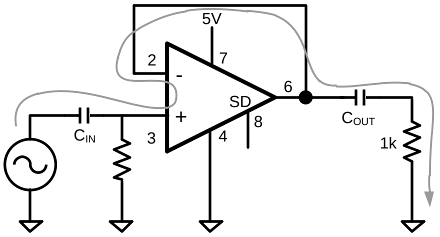
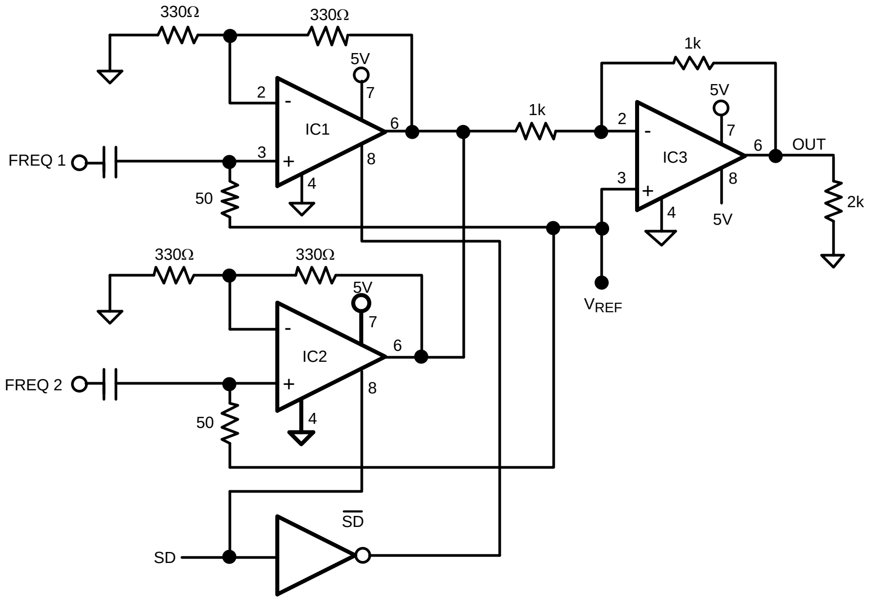


Figure 45. DC path while in shutdown

MULTIPLEXING 5 AND 10MHz

The LMH6639 may be used to implement a circuit which multiplexes two signals of different frequencies. Three LMH6639 high speed op-amps are used in the circuit of Figure 46 to accomplish the multiplexing function. Two LMH6639 are used to provide gain for the input signals, and the third device is used to provide output gain for the selected signal.



Note: Pin numbers pertain to SOIC-8 package

Figure 46. Multiplexer

Multiplexing signals “FREQ 1” and “FREQ 2” exhibit closed loop non-inverting gain of +2 each based upon identical 330Ω resistors in the gain setting positions of IC1 and IC2. The two multiplexing signals are combined at the input of IC3, which is the third LMH6639. This amplifier may be used as a unity gain buffer or may be used to set a particular gain for the circuit.

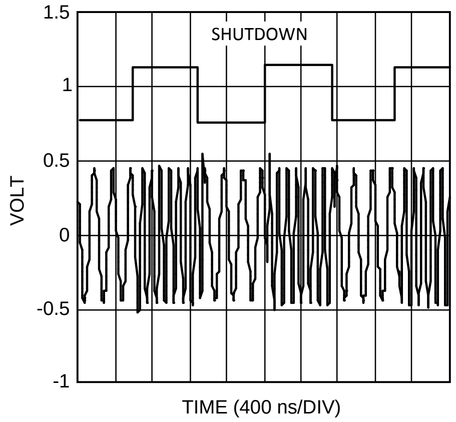


Figure 47. Switching between 5 and 10MHz

1k resistors are used to set an inverting gain of −1 for IC3 in the circuit of Figure 46. Figure 47 illustrates the waveforms produced. The upper trace shows the switching waveform used to switch between the 5MHz and 10MHz multiplex signals. The lower trace shows the output waveform consisting of 5MHz and 10MHz signals corresponding to the high or low state of the switching signal.

In the circuit of Figure 46, the outputs of IC1 and IC2 are tied together such that their output impedances are placed in parallel at the input of IC3. The output impedance of the disabled amplifier is high compared both to the output impedance of the active amplifier and the 330Ω gain setting resistors. The closed loop output resistance for the LMH6639 is around 0.2Ω. Thus the active state amplifier output impedance dominates the input node to IC3, while the disabled amplifier is assured of a high level of suppression of unwanted signals which might be present at the output.

SHUTDOWN OPERATION

With $\overline{SD}$ pin left floating, the device enters normal operation. However, since the $\overline{SD}$ pin has high input impedance, it is best tied to V^+ for normal operation. This will avoid inadvertent shutdown due to capacitive pick-up from nearby nodes. LMH6639 will typically go into shutdown when $\overline{SD}$ pin is more than 1.7V below V^+, regardless of operating supplies.

The $\overline{SD}$ pin can be driven by push-pull or open collector (open drain) output logic. Because the LMH6639's shutdown is referenced to V+, interfacing to the shutdown logic is rather simple, for both single and dual supply operation, with either form of logic used. Typical configurations are shown in Figure 48 and Figure 49 below for push-pull output:

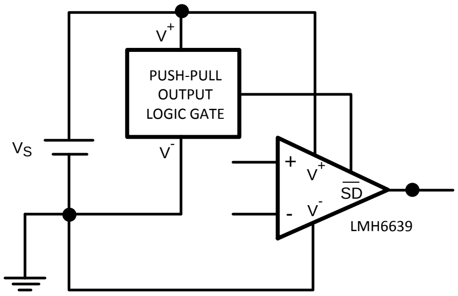


Figure 48. Shutdown Interface (Single Supply)

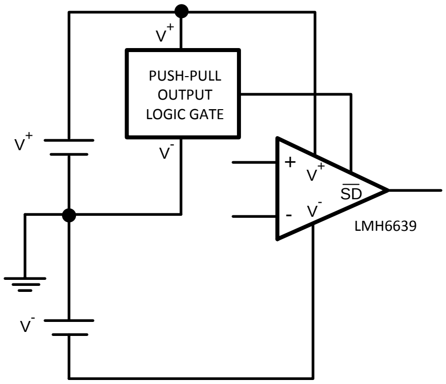


Figure 49. Shutdown Interface (Dual Supplies)

Common voltages for logic gates are +5V or +3V. To ensure proper power on/off with these supplies, the logic should be able to swing to 3.4V and 1.4V minimum, respectively.

LMH6639's shutdown pin can also be easily controlled in applications where the analog and digital sections are operated at different supplies. Figure 50 shows a configuration where a logic output, SD, can turn the LMH6639 on and off, independent of what supplies are used for the analog and the digital sections:

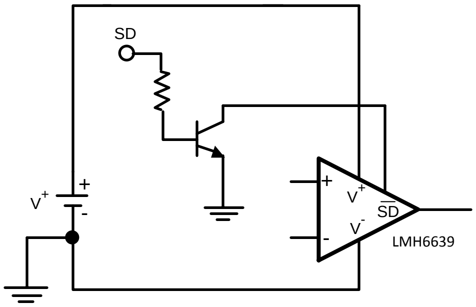


Figure 50. Shutdown Interface (Single Supply, Open Collector Logic)

The LMH6639 has an internal pull-up resistor on $\overline{SD}$ such that if left un-connected, the device will be in normal operation. Therefore, no pull-up resistor is needed on this pin. Another common application is where the transistor in Figure 50 above, would be internal to an open collector (open drain) logic gate; the basic connections will remain the same as shown.

PCB LAYOUT CONSIDERATION AND COMPONENTS SELECTION

Care should be taken while placing components on a PCB. All standard rules should be followed especially the ones for high frequency and/ or high gain designs. Input and output pins should be separated to reduce cross-talk, especially under high gain conditions. A groundplane will be helpful to avoid oscillations. In addition, a ground plane can be used to create micro-strip transmission lines for matching purposes. Power supply, as well as shutdown pin de-coupling will reduce cross-talk and chances of oscillations.

Another important parameter in working with high speed amplifiers is the component values selection. Choosing high value resistances reduces the cut-off frequency because of the influence of parasitic capacitances. On the other hand choosing the resistor values too low could "load down" the nodes and will contribute to higher overall power dissipation. Keeping resistor values at several hundreds of ohms up to several kΩ will offer good performance.

Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6639MA	8-Pin SOIC	CLC730027
LMH6639MF	SOT-23-6	CLC730116

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6639 MDC	Active	Production	DIESALE (Y) | 0	400 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	
LMH6639-MDC.A	Active	Production	DIESALE (Y) | 0	400 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	
LMH6639MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 39MA
LMH6639MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 39MA
LMH6639MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 39MA
LMH6639MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 39MA
LMH6639MF/NOPB	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A81A
LMH6639MF/NOPB.A	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A81A
LMH6639MFX/NOPB	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A81A
LMH6639MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A81A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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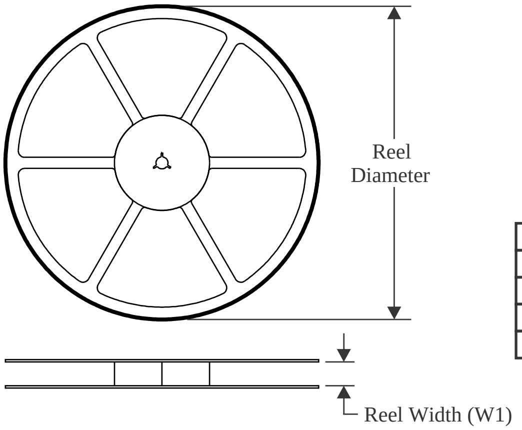
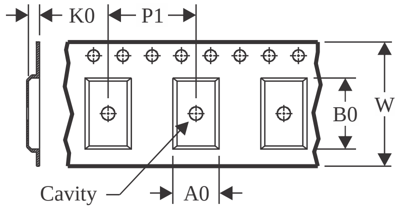
TAPE AND REEL INFORMATION

REEL DIMENSIONS

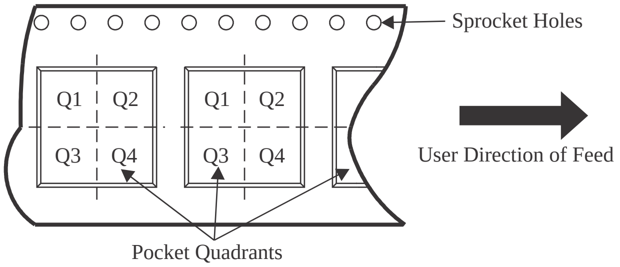


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

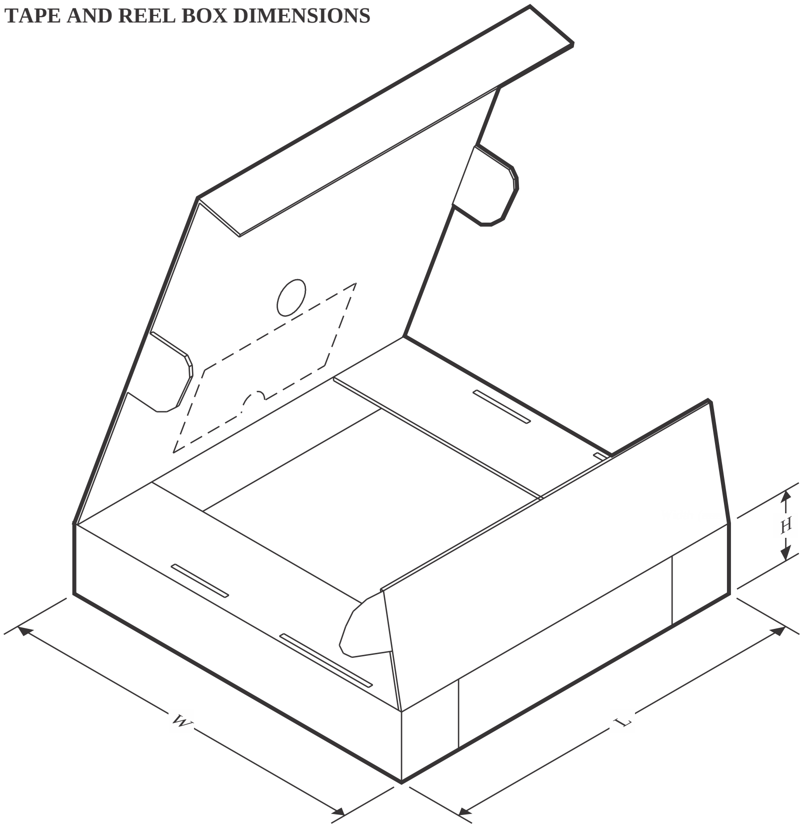
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6639MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6639MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6639MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

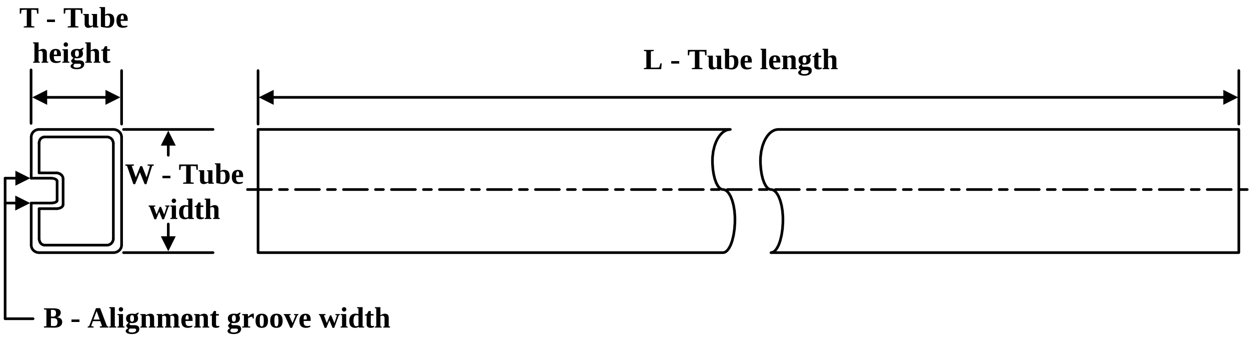
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6639MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6639MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMH6639MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0

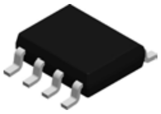
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6639MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6639MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

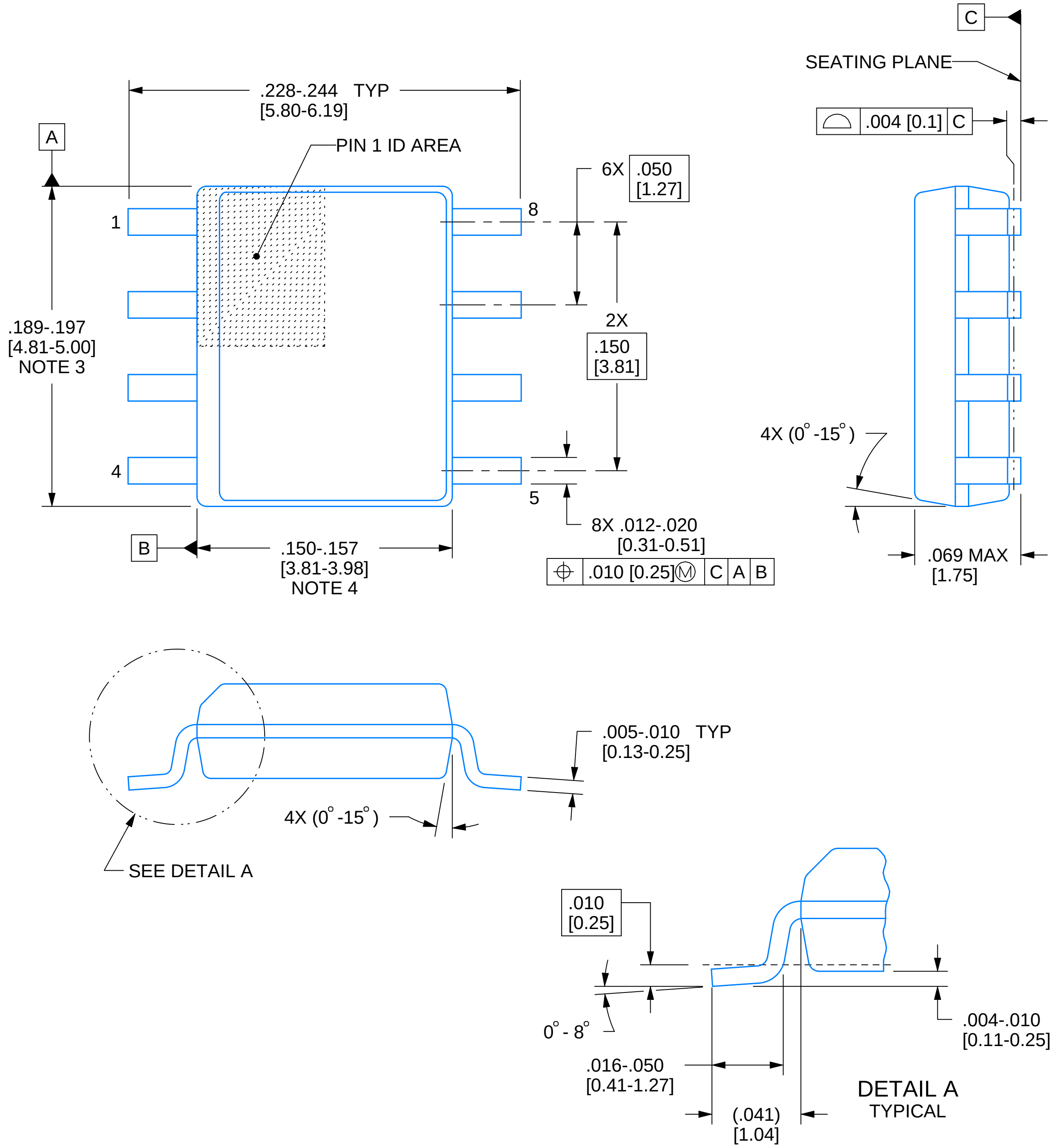
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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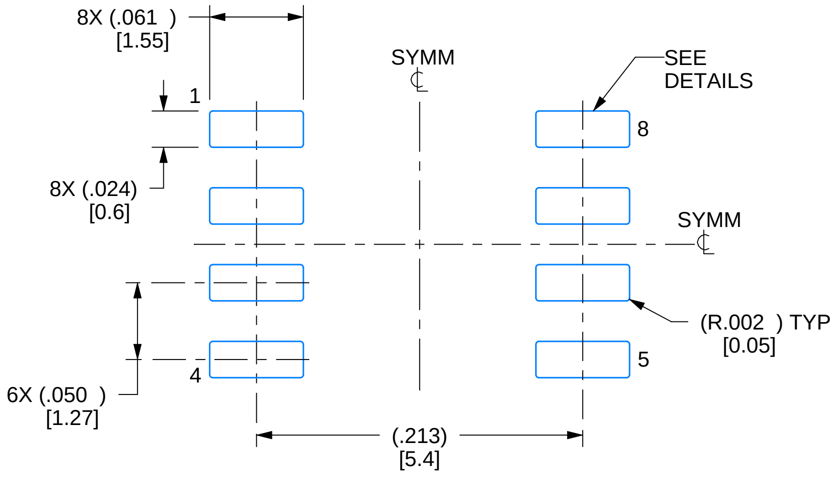
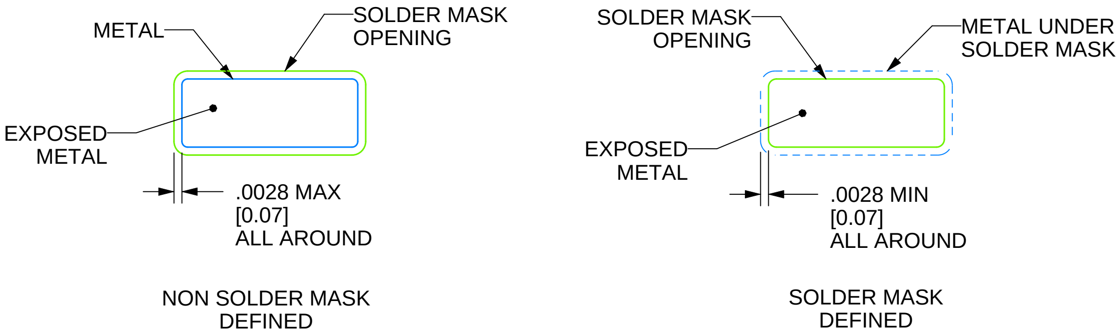
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



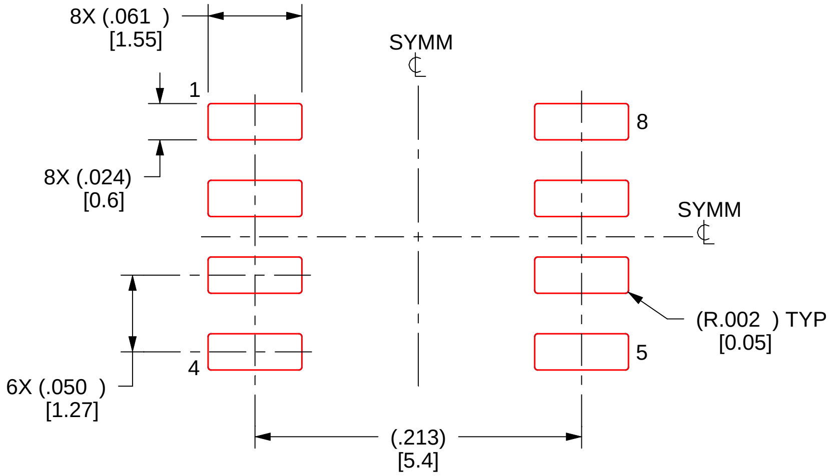
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

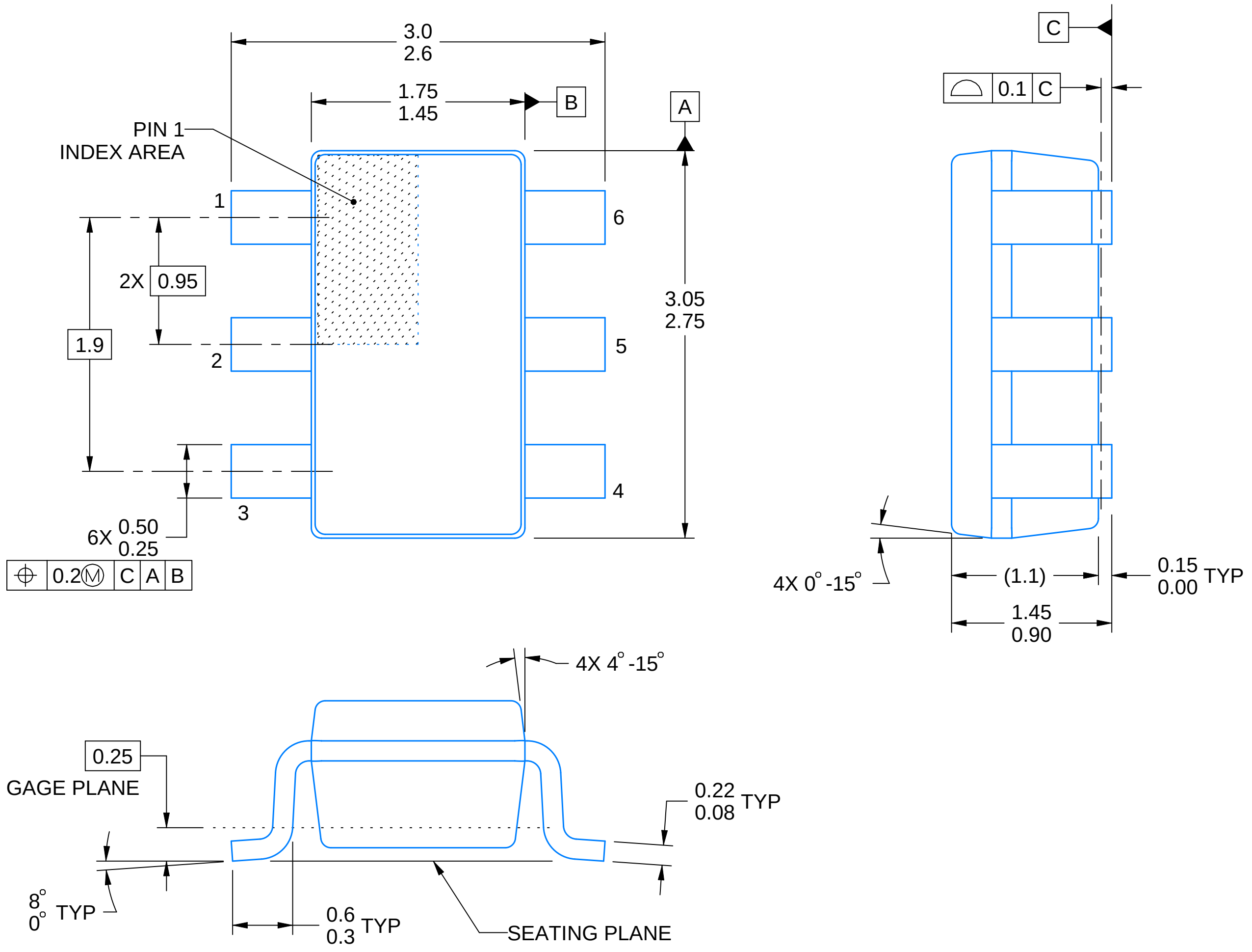
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

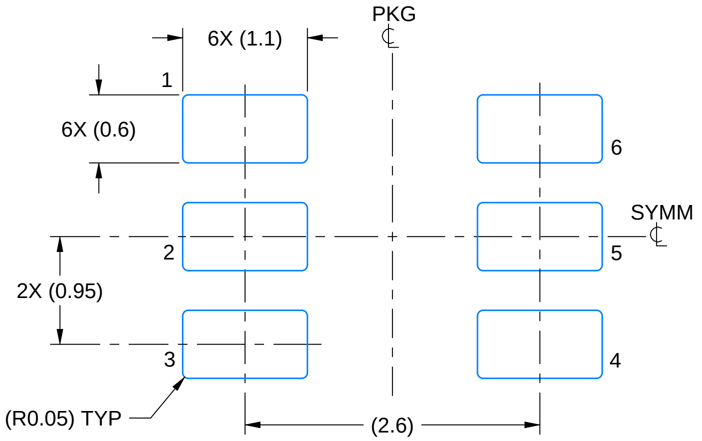
SMALL OUTLINE TRANSISTOR



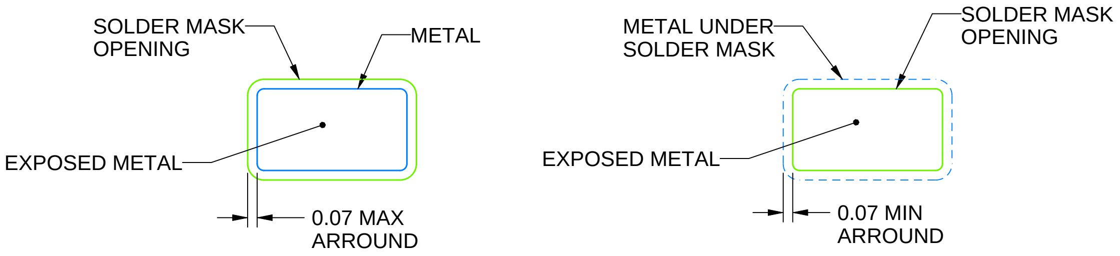
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



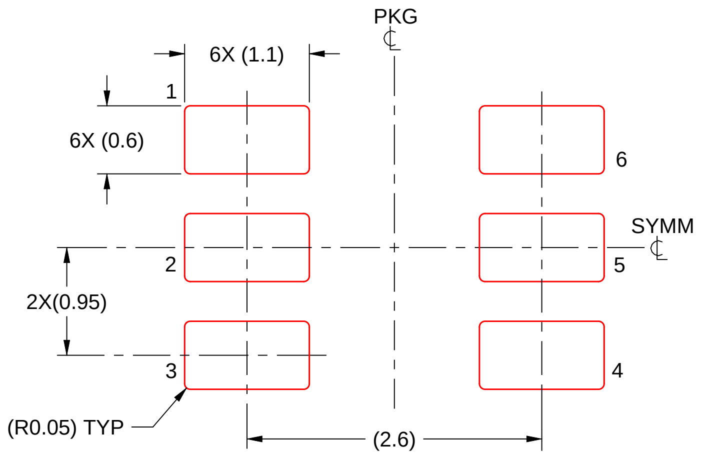
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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