LMK04616 Ultra-Low Noise and Low Power JESD204B Compliant Clock Jitter Cleaner With Dual-Loop PLLs

1 Features

- Dual-loop PLL architecture
- Ultra low noise (10 kHz to 20 MHz):
  - 48-fs RMS jitter at 1966.08 MHz
  - 50-fs RMS jitter at 983.04 MHz
  - 61-fs RMS jitter at 122.88 MHz
- –165-dBc/Hz noise floor at 122.88 MHz
- JESD204B support
  - Single shot, pulsed, and continuous SYSREF
- 16 differential output clocks in 8 frequency groups
  - Programmable output swing between 700 mVpp to 1600 mVpp
  - Each output pair can be configured to SYSREF clock output
  - 16-bit channel divider
  - Minimum SYSREF frequency of 25 kHz
  - Maximum output frequency of 2 GHz
  - Precision digital delay, dynamically adjustable
    - Digital delay (DDLY) of ½ × clock distribution path frequency (2 GHz maximum)
  - 60-ps step analog delay
  - 50% duty cycle output divides, 1 to 65535 (even and odd)
- Four reference inputs
  - Holdover mode, when inputs are lost
  - Automatic and manual switch-over modes
  - Loss-of-signal (LOS) detection
- 1.05-W typical power consumption with 16 outputs active
- Operates typically from a 1.8-V (outputs, inputs) and 3.3-V supply (digital, PLL1, PLL2_OSC, PLL2 core)
- Fully integrated programmable loop filter
- PLL2
  - PLL2 phase detector rate up to 250 MHz
  - OSCin frequency-doubler
  - Integrated low-noise VCO
- Internal power conditioning: better than –80 dBc PSRR on VDDO for 122.88-MHz differential outputs
- 3- or 4-wire SPI interface (4-wire is default)
- –40ºC to +85ºC industrial ambient temperature
- Supports 105ºC PCB temperature (measured at thermal pad)
- LMK04616: 10-mm × 10-mm NFBGA-144 package with 0.8-mm pitch

2 Applications

- Wireless infrastructure like LTE-BTS, small cells, remote radio units (RRU)
- Data converter and integrated transceiver clocking
- Networking, SONET/SDH, DSLAM
- Test and measurement

3 Description

The LMK0461x device family is the industry's highest performance and lowest power jitter cleaner with JESD204B support. The 16 clock outputs can be configured to drive eight JESD204B converters or other logic devices using device and SYSREF clocks. The 17th output can be configured to provide a signal from PLL2 or a copy from the external VCXO.

Features like fully integrated PLL1 and PLL2 loop filters, a high number of integrated LDOs, digital and analog delay, the flexibility to supply outputs with 3.3V, 2.5V and 1.8V as well as the option to generate multiple SYSREF domains simultaneously makes the device easy to use.

Not limited to JESD204B applications each of the 17 outputs can be configured for traditional clocking systems.

Device Information(1)

PART NUMBER	VCO FREQUENCY
LMK04616	5870 MHz to 6175 MHz

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

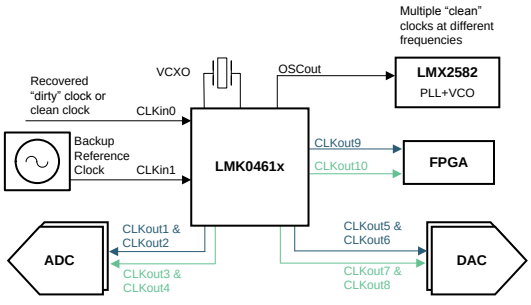


Table of Contents

4 Revision History

Changes from Revision A (May 2017) to Revision B **Page**

- Removed bulleted list under the *Dual Loop PLL Architecture* feature bullet ... 1
- Added *Ultra Low Noise* feature bullets ... 1
- Changed VCO frequency units from: 5.8 to 6.175 GHz to: 5870 MHz to 6175 MHz ... 1
- Changed VCO frequency from: 5800 MHz to: 5870 MHz ... 5
- Added PACKAGE column to device configuration information table ... 5
- Added Footnote and link to LMK04610 datasheet ... 5
- Added OSCout polarity information to the OSCout/OSCout* pin description ... 6
- Changed PLL1 phase detector maximum frequency from 40 MHz to 4 MHz ... 12
- Changed VCO tuning range minimum from: 5800 to: 5870 ... 12
- Changed V_{OD} symbol to $V_{OD,pp}$ to match mVpp units. ... 13
- Changed V_{OD} symbol to $V_{OD,pp}$ to match mVpp units. ... 14
- Added content to the *HSDS 4/6/8mA* section ... 21
- Added content to the *HCSL* section ... 22
- Changed the *VCXO Buffered Output* section ... 23
- Changed VCO frequency to 5870 MHz to 6175 MHz and updated max output frequency to 2058 MHz ... 24
- Added content to the *Programmable Output Formats* section ... 24

Revision History (continued)

- Changed *HSDS to LVPECL With Bias Voltage Vb* graphic caption ... 33
- Changed *HCSL to LVPECL* graphic ... 33
- Changed *HSDS to LVPECL With Bias Voltage Vb* graphic caption ... 34
- Changed *HSDS to LVPECL* graphic ... 34
- Added content to the *OSCout* section ... 37
- Added OSCin to OSCout differential results in clock inversion from OSCin to OSCout. ... 37
- Added Note to use TICS Pro EVM tool to calculate SDPLL loop filter values. ... 40
- Changed PLL1_PROP max from 255 to 127. ... 40
- Added PLL1_PROP_FL to table. ... 40
- Changed PLL1_INTG and PLL1_INTG_FL settings for specific case examples. ... 40
- Changed PLL1_FBCLK_INV and CLKinx_PLL1_INV for Low Pulse mode ... 41
- Changed PLL1_FBCLK_INV and CLKinx_PLL1_INV for High Pulse mode ... 41
- Deleted higher order poles information ... 41
- Added C3 maximum capacitance recommendation ... 41
- Deleted Examples of PLL1 Setting ... 41
- Changed the tuning range of the oscillator from: 5800 MHz to: 5870 MHz ... 43
- Added PLL2 DLD programming information and updated the PLLx DLD flowchart graphic ... 44
- Changed PLL1_STORAGE_CELL description from 40-bit thermometer code to 6-bit decimal value ... 47
- Clarified CTRL_VCXO represented as PLL1_STORAGE_CELL value ... 47
- Changed section from: *Low Skew Mode* to: *Zero Delay Mode (ZDM)* ... 52
- Changed CLKout7 to CLKout6 and CLKout8 to CLKout9 for zero delay feedback clocks. ... 52
- Changed Set Prop/Store-CP from "fast lock" value to "non-fast lock" value at end of flowchart ... 54
- Deleted references to tunable crystal ... 55
- Deleted use of external VCO for PLL2. ... 55
- Added register 0x85, 0x86, 0xF6, and 0xAD for PLL2 DLD to recommended programming sequence ... 58
- Changed PLL1_PROP from 8 bit to 7 bit field in register map ... 61
- Changed PLL1_PROP_FL from 8 bit to 7 bit field in register map ... 61
- Changed PLL1_STORAGE_CELL 40 bit to 6 bit field. Not a 40 bit thermometer code. Set registers 0x66, 0x67, 0x68, 0x69 to RSRVD in register map ... 61
- Changed PLL2_PROP from 8 bit to 6 bit field in register map ... 62
- Changed PLL2_INTG from 8 bit to 5 bit field in register map ... 62
- Added register 0xAC for field PLL1_TSTMODE_REF_FB_EN in register map ... 63
- Added register 0xAD for fields RESET_PLL2_DLD, PLL2_TSTMODE_REF_FB_EN, and PD_VCO_LDO in register map ... 63
- Added register 0xF6 for PLL2_DLD_EN in register map ... 63
- Changed channel 7 and 8 to channel 6 and 9 for feedback enable FBBUF_CHx_EN in register map ... 64
- Deleted unused DEVID values ... 66
- Changed reset value for CHIPID from 0x1 to 0x3 ... 66
- Changed reset value for CHIPVER from 0x1 to 0x15 ... 66
- Changed PLL1_PROP from 8 bit to 7 bit field in register definition ... 88
- Changed PLL1_PROP_FL from 8 bit to 7 bit field in register definition ... 88
- Deleted 'PLL1 Start-up in Holdover.' text from the PLL1_STARTUP_HOLDOVER_EN bit description ... 89
- Changed PLL2_PROP field size from 8 bits to 6 bits in register definition ... 93
- Changed PLL2_INTG field from 8 bit to 5 bit field in register 0x80 definition ... 95
- Added definition and requirement for setting PLL2_LD_WNDW_SIZE = 0 in register 0x85 definition ... 96
- Added definition and requirement for setting PLL2_LD_WNDW_SIZE_INITIAL = 0 in register 0x86 definition ... 96

Revision History (continued)

- Added note for using PLL1/2 REF/FB(SYS) status output for STAT0 100
- Added note for using PLL1/2 REF/FB(SYS) status output for STAT1 100
- Added note for using PLL1/2 REF/FB(SYS) status output for SYNC 103
- Added register 0xAC to register description. New field PLL1_TSTMODE_REF_FB_EN. 104
- Added register 0xAD to register description. New fields RESET_PLL2_DLD, PLL2_TSTMODE_REF_FB_EN, and PD_VCO_LDO..... 104
- Added register 0xF6 to register description. New field PLL2_DLD_EN 105
- Added register 0xF7 to register description. New field PLL2_DUAL_LOOP_EN 106
- Changed Channel 6 and 9 FBClock Buffers from: Low Skew to: Zero Delay Mode..... 118
- Changed OUTCH8 and OUTCH7 to OUTCH9 and OUTCH6..... 118
- Changed registers for WINDOW SIZE and LOCK COUNT. Updated equation to reflect the more general WINDOW SIZE and LOCK COUNT names and count frequency. Removed reference to holdover. Updated descriptive text 122
- Updated minimum lock time calculation example to reflect updated register names and count frequency 122
- Simplified HSDS format description 127

Changes from Original (March 2017) to Revision A **Page**

- Changed text from: –70-dBc PSRR to: –80dBc PSRR on VDDO..... 1
- Changed SPI Interface default from: 3-wire to: 4-wire 1
- Changed VCO frequency from: 5.8 to 6.2 GHz to: 5.8 to 6.175 GHz 1
- Changed VCO frequency from: 6200 MHz to: 6175 MHz 5
- Removed tablenote from the doubler input frequency parameter..... 12
- Changed VCO tuning range maximum from: 6200 to: 6175..... 12
- Changed tablenote text from: ATE tested at 2949.12 MHz to: ATE tested at 258-MHz Phase detector frequency..... 12
- Removed tablenote from the output frequency parameter..... 14
- Changed output frequency maximum from: 800 MHz to: 1000 MHz 14
- Added content to the *Driving CLKin and OSCin Pins With a Differential Source* section..... 30
- Updated Figure 36 40
- Changed the tuning range of the oscillator from: 6200 MHz to: 6175 MHz 43
- Updated Figure 48 53

5 Device Comparison Table

Table 1. Device Configuration Information

PART NUMBER	REFERENCE INPUTS	OSCout (BUFFERED OSCin CLOCK) AC-LVPECL/ AC-LVDS/ LVCMOS	PLL2 PROGRAMMABLE HCSL/HSDS OUTPUTS	VCO FREQUENCY	PACKAGE
LMK04610	2	1	10	5870 to 6175 MHz	VQFN-56(1)
LMK04616	4	1	16	5870 to 6175 MHz	NFBGA-144

(1) Refer to LMK04610 datasheet.

6 Pin Configuration and Functions

ZCR Package
144-Pin NFBGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	CLKout 14N		CLKout 13N	CLKout 12N		CLKout 11N	CLKout 10N		CLKout 9P	CLKout 8P		OSC INP
B	CLKout 14P		CLKout 13P	CLKout 12P		CLKout 11P	CLKout 10P		CLKout 9N	CLKout 8N		OSC INN
C	CLKout 15N	VDDO 14-15			VDDO 12-13			VDDO 10-11		VDDO 8_9		
D	CLKout 15P		NC	NC	NC					CTRL VCXO		OSC OUTP
E	STATUS 0		VDD_ PLL2_ OSC	PLL2_V COLDO _CAP					PLL1_C AP		VDD OSC	OSC OUTN
F	STATUS 1			PLL2_L DO_CA P					VDD PLL1			
G	SCL	SDIO	VDD_ PLL2_C ORE							CLKin SEL	CLKin0 N	CLKin0P
H	SYNC	SCS		VDD CORE						VDD _IO	CLKin1 N	CLKin1P
J	CLKout 0P	RESETN										CLKin2P
K	CLKout 0N	VDDO 0-1			VDDO 2-3			VDDO 4-5		VDDO 6-7		CLKin2 N
L	CLKout 1P		CLKout 2P	CLKout 3P		CLKout 4P	CLKout 5P		CLKout 6N	CLKout 7P		CLKin3P
M	CLKout 1N		CLKout 2N	CLKout 3N		CLKout 4N	CLKout 5N		CLKout 6P	CLKout 7N		CLKin3 N

OUTPUT | GND | VDD | INPUT | STATUS/Control
CAPS | OTHER | OSCin/out

A. LMK04616

Pin Functions: LMK04616 (1)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
POWER				
VDD_CORE	H4	—	P	3.3-V power supply for core
VDD_IO	H10	—	P	1.8-V to 3.3-V power supply for input block
VDD_OSC	E11	—	P	1.8-V to 3.3-V power supply for OSCout
VDD_PLL1	F9	—	P	3.3-V power supply for PLL 1
VDD_PLL2CORE	G3	—	P	3.3-V power supply for PLL 2
VDD_PLL2OSC	E3	—	P	3.3-V power supply for PLL2 VCO
VDDO_0/1	K2	—	P	1.8-V to 3.3-V power supply for CLKout0 and CLKout1
VDDO_2/3	K5	—	P	1.8-V to 3.3-V power supply for CLKout2 and CLKout3
VDDO_4/5	K8	—	P	1.8-V to 3.3-V power supply for CLKout4 and CLKout5
VDDO_6/7	K10	—	P	1.8-V to 3.3-V power supply for CLKout6 and CLKout7
VDDO_8/9	C10	—	P	1.8-V to 3.3-V power supply for CLKout8 and CLKout9
VDDO_10/11	C8	—	P	1.8-V to 3.3-V power supply for CLKout10 and CLKout11
VDDO_12/13	C5	—	P	1.8-V to 3.3-V power supply for CLKout12 and CLKout13
VDDO_14/15	C2	—	P	1.8-V to 3.3-V power supply for CLKout14 and CLKout15
VSS	A2, A5, A8, A11, B2, B5, B8, B11, C3, C4, C6, C7, C9, C11, C12, D2, D6, D7, D8, D9, D11, E2, E5, E6, E7, E8, E10, F2, F3, F5, F6, F7, F8, F10, F11, F12, G4, G5, G6, G7, G8, G9, H3, H5, H6, H7, H8, H9, J3, J4, J5, J6, J7, J8, J9, J10, J11, K3, K4, K6, K7, K9, K11, L2, L5, L8, L11, M2, M5, M8, M11	—	GND	Die attach pad. The DAP is an electrical connection and provides a thermal dissipation path. For proper electrical and thermal performance of the device, the DAP must be connected to the PCB ground plane.
PLL				
CTRL_VCXO	D10	—	Analog	VCXO control output
PLL1_CAP	E9	—	Analog	PLL1 LDO capacitance – 10-µF external
PLL2_LDO_CAP	F4	—	Analog	PLL2 LDO capacitance – 10-µF external
PLL2_VCO_LDO_CAP	E4	—	Analog	PLL2 LDO capacitance – 10-µF external
INPUT BLOCK				
OSCin	A12	I	Analog	Feedback to PLL1, reference input to PLL2. Accepts both differential or single-ended (VCXO)
OSCin*	B12			
CLKin_SEL	G10	I/O	CMOS	Manual reference input selection for PLL1 weak pullup resistor.
CLKin0	G12	I	Analog	Reference clock input port 0 for PLL1.
CLKin0*	G11			
CLKin1	H12	I	Analog	Reference clock input port 1 for PLL1.
CLKin1*	H11			
CLKin2	J12	I	Analog	Reference clock input port 2 for PLL1.
CLKin2*	K12			
CLKin3	L12	I	Analog	Reference clock input port 3 for PLL1.
CLKin3*	M12			
OUTPUT BLOCK				
OSCout	D12	O	Programmable	Buffered output of OSCin port. When using differential output mode, OSCout polarity is reversed from OSCin polarity.
OSCout*	E12			
CLKout0	J1	O	Programmable	Differential clock output pair 0.
CLKout0*	K1			

(1) See *Pin Connection Recommendations* section for recommended connections.

Pin Functions: LMK04616[1] (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
CLKout1	L1	O	Programmable	Differential clock output pair 1.
CLKout1*	M1			
CLKout2	L3	O	Programmable	Differential clock output pair 2.
CLKout2*	M3			
CLKout3	L4	O	Programmable	Differential clock output pair 3.
CLKout3*	M4			
CLKout4	L6	O	Programmable	Differential clock output pair 4.
CLKout4*	M6			
CLKout5	L7	O	Programmable	Differential clock output pair 5.
CLKout5*	M7			
CLKout6	M9	O	Programmable	Differential clock output pair 6.
CLKout6*	L9			
CLKout7	L10	O	Programmable	Differential clock output pair 7.
CLKout7*	M10			
CLKout8	A10	O	Programmable	Differential clock output pair 8.
CLKout8*	B10			
CLKout9	A9	O	Programmable	Differential clock output pair 9.
CLKout9*	B9			
CLKout10	B7	O	Programmable	Differential clock output pair 10.
CLKout10*	A7			
CLKout11	B6	O	Programmable	Differential clock output pair 11.
CLKout11*	A6			
CLKout12	B4	O	Programmable	Differential clock output pair 12.
CLKout12*	A4			
CLKout13	B3	O	Programmable	Differential clock output pair 13.
CLKout13*	A3			
CLKout14	B1	O	Programmable	Differential clock output pair 14.
CLKout14*	A1			
CLKout15	D1	O	Programmable	Differential clock output pair 15.
CLKout15*	C1			
DIGITAL CONTROL / INTERFACES				
NC	D3, D4, D5	—	Analog	Do not connect.
RESETN	J2	I	CMOS	Device reset input
SCL	G1	I	CMOS	SPI serial clock.
SCS*	H2	I	CMOS	SPI serial chip select (active low).
SDIO	G2	I/O	CMOS	SPI serial data input and output
STATUS0	E1	I/O	CMOS	Programmable status pin. See *STATUS0/1 and SYNC Pin Functions* for more details.
STATUS1	F1	I/O	CMOS	Programmable status pin. See *STATUS0/1 and SYNC Pin Functions* for more details.
SYNC	H1	I/O	CMOS	Synchronization of output divider, definition of OSCout divider or programmable status pin. See *STATUS0/1 and SYNC Pin Functions* for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
VDD_IO	Supply voltage for input(3)	–0.3	3.6	V
VDD_CORE	Supply voltage for digital(3)	–0.3	3.6	V
VDD_PLL1	Supply voltage for PLL1(3)	–0.3	3.6	V
VDD_PLL2CORE	Supply voltage for PLL2 core	–0.3	3.6	V
VDD_PLL2OSC	Supply voltage for PLL2 OSC(3)	–0.3	3.6	V
VDD_OSC	Supply voltage for OSCout(3)	–0.3	3.6	V
VDDO_x	Supply voltage for CLKoutX	–0.3	3.6	V
V_{IN_clk}	Input voltage for CLKinX and OSCin(3)	–0.3	(V_{DD_IO} + 0.3)	V
V_{IN_gpio}	Input voltage for digital and status pins (CLKin_SEL, SCK, SDIO, SCS*, STATUSx, SYNC, RESETN)	–0.3	2.1	V
T_L	Lead temperature (solder 4 s)		+260	°C
T_J	Junction temperature		125	°C
I_{IN}	Input current		20	mA
MSL	Moisture sensitivity level		3	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.
(3) Never to exceed 3.6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±250	
		Machine model	±150	

(1) This device is a high performance RF integrated circuit with an ESD rating up to 2-kV human-body model, up to 150-V machine model, and up to 250-V charged-device model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature			125	°C
T_A	Ambient temperature	–40	25	85	°C
T_{PCB}	PCB temperature (measured at thermal pad)			105	°C
VDD_IO	Supply voltage for input	1.7	1.8	3.465	V
VDD_CORE	Supply voltage for digital	3.135	3.3	3.465	V
VDD_PLL1	Supply voltage for PLL1	3.135	3.3	3.465	V
VDD_PLL2CORE	Supply voltage for PLL2 Core	3.135	3.3	3.465	V
VDD_PLL2OSC	Supply voltage for PLL2 OSC	3.135	3.3	3.465	V
VDD_OSC	Supply voltage for OSCout	1.7	1.8	3.465	V
VDDO_x	Supply voltage for CLKoutX	1.7	1.8	3.465	V

7.4 Thermal Information

THERMAL METRIC[1]			LMK04616 ZCR (NFBGA) 176 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]		45.0	°C/W
		14-layer, 200-mm × 150-mm board, 144 thermal vias, airflow = 0 LFM	23.3	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]		12.5	°C/W
		14-layer, 200-mm × 150-mm board, 144 thermal vias, airflow = 0 LFM	0.1	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]		25.2	°C/W
		14-layer, 200-mm × 150-mm board, 144 thermal vias, airflow = 0 LFM	18.3	
ψ_{JT}	Junction-to-top characterization parameter[5]		0.2	°C/W
		8-layer, 200-mm × 150-mm board, 21 thermal vias, airflow = 0 LFM	27.7	
ψ_{JB}	Junction-to-board characterization parameter[6]		24.9	°C/W
		8-layer, 200-mm × 150-mm board, 21 thermal vias, airflow = 0 LFM	0.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[7]		n/a	°C/W
		8-layer, 200-mm × 150-mm board, 21 thermal vias, airflow = 0 LFM	21.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Digital Input and Output Characteristics (CLKin_SEL, STATUSx, SYNC, RESETN)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (STATUSX, SYNC)	I_{OH} = –500 µA 1.8-V mode	1.2		1.9	V
V_{OL}	Low-level output voltage (STATUSX, SYNC)	I_{OL} = 500 µA 1.8-V mode	0		0.6	V
V_{OH}	High-level output voltage (SDIO)	I_{OH} = –500 µA during SPI read 1.8-V mode	1.2		1.9	V
V_{OL}	Low-level output voltage (SDIO)	I_{OL} = 500 µA during SPI read 1.8-V mode	0		0.6	V
V_{IH}	High-level input voltage (CLKin_SEL, STATUSX, SYNC, RESETN, SCK, SDIO, SCS*)		1.3		1.9	V
V_{IL}	Low-level input voltage (CLKin_SEL, STATUSX, SYNC, RESETN, SCK, SDIO, SCS*)		0		0.45	V
V_{MID}	Mid-level input voltage (CLKin_SEL, SYNC)		0.8		1.0	V
I_{IH}	High-level input current V_{IH} = 1.8 V (CLKin_SEL, RESETN)	Internal pullup	–10		10	µA
		Internal pulldown	10		60	
I_{IL}	Low-level input current V_{IL} = 0 V (CLKin_SEL, RESETN)	Internal pullup	–60		–10	µA
		Internal pulldown	–10		10	
I_{IH}	High-level input current (SCK, SDIO, SCS*, SYNC)	V_{IH} = 1.8 V	–10		10	µA
I_{IL}	Low-level input current (SCK, SDIO, SCS*, SYNC)	V_{IL} = 0	–10		10	µA
t_{LOW}		RESETN pin held low for device reset	25			ns

7.6 Clock Input Characteristics (CLKinX)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKin}	Clock input frequency	Single-ended, DC-coupled (1)	5		500	MHz
		Single-ended, AC-coupled (1)	5		500	
		Differential, AC-coupled (2)	5		600	
$SLEW_{DIFF}$	Differential input slew rate (3)	20% to 80%	0.2	6		V/ns
$SLEW_{SE}$	Single-ended input slew rate (3)	20% to 80%	0.1	3		V/ns
V_{CLKin}	Single-ended input voltage	DC-coupled to CLKinX; CLKinX* AC-coupled to Ground	0.5		3.3	Vpp
		AC-coupled to CLKinX; CLKinX* AC-coupled to Ground	0.5		3.3	

(1) See *Driving CLKin and OSCin Pins With a Single-Ended Source*.
(2) See *Driving CLKin and OSCin Pins With a Differential Source*.
(3) To meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended differential slew rate for all input clocks is 3 V/ns; this is especially true for single-ended clocks. Phase noise performance begins to degrade as the clock input slew rate is reduced. However, the device functions at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) are less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, TI also recommends using the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.

Clock Input Characteristics (CLKinX) (continued)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;

1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ID,pp}$	Peak-to-peak differential input voltage (4) See Figure 9	AC-coupled	0.4		3.3	Vpp
IDC	Input duty cycle		45%	50%	55%	
V_{Noise}	Rejected input voltage noise during LOS condition	No LOS state change with single-ended, peak-to-peak input voltage noise injects to either CLKinX or CLKinX* or to both in phase. Measured with 1-MHz sinusoidal signal			40	mV

(4) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.

7.7 Clock Input Characteristics (OSCin)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSCin}	PLL2 reference input (1)	Single-ended, AC-coupled (2)	10		300	MHz
		Differential, AC-coupled (3)	10		600	
$SLEW_{DIFF}$	Differential input slew rate (4)	20% to 80%	0.2	6		V/ns
$SLEW_{SE}$	Single-ended input slew rate (4)	20% to 80%	0.1	3		V/ns
V_{OSCin}	Single-ended input voltage	AC-coupled to OSCin; OSCin* AC-coupled to Ground	0.5		3.3	Vpp
$V_{ID,pp}$	Peak-to-peak differential input voltage (5) See Figure 9	AC-coupled	0.4		3.3	Vpp
IDC	Input duty cycle		45%	50%	55%	

(1) F_{OSCin} maximum frequency assured by characterization. Production tested at 122.88 MHz.
(2) See *Driving CLKin and OSCin Pins With a Single-Ended Source*.
(3) See *Driving CLKin and OSCin Pins With a Differential Source*.
(4) To meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended differential slew rate for all input clocks is 3 V/ns; this is especially true for single-ended clocks. Phase noise performance begins to degrade as the clock input slew rate is reduced. However, the device functions at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) are less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, TI also recommends using the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
(5) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.

7.8 PLL1 Specification Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PD1}	PLL1 phase detector frequency				4	MHz
V_{TUNE}	CTRL_VCXO tune voltage		0		3.3	V
PN10kHz	PLL 1/f noise at 10-kHz offset. Normalized to 1 GHz output frequency. (1)	10-Hz loop bandwidth		–130		dBc/Hz
		300-Hz loop bandwidth		–131		
BW_{min}	Minimum PLL1 bandwidth			3		Hz
BW_{max}	Maximum PLL1 bandwidth			300		Hz
PFD_{spur}	PLL1 PFD update spur	Measured with PLL1 only. PLL1 Bandwidth set to 50 Hz. PLL1 PFD update frequency 1 MHz.		–150	–100	dBc/Hz

(1) A specification in modeling PLL in-band phase noise is the 1/f flicker noise, $L_{PLL\_flicker}(f)$, which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10-kHz offset and a 1-GHz carrier frequency. PN10kHz = $L_{PLL\_flicker}$(10 kHz) – 20log(F_{out} / 1 GHz), where $L_{PLL\_flicker}(f)$ is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure $L_{PLL\_flicker}(f)$ it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). $L_{PLL\_flicker}(f)$ can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL\_flicker}(f)$ and $L_{PLL\_flat}(f)$.

7.9 PLL2 Specification Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{doubler\_max}$	Doubler input frequency	EN_PLL2_REF_2X = 1 (1); OSCin duty cycle 40% to 60%			125	MHz
f_{PD2}	Phase detector frequency (2)				250	MHz
PN10kHz	PLL 1/f noise at 10-kHz offset. (3) Normalized to 1-GHz output frequency	400-kHz loop bandwidth		–120		dBc/Hz
f_{VCO}	VCO tuning range		5870		6175	MHz
$\|\Delta T_{CL}\|$	Allowable temperature drift for continuous lock (4)	After programming for lock, no changes to output configuration are permitted to assure continuous lock			145	°C
BW_{min}	Minimum PLL2 bandwidth			90		kHz
BW_{max}	Maximum PLL2 bandwidth			1000		kHz

(1) The EN_PLL2_REF_2X bit enables/disables a frequency doubler mode for the PLL2 OSCin path.
(2) Assured by characterization. ATE tested at 258-MHz Phase detector frequency.
(3) A specification in modeling PLL in-band phase noise is the 1/f flicker noise, $L_{PLL\_flicker}(f)$, which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10-kHz offset and a 1-GHz carrier frequency. PN10kHz = $L_{PLL\_flicker}$(10 kHz) – 20log(F_{out} / 1 GHz), where $L_{PLL\_flicker}(f)$ is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure $L_{PLL\_flicker}(f)$ it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). $L_{PLL\_flicker}(f)$ can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL\_flicker}(f)$ and $L_{PLL\_flat}(f)$.
(4) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value and still have the part stay in lock; this implies the part will work over the entire frequency range. However, if the temperature drifts more than the maximum allowable drift for continuous lock, it will be necessary to reload the appropriate register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature must never drift outside the frequency range of –40°C to 105°C without violating specifications.

7.10 Clock Output Type Characteristics (CLKoutX)(1)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{CLKout}	Output frequency	4-mA HSDS				1000	MHz
		6-mA HSDS				1500	
		8-mA HSDS				2000	
		16-mA HCSL				1500	
ODC	Output duty cycle	4-mA HSDS		45%	50%	55%	
		6-mA HSDS		45%	50%	55%	
		8-mA HSDS		45%	50%	55%	
		8-mA HSDS, >1.5 GHz		40%		60%	
		16-mA HCSL		45%	50%	55%	
T_R	Output rise time	245.76 MHz, 20% to 80%, R_L = 100 Ω	4-mA HSDS		148		ps
			6-mA HSDS		164		
			8-mA HSDS		148		
			16-mA HCSL		73		
T_F	Output fall time	245.76 MHz, 80% to 20%, R_L = 100 Ω	4-mA HSDS		149		ps
			6-mA HSDS		163		
			8-mA HSDS		146		
			16-mA HCSL		74		
V_{OH}	Output high voltage	4-mA HSDS		0.5		0.75	V
		6-mA HSDS		0.72		1.06	
		8-mA HSDS		0.75		1.3	
		16-mA HSCL		0.75		1.04	
V_{OL}	Output low voltage	4-mA HSDS		0.1		0.18	V
		6-mA HSDS		0.15		0.26	
		8-mA HSDS		0.17		0.31	
		16-mA HSCL		0.0		0.05	
$V_{OD,pp}$	Differential output voltage	4-mA HSDS			958		mVpp
		6-mA HSDS			1380		
		8-mA HSDS			1544		
		16-mA HSCL			1807		
ΔV_{OD}	Change in V_{OD} for complementary output states	4-mA HSDS		–15		15	mVpp
		6-mA HSDS		–20		20	
		8-mA HSDS		–90		115	
		16-mA HCSL		–15		15	

(1) See test load description in *Output Termination Scheme*.

7.11 Oscillator Output Characteristics (OSCout)

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKout}	Output frequency (1)	2-pF load, 1.8-V LVCMOS (2)			200	MHz
		4-mA HSDS (2)			1000	
		8-mA HSDS (2)			1000	
		16-mA HCSL (2)			400	
ODC	Output duty cycle	2-pF load, 1.8-V LVCMOS	45%	50%	55%	
		4-mA HSDS	45%	50%	55%	
		8-mA HSDS	45%	50%	55%	
		16-mA HCSL	45%	50%	55%	
T_R / T_F	Output rise/fall time	20% to 80%, C_L = 2 pF, 1.8 V LVCMOS		156		ps
		80% to 20%, C_L = 2 pF, 1.8 V LVCMOS		273		
		< 300 MHz, 20 % to 80 %, R_L = 100 Ω, 4-mA HSDS		176	300	
		> 300 MHz, 20 % to 80 %, R_L = 100 Ω, 4-mA HSDS		152		
		< 300 MHz, 20% to 80%, R_L = 100 Ω, 8-mA HSDS		183	300	
		> 300 MHz, 20 % to 80 %, R_L = 100 Ω, 8-mA HSDS		138		
		20 % to 80 %, R_L = 100 Ω, 16-mA HCSL		135		
V_{OH}	Output high voltage	1-mA load, 1.8-V LVCMOS	1.44			V
		4-mA HSDS	0.46		0.7	
		8-mA HSDS	0.82		1.19	
		16-mA HCSL	0.61		0.89	
V_{OL}	Output low voltage	1-mA load, 1.8-V LVCMOS			0.36	V
		4-mA HSDS	0.1		0.22	
		8-mA HSDS	0.11		0.24	
		16-mA HCSL		0.02	0.06	
$V_{OD,pp}$	Differential output voltage	4-mA HSDS	600	775	950	mVpp
		8-mA HSDS	1240	1548		
		16-mA HCSL	1000	1360		
I_{OH}	Output high current (source)	V_{OUT} = 2 pF to GND, 1.8-V LVCMOS		–25		mA
I_{OL}	Output low current (sink)	V_{OUT} = 2 pF to GND, 1.8-V LVCMOS		26		mA
V_{OX}	Output common mode	DC-Coupled, 4-mA HSDS	0.1	0.34	0.45	V
		DC-Coupled, 8-mA HSDS	0.3	0.55	0.7	
		DC-Coupled, 16-mA HCSL		0.34		
R_{OUT}	Output impedance	I_{OUT} at V_{OUT} = 0.9 V		67		Ω

(1) OSCout Divider maximum input frequency is 1.5 GHz.
(2) See test load description in *Output Termination Scheme*.

7.12 Jitter and Phase Noise Characteristics for CLKoutX and OSCout

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$L(f)_{CLKout/OSCout}NF$	Noise floor 20-MHz offset ≤ 100-Hz loop bandwidth for PLL1 400-kHz loop bandwidth for PLL2 (1)	122.88 MHz	HSDS 4 mA		–166		dBc/Hz
			HSDS 6 mA		–166		
			HSDS 8 mA		–166		
			HCSL 16 mA		–165		
			OSCout, HSDS 4 mA		–161		
			OSCout, HSDS 8 mA		–161		
			OSCout, LVCMOS		–156		
$L(f)_{CLKout}NF,ADLY$	Noise floor with analog delay enabled 20-MHz offset ≤ 100-Hz loop bandwidth for PLL1 400-kHz loop bandwidth for PLL2 (1)	122.88 MHz, maximum analog delay setting	HSDS 4 mA		–151		dBc/Hz
			HSDS 6 mA		–151		
			HSDS 8 mA		–151		
			HCSL 16 mA		–151		
$L(f)_{CLKout}PN$	SSB phase noise (2) 122.88-MHz output frequency ≤ 100-Hz loop bandwidth for PLL1 400-kHz loop bandwidth for PLL2 (1) (3)	Offset = 100 Hz			–97		dBc/Hz
		Offset = 1 kHz			–126		
		Offset = 10 kHz			–139		
		Offset = 100 kHz			–147		
		Offset = 800 kHz			–158		
		Offset = 1 MHz			–159		
		Offset = 10 MHz	HSDS 8 mA		–166		
			HCSL 16 mA		–165		
$L(f)_{OSCout}PN$	SSB phase noise 122.88-MHz output frequency ≤ 100-Hz loop bandwidth for PLL1 400-kHz loop bandwidth for PLL2 (1) (3)	Offset = 100 Hz			–97		dBc/Hz
		Offset = 1 kHz			–136		
		Offset = 10 kHz			–148		
		Offset = 100 kHz			–157		
		Offset = 1 MHz	HSDS 4 mA		–160		
		Offset = 10 MHz	HSDS 8 mA		–160		
J_{CLKout}	f_{CLKout} = 122.88 MHz Integrated RMS jitter ≤ 100-Hz loop bandwidth for PLL1 400-kHz loop bandwidth for PLL2 (1) (4)	HSDS 8 mA, BW = 100 Hz to 20 MHz			160		fs rms
		HSDS 8 mA, BW = 10 kHz to 20 MHz			75		
		HCSL 16 mA, BW = 100 Hz to 20 MHz			160		
		HCSL 16 mA, BW = 10 kHz to 20 MHz			75		

(1) VCXO used is a 122.88-MHz Crystek CVHD-950-122.880.
(2) Phase noise is defined in dual-loop mode and in single PLL mode if OSCin is used as the ref input.
(3) The input is configured to either a full swing AC-coupled, single-ended signal or a LVDS like AC-coupled differential signal. The input frequency is 122.88 MHz. VDD_IN is at 1.8 V.
(4) PLL1 and PLL2 settings optimized to meet multicarrier GSM phase-noise specifications. For RMS jitter optimized settings, see *PLL1 and PLL2*.

7.13 Clock Output Skew and Isolation Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert T_{SKEW} \rvert$	Maximum CLKoutX to CLKoutY	Same format, after SYNC F_{CLK} = 245.76 MHz, R_L= 100 Ω, AC-coupled		60	95	|ps|
t_{PD}CLKin0_CLKoutX	Absolute propagation delay from CLKin0 to CLKout0	Buffer mode fin=fout=122.88 MHz CLKout0_TYPE = HSDS 8 mA		3		ns
$isolation_{SYSref-DeviceCLK}$typ	Isolation between a SYSref signal to a DeviceClk signal(1)	CLKout2 = 7.68 MHz (SYSref, HSDS 8 mA, aggressor) CLKout3 = 122.88 MHz (DeviceClk, HSDS 8 mA, victim)		–94		dBc
$isolation_{CLKoutX}$typ	Isolation between 2 adjacent CLKout channels(1)	CLKoutX = 153.6 MHz (HSDS 8 mA, aggressor) CLKoutY = 122.88 MHz (HSDS 8 mA, victim)		–70		dBc
$isolation_{OSCout-CLKout}$typ	Isolation between OSCout and CLKoutX channels(1)	OSCout = 30.72 MHz (HSDS 8 mA, aggressor) CLKoutY = 122.88 MHz (HSDS 8 mA, victim)		–99		dBc
$isolation_{PLL2PFD-DeviceCLK}$typ	Isolation between PLL2 PFD update and CLKoutX channels(1)	PLL2 PFD update frequency = 122.88 MHz (aggressor) CLKoutX = 491.52 MHz (HSDS 8 mA, victim)		–80		dBc
		PLL2 PFD update frequency = 122.88 MHz (aggressor) CLKoutX = 1228.8 MHz (HSDS 8 mA, victim)		–80		dBc

(1) Isolation in the victim channel is measured at aggressor frequency in power spectrum relative to the carrier (victim). Measured with < 100-Hz resolution bandwidth. Internal LDO must be enabled.

7.14 Clock Output Delay Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADLY}max	Maximum analog delay frequency				200	MHz
$tstep_{ADLY}$1st	1st Analog delay step size			300		ps
$tstep_{ADLY}$variation	Analog delay step size variation	Variation over all steps		66		ps
$tstep_{DDLY}$1.47456GHz	Digital delay step size at 1.47456 GHz	Half-step enabled		339		ps
$tstep_{DDLY}$variation	Digital delay step size variation			0		ps

7.15 DEFAULT POWER on RESET CLOCK OUTPUT Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40 °C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{CLKout-startup}$	Default OSCout clock frequency at device power on after RESETN = 1 (1) (2)	SYNC pin pulled Low at start up VCXO used is a 122.88-MHz Crystek CVHD-950-122.880		122.88		MHz

(1) Assured by characterization. ATE tested at 122.88 MHz.
(2) OSCout will oscillate at start-up at the frequency of the VCXO attached to OSCin port. All other outputs are disabled.

7.16 Power Supply Characteristics

3.135 V < VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE < 3.465 V;
1.7 V < VDD_IO, VDD_OSC, VDDO_x < 3.465 V; –40°C < T_A < 85°C and T_{PCB} ≤ 105°C. Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD_PD}	Power-down supply current			12	20	mA
P_{Total}	Total power consumption for LMK04616(1)	16 HSDS 8-mA clocks enabled at 122.88 MHz OSCout disabled, LOS disabled, Delays disabled PLL1 and PLL2 locked. 122.88 MHz at CLKin0 and 122.88-MHz VCXO		1050	1200	mW
		16 HSDS 4-mA clocks enabled at 122.88 MHz OSCout disabled, LOS disabled, analog and digital delay used on SYSREF PLL1 and PLL2 locked. 122.88 MHz at CLKin0 and 122.88-MHz VCXO		970	1100	mW
I_{DDO_X}	CLKoutX supply current	See P_{Total} Test Condition (HSDS 8-mA)		39.2	42.8	mA
I_{DDIO}	IO supply current	See P_{Total} Test Condition (HSDS 8-mA)		5.3	8.4	mA
I_{DD_PLL1}	PLL1 supply current	See P_{Total} Test Condition (HSDS 8-mA)		14.8	16.1	mA
$I_{DD\_PLL2CORE}$	PLL2 core supply current	See P_{Total} Test Condition (HSDS 8-mA)		45.5	52.0	mA
$I_{DD\_PLL2OSC}$	PLL2 OSC supply current	See P_{Total} Test Condition (HSDS 8-mA)		60.7	64.9	mA
I_{DD_CORE}	Core supply current	See P_{Total} Test Condition (HSDS 8-mA)		22.5	28.6	mA
I_{DD_OSC}	OSC supply current	See P_{Total} Test Condition (HSDS 8-mA)		3.2	4.1	mA

(1) See applications section *Power Supply Recommendations* for Icc for specific part configuration and how to calculate Icc for a specific design.

7.17 Typical Power Supply Noise Rejection Characteristics

Typical values at VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE = 3.3 V, VDD_IO, VDD_OSC, VDDOx = 1.8 V, T_A = 25°C, at the *Recommended Operating Conditions* and are *not* assured. Sinusoidal noise injected in either of the following supply nodes: VDD_PLL2OSC, VDD_PLL1, VDD_PLL2CORE, VDD_CORE, VDD_IO, VDD_OSC, or VDDOx

PARAMETER		TEST CONDITION	VDD_PLL1	VDD_PLL2 OSC	VDD_PLL2 CORE	VDD_CORE	VDD_OSC/ VDD_IO	VDDOx	UNIT
$PSNR_{10kHz}$	10-kHz spur on 122.88-MHz output	25-mV ripple on supply. Single HSDS 8-mA output enabled.	–59	–94	n/a	–104	–108	n/a	dBc
$PSNR_{100kHz}$	100-kHz spur on 122.88-MHz output		–71	–87	–101	n/a	n/a	–101	dBc
$PSNR_{500kHz}$	500-kHz spur on 122.88-MHz output		–87	–81	–90	n/a	n/a	–93	dBc
$PSNR_{1MHz}$	1-MHz spur on 122.88-MHz output		–100	–80	–83	n/a	n/a	–88	dBc
$PSNR_{10kHz}$	10-kHz spur on 122.88-MHz output	50-mV ripple on supply. Single HSDS 8-mA output enabled.	–53	–88	–109	–100	–104	–107	dBc
$PSNR_{100kHz}$	100-kHz spur on 122.88-MHz output		–65	–81	–98	n/a	n/a	–98	dBc
$PSNR_{500kHz}$	500-kHz spur on 122.88-MHz output		–81	–75	–84	–108	n/a	–87	dBc
$PSNR_{1MHz}$	1-MHz spur on 122.88-MHz output		–94	–74	–77	–104	n/a	–82	dBc

7.18 SPI Interface Timing

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td_S	Setup time for SDI edge to SCLK rising edge	See Figure 1	10			ns
td_H	Hold time for SDI edge from SCLK rising edge	See Figure 1	10			ns
t_{SCLK}	Period of SCLK	See Figure 1	50			ns
t_{HIGH}	High width of SCLK	See Figure 1	25			ns
t_{LOW}	Low width of SCLK	See Figure 1	25			ns
tc_S	Setup time for CS* falling edge to SCLK rising edge	See Figure 1	10			ns
tc_H	Hold time for CS* rising edge from SCLK rising edge	See Figure 1	30			ns
td_V	SCLK falling edge to valid read back data	See Figure 1			20	ns

7.19 Timing Diagram

Each serial interface access cycle is exactly (2 + N) bytes long, where N is the number of data bytes. A frame is initiated by asserting SCS* low. The frame ends when SCS* is de-asserted high. The first bit transferred is the R/W bit. The next 15 bits are the register address and the remaining bits are data. For all writes, data is committed in bytes as the 8th data bit of a data field is clocked in on the rising edge of SCL. If the write access is not an even multiple of 8 clocks, the trailing data bits are not committed. On read access, data is clocked out on the falling edge of SCL on the SDO pin.

Four-wire mode read back has the same timing as the SDIO pin.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

See *Programming* for more details.

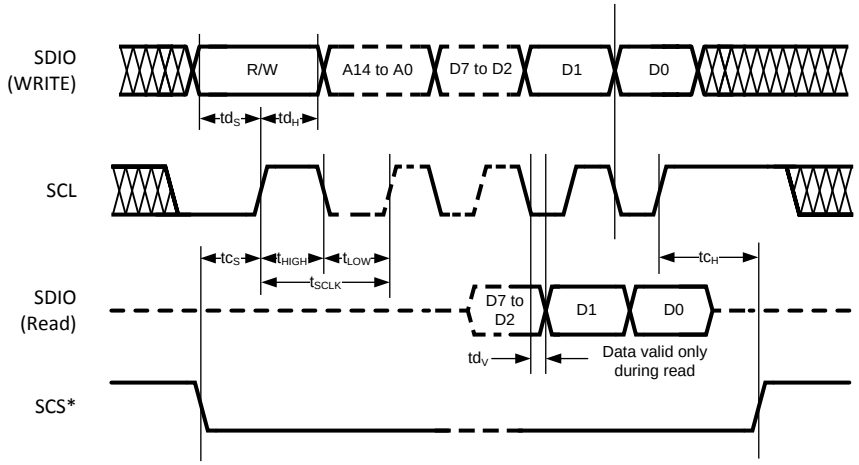


Figure 1. SPI Timing Diagram

7.20 Typical Characteristics

7.20.1 Clock Output AC Characteristics

NOTE

These plots show performance at frequencies beyond what the part is ensured to operate at to give the user an idea of the capabilities of the part, but they do not imply any sort of ensured specification.

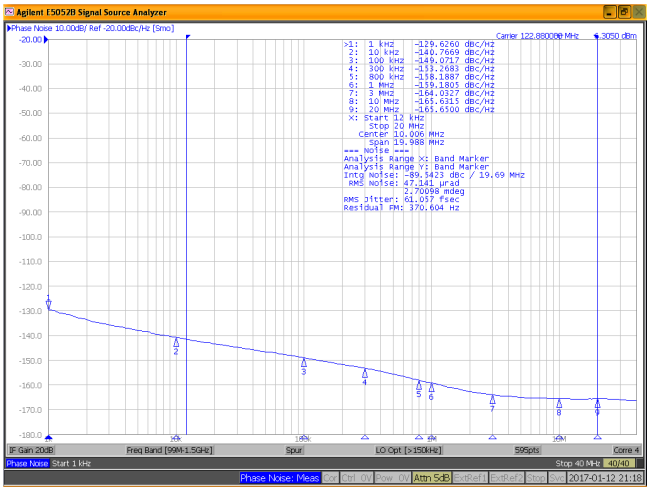


Figure 2. LMK0461x CLKout2 Phase Noise
VCO = 5898.24 MHz
CLKout2 Frequency = 122.88 MHz
HSDS 8 mA

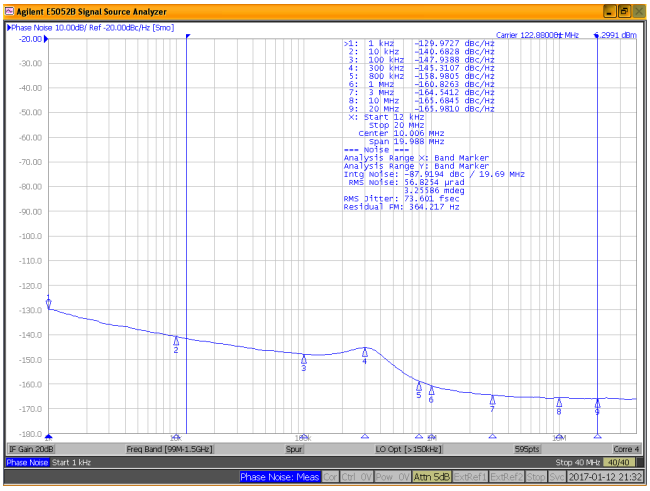


Figure 3. LMK0461x CLKout2 Phase Noise
VCO = 5898.24 MHz
CLKout2 Frequency = 122.88 MHz
HSDS 8 mA
With PLL2 3rd Order Pole

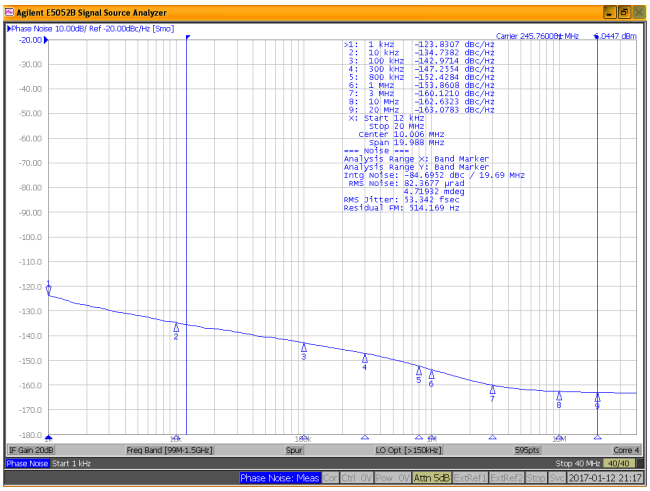


Figure 4. LMK0461x CLKout2 Phase Noise
VCO = 5898.24 MHz
CLKout2 Frequency = 245.76 MHz
HSDS 8 mA

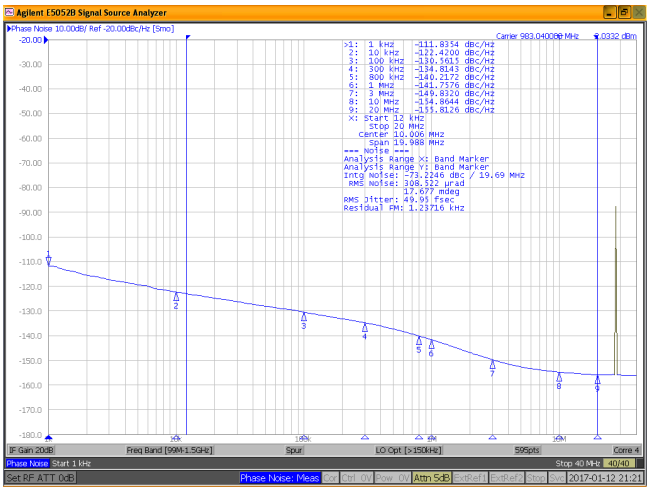


Figure 5. LMK0461x CLKout2 Phase Noise
VCO Frequency = 5898.24 MHz
CLKout2 Frequency = 983.04 MHz
HSDS 8 mA

Clock Output AC Characteristics (continued)

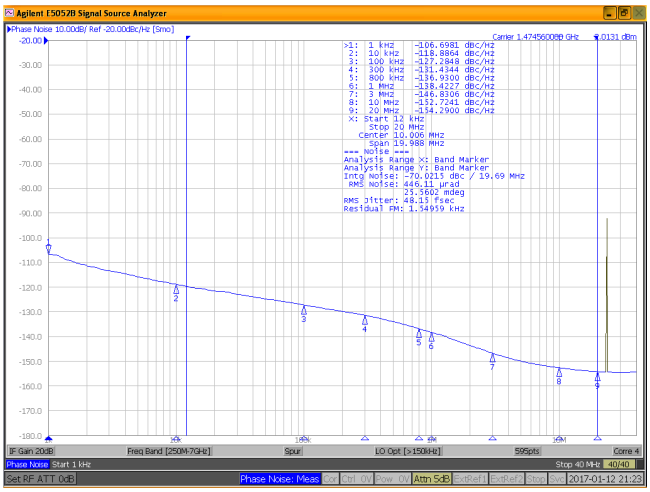


Figure 6. LMK0461x CLKout2 Phase Noise
VCO Frequency = 5898.24 MHz
CLKout2 Frequency = 1474.56 MHz
HSDS 8 mA

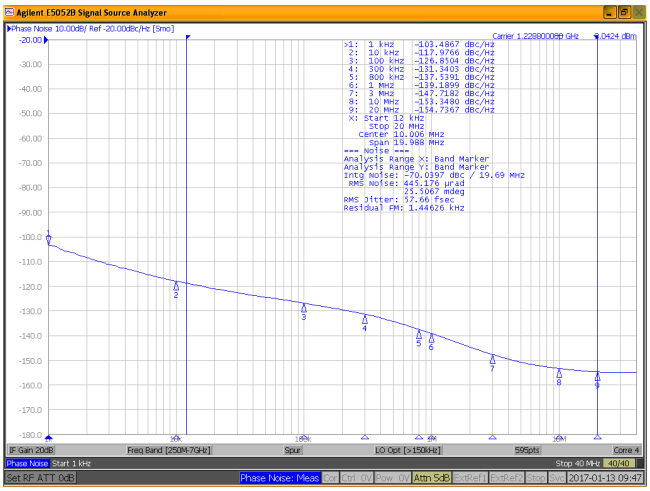


Figure 7. LMK0461x CLKout2 Phase Noise
VCO Frequency = 6144 MHz
CLKout2 Frequency = 1228.8 MHz
HSDS 8 mA

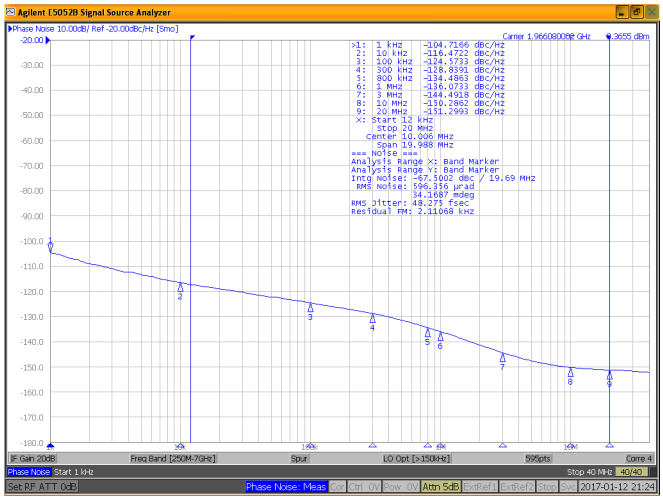


Figure 8. LMK0461x CLKout2 Phase Noise
VCO Frequency = 5898.24 MHz
CLKout2 Frequency = 1966.08 MHz
HSDS 8 mA

8 Parameter Measurement Information

8.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so the reader is able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD}, depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter; this signal does not exist in the IC with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 9 illustrates the two different definitions side-by-side for inputs and Figure 10 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

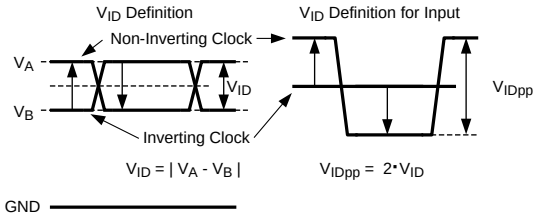


Figure 9. Two Different Definitions for Differential Input Signals

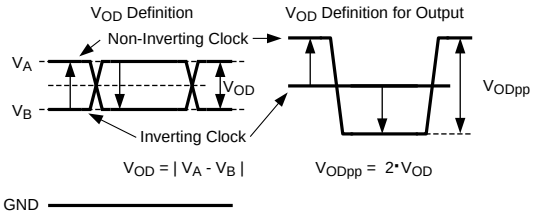


Figure 10. Two Different Definitions for Differential Output Signals

Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

8.2 Output Termination Scheme

This section describes the test loads setup during device characterization.

8.2.1 HSDS 4/6/8mA

Available on CLKoutX/CLKoutX* and OSCout/OSCout*. When OSCout is programmed for differential output from OSCin, the OSCout signal will be inverted from input.

$C_{PARA} \leq 3$ pF

Output Termination Scheme (continued)

The differential transmission line impedance is 100 Ω.

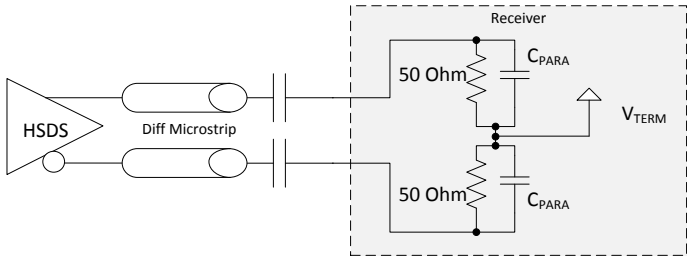


Figure 11. HSDS Test and Simulation Circuit

8.2.2 HCSL

Available on CLKoutX/CLKoutX* and OSCout/OSCout*. When OSCout is programmed for differential output from OSCin, the OSCout signal will be inverted from input..

C_{PARA} ≤ 3 pF

The differential transmission line impedance is 100 Ω.

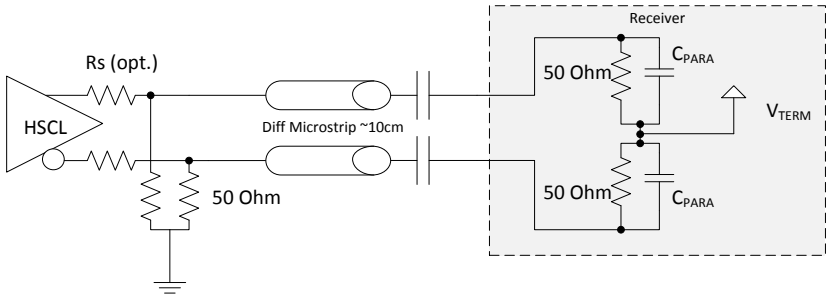


Figure 12. HCSL Test and Simulation Circuit

8.2.3 LVCMOS

Available at STATUS0/1 and OSCout/OSCout*.

C_{Load} = 10 pF

R_S is optional to adjust LVCMOS driver impedance to transmission line.

The transmission line impedance is 50 Ω.

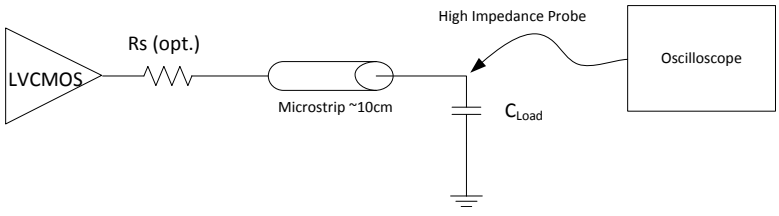


Figure 13. LVCMOS Test and Simulation Circuit

9 Detailed Description

9.1 Overview

The LMK04616 device is very flexible in meeting many application requirements. The typical use case for LMK04616 is a cascaded Dual Loop Jitter Cleaner with optional support for JESD204B.

NOTE

While the Clock outputs (CLKoutX) do not provide LVCMOS outputs, the OSCout may be used to provide LVCMOS outputs.

In addition to dual-loop operation, by powering down various blocks, the LMK04616 may be configured for single-loop or clock distribution modes also.

9.1.1 Jitter Cleaning

The dual-loop PLL architecture of LMK04616 provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 typically uses a narrow loop bandwidth (typically 10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while simultaneously suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This *cleaned* reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (typically 90 kHz to 500 kHz). The loop bandwidth for PLL2 is chosen to take advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO.

Ultra-low jitter is achieved by allowing the external VCXO phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

9.1.2 Four Redundant Reference Inputs (CLKin0/CLKin0*, CLKin1/CLKin1*, CLKin2/CLKin2*, and CLKin3/CLKin3*)

The LMK04616 has four reference clock inputs for PLL1. They are CLKin0, CLKin1, CLKin2, and CLKin3. The active clock is chosen based on CLKin_SEL_MODE. Automatic or manual switching can occur between the inputs.

Fast manual switching between CLKin0 and CLKin1 reference clocks is possible with external pin CLKin_SEL.

9.1.3 VCXO Buffered Output

The LMK04616 provides OSCout, which by default is a buffered copy of the PLL1 feedback or PLL2 reference input. This reference input is typically a low noise VCXO. This output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the LMK04616 is programmed.

The OSCout buffer output types are LVCMOS, HSDS, and HCSL. When using HSDS and HCSL output from OSCin, the output will be inverted from OSCin input.

OSCout has the option to fan out a copy of PLL2 output.

9.1.4 Frequency Holdover

LMK04616 supports holdover operation for PLL1 to keep the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established.

9.1.5 Integrated Programmable PLL1 and PLL2 Loop Filter

LMK04616 features programmable loop filter for PLL1 and PLL2. See *PLL1 and PLL2*.

Overview (continued)

9.1.6 Internal VCOs

LMK04616 has an internal VCO in PLL2 with 5870 MHz to 6175 MHz tuning range. The output of the VCO is routed through a mandatory divider (by 3, by 4, by 5, or by 6) to the Clock Distribution Path. This limits the Clock Distribution Path frequency to 2058 MHz. This same clock is also fed back to the PLL2 phase detector through the N-divider (feedback divider).

9.1.7 Clock Distribution

The LMK04616 features a total of 16 PLL2 clock outputs driven from one of the internal VCOs.

All PLL2 clock outputs have programmable output types. They can be programmed to HSDS or HCSL.

If OSCout is included in the total number of clock outputs the LMK04616 is able to distribute up to 17 differential clocks.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

9.1.7.1 Output Clock Divider

The output divider supports a divide range of 1 to 65535 (even and odd) with 50% output duty cycle.

9.1.7.2 Output Clock Delay

The clocks include both a analog and digital delay for phase adjustment of the clock outputs.

The analog delay allows a nominal 60-ps step size and range from 0 to 1.2 ns of total delay per output. See *Analog Delay* for further information.

The digital delay allows an output channel to be delayed from 1 to 255 VCO cycles. The delay step can be as small as half the period of the clock distribution path. For example, 1.5-GHz clock distribution path frequency results in 333-ps coarse tuning steps. The coarse (digital) delay value takes effect on the clock outputs after a SYNC event. See *Digital Delay* for further information.

1. Fixed Digital Delay (per output channel) – Allows all the output channels to have a known phase relationship upon a SYNC event. Typically performed at start-up.
2. Dynamic Digital Delay (per output) – Allows additional coarse adjustment per output.

9.1.7.3 Glitchless Half-Step and Glitchless Analog Delay

The device clocks include a features to ensure glitchless operation of the Half-Step and analog delay operations when enabled.

9.1.7.4 Programmable Output Formats

All LMK0461x clock outputs (CLKoutX) can be programmed to an HSDS or HCSL output type. The OSCout can be programmed to an HSDS, HCSL, or LVCMOS output type.

Any HSDS output type can be programmed to typical 800-, 1200-, or 1600-mVpp differential amplitude levels. When OSCout is programmed for differential output from OSCin, the OSCout signal will be inverted from input.

9.1.7.5 Clock Output SYNChronization

Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay.

The SYNC event must occur for digital delay values to take effect.

9.1.8 Status Pins

The LMK0461x provides status pins that can be monitored for feedback or in some cases used for input, depending upon device programming. For example:

- Indication of the loss-of signal (LOS) for CLKinX.
- Indication of the selected active clock input.

Overview (continued)

- PLL1 and PLL2 lock signal.
- Holdover Status.

The status pins can be programmed to a variety of other outputs including PLL divider outputs, combined PLL lock detect signals, readback, and so forth. See *Programming* for more information.

A full list of functions can be found in *STATUS0/1 and SYNC Pin Functions*.

9.2 Functional Block Diagram

Figure 14 illustrates the complete block diagram.

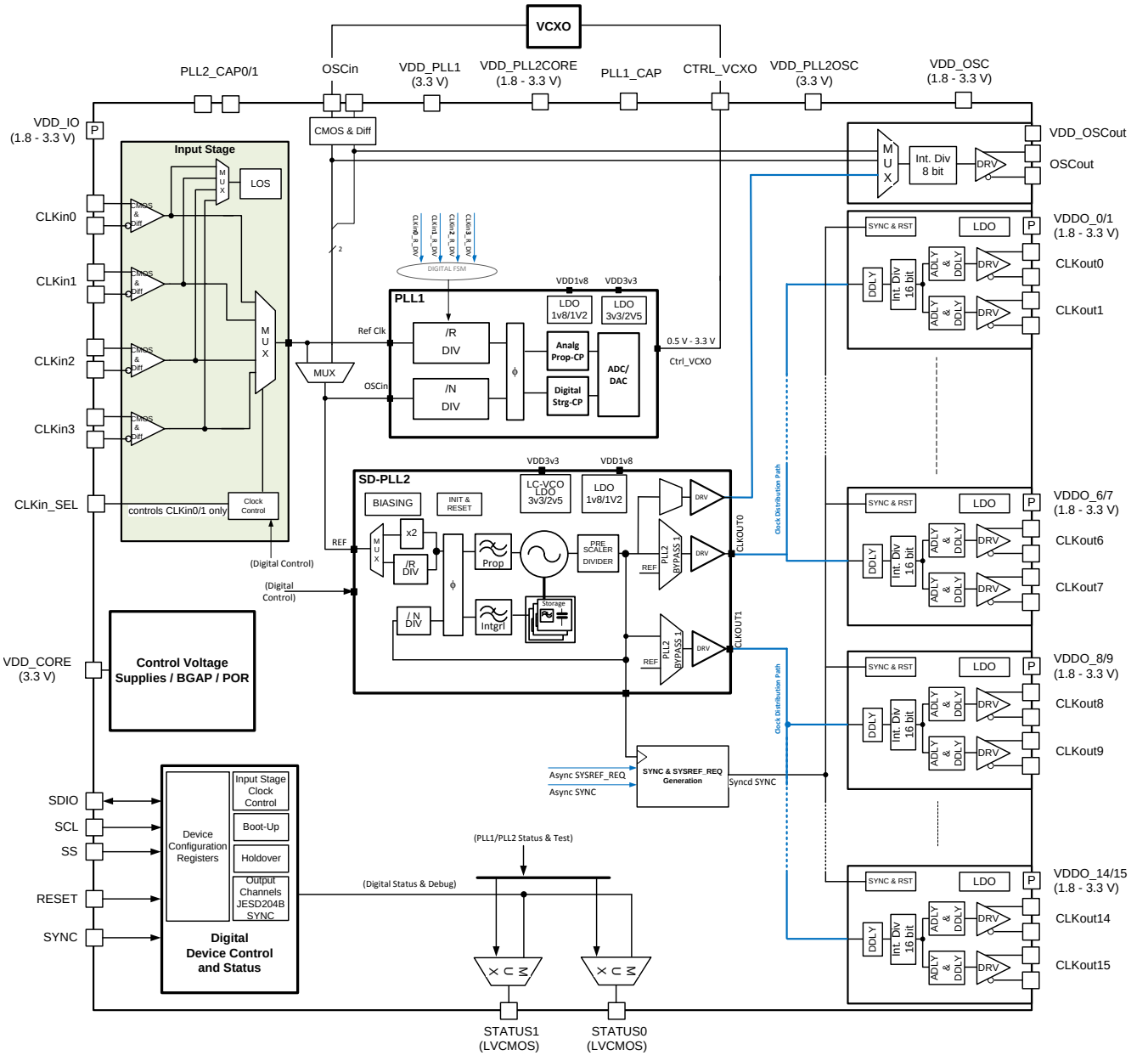


Figure 14. Detailed LMK04616 Block Diagram

9.3 Feature Description

9.3.1 Reference Inputs (CLKin0/CLKin0*, CLKin1/CLKin1*, CLKin2/CLKin2*, and CLKin3/CLKin3*)

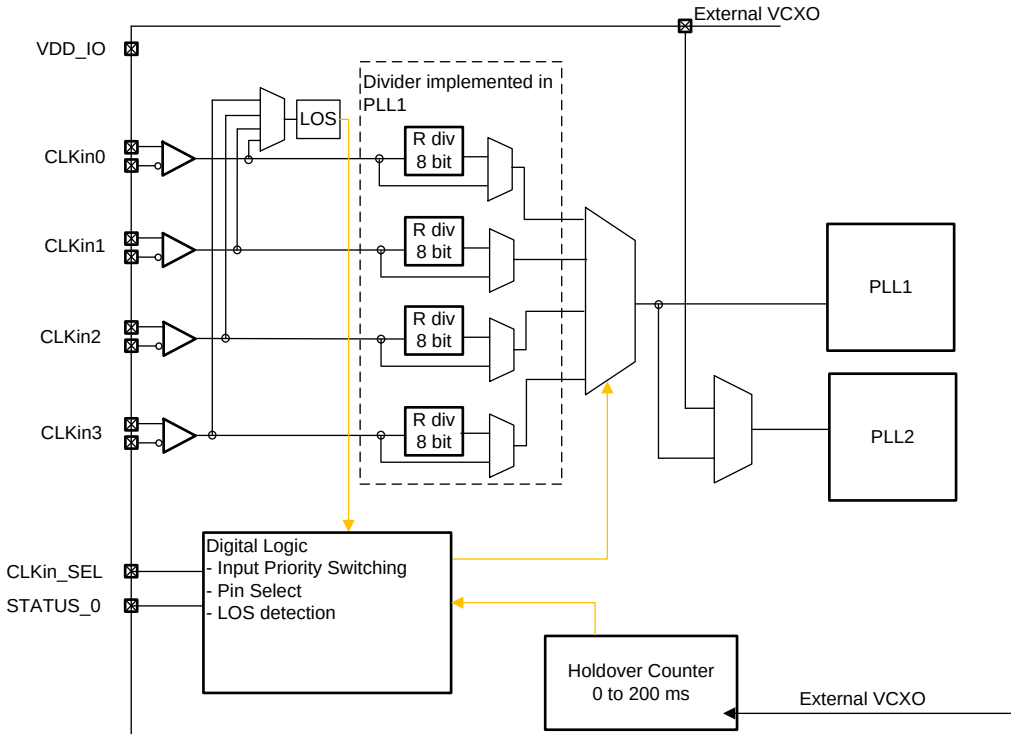


Figure 15. LMk04616 Clock Input Block

9.3.1.1 Input Clock Switching

Manual, pin select, and priority or automatic are three different kinds clock input switching modes can be set with the CLKIN_SEL_MODE register.

Below is information about how the active input clock is selected and what causes a switching event in the various clock input selection modes.

9.3.1.1.1 Input Clock Switching – Register Select Mode

When CLKIN_SEL_MODE = 2 then CLKin0, CLKin1, CLKin2, or CLKin3 is selected through register control (SW_REFINSEL[3:0]).

If holdover is entered in this mode, then the device will relock to the selected CLKinX upon holdover exit.

Table 2. Active Clock Input – Register Select Mode (SW_REFINSEL[3:0])

SW_REFINSEL[3:0]	ACTIVE CLOCK (LMK04616)
0001b	CLKin0
0010b	CLKin1
0100b	CLKin2
1000b	CLKin3

9.3.1.1.2 Input Clock Switching – Pin Select Mode (CLKin_SEL, STATUS0)

When CLKIN_SEL_MODE = 1, the CLKin_SEL pin selects which clock input is active. In LMK04616, CLKIN_SEL_MODE = 1 forces STATUS0 to be CLKIN_SEL0.

9.3.1.1.2.1 Configuring Pin Select Mode

The CLKinSEL1_INV bit inverts the polarity of CLKin_SEL and STATUS0 input pins.

Table 3 lists which input clock is active depending on CLKin_SEL state.

Table 3. Active Clock Input – Pin Select Mode (CLKin_SEL, STATUS0), CLKinSEL_INV = 0

PIN CLKin_SEL	PIN STATUS0	ACTIVE CLOCK
Low	Low	CLKin0
Low	High	CLKin1
High	Low	CLKin2
High	High	CLKin3

9.3.1.1.3 Input Clock Switching – Automatic Mode

When CLKINSEL1_MODE = 0, the input clock switching is in Automatic mode. The priority of each input clock can be individually set by programming CLKINx_PRIO[3:0] as shown in Table 4:

Table 4. Clock Input Priority Selection

CLKINx_PRIO[3:0]	CLKINx
0000b	Disabled
0001b	Priority 1 (Highest)
0010b	Priority 2 (High)
0100b	Priority 3 (Low)
1000b	Priority 4 (Lowest)

NOTE

Equal priority setting for two CLKINx inputs are not allowed.

The clock inputs in this mode are monitored by on-chip LOS detection circuits. The device reads the priority bits at start-up and locks to the input clock with highest priority. In the event of input clock loss, the internal PLL switches to the next available clock. TI recommends using Holdover Mode while using the Automatic Reference Clock Switching. See *Holdover* for programming the Holdover mode.

In this case, the outputs clocks will see minimum disturbance while switching from one clock to the other. In the event of reference clock loss, the PLL1 enters the holdover mode. After the internal logic switches the PLL1 input clock to the next available clock as per priority setting, PLL1 holdover exit is initiated and PLL1 relocks to the new clock with minimum disturbance. Flowchart below describes the sequence of operations in the *Automatic Reference Clock Switching* mode while holdover is enabled and programmed.

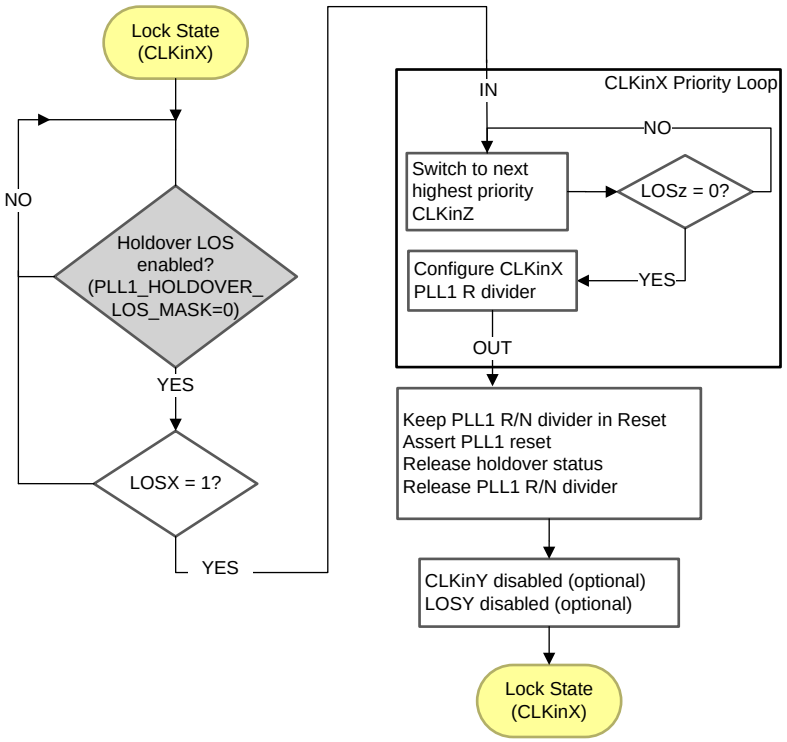


Figure 16. Input Clock Switching – Priority Loop

9.3.1.2 Loss of Signal Detection – LOS

The loss of signal detection circuit is available for all clock inputs. It has programmable assertion and de-assertion cycles. LOS detection circuit reliable operation is ensured with >200-mVpp differential or >200-mV single-ended CLKin amplitude and input frequencies between 10 MHz to 500 MHz. Maximum input frequency for the doubler in the LOS block is 250 MHz. The ratio between VCXO frequency and input frequency must be between 0.25 and 4.

9.3.1.2.1 LOS – Assertion

LOS assertion time is programmable between 1 to 8 VCXO clock cycles. The LOS assertion time is programmed through CLKINx_LOS_LAT_SEL[7:0]. LOS_LAT_SEL is an 8-Bit code. Additionally, CLKINx_LOS_FRQ_DBL_EN bit controls the frequency doubler for the LOS block. This is especially important for VCXO frequencies equal or smaller than CLKinX frequency.

For correct operation of LOS, the reference clock must be switched to logic low level (differential or single-ended).

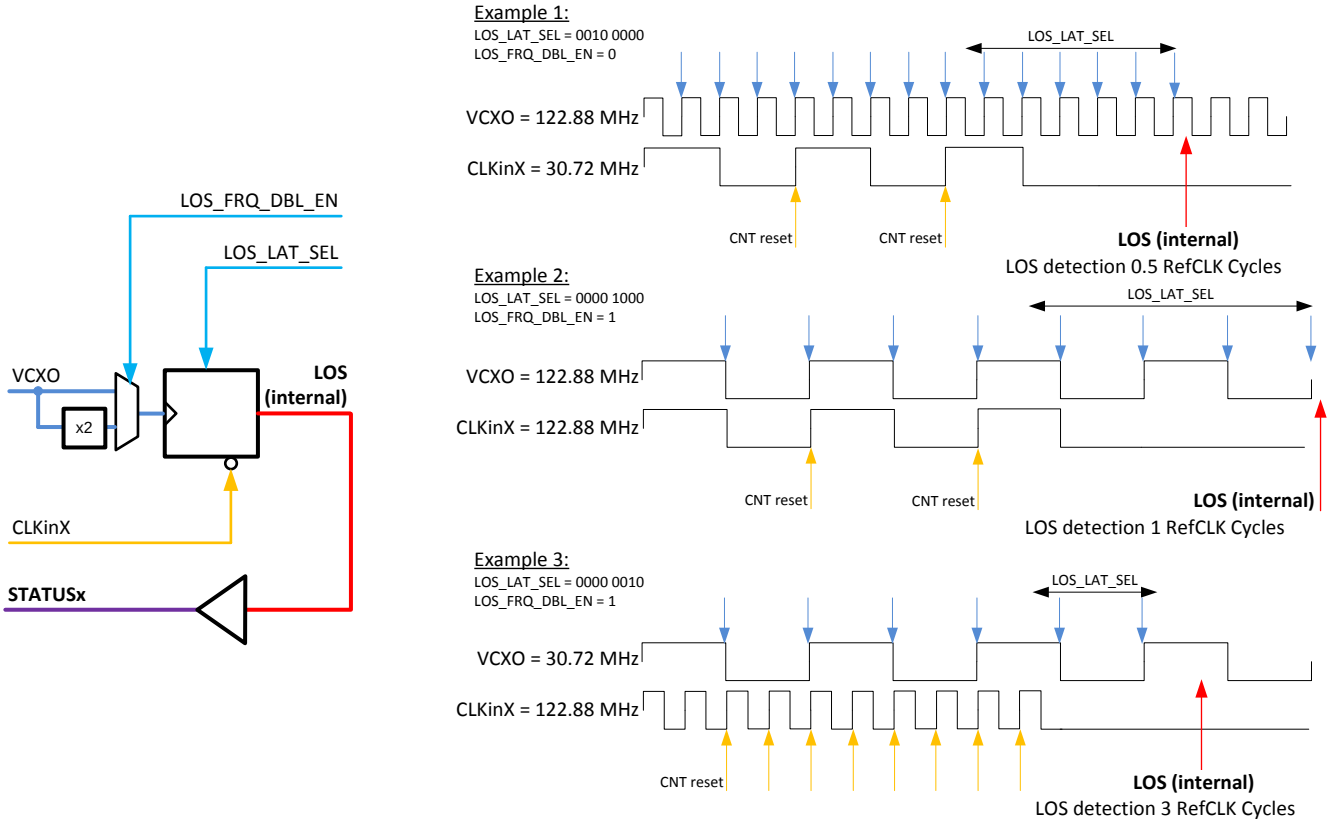


Figure 17. LOS Detection

Table 5. Recommended LOS Register Configurations

CLKin TO OSCin FREQUENCY RATIO	LOS_LAT_SEL	LOS_FRQ_DBL_EN	MAX LOS DETECTION LATENCY IN CLKin CYCLES
0.25	0010 0000b	0	0.5
0.5	0000 1000b	0	1
1	0000 1000b	1	1
1 (OSCin ≥ 250MHz)	0000 0100b	0	2
2	0000 0100b	1	2
4	0000 0010b	1	3

9.3.1.2.2 LOS – Reference Clock Recovery

LOS de-assertion can be programmed to 15 to 4095 reference clock cycles (CLKINx_LOS_REC_CNT[7:0]).

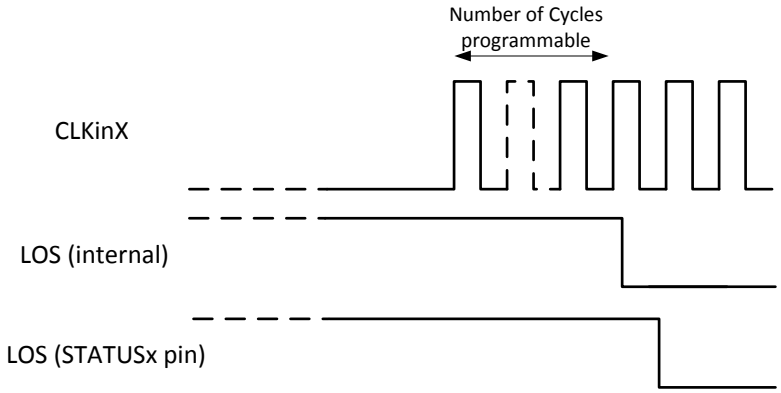


Figure 18. LOS Deassertion

9.3.1.3 Driving CLKin and OSCin Inputs

9.3.1.3.1 Driving CLKin and OSCin Pins With a Differential Source

The CLKin ports and OSCin can be driven by differential signals. TI recommends setting the input mode to differential (CLKINX_SE_MODE = 0) when using differential reference clocks. The LMK0461x internally AC couples the inputs with on-chip capacitors. An optional AC-coupling cap can be connected as shown in input termination sachems. The recommended circuits for driving the CLKin or OSCin pins with either LVDS or LVPECL are shown in Figure 19 and Figure 20.

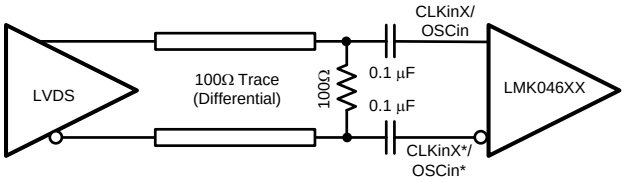


Figure 19. Termination for an LVDS Reference Clock Source

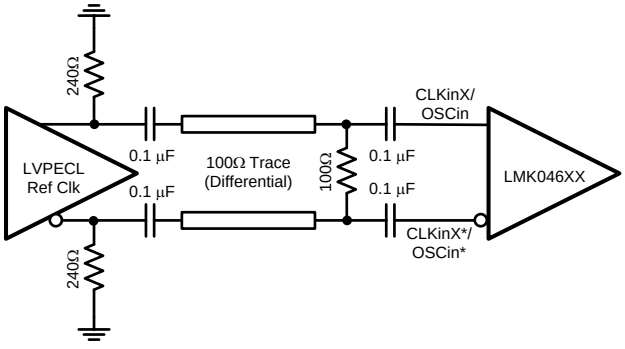


Figure 20. Termination for an LVPECL Reference Clock Source

Also, a reference clock source can produce a differential sine wave output can drive the CLKin pins using Figure 21.

NOTE

The signal level must conform to the requirements for the CLKin pins listed in *Clock Input Characteristics (CLKinX)*. CLKINX_SE_MODE is recommended to be set to differential mode (CLKINX_SE_MODE = 0).

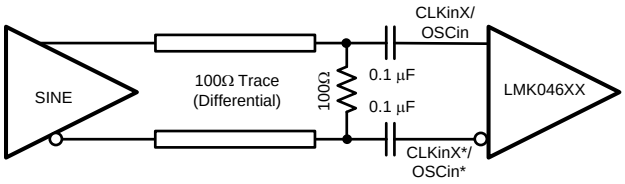


Figure 21. CLKinX/X* Termination for a Differential Sinewave Reference Clock Source

9.3.1.3.2 Driving CLKin and OSCin Pins With a Single-Ended Source

The CLKin pins of the LMK0461x family can be driven using a single-ended reference clock source, like a sine wave source or an LVCMOS or LVTTL source. Either AC coupling or DC coupling may be used. In the case of the sine wave source that is expecting a 50-Ω load, TI recommends using AC coupling as shown in Figure 22 with a 50-Ω termination.

NOTE

The signal level must conform to the requirements for the CLKin pins listed in *Clock Input Characteristics (CLKinX)*. CLKINX_SE_MODE is recommended to be set to single-ended mode (CLKINX_SE_MODE = 1).

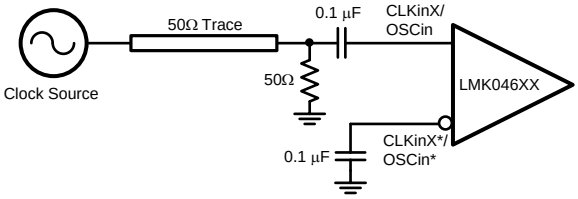


Figure 22. CLKinX/X* and OSCin AC-Coupled Single-Ended Termination

If the CLKin pins are being driven with a single-ended LVCMOS or LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, the CLKINX_SE_MODE should be set to single-ended buffer mode (CLKINX_SE_MODE = 1) and the voltage swing of the source must meet the specifications for DC-coupled, single-ended mode clock inputs given in *Clock Input Characteristics (CLKinX)*. If AC coupling is used, the CLKINX_SE_MODE should be set to the differential buffer mode (CLKINX_SE_MODE = 0). The voltage swing at the input pins must meet the specifications for AC-coupled, differential mode clock inputs given in *Clock Input Characteristics (CLKinX)*. In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC-coupling capacitor is sufficient.

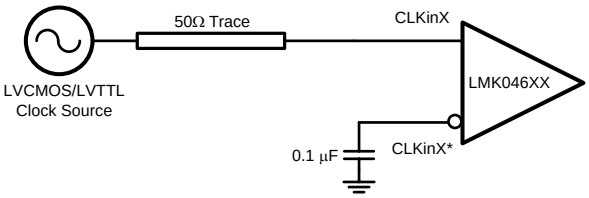


Figure 23. DC-Coupled LVCMOS or LVTTL Reference Clock

9.3.2 Clock Outputs (CLKoutX)

This section describes all related features of the clock outputs.

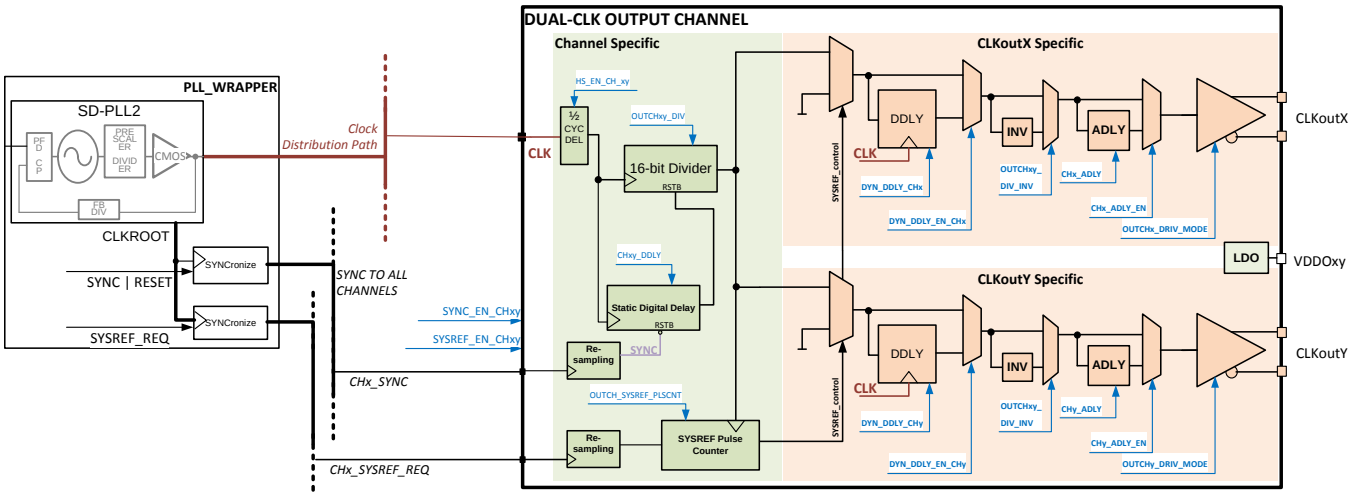


Figure 24. Clock Output Block and SYNC Clocking Path

9.3.2.1 HCSL

Figure 25 shows a typical implementation for the HCSL output driver mode. HCSL requires external 50-Ω termination resistors. Optionally, source resistors in the range from 22 Ω to 33 Ω are employed to eliminate ringing.

For HSCL outputs, set OUTCHxx_DRIV_MODE to 0x3F.

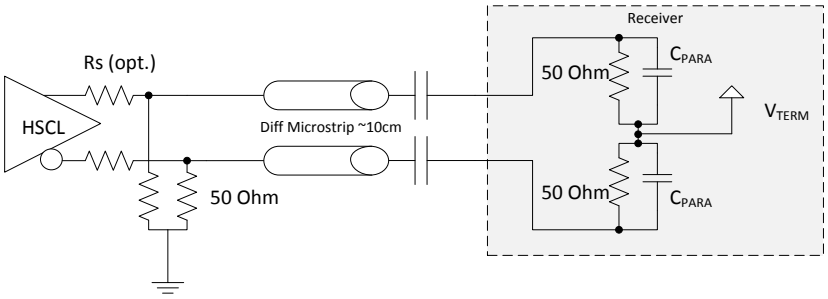


Figure 25. HCSL Output Termination

Figure 26 and Figure 27 show different connection methods to a LVPECL receiver.

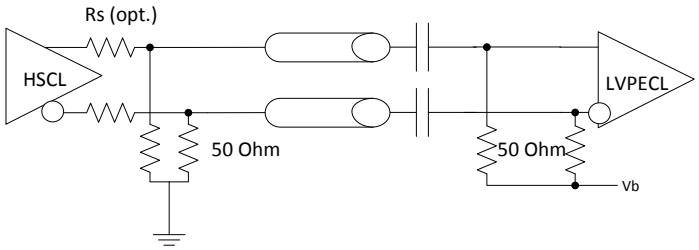


Figure 26. HCSL to LVPECL With Bias Voltage Vb (Voltage as Required for Receiver Bias)

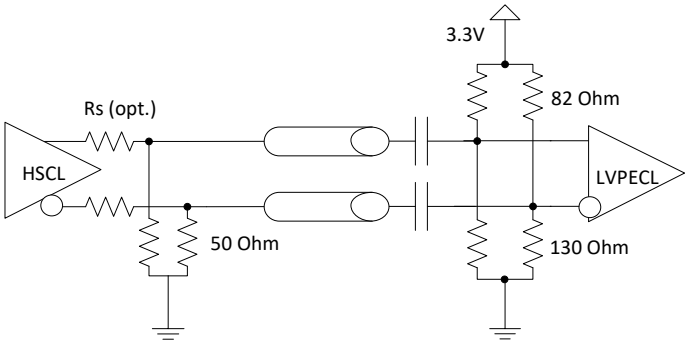


Figure 27. HCSL to LVPECL

9.3.2.2 HSDS

HSDS does not need external output termination (see Figure 28).

For HSDS: 8-mA outputs set OUTCHxx_DRIV_MODE to 0x18.

For HSDS: 6-mA outputs set OUTCHxx_DRIV_MODE to 0x14.

For HSDS: 4-mA outputs set OUTCHxx_DRIV_MODE to 0x10.

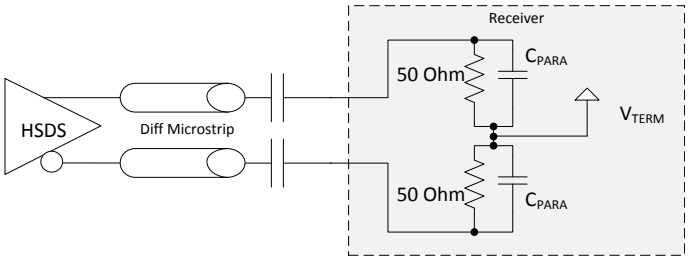


Figure 28. HSDS Output Termination

Figure 29 to Figure 31 show different connection methods to a LVPECL and LVDS receiver. In case of LVDS receivers, use HSDS 4-mA or HSDS 6-mA and for LVPECL use HSDS 8-mA setting.

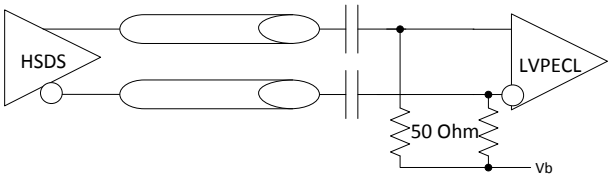


Figure 29. HSDS to LVPECL With Bias Voltage Vb (Voltage as Required for Receiver Bias)

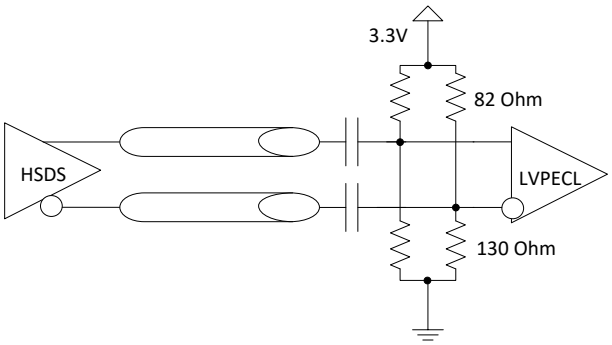


Figure 30. HSDS to LVPECL

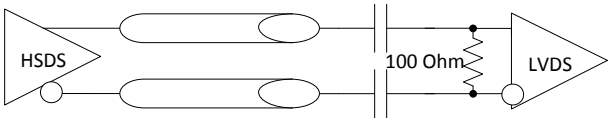


Figure 31. HSDS to LVDS

9.3.2.3 SYNC

See additional information about the SYNC pin in *STATUS0/1 and SYNC Pin Functions*.

SYNC aligns all clock outputs to start at a common rising clock distribution path clock edge. Clocks divided by 1 or divider bypass are not gated during the SYNC event.

SYNC is not available in buffer mode.

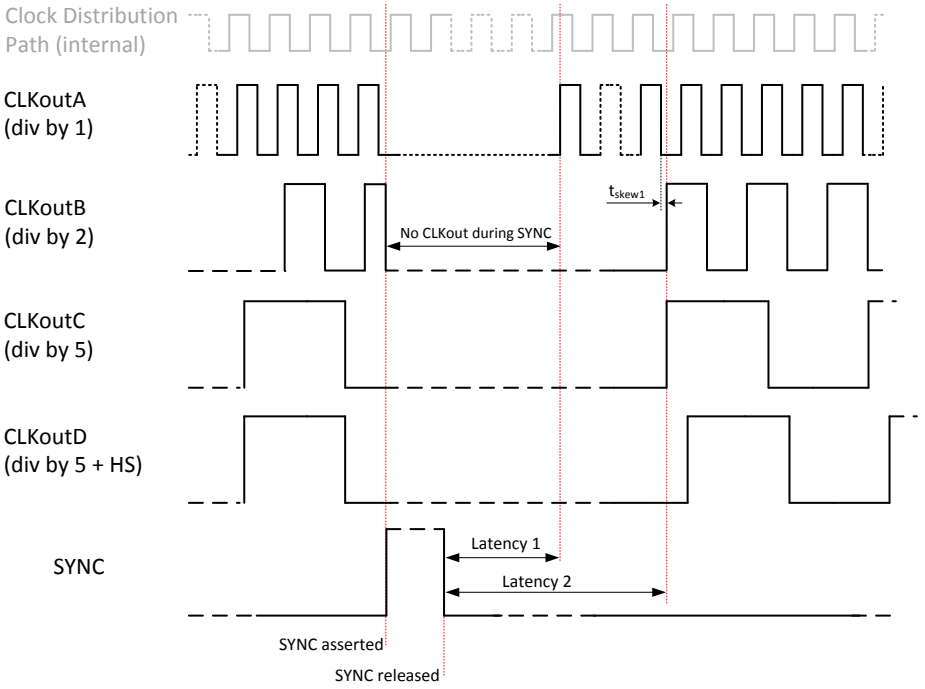


Figure 32. SYNC Example

9.3.2.4 Digital Delay

Digital (coarse) delay allows an output to be delayed by 1 to 255 periods of the clock distribution path frequency. The delay step can be as small as half the period of the clock distribution path frequency by using the HS_EN_CHx bit.

The digital delay step size calculates with: 1 / VCO frequency / prescaler

1. Fixed digital delay (per output channel)
2. Dynamic digital delay (per output)

9.3.2.4.1 Fixed Digital Delay

Fixed digital delay value takes effect on the clock outputs after a SYNC event. As such, the outputs are LOW for a while during the SYNC event. Applications that cannot accept clock breakup when adjusting digital delay should use dynamic digital delay.

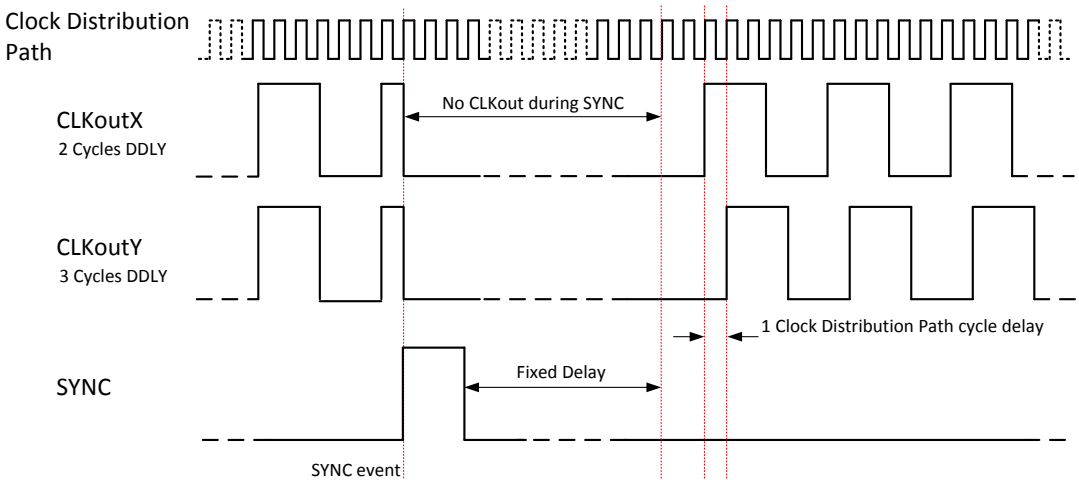


Figure 33. Fixed Digital Delay Example

Table 6. Digital Delay Register Controls

REGISTER NAME	DESCRIPTION
HS_EN_CHx	Enables a Half-Step for Channel X: 0.5 / VCO frequency / Prescaler
CHx_DDLY	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.3.2.4.2 Dynamic Digital Delay

Additionally, for the fixed digital delay per output channel, each output can be individually delayed using dynamic digital delay. Up to 5 periods of the clock distribution path frequency can be shifted.

The setting applies without SYNC to the output.

Table 7. Dynamic Digital Delay Register Controls

REGISTER NAME	DESCRIPTION
DYN_DDLY_CHx_EN	Enable CHx Dynamic Digital Delay.
DYN_DDLY_CHx	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.3.2.5 Analog Delay

Analog delay is available for all outputs. The typical step size is 60 ps and covers a total range of 1.3 ns.

Table 8. Analog Delay Register Controls

REGISTER NAME	DESCRIPTION
CHx_ADLY_EN	Enables Analog Delay for Channel X.
CHx_ADLY	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.

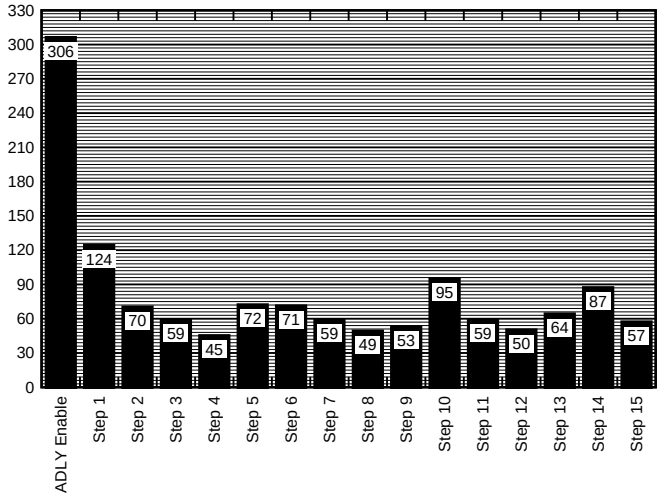


Figure 34. Analog Delay

9.3.3 OSCout

The default function for OSCout is providing two buffered LVCMOS copies (in phase or complementary) of the external VCXO. Additionally, an 8-bit divider is integrated. The multiplexer selects the VCXO input or high-speed clock distribution tree. The output type can be programmed to HSDS, HCSL, and LVCMOS. See *Output Termination Scheme* for test load descriptions. When OSCout is programmed for differential output from OSCin, the OSCout signal will be inverted from input.

NOTE

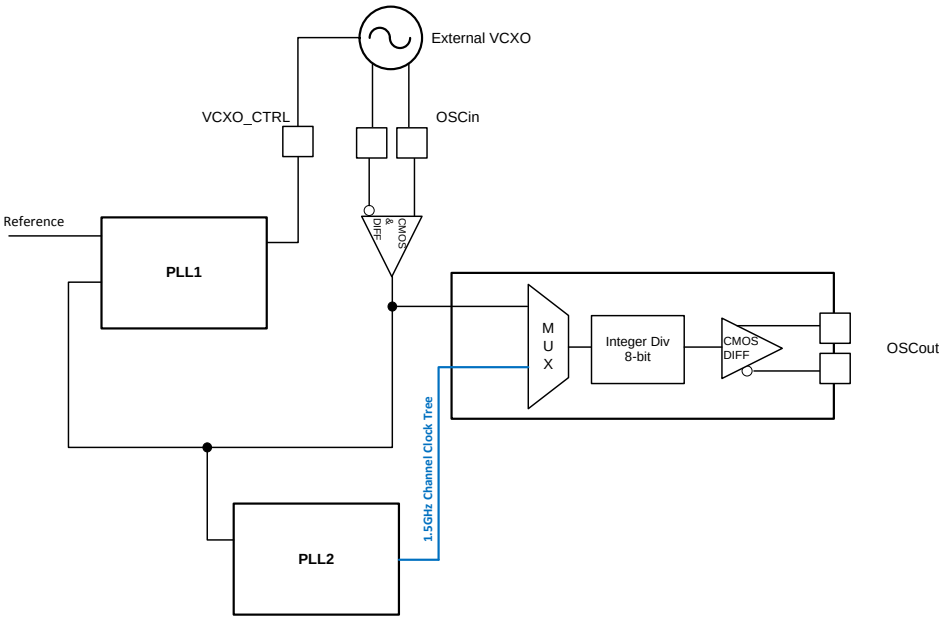


Figure 35. OSCout Block

9.3.3.1 Pin-Controlled OSCout Divider

During power up (see *Power-Up Sequence*) after RESET = 1, the state of the SYNC pin is sampled. The input level determines the OSCout divider setting.

NOTE

This function is only available after power up and RESET transition from LOW to HIGH.

Table 9. Pin-Controlled OSCout Divider Settings

SYNC PIN INPUT LEVEL AT POWER UP OR RESET TRANSITION FROM LOW TO HIGH	OSCout DIVIDER SETTING
LOW	1
OPEN	2
HIGH	4

9.3.4 STATUS0/1 and SYNC Pin Functions

Status and SYNC Pins supports 1.8-V logic and it can be configured as:

- Input
- Output

Common STATUS0/1 and SYNC Pin Functions describes the common input and output pin functions.

SYNC and STATUS0 have additional features that are restricted to the pins. See *Additional SYNC Pin Functions* and *Additional STATUS0 Pin Functions*.

9.3.4.1 Common STATUS0/1 and SYNC Pin Functions

Two status pins are available (STATUS0, STATUS1). STATUSx/SYNC_OUTPUT_HIZ = 1 configures the pins as input, while STATUSx/SYNC_OUTPUT_HIZ = 0 configures the pins as output. STATUSx/SYNC_INT_MUX register configures the pin functions in Table 10.

Table 10. Common STATUS0/1 and SYNC Pin Functions

FUNCTION	INPUT/OUTPUT	DESCRIPTION
SDO	Output	Serial Data Output for 4-wire SPI
LD1 and LD2	Output	Digital Lock Detect for PLL1 and PLL2
LD1	Output	Digital Lock Detect for PLL1
LD2	Output	Digital Lock Detect for PLL2
LD1 and LD2 and not Holdover	Output	PLL1 Lock Detect and PLL2 Lock Detect and not PLL1 Holdover
LD1 and not Holdover	Output	PLL1 Lock Detect and not PLL1 Holdover
LOS	Output	Output of LOS Block
Holdover status	Output	Output of Holdover Status. High = Holdover. Low = Normal operation
Holdover Control	Input	Manual Holdover entry through pin. See *Holdover*.
Copy SYNC pin	Output	Outputs a copy of SYNC pin
Copy CLKIN_SEL pin	Output	Outputs a copy of CLKIN_SEL pin
PLL2 Reference Clock	Output	PLL2 Reference Clock (Copy of OSCin divided by PLL2 R)
PLL1_R	Output	Output PLL1_R Clock Frequency
PLL2_R	Output	Output PLL2_R Clock Frequency
PLL1_N	Output	Output PLL1_N Clock Frequency
PLL2_N	Output	Output PLL2_N Clock Frequency
Logic High	Output	
Logic Low	Output	

9.3.4.2 Additional STATUS0 Pin Functions

This chapter describes the additional functions that are available on STATUS0 pin only.

Table 11. Additional STATUS0 Pin Functions

FUNCTION	INPUT/OUTPUT	DESCRIPTION
CLKIN_SEL0	Input	In LMK04616, the STATUS0 pin in combination with CLKIN_SEL selects the inputs in pin mode.

9.3.4.3 Additional SYNC Pin Functions

This chapter describes the additional functions that are available on SYNC pin only.

Table 12. Additional SYNC Pin Functions

FUNCTION	INPUT/OUTPUT	DESCRIPTION
OSCout Div Control	Input	Sampled Pin Logic state at power up configures default OSCout divider setting. Low level = divide by 1 Mid level = divide by 2 High level = divide by 4
SYNC	Input	SYNC_PIN_FUNC=0 → SYNC output channels. See *SYNC* SYNC_PIN_FUNC=1 → Sysref Request SYNC_PIN_FUNC=2 → Reset PLL1 N-/R-Dividers SYNC_PIN_FUNC=3 → Reserved

9.3.5 PLL1 and PLL2

LMK0461x has two programmable PLLs. PLL1 is a very low bandwidth PLL with an external VCXO. The bandwidth of the PLL1 can be programmed from 3 Hz to 300 Hz. PLL2 is a high bandwidth PLL using an on-chip, very low phase noise LC VCO. PLL2 bandwidth can be programmed from 90 kHz to 1 MHz. The detailed description about the individual PLLs is provided in the following sections.

9.3.5.1 PLL1

PLL1 in LMK0461x is a very low bandwidth PLL. The PLL is a fully programmable, ultra-flexible design and is intended to be used for jitter cleaning of the noisy input clock. The PLL uses a semi-digital architecture and there is no need for external loop filter. The loop-filter has separated integral and proportional paths, which can be programmed individually to define the PLL transfer. There is a possibility to add higher order poles by connecting a capacitor outside the chip with a fixed on-chip resistor R_{CTRL}. The block diagram of the PLL1 is shown in Figure 36. The PLL uses an external VCXO as a voltage controlled oscillator. Both positive and negative gain VCXOs are supported by LMK046xx.

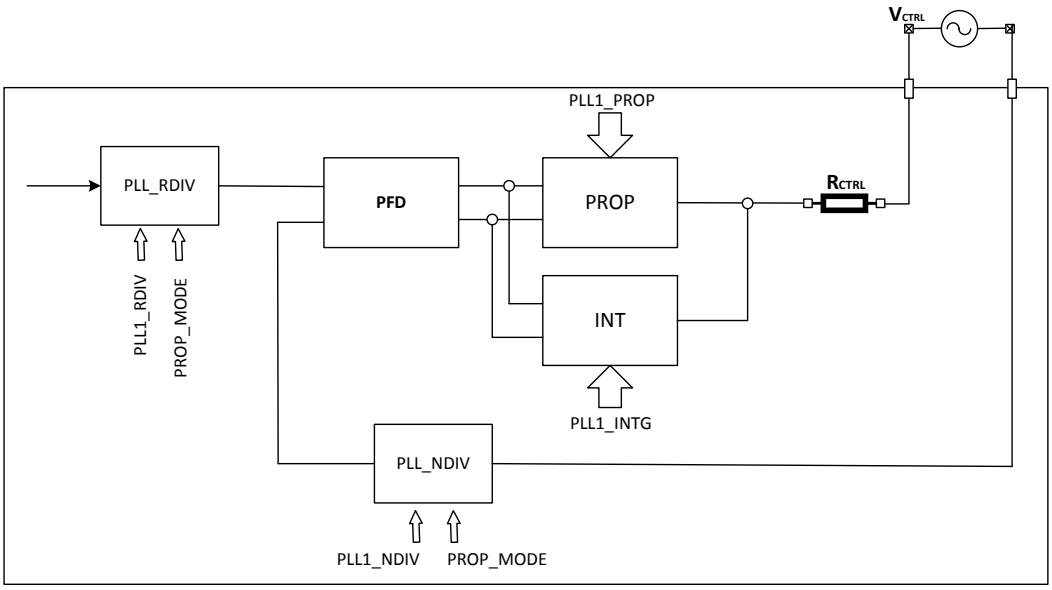


Figure 36. PLL1 Block Diagram

To reduce lock time, PLL1 supports two locking modes which can be individually configured by the user. When configured, PLL1 starts with Fastlock (with very high integral gain) and after lock, it switches to desired integral gain.

PLL1 Bandwidth depends on the VCXO gain and loop parameters. LMK0461x PLLs are designed with *active damping* technique. For a given VCXO gain and divider settings, the bandwidth can be programmed by using the PLL1_PROP settings. The higher the value, the higher the bandwidth.

Table 13 shows the internal PLL1 parameter, register and programming ranges. Use the TICS Pro EVM tool to calculate PLL1_PROP, PLL1_PROP_LF, PLL1_INTG, and PLL1_INTG_LF values.

Table 13. PLL1 Parameter and Register

PARAMETER	REGISTER	DESCRIPTION	MIN	TYP	MAX	UNIT
CLKINx_PLL1_RDIV	0x1B,0x1C,0X1D,0x1E, 0x1F,0x20,0x21,0x22	Input clock divider for PLL1	1		32771	
PLL1_NDIV	0x61,0x62	Feedback clock divider for PLL1	1		32771	
PLL1_PROP	0x5A	Proportional gain setting	0		127	
PLL1_PROP_FL	0x5B	Proportional gain setting for Fast Lock	0		127	
PLL1_INTG	0x59	Integral gain setting, C3 = 2.2 µF 1.92 MHz PDF, PLL1_PROP < 7	0	0	1	
PLL1_INTG_FL	0x59	Integral gain setting for Fast lock, C3 = 2.2 µF 1.92 MHz PDF, PLL1_PROP < 7	0	1	1	
PLL1_INTG	0x59	Integral gain setting, C3 = 2.2 µF 1.92 MHz PDF, PLL1_PROP ≥ 7	0	0	3	
PLL1_INTG_FL	0x59	Integral gain setting for Fast lock, C3 = 2.2 µF 1.92 MHz PDF, PLL1_PROP ≥ 7	0	3	3	
PLL1_INTG	0x59	Integral gain setting, C3 = 2.2 µF 0.12 MHz PDF, PLL1_PROP < 31	0	0	2	
PLL1_INTG_FL	0x59	Integral gain setting for Fast lock, C3 = 2.2 µF 0.12 MHz PDF, PLL1_PROP < 31	0	2	2	
PLL1_INTG	0x59	Integral gain setting, C3 = 2.2 µF 0.12 MHz PDF, PLL1_PROP ≥ 31	0	0	15	

Table 13. PLL1 Parameter and Register (continued)

PARAMETER	REGISTER	DESCRIPTION	MIN	TYP	MAX	UNIT
PLL1_INTG_FL	0x59	Integral gain setting for Fast lock, C3 = 2.2 µF 0.12 MHz PDF, PLL1_PROP ≥ 31	0	15	15	
R_{CTRL}				500		Ω

9.3.5.1.1 PLL1 Proportional Modes

PLL1 bandwidth can be increased or decreased even further by using the different PROP modes (see Table 14).

Table 14. PLL1 Proportional Modes

PROP MODE	REGISTER SETTINGS	DUTY CYCLE OF CLOCK
Default	PLL1_RDIV_4CY = 0 PLL1_NDIV_4CY = 0	50%
Low Pulse mode	PLL1_RDIV_4CY = 1 PLL1_NDIV_4CY = 1 PLL1_FBCLK_INV = 1 CLKINx_PLL1_INV = 1	(4/DIV) * 100
High Pulse mode	PLL1_RDIV_4CY = 1 PLL1_NDIV_4CY = 1 PLL1_FBCLK_INV = 0 CLKINx_PLL1_INV = 0	(1-4/DIV) * 100

In the default input mode, the proportional is effective for 50% of the PFD clock period. Using *low pulse mode*, the effect of the proportional is reduced which results in a reduced PLL bandwidth. Similarly, using the *high pulse mode*, the proportional is effective for more than half of the PFD cycle, which results in higher bandwidth.

PLL1_INTG settings affect the integral gain in the loop. TI recommends using setting 0 in normal mode and higher settings only for Fast lock using PLL1_INTG_FL.

9.3.5.1.2 PLL1 Higher Order Poles

There are no external resistors and capacitors required for the low bandwidth PLL1. However, to introduce 3rd order pole in the loop, external capacitor C3 can be attached to the control voltage, which in combination with the on-chip resistor, creates a pole at the desired frequency. Recommended maximum value of C3 for PLL1 lock is 2.2 µF.

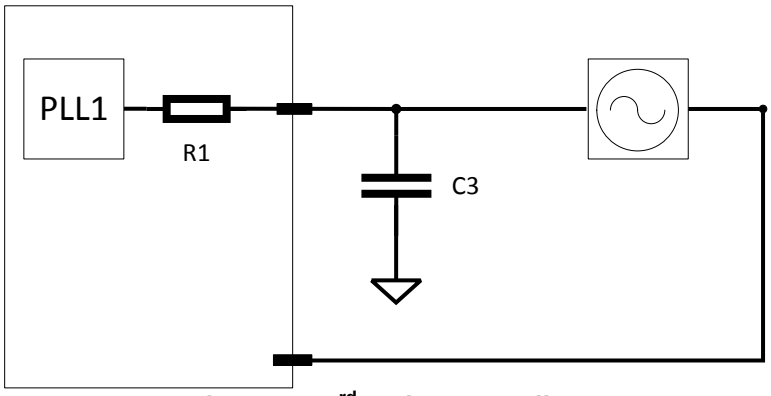


Figure 37. 3rd Order Loop Filter

9.3.5.2 PLL2

The second PLL in LMK046xx is a high bandwidth PLL requiring no external components. The PLL contains a very low phase noise on chip LC-based Voltage controlled oscillator (VCO). The VCO is very flexible and full programmable. Similar to PLL1, PLL2 is also a semi-digital PLL designed with an *active damping* concept. The bandwidth of the PLL can be programmed between 90 kHz to 1 MHz. PLL2 also has separated integral and proportional paths to control the VCO. The 3rd order pole can also be introduced by selecting the integrated resistors and capacitors.

The input clock frequency to the PLL2 can be doubled by using an integrated frequency doubler. Apart from that there are additional input modes possible to have more flexibility for bandwidth programming.

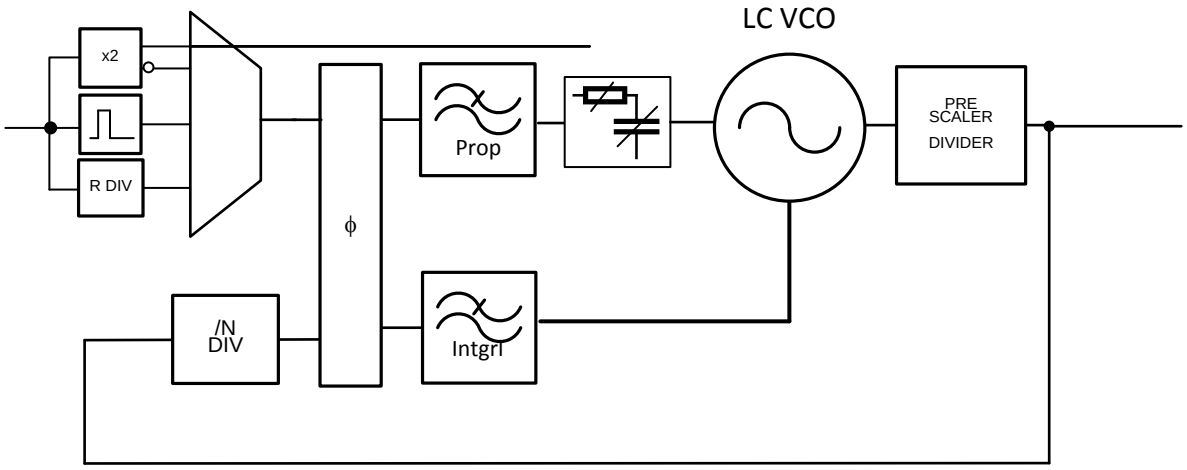


Figure 38. PLL2 Block Diagram

9.3.5.2.1 PLL2 Divider

PLL2 contains three dividers. Input clock can be divided down by using reference divider (PLL2_RDIV). Second divider is the high-frequency prescalar at the output of the VCO. Third divider is in the PLL feedback path which defines the PLL frequency multiplication ratio in combination with prescalar. Each of the three dividers is programmable with the registers as described in Table 15.

Table 15. PLL2 Divider

PARAMETER	REGISTER	DESCRIPTION	MIN	TYP	MAX	UNIT
PLL2_RDIV	0x76	Input clock divider for PLL2	1		31	
PLL2_NDIV	0x73, 0x74	Feedback clock divider for PLL2	1		65535	
PLL2_PRESCALER	0x146	The prescaler defines the Clock Distribution Frequency.	3		6	

9.3.5.2.2 PLL2 Input Modes

PLL2 has four input modes which can be selected by the user. These modes give more flexibility to adjust the PLL2 bandwidth. See Table 16.

Table 16. PLL2 Input Modes

INPUT MODE	DESCRIPTION
Doubler Mode	The Input clock gets multiplied by 2. The duty cycle of the clock is <50%.
Doubler invert mode	This mode is same like the doubler mode, where the input clock gets multiplied by 2, but the duty cycle of the output clock is >50%.
Pulse mode	The duty cycle of the input clock is adjusted to a fixed value and is >50%.
RDIV mode	The input divider is used to divide down the frequency with the range as shown in Table 15.

9.3.5.2.3 PLL2 Loop Filter

PLL2 design is based on semi-digital PLL architecture where the proportional and integral parts are separated from each other. Proportional gain and integral gain can be individually programmed by the user to define the bandwidth and noise transfer characteristics of the PLL2 in combination with the input modes.

Table 17. PLL2 Parameter and Register

PARAMETER	REGISTER	DESCRIPTION	MIN	TYP	MAX	UNIT
PLL2_PROP_SET	0x72	Proportional gain setting	0		63	
PLL2_CPROP	0x151	Proportional cap setting	3		5.4	pF
PLL2_INTG	0x80	Integral gain setting	0		31	
PLL2_RFILT	0x151	3rd order filter resistor selection	4.7		9.2	kΩ
PLL2_CFILT	0x153	3rd order filter capacitor selection	0	15	124	pF

The proportional gain can be changed using PLL2_PROP and PLL2_CPROP. The difference between the two modes is, PLL2_PROP controls the proportional charge pump current to define the gain and PLL2_CPROP controls the on-chip capacitor used in *active damping* to define the proportional gain. Higher values of PLL2_PROP result in higher proportional gain and Higher PLL2_CPROP values result in lower proportional gain.

9.3.5.2.4 PLL2 3rd Order Loop Filter

PLL2 also has programmable on-chip 3rd order loop filter in the proportional path to create additional pole for better noise cutting, as shown in Figure 38. The resistor and capacitor value can be programmed as shown in Table 18.

Table 18. 3rd Order Loop Filter

PARAMETER	DESCRIPTION	
R3	PLL2_EN_FILTER=1 → Enables resistor PLL2_RFILT=0 → 9.2 kΩ PLL2_RFILT=1 → 4.7 kΩ	
C3	PLL2_CFILT<5:0>	00000 → 0 pF 00001 → 4 pF .. 11111 →124 pF

9.3.5.2.5 PLL2 Voltage Controlled Oscillator (VCO)

PLL contains on chip very low phase noise LC oscillator. The tuning range of the oscillator is 5870 MHz to 6175 MHz. The VCO is tuned to the target frequency using the semi-digital control by the PLL loop. Due to the semi-digital control, the PLL loops tracks the temperature and input frequency change with its loop bandwidth.

9.3.5.2.6 Examples of PLL2 Setting

This section shows PLL2 setting examples to generate given loop bandwidth.

Table 19. PLL2 Settings

F_{IN_PLL2}	F_{VCO}	PLL2_RDIV	PLL2_NDIV	PRESCALER	INPUT MODE	PLL2_PROP	PLL2_INTG	PLL2_CPROP	R3, C3 (1)
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	21	0	5.4 pF	4.7 kΩ, 96 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	7	0	5.4 pF	4.7 kΩ, 96 pF

(1) See Table 18 for reference.

9.3.5.3 Digital Lock Detect

Both PLL1 and PLL2 support digital lock detect. Digital lock detect compares the phase between the reference path (R) and the feedback path (N) of the PLL. When the time error (phase error) between the two signals is less than a specified window size (ε), a lock detect count increments.

When the PLL1 lock detect count reaches a user specified value, PLL1_LOCKDET_CYC_CNT, lock detect is asserted true. Once digital lock detect is true, a single phase comparison outside the specified window causes the digital lock detect to be asserted false (see Figure 39).

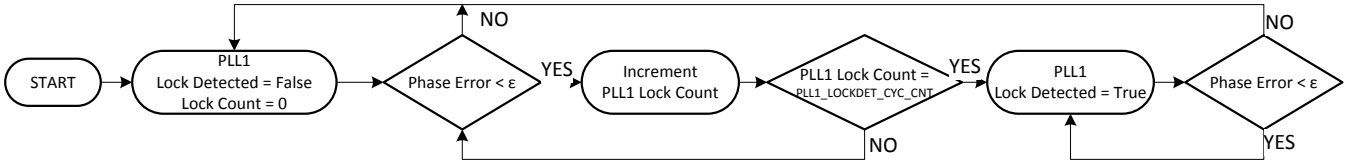


Figure 39. PLL1 Digital Lock Detect Flowchart

PLL2 DLD requires register 0xF6 = 0x02, 0x85 = 0x00, and 0x86 = 0x00 set. Then to program register 0xAD for valid digital lock detect. See *Recommended Programming Sequence*. When the PLL2 lock detect count reaches a user specified value, PLL2_LOCKDET_CYC_CNT, lock detect is asserted true. Once digital lock detect is true, a single phase comparison outside the specified window causes the digital lock detect to be asserted false (see Figure 40).

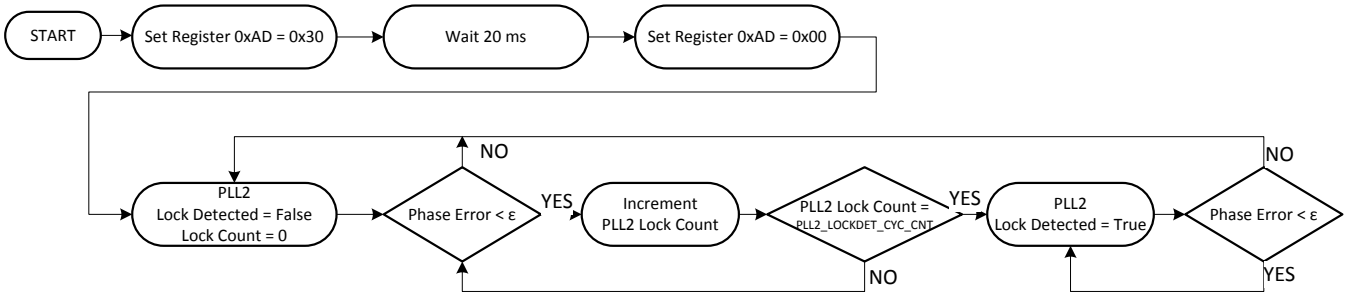


Figure 40. PLL2 Digital Lock Detect Flowchart

This incremental lock detect count feature functions as a digital filter to ensure that lock detect isn't asserted for only a brief time when the phases of R and N are within the specified tolerance for only a brief time during initial phase lock.

The digital lock detect signal can be monitored on the Status_LD1 or Status_LD2 pin. The pin may be programmed to output the status of lock detect for PLL1, PLL2, or both PLL1 and PLL2.

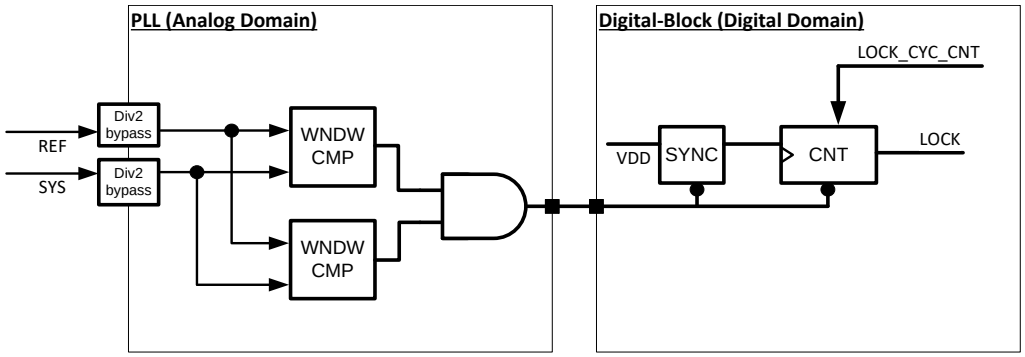


Figure 41. Digital Lock Detect Implementation

9.3.5.3.1 Calculating Digital Lock Detect Frequency Accuracy

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect feature can also be used with holdover to automatically exit holdover mode. See *Exiting Holdover* for more info.

9.3.6 Holdover

Holdover mode causes PLL2 to stay locked on frequency with minimal frequency drift when an input clock reference to PLL1 becomes invalid. While in holdover mode, the PLL1 charge pump is TRI-STATED and a fixed tuning voltage is set on CPout1 to operate PLL1 in open-loop.

9.3.6.1 Holdover Flowchart

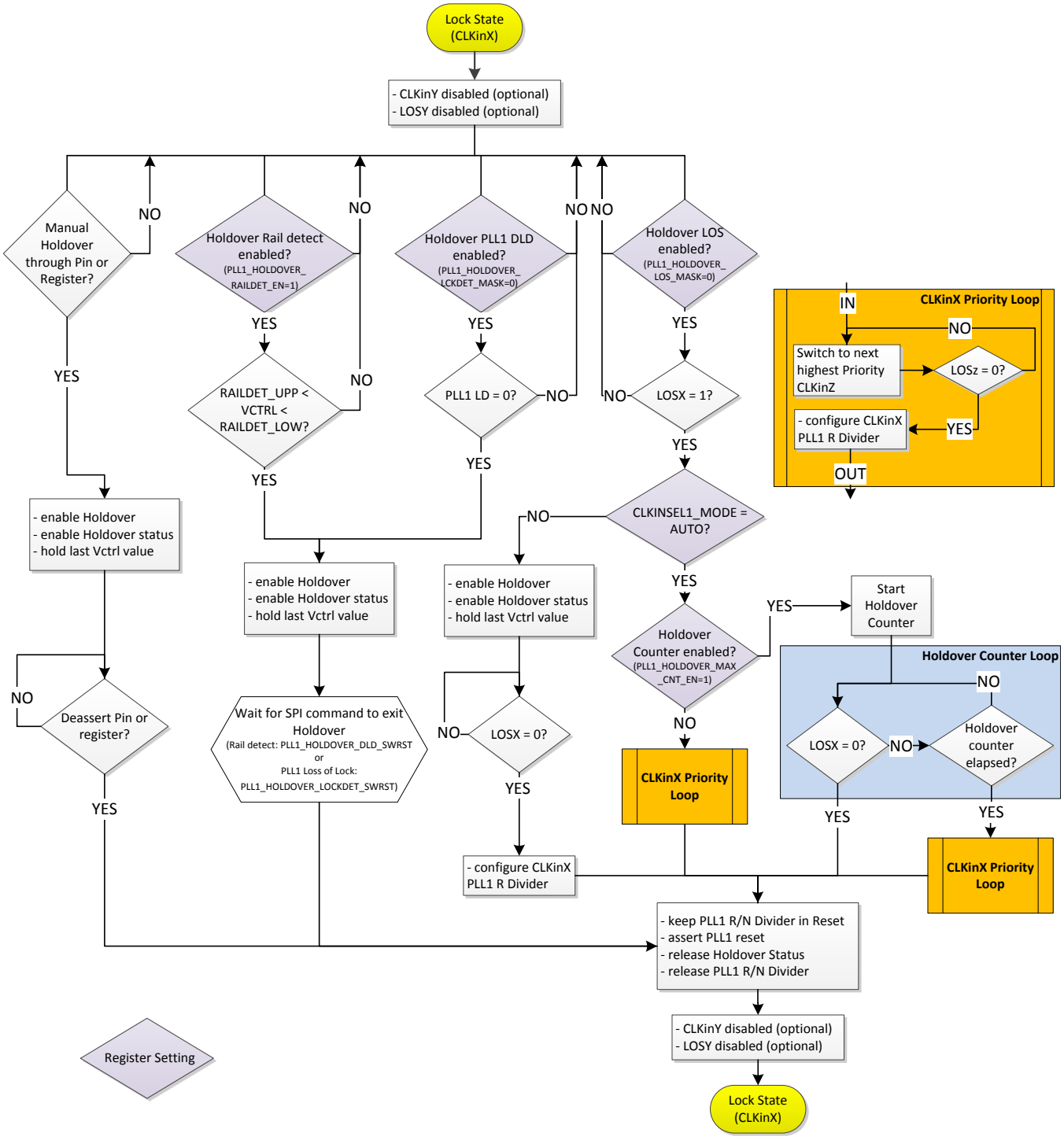


Figure 42. Holdover Flowchart Using LOS

9.3.6.2 Enable Holdover

Program HOLDOVER_EN = 1 to enable holdover mode for PLL1.

9.3.6.2.1 Automatic Tracked CTRL_VCXO Holdover Mode

In holdover mode, PLL1 retains the last used control voltage.

9.3.6.3 Enter Holdover

Holdover can be entered through different events.

- LOS_x detects reference loss.
- PLL1 DLD detects PLL1 unlock.
- CTRL_VCXO rail detect.
- Manual through register control
- Manual through pin
- Start-up into holdover

9.3.6.3.1 LOS_x Detect

Enter holdover if reference is lost.

9.3.6.3.2 PLL1 DLD Detect

Enter holdover if PLL1 is unlocked.

9.3.6.3.3 CTRL_VCXO Rail Detect

Rail detection allows to set upper and lower boundaries for the tuning voltage.

Once the boundaries are touched, the device enters holdover mode if this feature is enabled. The boundaries get compared against the current 6-bit value of the PLL1 storage cells array, PLL1_STORAGE_CELL. It can be determined whether the boundaries are absolute or relative boundaries.

Enter holdover if CTRL_VCXO represented as PLL1_STORAGE_CELL crosses a programmable high or low limit of CTRL_VCXO.

- If PLL1_STORAGE_CELL ≤ RAILDET_LOW, then go to holdover or into normal operation.
- If PLL1_STORAGE_CELL ≥ RAILDET_UPP, then go to holdover or into normal operation.

CTRL_VCXO_HIGH/LOW_RAIL granularity is 82.5 mV.

9.3.6.3.3.1 Absolute Limits

RAILDET_LOW and RAILDET_UPP values are considered as absolute numbers, being compared against current storage value.

9.3.6.3.3.2 Relative Limits

RAILDET_LOW and RAILDET_UPP values are considered as relative numbers. After PLL1 has locked the current storage value is added to the relative numbers to form the absolute boundary.

9.3.6.3.4 Manual Holdover Enable – Register Control

When PLL1_HOLDOVER_FORCE is 1 PLL1 enters holdover mode regardless of other conditions.

9.3.6.3.5 Manual Holdover Enable – Pin Control

The SYNC control pin can be programmed to control the entry and exit of holdover.

9.3.6.3.6 Start-Up into Holdover

During the initial programming, the LMK0461x can be configured to start-up into holdover. It presets the VCXO Control voltage to approximately 1.2 V. This allows PLL2 to lock to the VCXO reference. PLL1 locks as soon a valid reference input clock is detected. The holdover status can be optionally displayed at the status pins.

9.3.6.4 During Holdover

PLL1 is run in open-loop mode:

- PLL1 charge pump is set to TRI-STATE.
- PLL1 DLD is unasserted.
- The HOLDOVER status is asserted.
- During holdover, if the PLL2 was locked prior to entry of holdover mode, PLL2 DLD continues to be asserted.

- LOS engine searches for active input clock.
- PLL1 attempts to lock with the active clock input.

The HOLDOVER status signal can be monitored on the Status_LD1 or Status_LD2 pin by programming the PLL1_DLD_MUX or PLL2_DLD_MUX register to *Holdover Status*.

9.3.6.5 Exiting Holdover

Holdover mode can be exited in one of four ways.

- Manually by programming the device from the host.
- Manual through pin.
- Automatically by a clock operating within a specified ppm of the current PLL1 frequency on the active clock input.
- Automatically by LOS deassertion.
- Automatically by switching to next clock input after holdover counter overflow. The order of switching is set in a priority list.

9.3.6.6 Holdover Frequency Accuracy

The holdover frequency accuracy depends on the PLL1 loop bandwidth. A low loop bandwidth of ≤10 Hz results in less then 0.6-ppm accuracy typical.

9.3.6.7 Holdover Mode – Automatic Exit by LOS Deassertion

As soon as the reference clock is valid again and the LOS signal is deasserted, the PLL1_N and PLL1_R divider reset and PLL1 exits holdover.

9.3.6.8 Holdover Mode – Automatic Exit of Holdover With Holdover Counter

A programmable holdover counter can be set between 0 and 17 seconds count time. The counter starts counting as soon the device is in holdover.

If the reference clock is valid again within the specified time, the device exits holdover.

If the counter overflows, the device switches to the next clock input. The order of clock inputs is set in a priority list.

- Minimum Holdover counter configuration step size: 4.069 ns
- Holdover counter range: 0 – 17 s

9.3.7 JEDEC JESD204B

Table 20 illustrates the some possible SYNC and SYSREF modes.

Table 20. Possible SYNC/SYSREF_REQ Configurations

NAME	DESCRIPTION
SYNC Disabled	No SYNC occurs.
Pin or SPI SYNC	Basic SYNC functionality, SYNC pin polarity is selected by SYNC_POL. To achieve SYNC through SPI, toggle the SYNC_POL bit.
JESD204B Pulser on pin transition.	Produce SYSREF_PULSE_CNT programmed number of pulses on pin transition. SYNC_POL can be used to cause SYNC through SPI.
JESD204B Pulser on SPI programming.	Programming SYSREF_PULSE_CNT register starts sending the number of pulses.
External SYSREF request	When SYNC pin is asserted, continuous SYSERF pulses occur. Turning on and off of the pulses is SYNChronized to prevent runt pulses from occurring on SYSREF.
Continuous SYSREF	Continuous SYSREF signal.

LMK0461x family provides support for JEDEC JESD204B. High-frequency device clock and low frequency SYSREF clocks can be generated with programmable analog and digital delays and SYNC functionality. The device provides possibility to control the SYNC and SYSREF functions by SYNC pin (pin mode) or SPI programming. Each clock output can be used either as a device clock or SYSREF clock. Steps to use the SYNC and SYSREF modes are described in Figure 43.

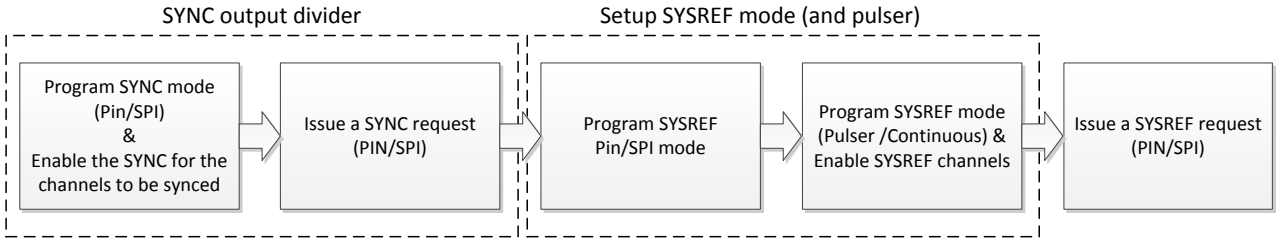


Figure 43. Manual SYSREF Setup

The programming of the SYNC and SYSREF modes can be already done at the device setup. One time SYNC for the output channels is issued automatically at the device start-up irrespective of the SYNC programming. Detail description on setting up the SYNC and SYSREF modes are described in the following sections.

9.3.7.1 SYNC Pins

The SYNC pin in LMK0461x family has multiple functions which can be configured by the user using SPI interface. Following table lists the possible function:

Table 21. SYNC Pins

BIT NAME	FUNCTION	
EN_SYNC_PIN_FUNC	Enables the different functions at the SYNC pin when 1	
SYNC_INV	Inverts SYNC Input when 1	
SYNC_PIN_FUNC[1:0]	00	SYNC output channels
	01	SYSREF Request
	10	Reset PLL1 N-divider and R-divider
	11	Reserved
SYNC_ANALOGDLY_EN	Enables the Analog delay at the SYNC input pin	
SYNC_ANALOGDLY[4:0]	Analog delay can be programed from 0-15. See *Analog Delay* for details	

9.3.7.2 SYNC modes

SYNC can be requested by either PIN or using the SPI interface. Following table lists the register values that must be programmed to use the SYNC functionality:

Table 22. Additional SYNC Bits

BIT NAME	FUNCTION
GLOBAL_SYNC	Global SW SYNC. Writing 1 puts the Device into SYNC mode. Writing 0 exits SYNC mode.
SYNC_EN_CH1 SYNC_EN_CH2 SYNC_EN_CH3_4 SYNC_EN_CH5 SYNC_EN_CH6 SYNC_EN_CH7_8 SYNC_EN_CH9 SYNC_EN_CH10	Enables the corresponding channel for SYNC functionality

Steps to configure each mode are described below.

- SYNC pin mode:
  1. EN_SYNC_PIN_FUNC should be set to 1. This enables the different functions supported by the SYNC pin.
  2. SYNC_PIN_FUNC[1:0] should be programmed to 00b (default). This sets the SYNC pin for SYNC function.
  3. SYNC_INV, when 0, SYNC is rising edge triggered. When set to 1, the SYNC pin is internaly inverted and is falling edge triggered.
  4. SYNC_EN_CHx should be set 1 for the channels which needs to SYNCed.
  5. Depending on the SYNC_INV value, the output channels are SYNChronized by either rising edge or the falling edge on the SYNC pin.
- SYNC SPI mode:
  1. EN_SYNC_PIN_FUNC should be set to 0. This disables the pin mode for SYNC function.
  2. SYNC_EN_CHx should be set 1 for the channels which must SYNCed.
  3. Writing 1 to the GLOBAL_SYNC puts the device into SYNC mode.

9.3.7.3 SYSREF Modes

Any channel can be programmed to generate SYSREF clock. There are different SYSREF modes supported by LMK0461x. SYSREF can be either fixed number of pulses or a continuous clock. There is a 5-bit register provided to program the number of pulses to be generated at each SYSREF request. Also, there is a possibility to control the number of pulses with the SYNC pin. Each SYSREF clock can be individually delayed. There are different options to introduce the delay in the SYSREF path. See *Digital Delay* and *Analog Delay* for programming the delays. Following bits needs to be programed to use the SYSREF feature:

Table 23. SYSREF Registers

BIT NAME	FUNCTION
EN_SYNC_PIN_FUNC	Enable SYNC_SYSREF features at SYNC pin
GLOBAL_CONT_SYSREF	Enable continuous SYSREF
GLOBAL_SYSREF	Trigger SYSREF, Self-clearing
OUTCH_SYSREF_PLSCNT	Set number of desired SYSREF pulses from 1 to 32. 0 Enables continuous SYSREF
SYSREF_EN_CH10 SYSREF_EN_CH9 SYSREF_EN_CH7_8 SYSREF_EN_CH6 SYSREF_EN_CH5 SYSREF_EN_CH3_4 SYSREF_EN_CH2 SYSREF_EN_CH1	Enable SYSREF feature at channel CHx

9.3.7.3.1 SYSREF Pulser

This mode allows for the output of 1 to 32 SYSREF pulses for every SYNC pin event or SPI programming. This implements the gapped periodic functionality of the JEDEC JESD204B specification.

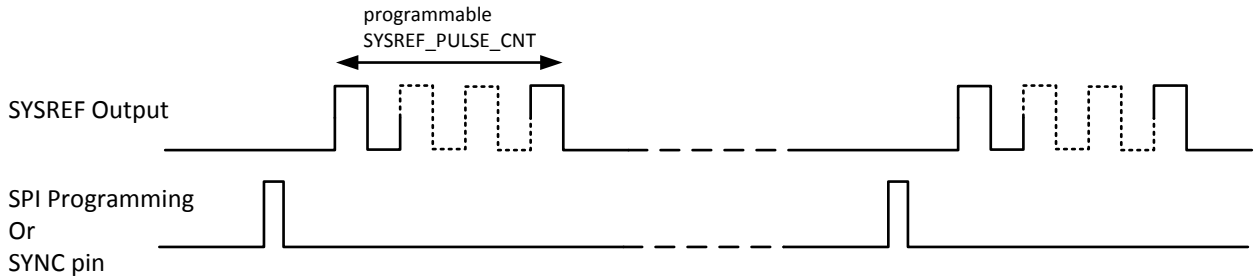


Figure 44. SYSREF Pulser

9.3.7.3.1.1 SPI Pulser Mode

OUTCH_SYSREF_PLSCNT is a 5-bit register that can be programmed to the required number of pulses.

When GLOBAL_SYSREF is programmed to 1, fixed number of pulses are defined by OUTCH_SYSREF_PLSCNT are generated at the output channels which are enabled for SYSREF. The GLOBAL_SYSREF bit is cleared automatically after fulfilling the SYSREF request.

9.3.7.3.1.2 Pin Pulser Mode

By programming EN_SYNC_PIN_FUNC= 1, SYNC_PIN_FUNC=01 and OUTCH_SYSREF_PLSCNT to the desired number of pulses, The SYSREF output is in pin control Pulser mode. The SYSREF clock can be initiated by a pulse at the SYNC pin. Fixed number of pulses as per the OUTCH_SYSREF_PLSCNT value are generated after a fixed latency.

9.3.7.3.1.3 Multiple SYSREF Frequencies

In case of multiple SYSREF frequencies the latencies until SYSREF pulses start are different. As shown in Figure 45, the different SYSREF signals are rising edge aligned with the device clock. The different SYSREF signals might not be rising edge aligned if different SYSREF frequencies are used.

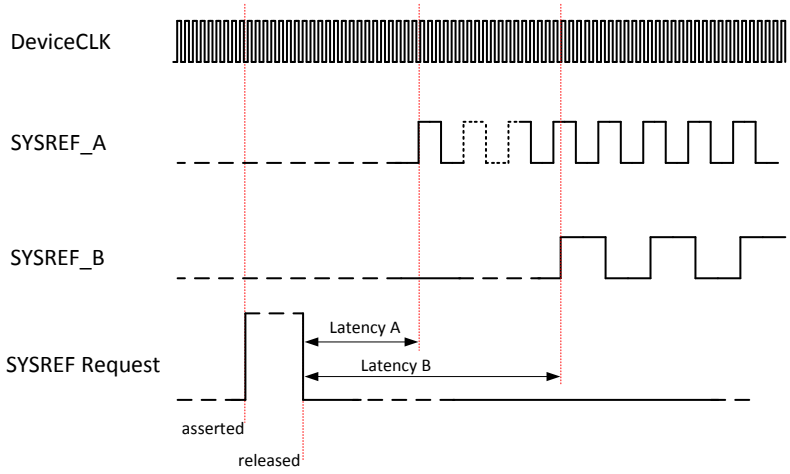


Figure 45. SYSREF Timing in Pulsor Mode With Different SYSREF Frequencies

9.3.7.3.2 Continuous SYSREF

This mode allows for continuous output of the SYSREF clock.

Setting GLOBAL_CONT_SYSREF to 1 allows for continuous output of the SYSREF clock.

Continuous operation of SYSREF is not recommended due to crosstalk from the SYSREF clock to device clock. JESD204B is designed to operate with a single burst of pulses to initialize the system at start-up, after which it is theoretically not required to send another SYSREF because the system continues to operate with deterministic phases.

If continuous operation of SYSREF is required, consider using a SYSREF output from a non-adjacent output or SYSREF from the OSCout pin to minimize crosstalk.

Figure 46. Continuous SYSREF

9.3.7.3.3 SYSREF Request

This mode allows an external source to SYNChronously turn on or off a continuous stream of SYSREF pulses using the SYNC pin.

When programming EN_SYNC_PIN_FUNC= 1, SYNC_PIN_FUNC=01 and OUTCH_SYSREF_PLSCNT=0, the SYSREF output is in pin mode. The SYSREF pulses can be controlled by the pulse width at the SYNC pin. When the SYNC pin is asserted, the channel is SYNChronously set to continuous mode providing continuous pulses at the SYSREF frequency until the SYNC pin is unasserted. SYSREF stops after completing the final pulse SYNChronously.

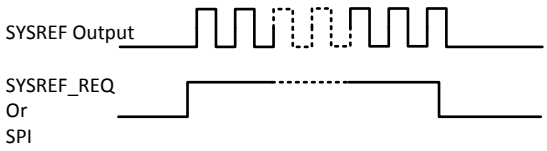


Figure 47. SYSREF Request

9.3.7.4 How to Enable SYSREF

Enabling JESD204B operation involves SYNChronizing all the clock dividers and programming of the delays, then configuring the actual SYSREF functionality.

9.3.7.4.1 Setup Example 1: Pulser Mode, Pin Controlled

1. Program EN_SYNC_PIN_FUNC=1, SYNC pin is enabled for SYSREF requests.
2. Program SYNC_PIN_FUNC=01, SYNC pin is programmed to accept the SYSREF requests.
3. Program OUTCH_SYSREF_PLSCNT= xx (max 32), programs the number of SYSREF pulses to be generated.
4. Program SYSREF_EN_CHxx=1, enables corresponding output channels to generate SYSREF clock pulses.
5. Apply rising Edge at SYNC pin generates xx number of at the enabled at the enabled channel.

9.3.7.4.2 Setup Example 2: Pulser Mode, Spi Controlled

1. Program EN_SYNC_PIN_FUNC=0, the SYSREF function on the SYNC pin is not enabled.
2. Program OUTCH_SYSREF_PLSCNT= xx (max 32), programs the number of SYSREF pulses to be generated.
3. Program SYSREF_EN_CHxx=1, enables corresponding output channels to generate SYSREF clock pulses.
4. Programming GLOBAL_SYSREF=1 generates the defined number of pulses on the SYSREF enabled channels.

9.3.8 Zero Delay Mode (ZDM)

The LMK0461x zero delay mode (ZDM) is an internal feedback loop that minimizes the phase error between output and reference input. The feedback can be selected from CLKout6 or CLKout9.

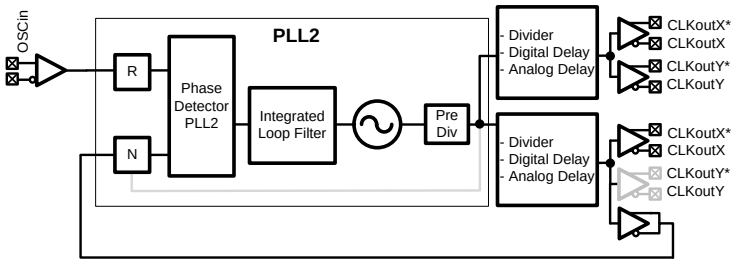


Figure 48. Zero Delay Mode

9.3.9 Power-Up Sequence

Figure 49 shows the steps to power up the device.

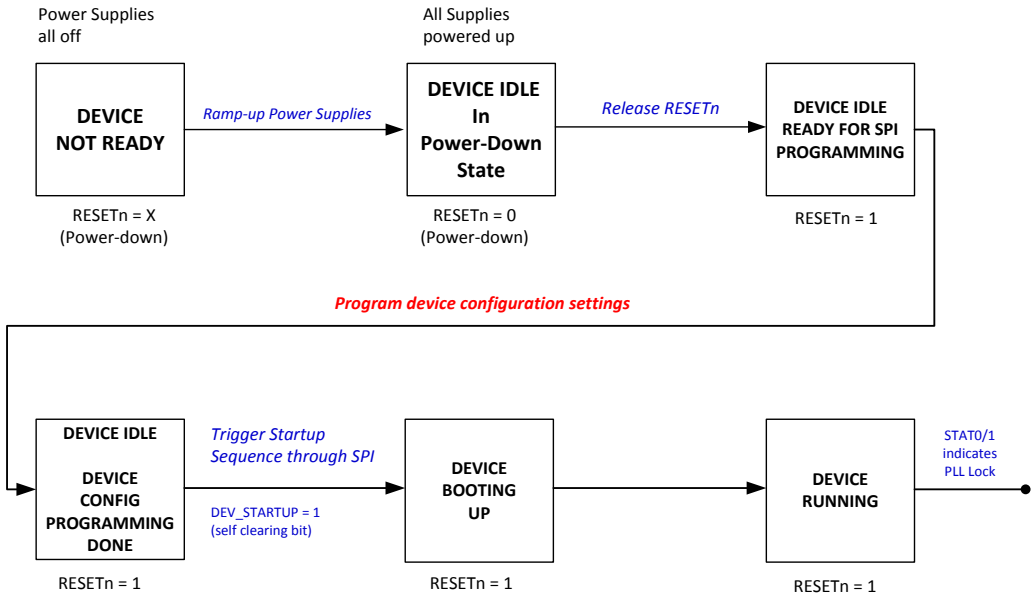


Figure 49. Simplified Power-Up Sequence

The first step is to apply all the supplies needed for device to be functional. The RESETn should be kept at logic 0 when power supplies start ramping. LMK046xx devices do not need any specific power up sequencing for the external power supplies. The on-chip POR logic makes sure that the device stays in power-down state until all the supplies are available.

After all the device power supplies are stable, RESETn can be released to logic 1. The device enters idle state and is now ready for the SPI programming.

After programming the device configuration, the DEV_start-up should be triggered using SPI, which initiates the device bootup sequence. The loading of the configurations to the corresponding functional blocks and enable sequencing is cared for by the on-chip state machines. One-time SYNC is also issued to the output channels during device booting. The lock signals for the PLLs can be observed at the STAT0/1.

Figure 50 shows the LMK0461x booting sequence of operations in details. Branch A, B, and C run in parallel.

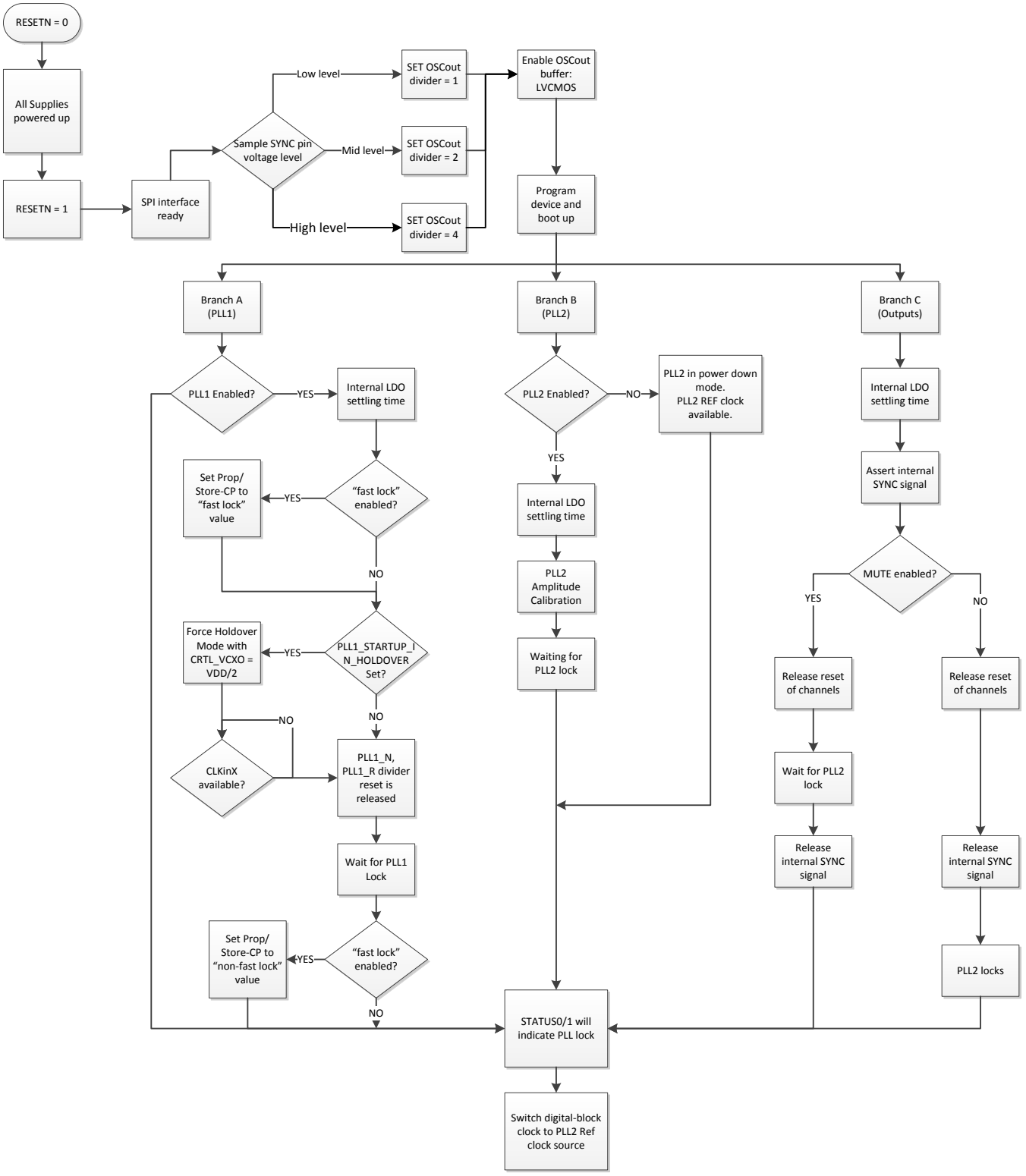


Figure 50. Detailed Power-Up Sequence

9.4 Device Functional Modes

The following section describes the settings to enable various modes of operation for the LMK0461x device family.

The LMK0461x device is a flexible device that can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

9.4.1 Dual PLL

illustrates the typical use case of the LMK0461x device family in dual-loop mode. In dual-loop mode the reference to PLL1 from CLKin0, CLKin1, CLKin2, or CLKin3. An external VCXO is used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO by using a narrow loop bandwidth. The VCXO output may be buffered through the OSCout port. The VCXO is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to 8 divide or delay blocks which drive up to 16 clock outputs.

Holdover functionality is optionally available when the input reference clock is lost. Holdover works by fixing the tuning voltage of PLL1 to the VCXO.

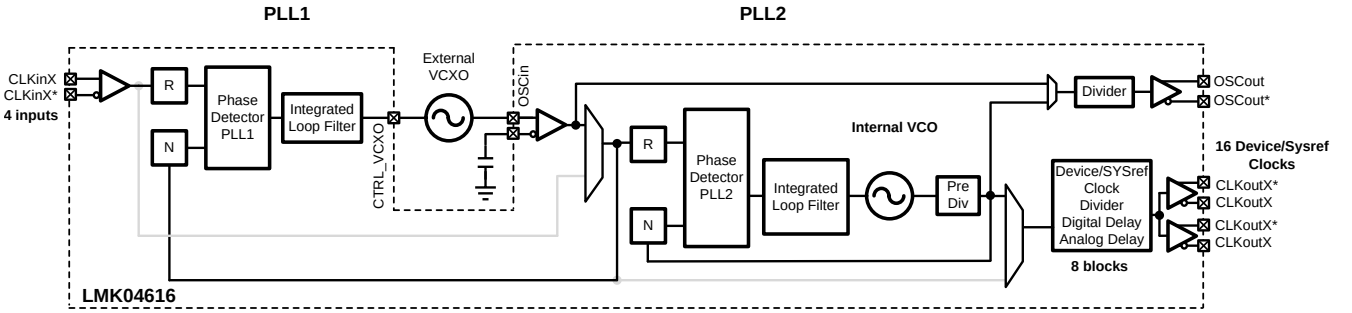


Figure 51. Simplified Functional Block Diagram for Dual-Loop Mode

9.4.2 Single PLL

No LOS detection and automatic reference switching available in this mode.

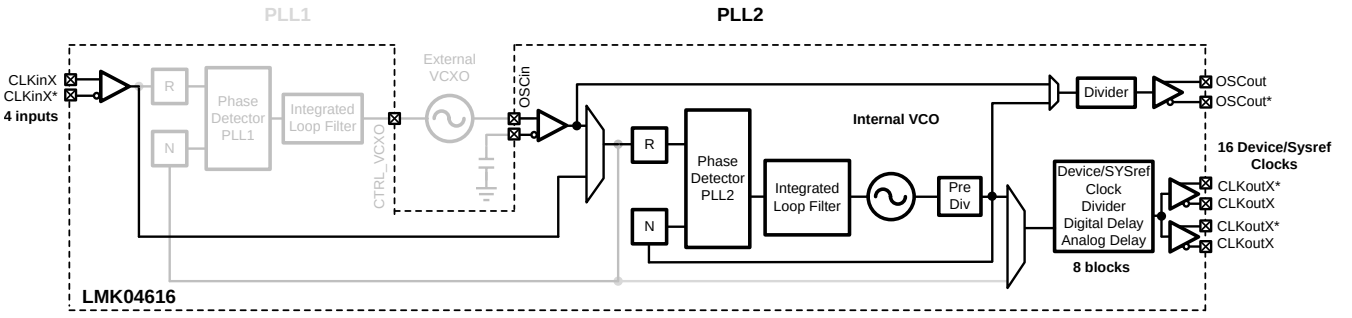


Figure 52. Simplified Functional Block Diagram for PLL2 Only or Clock Generator Mode

Device Functional Modes (continued)

9.4.3 PLL2 Bypass

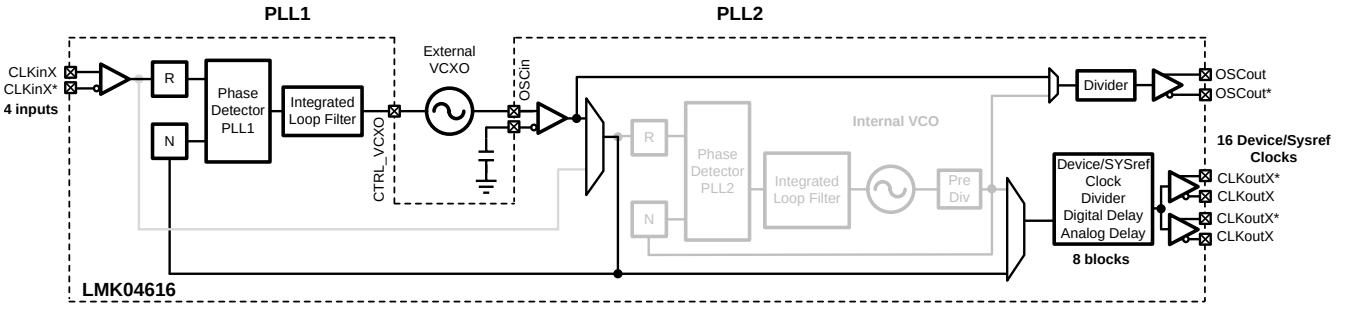


Figure 53. Simplified Functional Block Diagram for PLL1 Only or PLL2 Bypass Mode

9.4.4 Clock Distribution

No LOS detection and automatic Reference Switching available in this mode.

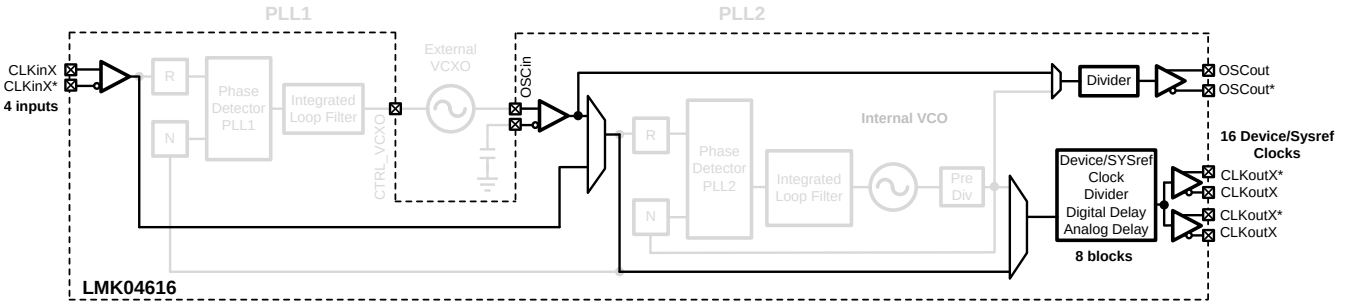


Figure 54. Simplified Functional Block Diagram for Clock Distribution Mode

9.5 Programming

LMK0461x device is programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 15-bit address field (A14 to A0) and a 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes *high* to latch the contents into the shift register. TI recommends programming registers in numeric order -- for example, 0x000 to 0x1FFF -- to achieve proper device operation. Each register consists of one or more fields that control the device functionality. See the electrical characteristics and Figure 1 for timing details.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

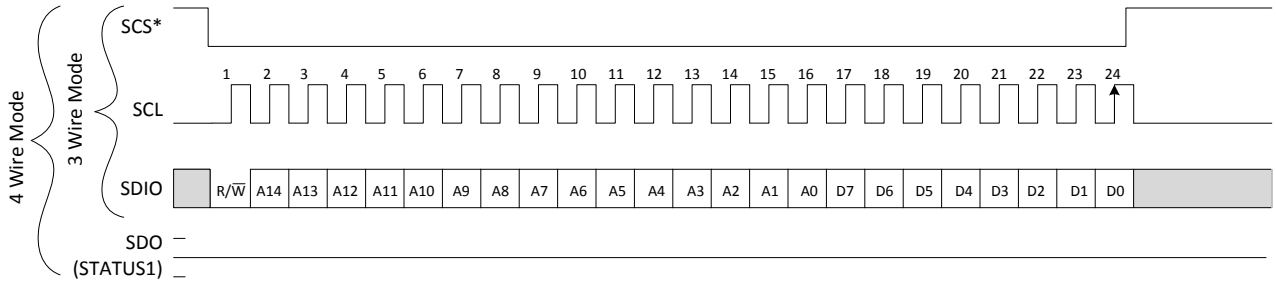


Figure 55. SPI Write

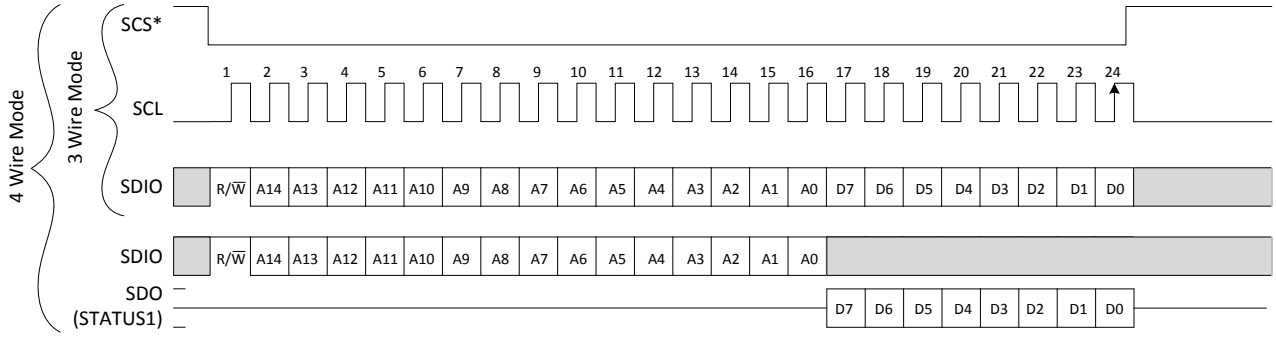


Figure 56. SPI Read

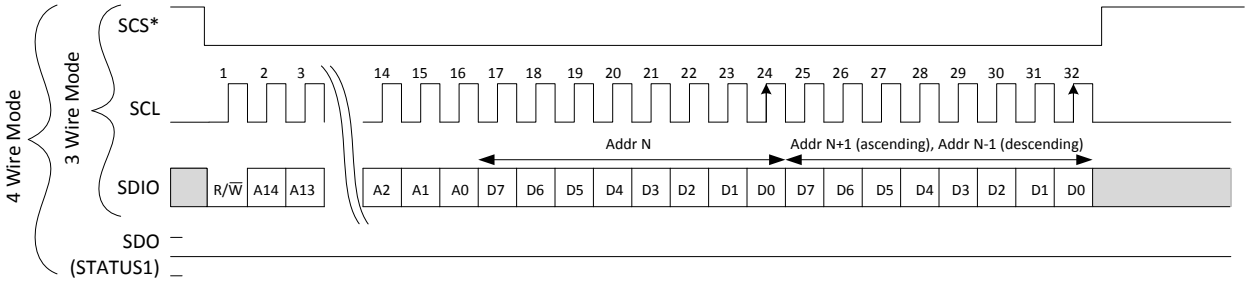


Figure 57. SPI Write – Streaming Mode

Programming (continued)

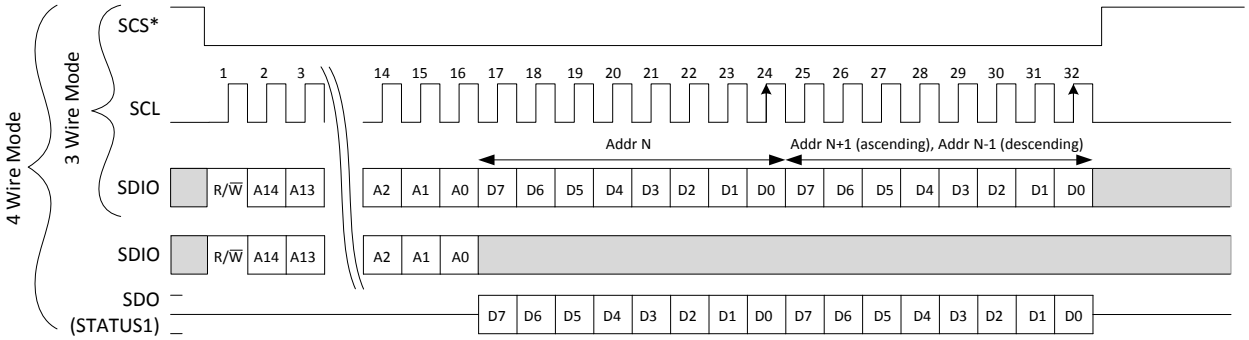


Figure 58. SPI Read – Streaming Mode

9.5.1 Recommended Programming Sequence

The default programming sequence from POR involves:

1. Toggle RESETn pin High-Low-High
2. Program all registers with Register 0x0011 bit 0 = 0
   - Register 0x85 = 0x00
   - Register 0x86 = 0x00
   - Register 0xF6 = 0x02
3. Program Register 0x0011 bit 0 = 1 to start the device
4. Enable PLL2 digital lock detect
   - 0xAD = 0x30
   - Delay 20 ms
   - 0xAD = 0x00

Also refer to *Power-Up Sequence*.

9.5.1.1 Readback

Readback of the complete register content is possible.

9.6 Register Maps

9.6.1 Register Map for Device Programming

Table 24 provides the register map for device programming. Any register can be read from the same data address it is written to.

Table 24. Register Map

ADDRESS	DATA							
[15:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	SWRST	LSB_FIRST	ADDR_ASCEND	SDO_ACTIVE	SDO_ACTIVE_CPY	ADDR_ASCEND_CPY	LSB_FIRST_CPY	SWRST_CPY
0x01	RSRVD							RSRVD1
0x02	RSRVD						RSRVD2[1:0]	
0x03	DEVID[1:0]		RSRVD		CHIPTYPE[3:0]			
0x04	CHIPID[15:8]							
0x05	CHIPID[7:0]							
0x06	CHIPVER[7:0]							
0x07	RSRVD							RSRVD3
0x08	RSRVD							RSRVD4
0x09	RSRVD							RSRVD5
0x0A	RSRVD							RSRVD6
0x0B	RSRVD							RSRVD7
0x0C	VENDORID[15:8]							
0x0D	VENDORID[7:0]							
0x0E	RSRVD							RSRVD8
0x0F	RSRVD							RSRVD9
0x10	RSRVD		OUTCH_MUTE	CLKINBLK_LOSLDO_EN	CH8TO15EN	CH0TO7EN	PLL2EN	PLL1EN
0x11	RSRVD							DEV_STARTUP
0x12	RSRVD					DIG_CLK_EN	PLL2_DIG_CLK_EN	PORCLKAFTERLOCK
0x13	RSRVD			PLL2_REF_DIGCLK_DIV[4:0]				
0x14	EN_SYNC_PIN_FUNC	RSRVD	GLOBAL_CONT_SYSREF	GLOBAL_SYSREF	INV_SYNC_INPUT_SYNC_CLK	SYNC_PIN_FUNC[1:0]		GLOBAL_SYNC
0x15	RSRVD				CLKIN_STAGGER_EN	CLKIN_SWRST	RSRVD	CLKINSEL1_INV
0x16	CLKINBLK_ALL_EN	CLKINSEL1_MODE[1:0]		CLKINBLK_EN_BUF_CLK_PLL	CLKINBLK_EN_BUF_BYP_PLL	RSRVD	RSRVD	RSRVD
0x17	RSRVD	CLKIN0_PLL1_INV	CLKIN0_LOS_FRQ_DBL_EN	CLKIN0_EN	CLKIN0_SE_MODE	CLKIN0_PRIO[2:0]		
0x18	RSRVD	CLKIN1_PLL1_INV	CLKIN1_LOS_FRQ_DBL_EN	CLKIN1_EN	CLKIN1_SE_MODE	CLKIN1_PRIO[2:0]		
0x19	RSRVD	CLKIN2_PLL1_INV	CLKIN2_LOS_FRQ_DBL_EN	CLKIN2_EN	CLKIN2_SE_MODE	CLKIN2_PRIO[2:0]		
0x1A	RSRVD	CLKIN3_PLL1_INV	CLKIN3_LOS_FRQ_DBL_EN	CLKIN3_EN	CLKIN3_SE_MODE	CLKIN3_PRIO[2:0]		
0x1B	CLKIN0_PLL1_RDIV[15:8]							
0x1C	CLKIN0_PLL1_RDIV[7:0]							
0x1D	CLKIN1_PLL1_RDIV[15:8]							
0x1E	CLKIN1_PLL1_RDIV[7:0]							
0x1F	CLKIN2_PLL1_RDIV[15:8]							
0x20	CLKIN2_PLL1_RDIV[7:0]							
0x21	CLKIN3_PLL1_RDIV[15:8]							
0x22	CLKIN3_PLL1_RDIV[7:0]							
0x23	CLKIN0_LOS_REC_CNT[7:0]							
0x24	CLKIN0_LOS_LAT_SEL[7:0]							

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA							
0x25	CLKIN1_LOS_REC_CNT[7:0]							
0x26	CLKIN1_LOS_LAT_SEL[7:0]							
0x27	CLKIN2_LOS_REC_CNT[7:0]							
0x28	CLKIN2_LOS_LAT_SEL[7:0]							
0x29	CLKIN3_LOS_REC_CNT[7:0]							
0x2A	CLKIN3_LOS_LAT_SEL[7:0]							
0x2B	RSRVD			SW_CLKLOS_TMR[4:0]				
0x2C	SW_REFINSEL[3:0]				SW_LOS_CH_SEL[3:0]			
0x2D	RSRVD			SW_ALLREFSON_TMR[4:0]				
0x2E	RSRVD		OSCIN_PD_LDO	OSCIN_SE_MODE	OSCIN_BUF_TO_OSCOUT_EN	OSCIN_OSCINSTAGE_EN	OSCIN_BUF_REF_EN	OSCIN_BUF_LOS_EN
0x2F	OSCOUT_LVCMOS_WEAK_DRIVE	OSCOUT_DIV_REGCONTROL	OSCOUT_PINSEL_DIV[1:0]		OSCOUT_SEL_VBG	OSCOUT_DIV_CLKEN	OSCOUT_SWRST	OSCOUT_SEL_SRC
0x30	OSCOUT_DIV[7:0]							
0x31	OSCOUT_DRV_MUTE[1:0]		OSCOUT_DRV_MODE[5:0]					
0x32	CH1415_SWRST	CH1213_SWRST	CH1011_SWRST	CH89_SWRST	CH67_SWRST	CH45_SWRST	CH23_SWRST	CH01_SWRST
0x33	OUTCH01_LDO_BYP_MODE	OUTCH01_LDO_MASK	OUTCH0_DRIV_MODE[5:0]					
0x34	OUTCH1_DRIV_MODE[5:0]						DIV_DCC_EN_CH0_1	OUTCH01_DIV_CLKEN
0x35	OUTCH23_LDO_BYP_MODE	OUTCH23_LDO_MASK	OUTCH2_DRIV_MODE[5:0]					
0x36	OUTCH3_DRIV_MODE[5:0]						DIV_DCC_EN_CH2_3	OUTCH23_DIV_CLKEN
0x37	OUTCH45_LDO_BYP_MODE	OUTCH45_LDO_MASK	OUTCH4_DRIV_MODE[5:0]					
0x38	OUTCH5_DRIV_MODE[5:0]						DIV_DCC_EN_CH4_5	OUTCH45_DIV_CLKEN
0x39	OUTCH67_LDO_BYP_MODE	OUTCH67_LDO_MASK	OUTCH6_DRIV_MODE[5:0]					
0x3A	OUTCH7_DRIV_MODE[5:0]						DIV_DCC_EN_CH6_7	OUTCH67_DIV_CLKEN
0x3B	OUTCH89_LDO_BYP_MODE	OUTCH89_LDO_MASK	OUTCH8_DRIV_MODE[5:0]					
0x3C	OUTCH9_DRIV_MODE[5:0]						DIV_DCC_EN_CH8_9	OUTCH89_DIV_CLKEN
0x3D	OUTCH1011_LDO_BYP_MODE	OUTCH1011_LDO_MASK	OUTCH10_DRIV_MODE[5:0]					
0x3E	OUTCH11_DRIV_MODE[5:0]						DIV_DCC_EN_CH10_11	OUTCH1011_DIV_CLKEN
0x3F	OUTCH1213_LDO_BYP_MODE	OUTCH1213_LDO_MASK	OUTCH12_DRIV_MODE[5:0]					
0x40	OUTCH13_DRIV_MODE[5:0]						DIV_DCC_EN_CH12_13	OUTCH1213_DIV_CLKEN
0x41	OUTCH1415_LDO_BYP_MODE	OUTCH1415_LDO_MASK	OUTCH14_DRIV_MODE[5:0]					
0x42	OUTCH15_DRIV_MODE[5:0]						DIV_DCC_EN_CH14_15	OUTCH1415_DIV_CLKEN
0x43	OUTCH01_DIV[15:8]							
0x44	OUTCH01_DIV[7:0]							
0x45	OUTCH23_DIV[15:8]							
0x46	OUTCH23_DIV[7:0]							
0x47	OUTCH45_DIV[15:8]							
0x48	OUTCH45_DIV[7:0]							
0x49	OUTCH67_DIV[15:8]							

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA							
0x4A	OUTCH67_DIV[7:0]							
0x4B	OUTCH89_DIV[15:8]							
0x4C	OUTCH89_DIV[7:0]							
0x4D	OUTCH1011_DIV[15:8]							
0x4E	OUTCH1011_DIV[7:0]							
0x4F	OUTCH1213_DIV[15:8]							
0x50	OUTCH1213_DIV[7:0]							
0x51	OUTCH1415_DIV[15:8]							
0x52	OUTCH1415_DIV[7:0]							
0x53	OUTCH1415_DIV_INV	OUTCH1213_DIV_INV	OUTCH1011_DIV_INV	OUTCH89_DIV_INV	OUTCH67_DIV_INV	OUTCH45_DIV_INV	OUTCH23_DIV_INV	OUTCH01_DIV_INV
0x54	PLL1_F_30	PLL1_EN_REGULATION	PLL1_PD_LD	PLL1_DIR_POS_GAIN	PLL1_LDO_WAIT_TMR[3:0]			
0x55	PLL1_LCKDET_BY_32	PLL1_FAST_LOCK	PLL1_LCKDET_LOS_MASK	PLL1_FBCLK_INV	RSRVD	PLL1_BYP_LOS	PLL1_PFD_UP_HOLDOVER	PLL1_PFD_DOWN_HOLDOVER
0x56	RSRVD			PLL1_LOL_NORESET	PLL1_RDIV_CLKEN	PLL1_RDIV_4CY	PLL1_NDIV_CLKEN	PLL1_NDIV_4CY
0x57	RSRVD		PLL1_HOLDOVER_DLD_SWRST	PLL1_RDIV_SWRST	PLL1_NDIV_SWRST	PLL1_HOLDOVERCNT_SWRST	PLL1_HOLDOVER_LOCKDET_SWRST	PLL1_SWRST
0x58	PLL1_LD_WNDW_SIZE[7:0]							
0x59	PLL1_INTG_FL [3:0]				PLL1_INTG [3:0]			
0x5A	RSRVD	PLL1_PROP[6:0]						
0x5B	RSRVD	PLL1_PROP_FL[6:0]						
0x5C	PLL1_HOLDOVER_EN	PLL1_STARTUP_HOLDOVER_EN	PLL1_HOLDOVER_FORCE	PLL1_HOLDOVER_RAIL_MODE	PLL1_HOLDOVER_MAX_CNT_EN	PLL1_HOLDOVER_LOS_MASK	PLL1_HOLDOVER_LCKDET_MASK	PLL1_HOLDOVER_RAILDET_EN
0x5D	PLL1_HOLDOVER_MAX_CNT[31:24]							
0x5E	PLL1_HOLDOVER_MAX_CNT[23:16]							
0x5F	PLL1_HOLDOVER_MAX_CNT[15:8]							
0x60	PLL1_HOLDOVER_MAX_CNT[7:0]							
0x61	PLL1_NDIV[15:8]							
0x62	PLL1_NDIV[7:0]							
0x63	PLL1_LOCKDET_CYC_CNT[23:16]							
0x64	PLL1_LOCKDET_CYC_CNT[15:8]							
0x65	PLL1_LOCKDET_CYC_CNT[7:0]							
0x66	RSRVD							
0x67	RSRVD							
0x68	RSRVD							
0x69	RSRVD							
0x6A	RSRVD		PLL1_STORAGE_CELL[5:0]					
0x6B	RSRVD			PLL1_RC_CLK_EN	RSRVD	PLL1_RC_CLK_DIV[2:0]		
0x6C	RSRVD			PLL2_VCO_PRESC_LOW_POWER	PLL2_BYP_OSC	PLL2_BYP_TOP	PLL2_BYP_BOT	PLL2_GLOBAL_BYP
0x6D	PLL2_EN_PULSE_GEN	PLL2_RDIV_BYP	PLL2_DBL_EN_INV	PLL2_PD_VARBIAS	PLL2_SMART_TRIM	PLL2_LCKDET_LOS_MASK	PLL2_RDIV_DBL_EN	PLL2_PD_LD
0x6E	PLL2_BYP_SYNC_TOP	PLL2_BYP_SYNC_BOTTOM	PLL2_EN_BYP_BUF	PLL2_EN_BUF_SYNC_TOP	PLL2_EN_BUF_SYNC_BOTTOM	PLL2_EN_BUF_OSCOUT	PLL2_EN_BUF_CLK_TOP	PLL2_EN_BUF_CLK_BOTTOM
0x6F	RSRVD					PLL2_RDIV_SWRST	PLL2_NDIV_SWRST	PLL2_SWRST
0x70	PLL2_C4_LF_SEL[3:0]				PLL2_R4_LF_SEL[3:0]			

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA						
0x71	PLL2_C3_LF_SEL[3:0]				PLL2_R3_LF_SEL[3:0]		
0x72	RSRVD	PLL2_PROP[5:0]					
0x73	PLL2_NDIV[15:8]						
0x74	PLL2_NDIV[7:0]						
0x75	PLL2_RDIV[15:8]						
0x76	PLL2_RDIV[7:0]						
0x77	PLL2_STRG_INITVAL[15:8]						
0x78	PLL2_STRG_INITVAL[7:0]						
0x7D	RSRVD	RAILDET_UPP[5:0]					
0x7E	RSRVD	RAILDET_LOW[5:0]					
0x7F	RSRVD	PLL2_AC_CAL_EN	PLL2_PD_AC	PLL2_IDACSET_RECAL[1:0]		PLL2_AC_REQ	PLL2_FAST_ACAL
0x80	RSRVD		PLL2_INTG[4:0]				
0x81	RSRVD		PLL2_AC_THRESHOLD[4:0]				
0x82	RSRVD		PLL2_AC_STRT_THRESHOLD[4:0]				
0x83	PLL2_AC_CMP_WAIT[3:0]			PLL2_AC_INIT_WAIT[3:0]			
0x84	RSRVD			PLL2_AC_JUMP_STEP[3:0]			
0x85	PLL2_LD_WNDW_SIZE[7:0]						
0x86	PLL2_LD_WNDW_SIZE_INITIAL[7:0]						
0x87	PLL2_LOCKDET_CYC_CNT[23:16]						
0x88	PLL2_LOCKDET_CYC_CNT[15:8]						
0x89	PLL2_LOCKDET_CYC_CNT[7:0]						
0x8A	PLL2_LOCKDET_CYC_CNT_INITIAL[23:16]						
0x8B	PLL2_LOCKDET_CYC_CNT_INITIAL[15:8]						
0x8C	PLL2_LOCKDET_CYC_CNT_INITIAL[7:0]						
0x8D	SPI_EN_THREE_WIRE_IF	RSRVD	SPI_SDIO_OUTPUT_MUTE	SPI_SDIO_OUTPUT_INV	SPI_SDIO_OUTPUT_WEAK_DRIVE	SPI_SDIO_EN_PULLUP	SPI_SDIO_EN_PULLDOWN
0x8E	RSRVD			SPI_SCL_EN_PULLUP	SPI_SCL_EN_PULLDOWN	SPI_SCS_EN_PULLUP	SPI_SCS_EN_PULLDOWN
0x8F	RSRVD	SPI_SDIO_OUTPUT_HIZ	SPI_SDIO_EN_INSTAGE	SPI_SDIO_EN_ML_INSTAGE	RSRVD	SPI_SDIO_OUTPUT_DATA	SPI_SDIO_INPUT_Y12	SPI_SDIO_INPUT_M12
0x90	RSRVD		SPI_SCL_ENB_INSTAGE	SPI_SCL_EN_ML_INSTAGE	RSRVD		SPI_SCL_INPUT_Y12	SPI_SCL_INPUT_M12
0x91	RSRVD		SPI_SCS_ENB_INSTAGE	SPI_SCS_EN_ML_INSTAGE	RSRVD		SPI_SCS_INPUT_Y12	SPI_SCS_INPUT_M12
0x92	STATUS0_MUX_SEL[2:0]			STATUS0_OUTPUT_MUTE	STATUS0_OUTPUT_INV	STATUS0_OUTPUT_WEAK_DRIVE	STATUS0_EN_PULLUP	STATUS0_EN_PULLDOWN
0x93	STATUS1_MUX_SEL[2:0]			STATUS1_OUTPUT_MUTE	STATUS1_OUTPUT_INV	STATUS1_OUTPUT_WEAK_DRIVE	STATUS1_EN_PULLUP	STATUS1_EN_PULLDOWN
0x94	STATUS1_INT_MUX[7:0]							
0x95	STATUS0_INT_MUX[7:0]							
0x96	RSRVD			PLL2_REF_CLK_EN	RSRVD	PLL2_REF_STATCLK_DIV[2:0]		
0x97	RSRVD	STATUS0_OUTPUT_HIZ	STATUS0_EN_INSTAGE	STATUS0_EN_ML_INSTAGE	RSRVD	STATUS0_OUTPUT_DATA	STATUS0_INPUT_Y12	STATUS0_INPUT_M12
0x98	RSRVD	STATUS1_OUTPUT_HIZ	STATUS1_EN_INSTAGE	STATUS1_EN_ML_INSTAGE	RSRVD	STATUS1_OUTPUT_DATA	STATUS1_INPUT_Y12	STATUS1_INPUT_M12
0x99	SYNC_MUX_SEL[2:0]			SYNC_OUTPUT_MUTE	SYNC_OUTPUT_INV	SYNC_OUTPUT_WEAK_DRIVE	SYNC_EN_PULLUP	SYNC_EN_PULLDOWN
0x9A	RSRVD							RSRVD
0x9B	RSRVD						CLKINSEL1_EN_PULLUP	CLKINSEL1_EN_PULLDOWN

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA							
0x9C	RSRVD		CLKINSEL1_ENB_INSTAGE	CLKINSEL1_EN_ML_INSTAGE	RSRVD		CLKINSEL1_INPUT_Y12	CLKINSEL1_INPUT_M12
0xAC	PLL1_TSTMODE_REF_FB_EN	RSRVD						
0xAD	RSRVD		RESET_PLL2_DLD[1:0]		RSRVD	PLL2_TSTMODE_REF_FB_EN	PD_VCO_LDO[1:0]	
0xAF	RSRVD			RSRVD			RSRVD	PLL2_RDIV_CLKEN
0xB0	RSRVD			RSRVD			RSRVD	PLL2_NDIV_CLKEN
0xBE	RSRVD		LOS	HOLDOVER_DLD	HOLDOVER_LOL	HOLDOVER_LOS	PLL2_LCK_DET	PLL1_LCK_DET
0xF6	RSRVD						PLL2_DLD_EN	RSRVD
0xFD	OUTCH01_DDLY[7:0]							
0xFF	OUTCH23_DDLY[7:0]							
0x101	OUTCH45_DDLY[7:0]							
0x103	OUTCH67_DDLY[7:0]							
0x105	OUTCH89_DDLY[7:0]							
0x107	OUTCH1011_DDLY[7:0]							
0x109	OUTCH1213_DDLY[7:0]							
0x10B	OUTCH1415_DDLY[7:0]							
0x10C	RSRVD	CH0_ADLY[4:0]					CH0_ADLY_EN	RSRVD
0x10D	RSRVD	CH1_ADLY[4:0]					CH1_ADLY_EN	RSRVD
0x10E	RSRVD	CH2_ADLY[4:0]					CH2_ADLY_EN	RSRVD
0x10F	RSRVD	CH3_ADLY[4:0]					CH3_ADLY_EN	RSRVD
0x110	RSRVD	CH4_ADLY[4:0]					CH4_ADLY_EN	RSRVD
0x111	RSRVD	CH5_ADLY[4:0]					CH5_ADLY_EN	RSRVD
0x112	RSRVD	CH6_ADLY[4:0]					CH6_ADLY_EN	RSRVD
0x113	RSRVD	CH7_ADLY[4:0]					CH7_ADLY_EN	RSRVD
0x114	RSRVD	CH8_ADLY[4:0]					CH8_ADLY_EN	RSRVD
0x115	RSRVD	CH9_ADLY[4:0]					CH9_ADLY_EN	RSRVD
0x116	RSRVD	CH10_ADLY[4:0]					CH10_ADLY_EN	RSRVD
0x117	RSRVD	CH11_ADLY[4:0]					CH11_ADLY_EN	RSRVD
0x118	RSRVD	CH12_ADLY[4:0]					CH12_ADLY_EN	RSRVD
0x119	RSRVD	CH13_ADLY[4:0]					CH13_ADLY_EN	RSRVD
0x11A	RSRVD	CH14_ADLY[4:0]					CH14_ADLY_EN	RSRVD
0x11B	RSRVD	CH15_ADLY[4:0]					CH15_ADLY_EN	RSRVD
0x124	RSRVD				CLKMUX[3:0]			
0x127	SYSREF_BYP_DYNDIGDLY_GATING_CH0_1	SYSREF_BYP_ANALOGDLY_GATING_CH0_1	SYNC_EN_CH0_1	HS_EN_CH0_1	DRIV_1_SLEW[1:0]		DRIV_0_SLEW[1:0]	

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA							
0x128	SYSREF_BYP_DYNDIGDLY_GATING_CH2_3	SYSREF_BYP_ANALOGDLY_GATING_CH2_3	SYNC_EN_CH2_3	HS_EN_CH2_3	DRIV_3_SLEW[1:0]		DRIV_2_SLEW[1:0]	
0x129	SYSREF_BYP_DYNDIGDLY_GATING_CH4_5	SYSREF_BYP_ANALOGDLY_GATING_CH4_5	SYNC_EN_CH4_5	HS_EN_CH4_5	DRIV_5_SLEW[1:0]		DRIV_4_SLEW[1:0]	
0x12A	SYSREF_BYP_DYNDIGDLY_GATING_CH6_7	SYSREF_BYP_ANALOGDLY_GATING_CH6_7	SYNC_EN_CH6_7	HS_EN_CH6_7	DRIV_7_SLEW[1:0]		DRIV_6_SLEW[1:0]	
0x12B	SYSREF_BYP_DYNDIGDLY_GATING_CH8_9	SYSREF_BYP_ANALOGDLY_GATING_CH8_9	SYNC_EN_CH8_9	HS_EN_CH8_9	DRIV_9_SLEW[1:0]		DRIV_8_SLEW[1:0]	
0x12C	SYSREF_BYP_DYNDIGDLY_GATING_CH10_11	SYSREF_BYP_ANALOGDLY_GATING_CH10_11	SYNC_EN_CH10_11	HS_EN_CH10_11	DRIV_11_SLEW[1:0]		DRIV_10_SLEW[1:0]	
0x12D	SYSREF_BYP_DYNDIGDLY_GATING_CH12_13	SYSREF_BYP_ANALOGDLY_GATING_CH12_13	SYNC_EN_CH12_13	HS_EN_CH12_13	DRIV_13_SLEW[1:0]		DRIV_12_SLEW[1:0]	
0x12E	SYSREF_BYP_DYNDIGDLY_GATING_CH14_15	SYSREF_BYP_ANALOGDLY_GATING_CH14_15	SYNC_EN_CH14_15	HS_EN_CH14_15	DRIV_15_SLEW[1:0]		DRIV_14_SLEW[1:0]	
0x12F	RSRVD						DYN_DDLY_CH0[2:0]	
0x130	RSRVD						DYN_DDLY_CH1[2:0]	
0x131	RSRVD						DYN_DDLY_CH2[2:0]	
0x132	RSRVD						DYN_DDLY_CH3[2:0]	
0x133	RSRVD						DYN_DDLY_CH4[2:0]	
0x134	RSRVD						DYN_DDLY_CH5[2:0]	
0x135	RSRVD						DYN_DDLY_CH6[2:0]	
0x136	RSRVD						DYN_DDLY_CH7[2:0]	
0x137	RSRVD						DYN_DDLY_CH8[2:0]	
0x138	RSRVD						DYN_DDLY_CH9[2:0]	
0x139	RSRVD						DYN_DDLY_CH10[2:0]	
0x13A	RSRVD						DYN_DDLY_CH11[2:0]	
0x13B	RSRVD						DYN_DDLY_CH12[2:0]	
0x13C	RSRVD						DYN_DDLY_CH13[2:0]	
0x13D	RSRVD						DYN_DDLY_CH14[2:0]	
0x13E	RSRVD						DYN_DDLY_CH15[2:0]	
0x140	RSRVD		OUTCH_SYSREF_PLSCNT[5:0]					
0x141	SYNC_INT_MUX[7:0]							
0x142	RSRVD	SYNC_OUTPUT_HIZ	SYNC_ENB_INSTAGE	SYNC_EN_ML_INSTAGE	RSRVD	SYNC_OUTPUT_DATA	SYNC_INPUT_Y12	SYNC_INPUT_M12
0x143	RSRVD			FBBUF_CH6_EN	RSRVD			FBBUF_CH9_EN
0x146	RSRVD	PLL2_NBYPASS_DIV2_FB	PLL2_PRESCALER[3:0]				PLL2_FBDIV_MUXSEL[1:0]	
0x149	RSRVD				PLL1_CLKINSEL1_ML_HOLDOVER	PLL1_SYNC_HOLDOVER	PLL1_STATUS1_HOLDOVER	PLL1_STATUS0_HOLDOVER
0x14A	RSRVD	SYNC_ANALOGDLY[4:0]					SYNC_ANALOGDLY_EN	SYNC_INV
0x14B	DYN_DDLY_CH15_EN	DYN_DDLY_CH14_EN	DYN_DDLY_CH13_EN	DYN_DDLY_CH12_EN	DYN_DDLY_CH11_EN	DYN_DDLY_CH10_EN	DYN_DDLY_CH9_EN	DYN_DDLY_CH8_EN

Register Maps (continued)

Table 24. Register Map (continued)

ADDRESS	DATA							
0x14C	DYN_DDLY_CH7_EN	DYN_DDLY_CH6_EN	DYN_DDLY_CH5_EN	DYN_DDLY_CH4_EN	DYN_DDLY_CH3_EN	DYN_DDLY_CH2_EN	DYN_DDLY_CH1_EN	DYN_DDLY_CH0_EN
0x14E	SYSREF_EN_CH14_15	SYSREF_EN_CH12_13	SYSREF_EN_CH10_11	SYSREF_EN_CH8_9	SYSREF_EN_CH6_7	SYSREF_EN_CH4_5	SYSREF_EN_CH2_3	SYSREF_EN_CH0_1
0x150	RSRVD				PLL2_PFD_DIS_SAMPLE	PLL2_PROG_PFD_RESET[2:0]		
0x151	RSRVD			PLL2_RFILT	RSRVD	PLL2_CP_EN_SAMPLE_BYP	PLL2_CPROP[1:0]	
0x152	RSRVD				PLL2_EN_FILTER	PLL2_CSAMPLE[2:0]		
0x153	RSRVD			PLL2_CFILT				

9.6.2 Device Register Descriptions

The following section details the fields of each register, the Power On Reset Defaults, and specific descriptions of each bit.

In some cases similar fields are located in multiple registers. In this case specific outputs may be designated as X or Y. In these cases the X will represent even numbers from 0 to 12 and the Y will represent odd numbers from 1 to 13. In the case where X and Y are both used in a bit name, then Y = X + 1.

9.6.2.1 CONFIGA

The CONFIGA Register provides control of the SPI operation. The data written to this register must always be symmetrical otherwise the write will not take place, that is, Bit0=Bit7, Bit1=Bit6, Bit2=Bit5, Bit3=Bit4. Back to Register Map.

Table 25. Register - 0x00

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SWRST	RWSC	0	Software Reset. Writing a 1 to SWRST will reset the device apart from the SPI programmable registers. SWRST is automatically cleared to 0.
[6]	LSB_FIRST	RW	0	Least Significant Bit First. This feature is not support, register data is always transmitted MSB first.
[5]	ADDR_ASCEND	RW	0	Address Increment Ascending. When set to 1 the address in streaming transactions is incremented by 1 after each data byte. When set to 0 the address is decremented by 1 in streaming transactions.
[4]	SDO_ACTIVE	RW	0	SDO Active. SDO is always active. This bit always reads 1.
[3]	SDO_ACTIVE_CPY	RW	0	SDO Active. Must be programmed equal to bit 4.
[2]	ADDR_ASCEND_CPY	RW	0	Address Increment Ascending. Must be programmed equal to bit 5.
[1]	LSB_FIRST_CPY	RW	0	Least Significant Bit First. Must be programmed equal to bit 6.
[0]	SWRST_CPY	RWSC	0	Software Reset. Must be programmed equal to bit 7.

9.6.2.2 RESERVED1

Reserved Register space. Back to Register Map.

Table 26. Register - 0x01

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD1	R	0	Reserved for compatibility.

9.6.2.3 RESERVED2

Reserved Register space. Back to Register Map.

Table 27. Register - 0x02

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	RSRVD	-	-	Reserved.
[1:0]	RSRVD2[1:0]	R	0x0	Reserved for compatibility.

9.6.2.4 CHIP_TYPE

The CHIP_TYPE Register defines the nature of this device. Back to Register Map.

Table 28. Register - 0x03

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	DEVID[1:0]	R	0x0	Device Identification. Indicates the device partname DEVID - Device 0 - LMK04616 1 - LMK04610
[5:4]	RSRVD	-	-	Reserved.
[3:0]	CHIPTYPE[3:0]	R	0x6	Chip Type. Indicates that this is a PLL Device.

9.6.2.5 CHIP_ID_BY1

The CHIP_ID is a vendor specific field recorded in registers CHIP_ID_BY1 and CHIP_ID_BY0. Back to Register Map.

Table 29. Register - 0x04

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CHIPID[15:8]	R	0x38	CHIP Identification.

9.6.2.6 CHIP_ID_BY0

The CHIP_ID lower byte is recorded in CHIP_ID_BY1 Back to Register Map.

Table 30. Register - 0x05

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CHIPID[7:0]	R	0x3	CHIP Identification.

9.6.2.7 CHIP_VER

The CHIP_VER Register records the mask set revision. Back to Register Map.

Table 31. Register - 0x06

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CHIPVER[7:0]	R	0x15	CHIP Version.

9.6.2.8 RESERVED3

Reserved Register space. Back to Register Map.

Table 32. Register - 0x07

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD3	R	0	Reserved for compatibility.

9.6.2.9 RESERVED4

Reserved Register space. Back to Register Map.

Table 33. Register - 0x08

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD4	R	0	Reserved for compatibility.

9.6.2.10 RESERVED5

Reserved Register space. Back to Register Map.

Table 34. Register - 0x09

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD5	R	0	Reserved for compatibility.

9.6.2.11 RESERVED6

Reserved Register space. Back to Register Map.

Table 35. Register - 0x0A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD6	R	0	Reserved for compatibility.

9.6.2.12 RESERVED7

Reserved Register space. Back to Register Map.

Table 36. Register - 0x0B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD7	R	0	Reserved for compatibility.

9.6.2.13 VENDOR_ID_BY1

The VENDOR_ID field is recorded in registers VENDOR_ID_BY1 and VENDOR_ID_BY0. Back to Register Map.

Table 37. Register - 0x0C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	VENDORID[15:8]	R	0x51	Vendor Identification.

9.6.2.14 VENDOR_ID_BY0

VENDOR_ID Lower Byte. Back to Register Map.

Table 38. Register - 0x0D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	VENDORID[7:0]	R	0x8	Vendor Identification.

9.6.2.15 RESERVED8

Reserved Register space. Back to Register Map.

Table 39. Register - 0x0E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD8	R	0	Reserved for compatibility.

9.6.2.16 RESERVED9

Reserved Register space. Back to Register Map.

Table 40. Register - 0x0F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD9	R	0	Reserved for compatibility.

9.6.2.17 STARTUP_CFG

The STARTUP_CFG Register provides control of the device operation at startup. Back to Register Map.

Table 41. Register - 0x10

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	OUTCH_MUTE	RW	0	Output Channel Mute. When OUTCH_MUTE is 1 the output drivers are disabled until the PLL's have locked.
[4]	CLKINBLK_LOSLDO_EN	RW	1	Enable LOS LDO during the startup sequence.
[3]	CH8TO15EN	RW	1	Enable Channels 8 to 15 during the startup sequence.
[2]	CH0TO7EN	RW	1	Enable Channels 0 to 7 during the startup sequence.
[1]	PLL2EN	RW	1	Activate PLL2 during the startup sequence.
[0]	PLL1EN	RW	1	Activate PLL1 during the startup sequence.

9.6.2.18 STARTUP

The STARTUP Register allows device activation to be triggered. Back to Register Map.

Table 42. Register - 0x11

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	DEV_STARTUP	RW	0	Device Startup. When DEV_STARTUP is 1 the device activation sequence is triggered. The device modules that are automatically enabled during the sequence is determined by the STARTUP_CFG register. If DEV_STARTUP is 1 on exit from software reset then the startup sequence will also be triggered.

9.6.2.19 DIGCLKCTRL

The DIGCLKCTRL Register allows control of the digital system clock. Back to Register Map.

Table 43. Register - 0x12

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2]	DIG_CLK_EN	RW	1	Digital Clock Enable. When DIG_CLK_EN is 1 the digital system clock is active. When DIG_CLK_EN is 0 the digital system clock is disabled.

Table 43. Register - 0x12 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[1]	PLL2_DIG_CLK_EN	RW	1	Enable PLL2 Digital Clock Buffer.
[0]	PORCLKAFTERLOCK	RW	0	POR Clock behaviour after Lock. If PORCLKAFTERLOCK is 0 then the system clock is switched from the POR Clock to the PLL2 Digital Clock after lock and the POR Clock oscillator is disabled. If PORCLKAFTERLOCK is 1 then the POR Clock will remain as the digital system clock regardless of the PLL Lock state.

9.6.2.20 PLL2REFCLKDIV

The PLL2REFCLKDIV Register controls the PLL2 Reference Clock Divider value. Back to Register Map.

Table 44. Register - 0x13

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4:0]	PLL2_REF_DIGCLK_DIV[4:0]	RW	0x0	PLL2 Ref Clock Divider for Digital Clock. Defines the divider ratio for the PLL2 Reference Clock that can be used as the digital system clock. PLL2_REF_DIGCLK_DIV - Divider Value b00000 - 32 b00001 - 16 b00010 - 8 b00100 - 4 b01000 - 2 b10000 - 1

9.6.2.21 GLBL_SYNC_SYSREF

The GLBL_SYNC_SYSREF Register provides software control of the SYSREF and SYNC features. Back to Register Map.

Table 45. Register - 0x14

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	EN_SYNC_PIN_FUNC	RW	0	Enable SYNC_SYSREF features at SYNC pin.
[6]	RSRVD	-	-	Reserved.
[5]	GLOBAL_CONT_SYSREF	RW	0	Enable continuous sysref.
[4]	GLOBAL_SYSREF	RWSC	0	Trigger sysref. Self-clearing.
[3]	INV_SYNC_INPUT_SYNC_CLK	RW	0	Invert the internal syncronization clock for SYNC input sync (For PLL1 N- and R-Divider Reset)
[2:1]	SYNC_PIN_FUNC[1:0]	RW	0x0	SYNC input pin function. SYNC_PIN_FUNC - Function 00 - SYNC output channels 01 - Sysref Request 10 - Reset PLL1 N- and R-Divider 11 - Reserved
[0]	GLOBAL_SYNC	RW	0	Global SW SYNC. Writing '1' puts the Device into SYNC mode. Writing '0' exits SYNC mode.

9.6.2.22 CLKIN_CTRL0

The CLKIN_CTRL0 Register provides control of CLK Input features. Back to Register Map.

Table 46. Register - 0x15

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.

Table 46. Register - 0x15 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[3]	CLKIN_STAGGER_EN	RW	1	CLKINBLK Staggered Activation/De-Activation. When CLKIN_STAGGER_EN is 1 the input clock stages are activated and de-activated one at a time.
[2]	CLKIN_SWRST	RWSC	0	CLKINBLK Software Reset. Writing a 1 to CLKIN_SWRST will reset reset the CLKIN Block. The CLKIN_SWRST is cleared automatically to 0.
[1]	RSRVD	-	-	Reserved.
[0]	CLKINSEL1_INV	RW	0	CLKIN_SEL Invert. CLKINSEL1_INV - Polarity 0 - Non-Inverted 1 - Inverted

9.6.2.23 CLKIN_CTRL1

The CLKIN_CTRL1 Register provides control of CLK Input features. Back to Register Map.

Table 47. Register - 0x16

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	CLKINBLK_ALL_EN	RW	0	CLK Inputs All Enabled after Clock Switch. If CLKINBLK_ALL_EN is 1 then all clock input paths remain enabled after a valid clock has been selected. If CLKINBLK_ALL_EN is 0 then the clock paths are disabled apart from the selected clock.
[6:5]	CLKINSEL1_MODE[1:0]	RW	0x0	CLK Input Select Mode. CLKINSEL1_MODE - CLOCK Selection Mode 0 - Auto 1 - Pin 2 - Register
[4]	CLKINBLK_EN_BUF_CLK_PLL	RW	0	Clock Buffer for PLL1 Enable.
[3]	CLKINBLK_EN_BUF_BYP_PLL	RW	0	Clock Buffer for PLL2 Enable (PLL1 By-Passed).
[2]	RSRVD	RW	0	Reserved.
[1]	RSRVD	RW	0	Reserved.
[0]	RSRVD	RW	0	Reserved.

9.6.2.24 CLKIN0CTRL

The CLKIN0CTRL Register provides control of the CLK0 input path. Back to Register Map.

Table 48. Register - 0x17

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	CLKIN0_PLL1_INV	RW	1	Inverts CLKIN0_PLL1_RDIV. 0=Non-Inverted 1=Inverted
[5]	CLKIN0_LOS_FRQ_DBL_EN	RW	0	CLKIN0 Loss of Source Frequency Doubler Enable.
[4]	CLKIN0_EN	RW	0	CLKIN0 Input Stage Enable (not clk buffer).
[3]	CLKIN0_SE_MODE	RW	1	CLKIN0 Signal Mode. CLKIN0_SE_MODE - Signal Mode Selection 0 - Differential 1 - Single-ended

Table 48. Register - 0x17 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[2:0]	CLKIN0_PRIO[2:0]	RW	0x1	CLKIN0 Priority. CLKIN0_PRIO - Clock Priority 0 - Clock Disabled 1 - Priority 1 - Highest 2 - Priority 2 3 - Priority 3 4 - Priority 4 - Lowest

9.6.2.25 CLKIN1CTRL

The CLKIN1CTRL Register provides control of the CLK1 input path. Back to Register Map.

Table 49. Register - 0x18

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	CLKIN1_PLL1_INV	RW	1	Inverts CLKIN1_PLL1_RDIV. 0=Non-Inverted 1=Inverted
[5]	CLKIN1_LOS_FRQ_DBL_EN	RW	0	CLKIN1 Loss of Source Frequency Doubler Enable.
[4]	CLKIN1_EN	RW	0	CLKIN1 Input Stage Enable. (not clk buffer).
[3]	CLKIN1_SE_MODE	RW	1	CLKIN1 Signal Mode. CLKIN1_SE_MODE - Signal Mode Selection 0 - Differential 1 - Single-ended
[2:0]	CLKIN1_PRIO[2:0]	RW	0x2	CLKIN1 Priority. CLKIN1_PRIO - Clock Priority 0 - Clock Disabled 1 - Priority 1 - Highest 2 - Priority 2 3 - Priority 3 4 - Priority 4 - Lowest

9.6.2.26 CLKIN2CTRL

The CLKIN2CTRL Register provides control of the CLK2 input path. Back to Register Map.

Table 50. Register - 0x19

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	CLKIN2_PLL1_INV	RW	0	Inverts CLKIN2_PLL1_RDIV. 0=Non-Inverted 1=Inverted
[5]	CLKIN2_LOS_FRQ_DBL_EN	RW	0	CLKIN2 Loss of Source Frequency Doubler Enable.
[4]	CLKIN2_EN	RW	0	CLKIN2 Input Stage Enable. (not clk buffer).
[3]	CLKIN2_SE_MODE	RW	1	CLKIN2 Signal Mode. CLKIN2_SE_MODE - Signal Mode Selection 0 - Differential 1 - Single-ended
[2:0]	CLKIN2_PRIO[2:0]	RW	0x3	CLKIN2 Priority. CLKIN2_PRIO - Clock Priority 0 - Clock Disabled 1 - Priority 1 - Highest 2 - Priority 2 3 - Priority 3 4 - Priority 4 - Lowest

9.6.2.27 CLKIN3CTRL

The CLKIN3CTRL Register provides control of the CLK3 input path. Back to Register Map.

Table 51. Register - 0x1A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	CLKIN3_PLL1_INV	RW	0	Inverts CLKIN3_PLL1_RDIV. 0=Non-Inverted 1=Inverted
[5]	CLKIN3_LOS_FRQ_DBL_EN	RW	0	CLKIN3 Loss of Source Frequency Doubler Enable.
[4]	CLKIN3_EN	RW	0	CLKIN3 Input Stage Enable. (not clk buffer).
[3]	CLKIN3_SE_MODE	RW	1	CLKIN3 Signal Mode. CLKIN3_SE_MODE - Signal Mode Selection 0 - Differential 1 - Single-ended
[2:0]	CLKIN3_PRIO[2:0]	RW	0x4	CLKIN3 Priority. CLKIN3_PRIO - Clock Priority 0 - Clock Disabled 1 - Priority 1 - Highest 2 - Priority 2 3 - Priority 3 4 - Priority 4 - Lowest

9.6.2.28 CLKIN0RDIV_BY1

The CLKIN0 RDIV Values is determined by CLKIN0RDIV_BY1 and CLKIN0RDIV_BY0. Back to Register Map.

Table 52. Register - 0x1B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN0_PLL1_RDIV[15:8]	RW	0x0	CLKIN0 PLL1 Reference Divider Value. CLKIN0_PLL1_RDIV - Reference Divider 0 - Reserved 1 - 1 .. - .. 65535 - 65535

9.6.2.29 CLKIN0RDIV_BY0

The CLKIN0RDIV_BY0 Register controls the lower 8-bits of the CLKIN0 Reference Divider. Back to Register Map.

Table 53. Register - 0x1C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN0_PLL1_RDIV[7:0]	RW	0x78	CLKIN0 PLL1 Reference Divider Value.

9.6.2.30 CLKIN1RDIV_BY1

The CLKIN1 RDIV Values is determined by CLKIN1RDIV_BY1 and CLKIN1RDIV_BY0. Back to Register Map.

Table 54. Register - 0x1D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN1_PLL1_RDIV[15:8]	RW	0x0	CLKIN1 PLL1 Reference Divider Value. CLKIN1_PLL1_RDIV - Reference Divider 0 - Reserved 1 - 1 .. - .. 65535 - 65535

9.6.2.31 CLKIN1RDIV_BY0

The CLKIN1RDIV_BY0 Register controls the lower 8-bits of the CLKIN1 Reference Divider. Back to Register Map.

Table 55. Register - 0x1E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN1_PLL1_RDIV[7:0]	RW	0x78	CLKIN1 PLL1 Reference Divider Value.

9.6.2.32 CLKIN2RDIV_BY1

The CLKIN2 RDIV Values is determined by CLKIN2RDIV_BY1 and CLKIN2RDIV_BY0. Back to Register Map.

Table 56. Register - 0x1F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN2_PLL1_RDIV[15:8]	RW	0x0	CLKIN2 PLL1 Reference Divider Value. CLKIN2_PLL1_RDIV - Reference Divider 0 - Reserved 1 - 1 .. - .. 65535 - 65535

9.6.2.33 CLKIN2RDIV_BY0

The CLKIN2RDIV_BY0 Register controls the lower 8-bits of the CLKIN2 Reference Divider. Back to Register Map.

Table 57. Register - 0x20

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN2_PLL1_RDIV[7:0]	RW	0x78	CLKIN2 PLL1 Reference Divider Value.

9.6.2.34 CLKIN3RDIV_BY1

The CLKIN3 RDIV Values is determined by CLKIN3RDIV_BY1 and CLKIN3RDIV_BY0. Back to Register Map.

Table 58. Register - 0x21

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN3_PLL1_RDIV[15:8]	RW	0x0	CLKIN3 PLL1 Reference Divider Value. CLKIN3_PLL1_RDIV - Reference Divider 0 - Reserved 1 - 1 .. - .. 65535 - 65535

9.6.2.35 CLKIN3RDIV_BY0

The CLKIN3RDIV_BY0 Register controls the lower 8-bits of the CLKIN3 Reference Divider. Back to Register Map.

Table 59. Register - 0x22

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN3_PLL1_RDIV[7:0]	RW	0x78	CLKIN3 PLL1 Reference Divider Value.

9.6.2.36 CLKIN0LOS_REC_CNT

The CLKIN0LOSCTRL Register sets the CLKIN0 Loss of Source recovery counter value. Back to Register Map.

Table 60. Register - 0x23

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN0_LOS_REC_CNT[7:0]	RW	0x14	CLKIN0 LOS Recovery Counter Value. CLKIN0_LOS_REC_CNT - Counter Value 0 - 15+0*16 1 - 15+1*16 2 - 15+2*16 3 - 15+3*16 .. - .. 255 - 15+255*16

9.6.2.37 CLKIN0LOS_LAT_SEL

The CLKIN0LOS_LAT_SEL Register sets the CLKIN0 Loss of Source latency. Back to Register Map.

Table 61. Register - 0x24

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN0_LOS_LAT_SEL[7:0]	RW	0x80	CLKIN0 LOS Max Latency for LOS Detection.

9.6.2.38 CLKIN1LOS_REC_CNT

The CLKIN1LOS_REC_CNT Register sets the CLKIN1 Loss of Source recovery counter value. Back to Register Map.

Table 62. Register - 0x25

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN1_LOS_REC_CNT[7:0]	RW	0x14	CLKIN1 LOS Recovery Counter Value. CLKIN1_LOS_REC_CNT - Counter Value 0 - 15+0*16 1 - 15+1*16 2 - 15+2*16 3 - 15+3*16 .. - .. 255 - 15+255*16

9.6.2.39 CLKIN1LOS_LAT_SEL

The CLKIN1LOS_LAT_SEL Register sets the CLKIN1 Loss of Source latency. Back to Register Map.

Table 63. Register - 0x26

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN1_LOS_LAT_SEL[7:0]	RW	0x80	CLKIN1 LOS Max Latency for LOS Detection.

9.6.2.40 CLKIN2LOS_REC_CNT

The CLKIN2LOS_REC_CNT Register sets the CLKIN2 Loss of Source recovery counter value. Back to Register Map.

Table 64. Register - 0x27

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN2_LOS_REC_CNT[7:0]	RW	0x14	CLKIN2 LOS Recovery Counter Value. CLKIN2_LOS_REC_CNT - Counter Value 0 - 15+0*16 1 - 15+1*16 2 - 15+2*16 3 - 15+3*16 .. - .. 255 - 15+255*16

9.6.2.41 CLKIN2LOS_LAT_SEL

The CLKIN2LOS_LAT_SEL Register sets the CLKIN2 Loss of Source latency. Back to Register Map.

Table 65. Register - 0x28

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN2_LOS_LAT_SEL[7:0]	RW	0x80	CLKIN2 LOS Max Latency for LOS Detection.

9.6.2.42 CLKIN3LOS_REC_CNT

The CLKIN3LOS_REC_CNT Register sets the CLKIN3 Loss of Source recovery counter value. Back to Register Map.

Table 66. Register - 0x29

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN3_LOS_REC_CNT[7:0]	RW	0x14	CLKIN3 LOS Recovery Counter Value. CLKIN3_LOS_REC_CNT - Counter Value 0 - 15+0*16 1 - 15+1*16 2 - 15+2*16 3 - 15+3*16 .. - .. 255 - 15+255*16

9.6.2.43 CLKIN3LOS_LAT_SEL

The CLKIN3LOS_LAT_SEL Register sets the CLKIN3 Loss of Source latency. Back to Register Map.

Table 67. Register - 0x2A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CLKIN3_LOS_LAT_SEL[7:0]	RW	0x80	CLKIN3 LOS Max Latency for LOS Detection.

9.6.2.44 CLKIN_SWCTRL0

The CLKIN_SWCTRL0 Register provides control of the input settling time after switching to another Ref channel for Loss Of Signal Inspection. Back to Register Map.

Table 68. Register - 0x2B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4:0]	SW_CLKLOS_TMR[4:0]	RW	0x0	Wait Time for a Valid LOS Detection. Used during Priority Switching in Auto CLKin selection mode.

9.6.2.45 CLKIN_SWCTRL1

The CLKIN_SWCTRL1 Register provides control of the Loss Of Signal Channel select. Back to Register Map.

Table 69. Register - 0x2C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	SW_REFINSEL[3:0]	RW	0x0	Software Mode Reference Input Select. SW_REFINSEL - Input Selected 0001 - CLKIN0 0010 - CLKIN1 0100 - CLKIN2 1000 - CLKIN3
[3:0]	SW_LOS_CH_SEL[3:0]	RW	0x0	Loss of Source Channel Select. SW_LOS_CH_SEL - Input Selected 0001 - CLKIN0 0010 - CLKIN1 0100 - CLKIN2 1000 - CLKIN3

9.6.2.46 CLKIN_SWCTRL2

The CLKIN_SWCTRL2 Register provides control of the input stage settling time when switching on all inputs in case of Loss Of Signal. Back to Register Map.

Table 70. Register - 0x2D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4:0]	SW_ALLREFSON_TMR[4:0]	RW	0x0	Wait Time to allow Clock Inputs to Settle.

9.6.2.47 OSCIN_CTRL

The OSCIN_CTRL Register provides control of the OSCIN signal path. Back to Register Map.

Table 71. Register - 0x2E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	OSCIN_PD_LDO	RW	0	OSCIN LDO Powerdown. OSCIN_PD_LDO - LDO State 0 - LDO On 1 - LDO Off
[4]	OSCIN_SE_MODE	RW	1	OSCin Signal Mode. OSCIN_SE_MODE - Signal Mode Selection 0 - Differential 1 - Single-ended
[3]	OSCIN_BUF_TO_OSCOUT_EN	RW	1	OSCin to OSCout Buffer Enable.
[2]	OSCIN_OSCINSTAGE_EN	RW	1	OSCin Clock Input Stage Enable.
[1]	OSCIN_BUF_REF_EN	RW	0	OSCin to PLL1 and PLL2 Ref Clock Buffer Enable.
[0]	OSCIN_BUF_LOS_EN	RW	0	OSCin to LOS Clock Buffer Enable.

9.6.2.48 OSCOUT_CTRL

The OSCOUT_CTRL Register controls the OSCOUT Function. Back to Register Map.

Table 72. Register - 0x2F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OSCOUT_LVCMOS_WEAK_DRIVE	RW	0	Enable OSCOUT LVCMOS weak drive.

Table 72. Register - 0x2F (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[6]	OSCOUT_DIV_REGCONTROL	RW	0	Enable OSCOUT Divider setting through configuration register rather than SYNC pin control.
[5:4]	OSCOUT_PINSEL_DIV[1:0]	R	0x0	OSCOUT pin-selected Divider. OSCOUT_PINSEL_DIV - Pin-Selected Oscout Divider ratio 00 - 1 01 - 2 10 - 2 11 - 4
[3]	OSCOUT_SEL_VBG	RW	0	OSCOUT Bandgap Source Select. When OSCOUT_SEL_VBG is 0 the PLL1 Bandgap is used for OSCOUT. If OSCOUT_SEL_VBG is 1 the Output Channel Bandgap is used.
[2]	OSCOUT_DIV_CLKEN	RW	1	OSCout Divider Clock Enable. (RESERVED for PG1p0)
[1]	OSCOUT_SWRST	RWSC	0	OSCOUT Software Reset. Writing a 1 to OSCOUT_SWRST will reset the OSCOUT Block. The OSCOUT_SWRST is cleared automatically to 0.
[0]	OSCOUT_SEL_SRC	RW	1	OSCout Clock source select. OSCOUT_SEL_SRC - Clock Source 0 - PLL2 Output 1 - OSCin

9.6.2.49 OSCOUT_DIV

The OSCOUT_DIV Register controls the OSCOUT Divider Back to Register Map.

Table 73. Register - 0x30

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OSCOUT_DIV[7:0]	RW	0x0	OSCOUT Divider. Set value of OSCOUT channel divider.

9.6.2.50 OSCOUT_DRV

The OSCOUT_DRV Register controls the OSCOUT Driver. Back to Register Map.

Table 74. Register - 0x31

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	OSCOUT_DRV_MUTE[1:0]	RW	0x0	OSCOUT Driver Mute Control. OSCOUT_DRV_MUTE sets the OSCOUT driver mute input after the internal reset has been de-asserted. During the reset sequence the mute input is set to 11. It is configured together with OSCOUT_DRV_MODE. OSCOUT_DRV_MUTE,OSCOUT_DRV_MODE - Output State 00,XXXXXX - OSCOUT Driver is Active 01,11XXXX - OSCOUT_P operating normal, OSCOUT_N Low 01,01XXXX - OSCOUT_P operating normal, OSCOUT_N Operating normal 01,10XX00 - OSCOUT_P High, OSCOUT_N High 01,10XX01 - OSCOUT_P operating normal, OSCOUT_N operating normal 01,10XX10 - OSCOUT_P operating normal, OSCOUT_N operating normal 01,10XX11 - OSCOUT_P operating normal, OSCOUT_N operating normal 10,11XXXX - OSCOUT_P Low, OSCOUT_N operating normal 10,01XXXX - OSCOUT_P Low, OSCOUT_N High 10,10XX00 - OSCOUT_P High, OSCOUT_N High 10,10XX01 - OSCOUT_P Low, OSCOUT_N High 10,10XX10 - OSCOUT_P Low, OSCOUT_N High 10,10XX11 - OSCOUT_P Low, OSCOUT_N High 11,11XXXX - OSCOUT_P Low, OSCOUT_N Low 11,01XXXX - OSCOUT_P Low, OSCOUT_N High 11,10XX00 - OSCOUT_P High, OSCOUT_N High 11,10XX01 - OSCOUT_P Low, OSCOUT_N High 11,10XX10 - OSCOUT_P Low, OSCOUT_N High 11,10XX11 - OSCOUT_P Low, OSCOUT_N High
[5:0]	OSCOUT_DRV_MODE[5:0]	RW	0x3F	OSCOUT Driver Mode. OSCOUT_DRV_MODE - Output stage configuration 00XXXX - Power Down 01XXXX - HSDS Mode 10XXXX - HSCL Mode 11XXXX - LVCMOS Mode XX00XX - HSDS, HSCL: ITail: 4mA, LVCMOS: OSCOUT_P tristate XX01XX - HSDS, HSCL: ITail: 6mA, LVCMOS: OSCOUT_P Weak Drive XX10XX - HSDS, HSCL: ITail: 8mA, LVCMOS: OSCOUT_P Normal Drive Inverted XX11XX - ITail HSDS: 8mA, HSCL: 16mA, LVCMOS: OSCOUT_P Normal Drive Non-Inverted XXXX00 - Rload HSDS: open, HSCL: open, LVCMOS: OSCOUT_N tristate XXXX01 - Rload HSDS: open, HSCL: 50Ohm, LVCMOS: OSCOUT_N Weak Drive XXXX10 - Rload HSDS: open, HSCL: 100Ohm for Itail=4mA, 6mA, 8mA, LVCMOS: OSCOUT_N Normal Drive Inverted XXXX11 - Rload HSDS: open, HSCL: 200Ohm for Itail=4mA, LVCMOS: OSCOUT_N Normal Drive Non-Inverted

9.6.2.51 OUTCH_SWRST

The OUTCH_SWRST Register allows software reset to applied independently to each output channel. Back to Register Map.

Table 75. Register - 0x32

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	CH1415_SWRST	RWSC	0	CH1415 Software Reset. Writing a 1 to CH1415_SWRST will reset CH1415. CH1415_SWRST is cleared automatically to 0.
[6]	CH1213_SWRST	RWSC	0	CH1213 Software Reset. Writing a 1 to CH1213_SWRST will reset CH1213. CH1213_SWRST is cleared automatically to 0.
[5]	CH1011_SWRST	RWSC	0	CH1011 Software Reset. Writing a 1 to CH1011_SWRST will reset CH1011. CH1011_SWRST is cleared automatically to 0.
[4]	CH89_SWRST	RWSC	0	CH89 Software Reset. Writing a 1 to CH89_SWRST will reset CH89. CH89_SWRST is cleared automatically to 0.
[3]	CH67_SWRST	RWSC	0	CH67 Software Reset. Writing a 1 to CH67_SWRST will reset CH67. CH67_SWRST is cleared automatically to 0.
[2]	CH45_SWRST	RWSC	0	CH45 Software Reset. Writing a 1 to CH45_SWRST will reset CH45. CH45_SWRST is cleared automatically to 0.
[1]	CH23_SWRST	RWSC	0	CH23 Software Reset. Writing a 1 to CH23_SWRST will reset CH23. CH23_SWRST is cleared automatically to 0.
[0]	CH01_SWRST	RWSC	0	CH01 Software Reset. Writing a 1 to CH01_SWRST will reset CH01. CH01_SWRST is cleared automatically to 0.

9.6.2.52 OUTCH01CNTL0

The OUTCH01CNTRL0 Register controls Output CH0_1 Back to Register Map.

Table 76. Register - 0x33

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH01_LDO_BYP_MODE	RW	0	OUTCH01 LDO Bypass. OUTCH01_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH01_LDO_MASK	RW	0	OUTCH01 LDO Mask. If OUTCH01_LDO_MASK is 1 then CH01 LDO is masked from the Power Up Sequence and enabled directly.
[5:0]	OUTCH0_DRIV_MODE[5:0]	RW	0x18	OUTCH0 Clock Driver Mode Setting. OUTCH_DRIV_MODE - Function 00XXXX - Power Down 010000 - HSDS, Itail 4mA, RLoad 25 Ohm 010100 - HSDS, Itail 6mA, RLoad 25 Ohm 011000 - HSDS, Itail 8mA, RLoad 25 Ohm 111011 - HCSL, Itail 8mA, RLoad open 111111 - HCSL, Itail 16mA, RLoad open 111001 - HCSL, Itail 8mA, RLoad 50 Ohm 111101 - HCSL, Itail 16mA, RLoad 50 Ohm

9.6.2.53 OUTCH01CNTL1

The OUTCH01CNTRL1 Register controls Output CH0_1 Back to Register Map.

Table 77. Register - 0x34

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH1_DRIV_MODE[5:0]	RW	0x18	OUTCH1 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH0_1	RW	1	Output CH0_1 Divier Duty Cycle Correction Enable

Table 77. Register - 0x34 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[0]	OUTCH01_DIV_CLKEN	RW	1	OUTCH01 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.54 OUTCH23CNTL0

The OUTCH23CNTL0 Register controls Output CH2_3 Back to Register Map.

Table 78. Register - 0x35

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH23_LDO_BYP_MODE	RW	0	OUTCH23 LDO Bypass. OUTCH23_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH23_LDO_MASK	RW	0	OUTCH23 LDO Mask. If OUTCH23_LDO_MASK is 1 then CH23 LDO is masked from the Power Sequence.
[5:0]	OUTCH2_DRIV_MODE[5:0]	RW	0x18	OUTCH2 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.55 OUTCH23CNTL1

The OUTCH23CNTRL1 Register controls Output CH2_3 Back to Register Map.

Table 79. Register - 0x36

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH3_DRIV_MODE[5:0]	RW	0x18	OUTCH3 Clock Driver Mode Setting. See CHANNEL0 for description.
[1]	DIV_DCC_EN_CH2_3	RW	1	Output CH2_3 Divider Duty Cycle Correction Enable
[0]	OUTCH23_DIV_CLKEN	RW	1	OUTCH23 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.56 OUTCH45CNTL0

The OUTCH45CNTRL0 Register controls Output CH4_5 Back to Register Map.

Table 80. Register - 0x37

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH45_LDO_BYP_MODE	RW	0	OUTCH45 LDO Bypass. OUTCH45_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH45_LDO_MASK	RW	0	OUTCH45 LDO Mask. If OUTCH45_LDO_MASK is 1 then CH45 LDO is masked from the Power Sequence.
[5:0]	OUTCH4_DRIV_MODE[5:0]	RW	0x18	OUTCH4 Clock Driver Mode Setting. See OUTCH0 for description.

9.6.2.57 OUTCH45CNTL1

The OUTCH45CNTRL1 Register controls Output CH4_5 Back to Register Map.

Table 81. Register - 0x38

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH5_DRIV_MODE[5:0]	RW	0x18	OUTCH5 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH4_5	RW	1	Output CH4_5 Divider Duty Cycle Correction Enable
[0]	OUTCH45_DIV_CLKEN	RW	1	OUTCH45 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.58 OUTCH67CNTL0

The OUTCH67CNTRL0 Register controls Output CH6_7 Back to Register Map.

Table 82. Register - 0x39

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH67_LDO_BYP_MODE	RW	0	OUTCH67 LDO Bypass. OUTCH67_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH67_LDO_MASK	RW	0	OUTCH67 LDO Mask. If OUTCH67_LDO_MASK is 1 then CH67 LDO is masked from the Power Sequence.
[5:0]	OUTCH6_DRIV_MODE[5:0]	RW	0x18	OUTCH6 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.59 OUTCH67CNTL1

The OUTCH67CNTRL1 Register controls Output CH6_7 Back to Register Map.

Table 83. Register - 0x3A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH7_DRIV_MODE[5:0]	RW	0x18	OUTCH7 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH6_7	RW	0	Output CH6_7 Divider Duty Cycle Correction Enable
[0]	OUTCH67_DIV_CLKEN	RW	1	OUTCH67 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.60 OUTCH89CNTL0

The OUTCH89CNTRL0 Register controls Output CH8_9 Back to Register Map.

Table 84. Register - 0x3B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH89_LDO_BYP_MODE	RW	0	OUTCH89 LDO Bypass. OUTCH89_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH89_LDO_MASK	RW	0	OUTCH89 LDO Mask. If OUTCH89_LDO_MASK is 1 then CH89 LDO is masked from the Power Sequence.
[5:0]	OUTCH8_DRIV_MODE[5:0]	RW	0x18	OUTCH8 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.61 OUTCH89CNTL1

The OUTCH89CNTRL1 Register controls Output CH8_9 Back to Register Map.

Table 85. Register - 0x3C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH9_DRIV_MODE[5:0]	RW	0x18	OUTCH9 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH8_9	RW	0	Output CH8_9 Divider Duty Cycle Correction Enable
[0]	OUTCH89_DIV_CLKEN	RW	1	OUTCH89 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.62 OUTCH1011CNTL0

The OUTCH1011CNTRL0 Register controls Output CH10_11 Back to Register Map.

Table 86. Register - 0x3D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH1011_LDO_BYP_MODE	RW	0	OUTCH1011 LDO Bypass. OUTCH1011_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH1011_LDO_MASK	RW	0	OUTCH1011 LDO Mask. If OUTCH1011_LDO_MASK is 1 then CH1011 LDO is masked from the Power Sequence.
[5:0]	OUTCH10_DRIV_MODE[5:0]	RW	0x18	OUTCH10 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.63 OUTCH1011CNTL1

The OUTCH1011CNTRL1 Register controls Output CH10_11 Back to Register Map.

Table 87. Register - 0x3E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH11_DRIV_MODE[5:0]	RW	0x18	OUTCH11 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH10_11	RW	0	Output CH10_11 Divider Duty Cycle Correction Enable
[0]	OUTCH1011_DIV_CLKEN	RW	1	OUTCH1011 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.64 OUTCH1213CNTL0

The OUTCH1213CNTRL0 Register controls Output CH12_13 Back to Register Map.

Table 88. Register - 0x3F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH1213_LDO_BYP_MODE	RW	0	OUTCH1213 LDO Bypass. OUTCH1213_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH1213_LDO_MASK	RW	0	OUTCH1213 LDO Mask. If OUTCH1213_LDO_MASK is 1 then CH1213 LDO is masked from the Power Sequence.
[5:0]	OUTCH12_DRIV_MODE[5:0]	RW	0x18	OUTCH12 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.65 OUTCH1213CNTL1

The OUTCH1213CNTRL1 Register controls Output CH12_13 Back to Register Map.

Table 89. Register - 0x40

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH13_DRIV_MODE[5:0]	RW	0x18	OUTCH13 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH12_13	RW	0	Output CH12_13 Divider Duty Cycle Correction Enable
[0]	OUTCH1213_DIV_CLKEN	RW	1	OUTCH1213 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.66 OUTCH1415CNTL0

The OUTCH1415CNTRL0 Register controls Output CH14_15 Back to Register Map.

Table 90. Register - 0x41

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH1415_LDO_BYP_MODE	RW	0	OUTCH1415 LDO Bypass. OUTCH1415_LDO_BYP_MODE - LDO State 0 - Enabled 1 - Bypassed
[6]	OUTCH1415_LDO_MASK	RW	0	OUTCH1415 LDO Mask. If OUTCH1415_LDO_MASK is 1 then CH1415 LDO is masked from the Power Sequence.
[5:0]	OUTCH14_DRIV_MODE[5:0]	RW	0x18	OUTCH14 Clock Driver Mode Setting. See CHANNEL0 for description.

9.6.2.67 OUTCH1415CNTL1

The OUTCH1415CNTRL1 Register controls Output CH14_15 Back to Register Map.

Table 91. Register - 0x42

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	OUTCH15_DRIV_MODE[5:0]	RW	0x18	OUTCH15 Clock Driver Mode Setting.
[1]	DIV_DCC_EN_CH14_15	RW	0	Output CH14_15 Divider Duty Cycle Correction Enable
[0]	OUTCH1415_DIV_CLKEN	RW	1	OUTCH1415 Channel Divider Clock Enable. Enables output channel PLL Clock Buffer.

9.6.2.68 OUTCH01DIV_BY1

The OUTCH01DIV_BY1,BY0 Registers set the OUTCH01 Divider Value. Back to Register Map.

Table 92. Register - 0x43

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH01_DIV[15:8]	RW	0x0	OUTCH01 Divider Value. Sets the divider value for output channels 0 and 1. An automatic reset is issued whenever the divider value is changed.

9.6.2.69 OUTCH01DIV_BY0

The OUTCH01DIV_BY0 Register sets the lower 7 bits of the OUTCH01 Divider Value. Back to Register Map.

Table 93. Register - 0x44

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH01_DIV[7:0]	RW	0x1	OUTCH01 Divider Value.

9.6.2.70 OUTCH23DIV_BY1

The OUTCH23DIV_BY1,BY0 Registers set the OUTCH23 Divider Value. Back to Register Map.

Table 94. Register - 0x45

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH23_DIV[15:8]	RW	0x0	OUTCH23 Divider Value. Sets the divider value for output channels 2 and 3. An automatic reset is issued whenever the divider value is changed.

9.6.2.71 OUTCH23DIV_BY0

The OUTCH23DIV_BY0 Register sets the lower 7 bits of the OUTCH23 Divider Value. Back to Register Map.

Table 95. Register - 0x46

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH23_DIV[7:0]	RW	0x2	OUTCH23 Divider Value.

9.6.2.72 OUTCH45DIV_BY1

The OUTCH45DIV_BY1,BY0 Registers set the OUTCH45 Divider Value. Back to Register Map.

Table 96. Register - 0x47

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH45_DIV[15:8]	RW	0x0	OUTCH45 Divider Value. Sets the divider value for output channels 4 and 5. An automatic reset is issued whenever the divider value is changed.

9.6.2.73 OUTCH45DIV_BY0

The OUTCH45DIV_BY0 Register sets the lower 7 bits of the OUTCH45 Divider Value. Back to Register Map.

Table 97. Register - 0x48

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH45_DIV[7:0]	RW	0x8	OUTCH45 Divider Value.

9.6.2.74 OUTCH67DIV_BY1

The OUTCH67DIV_BY1,BY0 Registers set the OUTCH67 Divider Value. Back to Register Map.

Table 98. Register - 0x49

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH67_DIV[15:8]	RW	0x0	OUTCH67 Divider Value. Sets the divider value for output channels 6 and 7. An automatic reset is issued whenever the divider value is changed.

9.6.2.75 OUTCH67DIV_BY0

The OUTCH67DIV_BY0 Register sets the lower 7 bits of the OUTCH67 Divider Value. Back to Register Map.

Table 99. Register - 0x4A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH67_DIV[7:0]	RW	0x20	OUTCH67 Divider Value.

9.6.2.76 OUTCH89DIV_BY1

The OUTCH89DIV_BY1,BY0 Registers set the OUTCH89 Divider Value. Back to Register Map.

Table 100. Register - 0x4B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH89_DIV[15:8]	RW	0x0	OUTCH89 Divider Value. Sets the divider value for output channels 8 and 9. An automatic reset is issued whenever the divider value is changed.

9.6.2.77 OUTCH89DIV_BY0

The OUTCH89DIV_BY0 Register sets the lower 7 bits of the OUTCH89 Divider Value. Back to Register Map.

Table 101. Register - 0x4C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH89_DIV[7:0]	RW	0x3	OUTCH89 Divider Value.

9.6.2.78 OUTCH1011DIV_BY1

The OUTCH1011DIV_BY1,BY0 Registers set the OUTCH1011 Divider Value. Back to Register Map.

Table 102. Register - 0x4D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1011_DIV[15:8]	RW	0x0	OUTCH1011 Divider Value. Sets the divider value for output channels 10 and 11. An automatic reset is issued whenever the divider value is changed.

9.6.2.79 OUTCH1011DIV_BY0

The OUTCH1011DIV_BY0 Register sets the lower 7 bits of the OUTCH1011 Divider Value. Back to Register Map.

Table 103. Register - 0x4E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1011_DIV[7:0]	RW	0x5	OUTCH1011 Divider Value.

9.6.2.80 OUTCH1213DIV_BY1

The OUTCH1213DIV_BY1,BY0 Registers set the OUTCH1213 Divider Value. Back to Register Map.

Table 104. Register - 0x4F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1213_DIV[15:8]	RW	0x0	OUTCH1213 Divider Value. Sets the divider value for output channels 12 and 13. An automatic reset is issued whenever the divider value is changed.

9.6.2.81 OUTCH1213DIV_BY0

The OUTCH1213DIV_BY0 Register sets the lower 7 bits of the OUTCH1213 Divider Value. Back to Register Map.

Table 105. Register - 0x50

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1213_DIV[7:0]	RW	0x9	OUTCH1213 Divider Value.

9.6.2.82 OUTCH1415DIV_BY1

The OUTCH1415DIV_BY1,BY0 Registers set the OUTCH1415 Divider Value. Back to Register Map.

Table 106. Register - 0x51

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1415_DIV[15:8]	RW	0x0	OUTCH1415 Divider Value. Sets the divider value for output channels 14 and 15. An automatic reset is issued whenever the divider value is changed.

9.6.2.83 OUTCH1415DIV_BY0

The OUTCH1415DIV_BY0 Register sets the lower 7 bits of the OUTCH1415 Divider Value. Back to Register Map.

Table 107. Register - 0x52

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	OUTCH1415_DIV[7:0]	RW	0x1F	OUTCH1415 Divider Value.

9.6.2.84 OUTCH_DIV_INV

The OUTCH_DIV_INV Register controls inversion of the dividier output clock. Back to Register Map.

Table 108. Register - 0x53

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	OUTCH1415_DIV_INV	RW	0	OUTCH1415 Divider Output Invert. When OUTCH1415_DIV_INV is 1 the divider output for channels 14 and 15 is inverted.
[6]	OUTCH1213_DIV_INV	RW	0	OUTCH1213 Divider Output Invert. When OUTCH1213_DIV_INV is 1 the divider output for channels 12 and 13 is inverted.
[5]	OUTCH1011_DIV_INV	RW	0	OUTCH1011 Divider Output Invert. When OUTCH1011_DIV_INV is 1 the divider output for channels 10 and 11 is inverted.
[4]	OUTCH89_DIV_INV	RW	0	OUTCH89 Divider Output Invert. When OUTCH89_DIV_INV is 1 the divider output for channels 8 and 9 is inverted.
[3]	OUTCH67_DIV_INV	RW	0	OUTCH67 Divider Output Invert. When OUTCH67_DIV_INV is 1 the divider output for channels 6 and 7 is inverted.
[2]	OUTCH45_DIV_INV	RW	0	OUTCH45 Divider Output Invert. When OUTCH45_DIV_INV is 1 the divider output for channels 4 and 5 is inverted.
[1]	OUTCH23_DIV_INV	RW	0	OUTCH23 Divider Output Invert. When OUTCH23_DIV_INV is 1 the divider output for channels 2 and 3 is inverted.
[0]	OUTCH01_DIV_INV	RW	0	OUTCH01 Divider Output Invert. When OUTCH01_DIV_INV is 1 the divider output for channels 0 and 1 is inverted.

9.6.2.85 PLL1CTRL0

The PLL1CTRL0 Register provides control of the following PLL1 related features. Back to Register Map.

Table 109. Register - 0x54

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL1_F_30	RW	0	PLL1 RC Freq 0 = 122 MHz 1 = 32MHz. PLL1_F_30 - PLL1 RC Frequency 0 - 122 MHz 1 - 32 MHz
[6]	PLL1_EN_REGULATION	RW	0	PLL1 Prop-CP Enable Regulation
[5]	PLL1_PD_LD	RW	1	PLL1 Window Comparator Powerdown. PLL1_PD_LD - PLL1 Window Comparator 0 - Enabled 1 - Off
[4]	PLL1_DIR_POS_GAIN	RW	1	PLL1 VCXO pos/neg Gain. PLL1_DIR_POS_GAIN - Polarity 0 - Positive 1 - Negative
[3:0]	PLL1_LDO_WAIT_TMR[3:0]	RW	0x0	PLL1 LDO Wait Timer. The PLL1 LDO Wait Timer counts a number of clock cycles equal to 32*(PLL1_LDO_WAIT_TMR+31) before releasing the PLL1 NDIV and RDIV resets.

9.6.2.86 PLL1CTRL1

The PLL1CTRL1 Register provides control over PLL1 related features. Back to Register Map.

Table 110. Register - 0x55

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL1_LCKDET_BY_32	RW	0	PLL1 Lock Detect counter multiply with 32.
[6]	PLL1_FAST_LOCK	RW	1	PLL1 Fast Lock Enable.
[5]	PLL1_LCKDET_LOS_MASK	RW	0	PLL1 Lock Detect LOS Mask. When PLL1_LCKDET_LOS_MASK is 1 then Loss of Source has no effect on the PLL1 Lock Detect circuit.
[4]	PLL1_FBCLK_INV	RW	1	PLL1 Feedback Clock Inversion. When PLL1_FBCLK_INV is 1 then the Feedback Clock divider output is inverted.
[3]	RSRVD	-	-	Reserved.
[2]	PLL1_BYP_LOS	RW	0	PLL1 Bypass Loss of Source indication. When PLL1_BYP_LOS is 1 the PLL1 controller ignores the LOS indicator.
[1]	PLL1_PFD_UP_HOLDOVER	RW	0	PLL1 PFD UP-Input value during Holdover.
[0]	PLL1_PFD_DOWN_HOLDOVER	RW	0	PLL1 PFD DN-Input value during Holdover.

9.6.2.87 PLL1CTRL2

The PLL1CTRL2 Register provides control over PLL1 related features. Back to Register Map.

Table 111. Register - 0x56

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	PLL1_LOL_NORESET	RW	0	If set to 1, PLL1 will not be reset on a Loss-of-Lock event.
[3]	PLL1_RDIV_CLKEN	RW	1	PLL1 RDIV Clock Enable.
[2]	PLL1_RDIV_4CY	RW	1	PLL1 RDIV Enable tied clock low phase to 4cycs. Independent from divider setting.
[1]	PLL1_NDIV_CLKEN	RW	1	PLL1 NDIV Clock Enable
[0]	PLL1_NDIV_4CY	RW	1	PLL1 NDIV Enable tied clock low phase to 4cycs. Independent from divider setting.

9.6.2.88 PLL1_SWRST

The PLL1_SWRST Register provides control of the PLL1 software reset's Back to Register Map.

Table 112. Register - 0x57

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	PLL1_HOLDOVER_DLD_SWRST	RWSC	0	PLL1 Holdover DLD Software Reset. Writing a 1 to PLL1_HOLDOVER_DLD_SWRST will activate the reset. PLL1_HOLDOVER_DLD_SWRST is cleared automatically to 0.
[4]	PLL1_RDIV_SWRST	RWSC	0	PLL1 R-Divider Software Reset. Writing a 1 to PLL1_RDIV_SWRST will reset the R-Divider. PLL1_RDIV_SWRST is cleared automatically to 0.
[3]	PLL1_NDIV_SWRST	RWSC	0	PLL1 N-Divider Software Reset. Writing a 1 to PLL1_NDIV_SWRST will reset the N-Divider. PLL1_NDIV_SWRST is cleared automatically to 0.
[2]	PLL1_HOLDOVERCNT_SWRST	RWSC	0	PLL1 Holdover Counter Software Reset. Writing a 1 to PLL1_HOLDOVERCNT_SWRST will activate the reset. PLL1_HOLDOVERCNT_SWRST is cleared automatically to 0.

Table 112. Register - 0x57 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[1]	PLL1_HOLDOVER_LOCKDET_SWRST	RWSC	0	PLL1 Holdover Lock Detect Software Reset. Writing a 1 to PLL1_HOLDOVER_LOCKDET_SWRST will activate the reset. PLL1_HOLDOVER_LOCKDET_SWRST is cleared automatically to 0.
[0]	PLL1_SWRST	RWSC	0	PLL1 Software Reset. Writing a 1 to PLL1_SWRST will reset PLL1 PLL1_SWRST is cleared automatically to 0.

9.6.2.89 PLL1WNDWSIZE

The PLL1WNDWSIZE Register sets the PLL1 Window Comparator Size. Back to Register Map.

Table 113. Register - 0x58

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_LD_WNDW_SIZE[7:0]	RW	0x3F	PLL1 Window Comparator Size.

9.6.2.90 PLL1STRCELL

The PLL1STRCELL Register provides control of the Storage Cell settings. Back to Register Map.

Table 114. Register - 0x59

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	PLL1_INTG_FL[3:0]	RW	0x1	PLL1 Integral Gain setting during Fast Lock.
[3:0]	PLL1_INTG[3:0]	RW	0x1	PLL1 Integral Gain setting.

9.6.2.91 PLL1CPSETTING

The PLL1CPSETTING Register provides control of the Chargepump Current/Bandwidth Setting. Back to Register Map.

Table 115. Register - 0x5A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	RW	0x0	Reserved.
[6:0]	PLL1_PROP[6:0]	RW	0x8	Prop-CP Current/Bandwidth Setting.

9.6.2.92 PLL1CPSETTING_FL

The PLL1CPSETTING_FL Register provides control of the Chargepump Current/Bandwidth Setting during Fast Lock. Back to Register Map.

Table 116. Register - 0x5B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	RW	0x1	Reserved
[6:0]	PLL1_PROP_FL[6:0]	RW	0x7F	Prop-CP Current/Bandwidth Setting for Fast Lock.

9.6.2.93 PLL1_HOLDOVER_CTRL1

The PLL1_HOLDOVER_CTRL1 Register provides control of the PLL1 holdover operation. Back to Register Map.

Table 117. Register - 0x5C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL1_HOLDOVER_EN	RW	1	Enable PLL1 Holdover function. When PLL1_HOLDOVER_EN is 1 the holdover circuit is enabled. When PLL1_HOLDOVER_EN is 0 the holdover circuit is disabled.

Table 117. Register - 0x5C (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[6]	PLL1_STARTUP_HOLDOVER_EN	RW	1	When PLL1_HOLDOVER_FORCE is 1, PLL1 enters holdover mode immediately on startup.
[5]	PLL1_HOLDOVER_FORCE	RW	0	PLL1 Force Holdover Operation. When PLL1_HOLDOVER_FORCE is 1 PLL1 enters holdover mode regardless of other conditions.
[4]	PLL1_HOLDOVER_RAIL_MODE	RW	0	PLL1 Rail Detection Level Relative or absolute. PLL1_HOLDOVER_RAIL_MODE - Level Mode 0 - Absolute-Level 1 - Relative to Level set at Lock
[3]	PLL1_HOLDOVER_MAX_CNT_EN	RW	1	PLL1 Holdover Max Counter enable. Wait for PLL1_HOLDOVER_MAXCNT cycles before starting Auto-CLKin-Switch procedure.
[2]	PLL1_HOLDOVER_LOS_MASK	RW	0	PLL1 Holdover LOS Mask. When PLL1_HOLDOVER_LOS_MASK is 1 then Loss of Source has no effect in the activation of holdover.
[1]	PLL1_HOLDOVER_LCKDET_MASK	RW	1	PLL1 Holdover Lock Detect Mask. When PLL1_HOLDOVER_LCKDET_MASK is 1 then Lock Detect has no effect in the activation of holdover.
[0]	PLL1_HOLDOVER_RAILDET_EN	RW	0	PLL1 Holdover Rail Detection Enable. When PLL1_HOLDOVER_RAILDET_EN is 1 the rail detection circuit is enabled. When PLL1_HOLDOVER_RAILDET EN is 0 the rail detection circuit is disabled.

9.6.2.94 PLL1_HOLDOVER_MAXCNT_BY3

The PLL1_HOLDOVER_MAXCNT field is set by PLL1_HOLDOVER_MAXCNT_BY3,BY2,BY1 and BY0. Back to Register Map.

Table 118. Register - 0x5D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_HOLDOVER_MAX_CNT[31:24]	RW	0x0	PLL1 Maximum Holdover Count. When the value specified by PLL1_HOLDOVER_MAX_CNT is reached then the device will attempt to switch to any available reference clocks.

9.6.2.95 PLL1_HOLDOVER_MAXCNT_BY2

The PLL1_HOLDOVER_MAXCNT1 Register sets bits [23:16] Back to Register Map.

Table 119. Register - 0x5E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_HOLDOVER_MAX_CNT[23:16]	RW	0x1	PLL1 Maximum Holdover Count.

9.6.2.96 PLL1_HOLDOVER_MAXCNT_BY1

The PLL1_HOLDOVER_MAXCNT0 Register sets bits [15:8] Back to Register Map.

Table 120. Register - 0x5F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_HOLDOVER_MAX_CNT[15:8]	RW	0x84	PLL1 Maximum Holdover Count.

9.6.2.97 PLL1_HOLDOVER_MAXCNT_BY0

The PLL1_HOLDOVER_MAXCNT0 Register sets bits [7:0] Back to Register Map.

Table 121. Register - 0x60

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_HOLDOVER_MAX_CNT[7:0]	RW	0x80	PLL1 Maximum Holdover Count.

9.6.2.98 PLL1_NDIV_BY1

The PLL1_NDIV value is set by Register's PLL1_NDIV_BY1 and PLL1_NDIV_BY0 Back to Register Map.

Table 122. Register - 0x61

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_NDIV[15:8]	RW	0x0	PLL1 N-Feedback Divider Value. PLL1_NDIV - N-Feedback Divider 0 - Reserved 1 - 1 .. - .. 65535 - 65535

9.6.2.99 PLL1_NDIV_BY0

The PLL1_NDIV_BY0 Register sets bits [7:0] Back to Register Map.

Table 123. Register - 0x62

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_NDIV[7:0]	RW	0x78	PLL1 N-Feedback Divider Value.

9.6.2.100 PLL1_LOCKDET_CYC_CNT_BY2

The PLL1_LOCKDET_CYC_CNT is set by registers PLL1_LOCKDET_CYC_CNT_BY2, PLL1_LOCKDET_CYC_CNT_BY1 and PLL1_LOCKDET_CYC_CNT_BY0 Back to Register Map.

Table 124. Register - 0x63

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_LOCKDET_CYC_CNT[23:16]	RW	0x0	PLL1 Lock Detect Cycle Counter.

9.6.2.101 PLL1_LOCKDET_CYC_CNT_BY1

The PLL1_LOCKDET_CYC_CNT_BY1 Register sets bits [15:8] Back to Register Map.

Table 125. Register - 0x64

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_LOCKDET_CYC_CNT[15:8]	RW	0x40	PLL1 Lock Detect Cycle Counter.

9.6.2.102 PLL1_LOCKDET_CYC_CNT_BY0

The PLL1_LOCKDET_CYC_CNT_BY0 Register sets bits [7:0] Back to Register Map.

Table 126. Register - 0x65

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_LOCKDET_CYC_CNT[7:0]	RW	0x0	PLL1 Lock Detect Cycle Counter.

9.6.2.103 RSRVD_0x66

Table 127. Register - 0x66

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	RSRVD	R	0x0	Reserved.

9.6.2.104 RSRVD_0x67

Table 128. Register - 0x67

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_STORAGE_CELL[31:24]	R	0x0	PLL1 Storage Cell Value.

9.6.2.105 RSRVD_0x68

Table 129. Register - 0x68

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_STORAGE_CELL[23:16]	R	0x0	PLL1 Storage Cell Value.

9.6.2.106 RSRVD_0x69

Table 130. Register - 0x69

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL1_STORAGE_CELL[15:8]	R	0x0	PLL1 Storage Cell Value.

9.6.2.107 PLL1_STRG

The PLL1_STRG reads current storage cell value of PLL1. Back to Register Map.

Table 131. Register - 0x6A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	R	0x0	Reserved
[5:0]	PLL1_STORAGE_CELL[5:0]	R	0x0	PLL1 Storage Cell Value.

9.6.2.108 PLL1RCCLKDIV

The PLL1RCCLKDIV Register controls the PLL1 RC Clock Divider Back to Register Map.

Table 132. Register - 0x6B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	PLL1_RC_CLK_EN	RW	1	PLL1 RC Clock Enable.
[3]	RSRVD	-	-	Reserved.
[2:0]	PLL1_RC_CLK_DIV[2:0]	RW	0x7	PLL1 RC Clk Divider value. Sets the divider value for the PLL1 RC clock that is derived from the PLL2 VCO Clock. PLL1_RC_CLK_DIV - Divider Value 0 - 1 1 - 2 .. - .. 7 - 8

9.6.2.109 PLL2_CTRL0

The PLL2_CTRL0 Register provides control of PLL2 features. Back to Register Map.

Table 133. Register - 0x6C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	PLL2_VCO_PRESC_LOW_POWER	RW	0	PLL2 Prescaler Low Power Mode.
[3]	PLL2_BYP_OSC	RW	0	Clock Source for Oscout Buffer. PLL2_BYP_OSC - Oscout Clock Source 0 - PLL2 Output 1 - PLL2 Input
[2]	PLL2_BYP_TOP	RW	0	Clock Source for Top Outputs. PLL2_BYP_TOP - Top Outputs Clock Source 0 - PLL2 Output 1 - PLL2 Input
[1]	PLL2_BYP_BOT	RW	0	Clock Source for Bottom Outputs. PLL2_BYP_BOT - Bottom Outputs Clock Source 0 - PLL2 Output 1 - PLL2 Input
[0]	PLL2_GLOBAL_BYP	RW	0	PLL2 Global Bypass Enable. PLL2_GLOBAL_BYP - PLL2 Input Clock Source 0 - OSCin 1 - CLKIN0..3

9.6.2.110 PLL2_CTRL1

The PLL2_CTRL1 Register provides control of PLL2 features. Back to Register Map.

Table 134. Register - 0x6D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL2_EN_PULSE_GEN	RW	0	Enable Pulse Generator in PLL2 R input block.
[6]	PLL2_RDIV_BYP	RW	0	PLL2 R-Divider Bypass. When PLL2_RDIV_BYP is 1 the R-Divider is by-passed.
[5]	PLL2_DBL_EN_INV	RW	0	PLL2 Doubler Enable Invert. When PLL2_DBL_EN_INV is 1 the output of the PLL2 Doubler is inverted.
[4]	PLL2_PD_VARBIAS	RW	0	VCO Varactor Biasing PD.
[3]	PLL2_SMART_TRIM	RW	1	PLL2 Smart trim enable. If PLL2_SMART_TRIM is set to 1 then the initial calibration threshold is set by PLL2_AC_STRT_THRESHOLD and the final threshold is set by PLL2_AC_THRESHOLD. If PLL2_SMART_TRIM is 0 the threshold is set by PLL2_AC_THRESHOLD at all times.
[2]	PLL2_LCKDET_LOS_MASK	RW	1	PLL2 Lock Detect LOS Mask. When PLL2_LCKDET_LOS_MASK is 1 then Loss of Source has no effect on the PLL2 Lock Detect circuit.
[1]	PLL2_RDIV_DBL_EN	RW	0	PLL2 R-Divider Doubler Enable.
[0]	PLL2_PD_LD	RW	1	PLL2 Window Comparator Powerdown.

9.6.2.111 PLL2_CTRL2

The PLL2_CTRL2 Register provides control of PLL2 features. Back to Register Map.

Table 135. Register - 0x6E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL2_BYP_SYNC_TOP	RW	0	RESERVED
[6]	PLL2_BYP_SYNC_BOTTOM	RW	0	RESERVED
[5]	PLL2_EN_BYP_BUF	RW	0	PLL2 Enable Bypass Clock Buffer.

Table 135. Register - 0x6E (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[4]	PLL2_EN_BUF_SYNC_TOP	RW	1	PLL2 Enable Clock Buffer for Re-clocked SYNC signal to TOP Output-CHs.
[3]	PLL2_EN_BUF_SYNC_BOTTOM	RW	1	PLL2 Enable Clock Buffer for Re-clocked SYNC signal to Bottom Output-CHs.
[2]	PLL2_EN_BUF_OSCOUT	RW	0	PLL2 Enable Clock Buffer for OSCOut.
[1]	PLL2_EN_BUF_CLK_TOP	RW	1	PLL2 Enable Clock Buffer for Top Output-CHs.
[0]	PLL2_EN_BUF_CLK_BOTTOM	RW	1	PLL2 Enable Clock Buffer for Bottom Output-CHs.

9.6.2.112 PLL2_SWRST

The PLL2_SWRST Register allows activation of the following PLL2 related software resets. Back to Register Map.

Table 136. Register - 0x6F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2]	PLL2_RDIV_SWRST	RWSC	0	PLL2 R-Divider Software Reset. Writing a 1 to PLL2_RDIV_SWRST will reset the R-Divider. PLL2_RDIV_SWRST is cleared automatically to 0.
[1]	PLL2_NDIV_SWRST	RWSC	0	PLL2 N-Divider Software Reset. Writing a 1 to PLL2_NDIV_SWRST will reset the N-Divider. PLL2_NDIV_SWRST is cleared automatically to 0.
[0]	PLL2_SWRST	RWSC	0	PLL2 Software Reset. Writing a 1 to PLL2_SWRST will reset PLL2 PLL2_SWRST is cleared automatically to 0.

9.6.2.113 PLL2_LF_C4R4

The PLL2_LF_C4R4 Register sets the values for C4 and R4 Back to Register Map.

Table 137. Register - 0x70

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	PLL2_C4_LF_SEL[3:0]	RW	0x0	PLL2 Loop Filter C4 Value.
[3:0]	PLL2_R4_LF_SEL[3:0]	RW	0x0	PLL2 Loop Filter R4 Value.

9.6.2.114 PLL2_LF_C3R3

The PLL2_LF_C3R3 Register sets the values for C3 and R3 Back to Register Map.

Table 138. Register - 0x71

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	PLL2_C3_LF_SEL[3:0]	RW	0x0	PLL2 Loop Filter C3 Value.
[3:0]	PLL2_R3_LF_SEL[3:0]	RW	0x0	PLL2 Loop Filter R3 Value.

9.6.2.115 PLL2_CP_SETTING

The PLL2_CP_SETTING Register provides control of the PLL2 Chargepump. Back to Register Map.

Table 139. Register - 0x72

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	RW	0x0	Reserved.
[5:0]	PLL2_PROP[5:0]	RW	0x3	PLL2 Charge pump Setting.

9.6.2.116 PLL2_NDIV_BY1

The PLL2 N-Divider Value is set by Register's PLL2_NDIV_BY1 and PLL2_NDIV_BY0. Back to Register Map.

Table 140. Register - 0x73

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_NDIV[15:8]	RW	0x0	PLL2 N-Divider Value.

9.6.2.117 PLL2_NDIV_BY0

The PLL2_NDIV_BY0 Register sets bits [7:0] Back to Register Map.

Table 141. Register - 0x74

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_NDIV[7:0]	RW	0x20	PLL2 N-Divider Value.

9.6.2.118 PLL2_RDIV_BY1

RESERVED. Back to Register Map.

Table 142. Register - 0x75

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_RDIV[15:8]	RW	0x0	PLL2 R-Divider Value. PLL2 R-Divider configuration limited to bits [5..0].

9.6.2.119 PLL2_RDIV_BY0

The PLL2_RDIV Register sets the PLL2 R-Divider bits [5:0]. Back to Register Map.

Table 143. Register - 0x76

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_RDIV[7:0]	RW	0x0	PLL2 R-Divider Value. PLL2 R-Divider configuration limited to bits [5..0].

9.6.2.120 PLL2_STRG_INIT_BY1

The PLL2_STRG_INIT_BY1 Register Back to Register Map.

Table 144. Register - 0x77

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_STRG_INITVAL[15:8]	RW	0x0	PLL2 Storage-CP Init Value.

9.6.2.121 PLL2_STRG_INIT_BY0

The PLL2_STRG_INIT_BY0 Register Back to Register Map.

Table 145. Register - 0x78

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_STRG_INITVAL[7:0]	RW	0xFF	PLL2 Storage-CP Init Value.

9.6.2.122 RAILDET_UP

The Rail Detect Upper Limit Back to Register Map.

Table 146. Register - 0x7D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.

Table 146. Register - 0x7D (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[5:0]	RAILDET_UPP[5:0]	RW	0x0	Upper Rail Detection Limit.

9.6.2.123 RAILDET_LOW

The Rail Detect Lower Limit Back to Register Map.

Table 147. Register - 0x7E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5:0]	RAILDET_LOW[5:0]	RW	0x0	Lower Rail Detection Limit.

9.6.2.124 PLL2_AC_CTRL

The PLL2_AC_CTRL Register provides control of PLL2 Amplitude Calibration features. Back to Register Map.

Table 148. Register - 0x7F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	PLL2_AC_CAL_EN	RW	1	PLL2 Amplitude Calibration Enable.
[4]	PLL2_PD_AC	RW	1	VCO Peak detector Power down. 1=off, 0=enabled.
[3:2]	PLL2_IDACSET_RECAL[1:0]	RW	0x1	PLL2 IDAC Re-Calibration Setting. When the difference between consecutive IDACSET values is greater than PLL2_IDACSET_RECAL the amplitude calibration is restarted.
[1]	PLL2_AC_REQ	RWSC	0	PLL2 Amplitude Calibration Request.
[0]	PLL2_FAST_ACAL	RW	0	PLL2 Fast Amplitude Calibration Enable.

9.6.2.125 PLL2_CURR_STOR_CELL

The PLL2_CURR_STOR_CELL Register is described below. Back to Register Map.

Table 149. Register - 0x80

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	RW	0x0	Reserved.
[4:0]	PLL2_INTG[4:0]	RW	0x3	PLL2 Integral gain setting.

9.6.2.126 PLL2_AC_THRESHOLD

The PLL2_AC_THRESHOLD Register sets the Amplitude Calibration Threshold Back to Register Map.

Table 150. Register - 0x81

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4:0]	PLL2_AC_THRESHOLD[4:0]	RW	0x0	PLL2 VCO Amplitude Calibration Threshold.

9.6.2.127 PLL2_AC_STRT_THRESHOLD

The PLL2_AC_THRESHOLD Register sets the Amplitude Calibration Starting Threshold Back to Register Map.

Table 151. Register - 0x82

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.

Table 151. Register - 0x82 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[4:0]	PLL2_AC_STRT_THRESHOLD[4:0]	RW	0x0	PLL2 VCO Amplitude Calibration Starting Threshold.

9.6.2.128 PLL2_AC_WAIT_CTRL

The PLL2_AC_WAIT_CTRL Register sets the Amplitude Calibration Wait Periods. Back to Register Map.

Table 152. Register - 0x83

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	PLL2_AC_CMP_WAIT[3:0]	RW	0x0	PLL2 VCO Amplitude Calibration Delay between IDAC Code Changes. Delay is equal to PLL2_AC_CMP_WAIT*4*Clock Period (Clock Period 100ns).
[3:0]	PLL2_AC_INIT_WAIT[3:0]	RW	0x0	PLL2 VCO Amplitude Calibration Initial Comparator Delay. Delay is equal to PLL2_AC_INIT_WAIT*4*Clock Period.

9.6.2.129 PLL2_AC_JUMPSTEP

The PLL2_AC_JUMPSTEP Register provides control of the PLL2 Amplitude Calibration step size. Back to Register Map.

Table 153. Register - 0x84

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.
[3:0]	PLL2_AC_JUMP_STEP[3:0]	RW	0xF	PLL2 IDAC Code Jump Step. When PLL2_FAST_ACAL is 1 then the IDACSET step value is set by PLL2_AC_JUMP_STEP.

9.6.2.130 PLL2_LD_WNDW_SIZE

The PLL2_LD_WNDW_SIZE Register sets the PLL2 Window Comparator Setting. Back to Register Map.

Table 154. Register - 0x85

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LD_WNDW_SIZE[7:0]	RW	0x1	PLL2 Window Comparator Size Setting. PLL2 Window comparator size after PLL2 AC Calibration and initial lock. Always set to 0. 0: 1 ns. 1 to 255: Reserved

9.6.2.131 PLL2_LD_WNDW_SIZE_INITIAL

The PLL2_LD_WNDW_SIZE_INITIAL Register sets the PLL2 Window Comparator Initial Setting. Back to Register Map.

Table 155. Register - 0x86

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LD_WNDW_SIZE_INITIAL[7:0]	RW	0x7F	PLL2 Window Comparator Size Initial Setting. Window comparator size prior to PLL2 AC Calibration and initial lock. Always set to 0. 0: 1 ns. 1 to 255: Reserved

9.6.2.132 PLL2_LOCKDET_CYC_CNT_BY2

The PLL2 Lock Detection Cycle Count is set by PLL2_LOCKDET_CYC_CNT_BY2, PLL2_LOCKDET_CYC_CNT_BY1 and PLL2_LOCKDET_CYC_CNT_BY0. Back to Register Map.

Table 156. Register - 0x87

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT[23:16]	RW	0x0	PLL2 Lock detection cycle counter.

9.6.2.133 PLL2_LOCKDET_CYC_CNT_BY1

The PLL2_LOCKDET_CYC_CNT_BY1 Register sets bits [15:8] Back to Register Map.

Table 157. Register - 0x88

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT[15:8]	RW	0x40	PLL2 Lock detection cycle counter.

9.6.2.134 PLL2_LOCKDET_CYC_CNT_BY0

The PLL2_LOCKDET_CYC_CNT_BY0 Register sets bits [7:0] Back to Register Map.

Table 158. Register - 0x89

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT[7:0]	RW	0x0	PLL2 Lock detection cycle counter.

9.6.2.135 PLL2_LOCKDET_CYC_CNT_INITIAL_BY2

The PLL2 Lock Detection Initial Cycle Count is set by PLL2_LOCKDET_CYC_CNT_INITIAL_BY2, PLL2_LOCKDET_CYC_CNT_INITIAL_BY1 and PLL2_LOCKDET_CYC_CNT_INITIAL_BY0. This counter is used for initial PLL2 Lock before final Amplitude Calibration has finished. Back to Register Map.

Table 159. Register - 0x8A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT_INITIAL[23:16]	RW	0x0	PLL2 Lock detection initial cycle counter.

9.6.2.136 PLL2_LOCKDET_CYC_CNT_INITIAL_BY1

The PLL2_LOCKDET_CYC_CNT_INITIAL_BY1 Register sets bits [15:8] Back to Register Map.

Table 160. Register - 0x8B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT_INITIAL[15:8]	RW	0x40	PLL2 Lock detection initial cycle counter.

9.6.2.137 PLL2_LOCKDET_CYC_CNT_INITIAL_BY0

The PLL2_LOCKDET_CYC_CNT_INITIAL_BY0 Register sets bits [7:0] Back to Register Map.

Table 161. Register - 0x8C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	PLL2_LOCKDET_CYC_CNT_INITIAL[7:0]	RW	0x0	PLL2 Lock detection initial cycle counter.

9.6.2.138 IOCTRL_SPI0

The IOCTRL_SPI0 Register provides control of the SDIO Input/Output Driver. Back to Register Map.

Table 162. Register - 0x8D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SPI_EN_THREE_WIRE_IF	RW	0	SPI 3-Wire Selection. 1=3-Wire, 0=4-Wire. When configured for 4 wire operation the SDO output is connected to the STATUS1 output pad.
[6:5]	RSRVD	-	-	Reserved.
[4]	SPI_SDIO_OUTPUT_MUTE	RW	0	SDIO Output Mute. When SPI_SDIO_OUTPUT_MUTE is 1 the SDIO output driver is forced to 0 if it is enabled.
[3]	SPI_SDIO_OUTPUT_INV	RW	0	SDIO Output Invert. When SPI_SDIO_OUTPUT_INV is 1 the SDIO output is inverted.
[2]	SPI_SDIO_OUTPUT_WEAK_DRIVE	RW	0	SDIO Output Weak Drive Strength. When SPI_SDIO_OUTPUT_WEAK DRIVE is 1 the SDIO output is configured with a low slew rate.
[1]	SPI_SDIO_EN_PULLUP	RW	0	SPI SDIO Pull Up Enable. When SPI_SDIO_PULLUP_EN is 1 a pullup resistor is activated.
[0]	SPI_SDIO_EN_PULLDOWN	RW	0	SPI SDIO Pull Down Enable. When SPI_SDIO_PULLDWN_EN is 1 a pulldown resistor is activated.

9.6.2.139 IOCTRL_SPI1

The IOCTRL_SPI1 Register provides control of the SCL and SCS input drivers. Back to Register Map.

Table 163. Register - 0x8E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.
[3]	SPI_SCL_EN_PULLUP	RW	0	SPI SCL Pull Up Enable. When SPI_SCL_PULLUP_EN is 1 a pullup resistor is activated.
[2]	SPI_SCL_EN_PULLDOWN	RW	0	SPI SCL Pull Down Enable. When SPI_SCL_PULLDWN_EN is 1 a pulldown resistor is activated.
[1]	SPI_SCS_EN_PULLUP	RW	0	SPI SCS Pull Up Enable. When SPI_SCS_PULLUP_EN is 1 a pullup resistor is activated.
[0]	SPI_SCS_EN_PULLDOWN	RW	0	SPI SCS Pull Down Enable. When SPI_SCS_PULLDWNEN_EN is 1 a pulldown resistor is activated.

9.6.2.140 IOTEST_SDIO

The IOTEST_SDIO Register provides control of the SDIO driver and test features. Back to Register Map.

Table 164. Register - 0x8F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	0	Reserved.
[6]	SPI_SDIO_OUTPUT_HIZ	RW	1	SPI SDIO Output Driver High Impedance. When SPI_SDIO_OUTPUT_HIZ is set to 1 the SDIO output driver stage is disabled. Only when SPI_SDIO_IOTESTEN is 1.
[5]	SPI_SDIO_ENB_INSTAGE	RW	0	SPI SDIO Input Stage Enable BAR. When SPI_SDIO_INPUT_ENB is 0 the SDIO Input stage is enabled. Whenever SPI_SDIO_INPUT_ENB is set to 1 the SPI interface is rendered inoperable and can only be recovered by a hardware reset.
[4]	SPI_SDIO_EN_ML_INSTAGE	RW	0	SPI SDIO Input Stage Enable Multi-level. When SPI_SDIO_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3]	RSRVD	-	0	Reserved.

Table 164. Register - 0x8F (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[2]	SPI_SDIO_OUTPUT_DATA	RW	0	SPI SDIO Output Data. Controls the SDIO output data value when SPI_SDIO_IOTESTEN is set to 1.
[1]	SPI_SDIO_INPUT_Y12	R	0	SPI SDIO Input Y12 Value. Indicates the logic level present on the SDIO Y12 pin. This feature is currently not supported.
[0]	SPI_SDIO_INPUT_M12	R	0	SPI SDIO Input M12 Value. Indicates the logic level present on the SDIO M12 pin. This feature is currently not supported.

9.6.2.141 IOTEST_SCL

The IOTEST_SCL Register provides control of the SCL driver and test features. Back to Register Map.

Table 165. Register - 0x90

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	SPI_SCL_ENB_INSTAGE	RW	0	SPI SCL Input Stage Enable BAR. When SPI_SCL_INPUT_ENB is 0 the SCL Input stage is enabled. Whenever SPI_SCL_INPUT_ENB is set to 1 the SPI interface is rendered inoperable and can only be recovered by a hardware reset.
[4]	SPI_SCL_EN_ML_INSTAGE	RW	0	SPI SCL Input Stage Enable Multi-level. When SPI_SCL_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3:2]	RSRVD	-	-	Reserved.
[1]	SPI_SCL_INPUT_Y12	R	0	SPI SCL Input Y12 Value. Indicates the logic level present on the SCL Y12 pin. This feature is currently not supported.
[0]	SPI_SCL_INPUT_M12	R	0	SPI SCL Input M12 Value. Indicates the logic level present on the SCL M12 pin. This feature is currently not supported.

9.6.2.142 IOTEST_SCS

The IOTEST_SCS Register provides control of the SCS driver and test features. Back to Register Map.

Table 166. Register - 0x91

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	SPI_SCS_ENB_INSTAGE	RW	0	SPI SCS Input Stage Enable BAR. When SPI_SCS_INPUT_ENB is 0 the SCS Input stage is enabled. Whenever SPI_SCS_INPUT_ENB is set to 1 the SPI interface is rendered inoperable and can only be recovered by a hardware reset.
[4]	SPI_SCS_EN_ML_INSTAGE	RW	0	SPI SCS Input Stage Enable Multi-level. When SPI_SCS_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3:2]	RSRVD	-	-	Reserved.
[1]	SPI_SCS_INPUT_Y12	R	0	SPI SCS Input Y12 Value. Indicates the logic level present on the SCS Y12 pin. This feature is currently not supported.
[0]	SPI_SCS_INPUT_M12	R	0	SPI SCS Input M12 Value. Indicates the logic level present on the SCS M12 pin. This feature is currently not supported.

9.6.2.143 IOCTRL_STAT0

The IOCTRL_STAT0 Register provides control of the STATUS0 Input/Output Driver. Back to Register Map.

Table 167. Register - 0x92

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	STATUS0_MUX_SEL[2:0]	RW	0x4	STAT0 Output Mux Select. When selecting PLL1 or 2 REF/FB clock, also set corresponding PLLx_TSTMODE_REF_FB_EN bit. STATUS0_MUX_SEL - STATUS0 Output 000 - PLL1 REF CLK 001 - PLL2 REF CLK 010 - PLL1 FB (SYS) CLK 011 - PLL2 FB (SYS) CLK 1XX - Signal selected by STATUS0_INT_MUX (digital)
[4]	STATUS0_OUTPUT_MUTE	RW	0	STATUS0 Output Mute. When STATUS0_OUTPUT_MUTE is 1 the STATUS0 output driver is forced to 0 if it is enabled.
[3]	STATUS0_OUTPUT_INV	RW	0	STATUS0 Output Invert. When STATUS0_OUTPUT_INV is 1 the STATUS0 output is inverted.
[2]	STATUS0_OUTPUT_WEAK_DRIVE	RW	0	STATUS0 Output Weak drivestrength. When STATUS0_OUTPUT_WEAK DRIVE is 1 the STATUS0 output is configured with a lower slew rate.
[1]	STATUS0_EN_PULLUP	RW	0	STATUS0 Pull Up Enable. When STATUS0_PULLUPEN_EN is 1 a pullup resistor is activated.
[0]	STATUS0_EN_PULLDOWN	RW	0	STATUS0 Pull Down Enable. When STATUS0_PULLDWN_EN is 1 a pulldown resistor is activated.

9.6.2.144 IOCTRL_STAT1

The IOCTRL_STAT1 Register provides control of the STATUS1 Input/Output Driver. Back to Register Map.

Table 168. Register - 0x93

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	STATUS1_MUX_SEL[2:0]	RW	0x4	STAT1 Output Mux Select. When selecting PLL1 or 2 REF/FB clock, also set corresponding PLLx_TSTMODE_REF_FB_EN bit. STATUS1_MUX_SEL - STATUS1 Output 000 - PLL1 REF CLK 001 - PLL2 REF CLK 010 - PLL1 FB (SYS) CLK 011 - PLL2 FB (SYS) CLK 1XX - Signal selected by STATUS1_INT_MUX (digital)
[4]	STATUS1_OUTPUT_MUTE	RW	0	STATUS1 Output Mute. When STATUS1_OUTPUT_MUTE is 1 the STATUS1 output driver is forced to 0 if it is enabled.
[3]	STATUS1_OUTPUT_INV	RW	0	STATUS1 Output Invert. When STATUS1_OUTPUT_INV is 1 the STATUS1 output is inverted.
[2]	STATUS1_OUTPUT_WEAK_DRIVE	RW	0	STATUS1 Output weak drive. When STATUS1_OUTPUT_WEAK_DRIVE is 1 the STATUS1 output is configured with a lower slew rate.
[1]	STATUS1_EN_PULLUP	RW	0	STATUS1 Pull Up Enable. When STATUS1_PULLUP_EN is 1 a pullup resistor is activated.
[0]	STATUS1_EN_PULLDOWN	RW	0	STATUS1 Pull Down Enable. When STATUS1_PULLDWN_EN is 1 a pulldown resistor is activated.

9.6.2.145 STAT1MUX

The STAT1MUX Register controls the status signal that is routed to the STATUS0 output. Back to Register Map.

Table 169. Register - 0x94

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	STATUS1_INT_MUX[7:0]	RW	0x4	STAT1 Integrated Mux Select. STAT1_INT_MUX - STATUS1 Output 0 - PLL1 Lock Detect and PLL2 Lock Detect 1 - PLL1 Lock Detect 2 - PLL2 Lock Detect 3 - CLKINBLK LOS 4 - SPI Output Data 5 - Reserved 6 - Reserved 7 - Reserved 8 - HOLDOVER_EN 9 - Mirror of SYNC_INPUT 10 - Mirror of CLKINSEL1 INPUT 11 - Reserved 12 - Reserved 13 - PLL2 Reference Clock 14 - Reserved 15 - PLL1 Lock Detect and PLL2 Lock Detect and not PLL1 Holdover 16 - PLL1 Lock Detect and not PLL1 Holdover 17 - Logic 1 18 - Logic 0

9.6.2.146 STAT0MUX

The STAT0MUX Register controls the status signal that is routed to the STATUS1 output. Back to Register Map.

Table 170. Register - 0x95

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	STATUS0_INT_MUX[7:0]	RW	0x0	STAT0 Integrated Mux Select. STAT0_INT_MUX - STATUS0 Output 0 - PLL1 Lock Detect and PLL2 Lock Detect 1 - PLL1 Lock Detect 2 - PLL2 Lock Detect 3 - CLKINBLK LOS 4 - SPI Output Data 5 - Reserved 6 - Reserved 7 - Reserved 8 - HOLDOVER_EN 9 - Mirror of SYNC_INPUT 10 - Mirror of CLKINSEL1 INPUT 11 - Reserved 12 - Reserved 13 - PLL2 Reference Clock 14 - Reserved 15 - PLL1 Lock Detect and PLL2 Lock Detect and not PLL1 Holdover 16 - PLL1 Lock Detect and not PLL1 Holdover 17 - Logic 1 18 - Logic 0

9.6.2.147 STATPLL2CLKDIV

The STATPLL2CLKDIV Register controls the PLL2 Status Output Clock Divider Back to Register Map.

Table 171. Register - 0x96

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	PLL2_REF_CLK_EN	RW	1	PLL2 Ref Clock Enable.
[3]	RSRVD	-	-	Reserved.
[2:0]	PLL2_REF_STATCLK_DIV[2:0]	RW	0x0	PLL2 Ref Clock Divider for Status Outputs. Sets the divider value for the PLL2 VCO clock that can be routed to the STAT0/1 outputs. PLL2_REF_STATCLK_DIV - Divider Value 0 - 1 1 - 2 .. - .. 7 - 8

9.6.2.148 IOTEST_STAT0

The IOTEST_STAT0 Register provides control of the STATUS0 driver and test features. Back to Register Map.

Table 172. Register - 0x97

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	STATUS0_OUTPUT_HIZ	RW	0	STATUS0 Output Driver High Impedance. When STATUS0_OUTPUT_HIZ is set to 1 the STATUS0 output driver stage is disabled.
[5]	STATUS0_ENB_INSTAGE	RW	1	STATUS0 Input Stage Enable BAR. When STATUS0_INPUT_ENB is 0 the STATUS0 Input stage is enabled. When STATUS0_INPUT_ENB is set to 1 the STATUS0 input stage is disabled.
[4]	STATUS0_EN_ML_INSTAGE	RW	0	STATUS0 Input Stage Enable Multi-level. When STATUS0_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3]	RSRVD	-	-	Reserved.
[2]	STATUS0_OUTPUT_DATA	RW	0	STATUS0 Output Data. Set the STATUS0 output data value when STATUS0_IOTESTEN is 1.
[1]	STATUS0_INPUT_Y12	R	0	STATUS0 Input Y12 Value. Indicates the logic level present on the STATUS0 Y12 pin.
[0]	STATUS0_INPUT_M12	R	0	STATUS0 Input M12 Value. Indicates the logic level present on the STATUS0 M12 pin.

9.6.2.149 IOTEST_STAT1

The IOTEST_STAT1 Register provides control of the STATUS1 driver and test features. Back to Register Map.

Table 173. Register - 0x98

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	STATUS1_OUTPUT_HIZ	RW	0	STATUS1 Output Driver High Impedance. When STATUS1_OUTPUT_HIZ is set to 1 the STATUS1 output driver stage is disabled.
[5]	STATUS1_ENB_INSTAGE	RW	1	STATUS1 Input Stage Enable BAR. When STATUS1_INPUT_ENB is 0 the STATUS1 Input stage is enabled. When STATUS1_INPUT_ENB is set to 1 the STATUS1 input stage is disabled.

Table 173. Register - 0x98 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[4]	STATUS1_EN_ML_INSTAGE	RW	0	STATUS1 Input Stage Enable Multi-level. When STATUS1_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3]	RSRVD	-	-	Reserved.
[2]	STATUS1_OUTPUT_DATA	RW	0	STATUS1 Output Data. Set the STATUS1 output data value when STATUS1_IOTESTEN is 1.
[1]	STATUS1_INPUT_Y12	R	0	STATUS1 Input Y12 Value. Indicates the logic level present on the STATUS1 Y12 (high-level) pin.
[0]	STATUS1_INPUT_M12	R	0	STATUS1 Input M12 Value. Indicates the logic level present on the STATUS1 M12 (mid-level) pin.

9.6.2.150 IOCTRL_SYNC

The IOCTRL_SYNC Register provides control of the SYNC Input. Back to Register Map.

Table 174. Register - 0x99

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	SYNC_MUX_SEL[2:0]	RW	0x4	SYNC Output Mux Select. When selecting PLL1 or 2 REF/FB clock, also set corresponding PLLx_TSTMODE_REF_FB_EN bit. SYNC_MUX_SEL - SYNC Output 000 - PLL1 REF CLK 001 - PLL2 REF CLK 010 - PLL1 FB (SYS) CLK 011 - PLL2 FB (SYS) CLK 1XX - Signal selected by SYNC_INT_MUX (digital)
[4]	SYNC_OUTPUT_MUTE	RW	0	SYNC Output Mute. When SYNC_OUTPUT_MUTE is 1 the SYNC output driver is forced to 0 if it is enabled.
[3]	SYNC_OUTPUT_INV	RW	0	SYNC Output Invert. When SYNC_OUTPUT_INV is 1 the SYNC output is inverted.
[2]	SYNC_OUTPUT_WEAK_DRIVE	RW	0	SYNC Output weak drive. When SYNC_OUTPUT_WEAK_DRIVE is 1 the SYNC output is configured with a lower slew rate.
[1]	SYNC_EN_PULLUP	RW	0	SYNC Pull Up Enable. When SYNC_PULLUPEN_EN is 1 a pullup resistor is activated.
[0]	SYNC_EN_PULLDOWN	RW	0	SYNC Pull Down Enable. When SYNC_PULLDWN_EN is 1 a pulldown resistor is activated.

9.6.2.151 DUMMY_REGISTER_1

Placeholder 1. Back to Register Map.

Table 175. Register - 0x9A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	RSRVD	-	-	Reserved.

9.6.2.152 IOCTRL_CLKINSEL1

The IOCTRL_CLKINSEL1 Register provides control of the CLKINSEL1 Input. Back to Register Map.

Table 176. Register - 0x9B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	RSRVD	-	-	Reserved.
[1]	CLKINSEL1_EN_PULLUP	RW	0	CLKIN_SEL1 Pull Up Enable. When CLKINSEL1_PULLUP_EN is 1 a pullup resistor is activated.

Table 176. Register - 0x9B (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[0]	CLKINSEL1_EN_PULLDOWN	RW	0	CLKIN_SEL1 Pull Down Enable. When CLKINSEL1_PULLDWN_EN is 1 a pulldown resistor is activated.

9.6.2.153 IOTEST_CLKINSEL1

The IOTEST_CLKINSEL1 Register provides control of the CLKINSEL1 driver test features. Back to Register Map.

Table 177. Register - 0x9C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	CLKINSEL1_ENB_INSTAGE	RW	0	CLKINSEL1 Input Stage Enable BAR. When CLKINSEL1_INPUT_ENB is 0 the CLKINSEL1 Input stage is enabled.
[4]	CLKINSEL1_EN_ML_INSTAGE	RW	0	CLKINSEL1 Input Stage Enable Multi-level. When CLKINSEL1_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3:2]	RSRVD	-	-	Reserved.
[1]	CLKINSEL1_INPUT_Y12	R	0	CLKINSEL1 Input Y12 Value. Indicates the logic level present on the CLKINSEL1 Y12 (high-level) pin.
[0]	CLKINSEL1_INPUT_M12	R	0	CLKINSEL1 Input M12 Value. Indicates the logic level present on the CLKINSEL1 M12 (mid-level) pin.

9.6.2.154 PLL1_TSTMODE

The PLL1_TSTMODE Register supports PLL1 Test by enabling output of PLL1 phase detector inputs.Back to Register Map.

Table 178. Register - 0xAC

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	PLL1_TSTMODE_REF_FB_EN	RW	0	Set this bit when STATUS0_MUX_SEL, STATUS1_MUX_SEL, or SYNC_MUX_SEL selects a PLL1 REF clock or FB (SYS) clock output. 0: PLL1 REF or PLL1 FB (SYS) clock not selected by any mux 1: PLL1 REF or PLL1 FB (SYS) clock selected by at least one mux
[6:0]	RSRVD	RW	0	Reserved.

9.6.2.155 PLL2_CTRL

The PLL2_CTRL Register supports other PLL2 features. Back to Register Map.

Table 179. Register - 0xAD

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5:4]	RESET_PLL2_DLD	RW	0	Before using PLL2 DLD signal, set this field to 0x3, wait 20 ms, set to 0x0. Refer to PLL2 DLD flow chart in Figure 40. 0x0: Clear reset state 0x1: Reserved 0x2: Reserved 0x3: Reset set
[3]	RSRVD	-	-	Reserved.

Table 179. Register - 0xAD (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[2]	PLL2_TSTMODE_REF_FB_EN	RW	0	Set this bit when STATUS0_MUX_SEL, STATUS1_MUX_SEL, or SYNC_MUX_SEL selects a PLL1 REF clock or FB (SYS) clock output. 0: PLL1 REF or PLL1 FB (SYS) clock not selected by any mux 1: PLL1 REF or PLL1 FB (SYS) clock selected by at least one mux
[1:0]	PD_VCO_LDO	RW	0	Set for modes not using PLL2 VCO. 0x0: VCO LDO active 0x1: Reserved 0x2: Reserved 0x3: VCO LDO disabled

9.6.2.156 PLL2_RDIV_CLKEN

The PLL2_RDIV_CLKEN Register supports PLL2 R-Divider enable. Back to Register Map.

Table 180. Register - 0xAF

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	PLL2_RDIV_CLKEN	RW	0	PLL2 R-Divider Clock Enable.

9.6.2.157 PLL2_NDIV_CLKEN

The PLL2_NDIV_CLKEN Register supports PLL2 N-Divider enable. Back to Register Map.

Table 181. Register - 0xB0

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:1]	RSRVD	-	-	Reserved.
[0]	PLL2_NDIV_CLKEN	RW	1	PLL2 N-Divider Clock Enable.

9.6.2.158 STATUS

The STATUS Register provides access to the following status signals. Back to Register Map.

Table 182. Register - 0xBE

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5]	LOS	R	0	Loss of Source
[4]	HOLDOVER_DLD	R	0	Holdover - Digital Lock Detect
[3]	HOLDOVER_LOL	R	0	Holdover - Loss of Lock
[2]	HOLDOVER_LOS	R	0	Holdover - Loss of Source
[1]	PLL2_LCK_DET	R	0	PLL2 Lock Detect
[0]	PLL1_LCK_DET	R	0	PLL1 Lock Detect

9.6.2.159 PLL2_DLD_EN

The PLL2_DLD_EN Register supports PLL2 DLD EN Feature Back to Register Map.

Table 183. Register - 0xF6

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:2]	RSRVD	RW	0	Reserved
[1]	PLL2_DLD_EN	RW	0	Enable for PLL2 DLD 0: Non PLL2 modes 1: PLL2 DLD enabled

Table 183. Register - 0xF6 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[0]	RSRVD	FW	0	Reserved

9.6.2.160 PLL2_DUAL_LOOP

The PLL2_DUAL_LOOP Register supports Dual Loop Feature Back to Register Map.

Table 184. Register - 0xF7

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	R	0	Reserved.
[6:5]	PLL2_DUAL_LOOP_EN	RW	0	Dual Loop enable 0x0: Non-Dual Loop mode 0x1: Reserved 0x2: Reserved 0x3: Dual Loop mode
[4:0]	RSRVD	RW	0	Reserved.

9.6.2.161 CH01_DDLY_BY0

Register CH01_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 185. Register - 0xFD

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH01_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.162 CH23_DDLY_BY0

Register CH23_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 186. Register - 0xFF

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH23_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.163 CH45_DDLY_BY0

Register CH45_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 187. Register - 0x101

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH45_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.164 CH67_DDLY_BY0

Register CH67_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 188. Register - 0x103

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH67_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.165 CH89_DDLY_BY0

Register CH89_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 189. Register - 0x105

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH89_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.166 CH1011_DDLY_BY0

Register CH1011_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 190. Register - 0x107

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH1011_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.167 CH1213_DDLY_BY0

Register CH1213_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 191. Register - 0x109

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH1213_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.168 CH1415_DDLY_BY0

Register CH1415_DDLY_BY0 provides control of the following JESD204B control signals Back to Register Map.

Table 192. Register - 0x10B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	CH1415_DDLY[7:0]	RW	0x0	Sets number of Digital Delay steps for Channel X. The channel delays 0 to 255 Clock Distribution Path periods compared to other channels.

9.6.2.169 OUTCH0_JESD_CTRL

Register OUTCH0_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 193. Register - 0x10C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH0_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH0_ADLY_EN	RW	0	Enables Analog Delay for Channel 0.
[0]	RSRVD	-	-	Reserved.

9.6.2.170 OUTCH1_JESD_CTRL

Register OUTCH1_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 194. Register - 0x10D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH1_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH1_ADLY_EN	RW	0	Enables Analog Delay for Channel 1.
[0]	RSRVD	-	-	Reserved.

9.6.2.171 OUTCH2_JESD_CTRL

Register OUTCH2_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 195. Register - 0x10E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH2_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH2_ADLY_EN	RW	0	Enables Analog Delay for Channel 2.
[0]	RSRVD	-	-	Reserved.

9.6.2.172 OUTCH3_JESD_CTRL

Register OUTCH3_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 196. Register - 0x10F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH3_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH3_ADLY_EN	RW	0	Enables Analog Delay for Channel 3.
[0]	RSRVD	-	-	Reserved.

9.6.2.173 OUTCH4_JESD_CTRL

Register OUTCH4_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 197. Register - 0x110

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH4_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH4_ADLY_EN	RW	0	Enables Analog Delay for Channel 4.
[0]	RSRVD	-	-	Reserved.

9.6.2.174 OUTCH5_JESD_CTRL

Register OUTCH5_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 198. Register - 0x111

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH5_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH5_ADLY_EN	RW	0	Enables Analog Delay for Channel 5.
[0]	RSRVD	-	-	Reserved.

9.6.2.175 OUTCH6_JESD_CTRL

Register OUTCH6_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 199. Register - 0x112

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH6_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH6_ADLY_EN	RW	0	Enables Analog Delay for Channel 6.
[0]	RSRVD	-	-	Reserved.

9.6.2.176 OUTCH7_JESD_CTRL

Register OUTCH7_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 200. Register - 0x113

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH7_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH7_ADLY_EN	RW	0	Enables Analog Delay for Channel 7.
[0]	RSRVD	-	-	Reserved.

9.6.2.177 OUTCH8_JESD_CTRL

Register OUTCH8_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 201. Register - 0x114

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH8_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH8_ADLY_EN	RW	0	Enables Analog Delay for Channel 8.
[0]	RSRVD	-	-	Reserved.

9.6.2.178 OUTCH9_JESD_CTRL

Register OUTCH9_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 202. Register - 0x115

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH9_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH9_ADLY_EN	RW	0	Enables Analog Delay for Channel 9.
[0]	RSRVD	-	-	Reserved.

9.6.2.179 OUTCH10_JESD_CTRL

Register OUTCH10_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 203. Register - 0x116

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH10_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH10_ADLY_EN	RW	0	Enables Analog Delay for Channel 10.
[0]	RSRVD	-	-	Reserved.

9.6.2.180 OUTCH11_JESD_CTRL

Register OUTCH11_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 204. Register - 0x117

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH11_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH11_ADLY_EN	RW	0	Enables Analog Delay for Channel 11.
[0]	RSRVD	-	-	Reserved.

9.6.2.181 OUTCH12_JESD_CTRL

Register OUTCH12_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 205. Register - 0x118

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH12_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH12_ADLY_EN	RW	0	Enables Analog Delay for Channel 12.
[0]	RSRVD	-	-	Reserved.

9.6.2.182 OUTCH13_JESD_CTRL

Register OUTCH13_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 206. Register - 0x119

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH13_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH13_ADLY_EN	RW	0	Enables Analog Delay for Channel 13.
[0]	RSRVD	-	-	Reserved.

9.6.2.183 OUTCH14_JESD_CTRL

Register OUTCH14_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 207. Register - 0x11A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH14_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH14_ADLY_EN	RW	0	Enables Analog Delay for Channel 14.
[0]	RSRVD	-	-	Reserved.

9.6.2.184 OUTCH15_JESD_CTRL

Register OUTCH15_JESD_CTRL provides control of the following JESD204B control signals Back to Register Map.

Table 208. Register - 0x11B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	CH15_ADLY[4:0]	RW	0x0	Analog Steps can be programmed from 0 to 15. The resulting delay is shown in Figure 34.
[1]	CH15_ADLY_EN	RW	0	Enables Analog Delay for Channel 15.
[0]	RSRVD	-	-	Reserved.

9.6.2.185 CLKMUXVECTOR

The CLKMUXVECTOR Register reflects the current status of the RefClk Mux Back to Register Map.

Table 209. Register - 0x124

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.
[3:0]	CLKMUX[3:0]	R	0x0	CLKmux status.

9.6.2.186 OUTCH01CNTL2

The OUTCH01CNTRL2 Register controls Output CH0_1 Back to Register Map.

Table 210. Register - 0x127

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH0_1	RW	0	Bypass CH0_1 Dynamic Digital Delay Gating

Table 210. Register - 0x127 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH0_1	RW	0	Bypass CH0_1 Analog Delay Gating
[5]	SYNC_EN_CH0_1	RW	0	Output CH0_1 SYNC Enable
[4]	HS_EN_CH0_1	RW	0	Output CH0_1 Enable Half-cycle delay
[3:2]	DRIV_1_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH1.
[1:0]	DRIV_0_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH0.

9.6.2.187 OUTCH23CNTL2

The OUTCH23CNTRL2 Register controls Output CH2_3 Back to Register Map.

Table 211. Register - 0x128

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH2_3	RW	0	Bypass CH2_3 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH2_3	RW	0	Bypass CH2_3 Analog Delay Gating
[5]	SYNC_EN_CH2_3	RW	0	Output CH2_3 SYNC Enable
[4]	HS_EN_CH2_3	RW	0	Output CH2_3 Enable Half-cycle delay
[3:2]	DRIV_3_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH3.
[1:0]	DRIV_2_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH2.

9.6.2.188 OUTCH45CNTL2

The OUTCH45CNTRL2 Register controls Output CH4_5 Back to Register Map.

Table 212. Register - 0x129

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH4_5	RW	0	Bypass CH4_5 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH4_5	RW	0	Bypass CH4_5 Analog Delay Gating
[5]	SYNC_EN_CH4_5	RW	0	Output CH4_5 SYNC Enable
[4]	HS_EN_CH4_5	RW	0	Output CH4_5 Enable Half-cycle delay
[3:2]	DRIV_5_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH5.
[1:0]	DRIV_4_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH4.

9.6.2.189 OUTCH67CNTL2

The OUTCH67CNTRL2 Register controls Output CH6_7 Back to Register Map.

Table 213. Register - 0x12A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH6_7	RW	0	Bypass CH6_7 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH6_7	RW	0	Bypass CH6_7 Analog Delay Gating
[5]	SYNC_EN_CH6_7	RW	0	Output CH6_7 SYNC Enable
[4]	HS_EN_CH6_7	RW	0	Output CH6_7 Enable Half-cycle delay
[3:2]	DRIV_7_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH7.
[1:0]	DRIV_6_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH6.

9.6.2.190 OUTCH89CNTL2

The OUTCH89CNTRL2 Register controls Output CH8_9 Back to Register Map.

Table 214. Register - 0x12B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH8_9	RW	0	Bypass CH8_9 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH8_9	RW	0	Bypass CH8_9 Analog Delay Gating
[5]	SYNC_EN_CH8_9	RW	0	Output CH8_9 SYNC Enable
[4]	HS_EN_CH8_9	RW	0	Output CH8_9 Enable Half-cycle delay
[3:2]	DRIV_9_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH9.
[1:0]	DRIV_8_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH8.

9.6.2.191 OUTCH1011CNTL2

The OUTCH1011CNTRL2 Register controls Output CH10_11 Back to Register Map.

Table 215. Register - 0x12C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH10_11	RW	0	Bypass CH10_11 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH10_11	RW	0	Bypass CH10_11 Analog Delay Gating
[5]	SYNC_EN_CH10_11	RW	0	Output CH10_11 SYNC Enable
[4]	HS_EN_CH10_11	RW	0	Output CH10_11 Enable Half-cycle delay
[3:2]	DRIV_11_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH11.
[1:0]	DRIV_10_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH10.

9.6.2.192 OUTCH1213CNTL2

The OUTCH1213CNTRL2 Register controls Output CH12_13 Back to Register Map.

Table 216. Register - 0x12D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH12_13	RW	0	Bypass CH12_13 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH12_13	RW	0	Bypass CH12_13 Analog Delay Gating
[5]	SYNC_EN_CH12_13	RW	0	Output CH12_13 SYNC Enable
[4]	HS_EN_CH12_13	RW	0	Output CH12_13 Enable Half-cycle delay
[3:2]	DRIV_13_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH13.
[1:0]	DRIV_12_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH12.

9.6.2.193 OUTCH1415CNTL2

The OUTCH1415CNTRL2 Register controls Output CH14_15 Back to Register Map.

Table 217. Register - 0x12E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_BYP_DYNDIGDLY_GATING_CH14_15	RW	0	Bypass CH14_15 Dynamic Digital Delay Gating
[6]	SYSREF_BYP_ANALOGDLY_GATING_CH14_15	RW	0	Bypass CH14_15 Analog Delay Gating
[5]	SYNC_EN_CH14_15	RW	0	Output CH14_15 SYNC Enable

Table 217. Register - 0x12E (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[4]	HS_EN_CH14_15	RW	0	Output CH14_15 Enable Half-cycle delay
[3:2]	DRIV_15_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH15.
[1:0]	DRIV_14_SLEW[1:0]	RW	0x0	Slew Rate Setting OUTCH14.

9.6.2.194 OUTCH0_JESD_CTRL1

The OUTCH0_JESD_CTRL1 Register controls Output CH0 Back to Register Map.

Table 218. Register - 0x12F

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH0[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.195 OUTCH1_JESD_CTRL1

The OUTCH1_JESD_CTRL1 Register controls Output CH1 Back to Register Map.

Table 219. Register - 0x130

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH1[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.196 OUTCH2_JESD_CTRL1

The OUTCH2_JESD_CTRL1 Register controls Output CH2 Back to Register Map.

Table 220. Register - 0x131

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH2[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.197 OUTCH3_JESD_CTRL1

The OUTCH3_JESD_CTRL1 Register controls Output CH3 Back to Register Map.

Table 221. Register - 0x132

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH3[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.198 OUTCH4_JESD_CTRL1

The OUTCH4_JESD_CTRL1 Register controls Output CH4 Back to Register Map.

Table 222. Register - 0x133

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH4[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.199 OUTCH5_JESD_CTRL1

The OUTCH5_JESD_CTRL1 Register controls Output CH5 Back to Register Map.

Table 223. Register - 0x134

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH5[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.200 OUTCH6_JESD_CTRL1

The OUTCH6_JESD_CTRL1 Register controls Output CH6 Back to Register Map.

Table 224. Register - 0x135

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH6[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.201 OUTCH7_JESD_CTRL1

The OUTCH7_JESD_CTRL1 Register controls Output CH7 Back to Register Map.

Table 225. Register - 0x136

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH7[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.202 OUTCH8_JESD_CTRL1

The OUTCH8_JESD_CTRL1 Register controls Output CH8 Back to Register Map.

Table 226. Register - 0x137

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH8[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.203 OUTCH9_JESD_CTRL1

The OUTCH9_JESD_CTRL1 Register controls Output CH9 Back to Register Map.

Table 227. Register - 0x138

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH9[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.204 OUTCH10_JESD_CTRL1

The OUTCH10_JESD_CTRL1 Register controls Output CH10 Back to Register Map.

Table 228. Register - 0x139

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH10[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.205 OUTCH11_JESD_CTRL1

The OUTCH11_JESD_CTRL1 Register controls Output CH11 Back to Register Map.

Table 229. Register - 0x13A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH11[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.206 OUTCH12_JESD_CTRL1

The OUTCH12_JESD_CTRL1 Register controls Output CH12 Back to Register Map.

Table 230. Register - 0x13B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH12[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.207 OUTCH13_JESD_CTRL1

The OUTCH13_JESD_CTRL1 Register controls Output CH13 Back to Register Map.

Table 231. Register - 0x13C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH13[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.208 OUTCH14_JESD_CTRL1

The OUTCH14_JESD_CTRL1 Register controls Output CH14 Back to Register Map.

Table 232. Register - 0x13D

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH14[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.209 OUTCH15_JESD_CTRL1

The OUTCH15_JESD_CTRL1 Register controls Output CH15 Back to Register Map.

Table 233. Register - 0x13E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:3]	RSRVD	-	-	Reserved.
[2:0]	DYN_DDLY_CH15[2:0]	RW	0x0	Sets number of Dynamic Digital Delay steps for Output X. The Output delays 0 to 5 Clock Distribution Path periods compared to other channels.

9.6.2.210 SYSREF_PLS_CNT

Sysref Pulse Count Configuration Back to Register Map.

Table 234. Register - 0x140

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:6]	RSRVD	-	-	Reserved.
[5:0]	OUTCH_SYSREF_PLSCNT[5:0]	RW	0x0	Set number of desired sysref pulses. 0 Enables continuous sysref.

9.6.2.211 SYNCMUX

The SYNCMUX Register controls the status signal that is routed to the SYNC output. Back to Register Map.

Table 235. Register - 0x141

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:0]	SYNC_INT_MUX[7:0]	RW	0x4	SYNC Integrated Mux Select. SYNC_INT_MUX - SYNC Output 0 - PLL1 Lock Detect and PLL2 Lock Detect 1 - PLL1 Lock Detect 2 - PLL2 Lock Detect 3 - CLKINBLK LOS 4 - SPI Output Data 5 - Reserved 6 - Reserved 7 - Reserved 8 - HOLDOVER_EN 9 - Mirror of SYNC_INPUT 10 - Mirror of CLKINSEL1 INPUT 11 - Reserved 12 - Reserved 13 - PLL2 Reference Clock 14 - Reserved 15 - PLL1 Lock Detect and PLL2 Lock Detect and not PLL1 Holdover 16 - PLL1 Lock Detect and not PLL1 Holdover 17 - Logic 1 18 - Logic 0

9.6.2.212 IOTEST_SYNC

The IOTEST_SYNC Register provides control of the SYNC driver and test features. Back to Register Map.

Table 236. Register - 0x142

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	SYNC_OUTPUT_HIZ	RW	1	SYNC Output Driver High Impedance. When SYNC_OUTPUT_HIZ is set to 1 the SYNC output driver stage is disabled.
[5]	SYNC_ENB_INSTAGE	RW	1	SYNC Input Stage Enable BAR. When SYNC_INPUT_ENB is 0 the SYNC Input stage is enabled. When SYNC_INPUT_ENB is set to 1 the SYNC input stage is disabled.
[4]	SYNC_EN_ML_INSTAGE	RW	1	SYNC Input Stage Enable Multi-level. When SYNC_INPUT_ENML is 1 the input stage is configured for multi-level mode.
[3]	RSRVD	-	-	Reserved.
[2]	SYNC_OUTPUT_DATA	RW	0	SYNC Output Data. Set the SYNC output data value when SYNC_IOTESTEN is 1.
[1]	SYNC_INPUT_Y12	R	0	SYNC Input Y12 Value. Indicates the logic level present on the SYNC Y12 pin.
[0]	SYNC_INPUT_M12	R	0	SYNC Input M12 Value. Indicates the logic level present on the SYNC M12 pin.

9.6.2.213 OUTCH_ZDM

Low Skew Feedback Buffer Settings Back to Register Map.

Table 237. Register - 0x143

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	FBBUF_CH6_EN	RW	0	Enable Channel 6 Zero Delay Mode FBClock Buffer
[3:1]	RSRVD	-	-	Reserved.
[0]	FBBUF_CH9_EN	RW	0	Enable Channel 9 Zero Delay Mode FBClock Buffer

9.6.2.214 PLL2_CTRL3

The PLL2_CTRL3 Register provides control of PLL2 features. Back to Register Map.

Table 238. Register - 0x146

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6]	PLL2_NBYPASS_DIV2_FB	RW	0	Enable By-2 Divider in PLL2 Feedback. nbypass_div2_fb - PLL2 Feedback by-2 Divider 0 - Divider Off 1 - Divider On
[5:2]	PLL2_PRESCALER[3:0]	RW	0x0	PLL2 VCO Prescaler Configuration. PLL2_PRESCALER - Effect 00XX - PLL2 VCO Prescaler DIV3 01XX - PLL2 VCO Prescaler DIV4 10XX - PLL2 VCO Prescaler DIV5 11XX - PLL2 VCO Prescaler DIV6
[1:0]	PLL2_FBDIV_MUXSEL[1:0]	RW	0x0	PLL2 Feedback MUX control. PLL2_FBDIV_MUXSEL - Effect 00 - Feedback Prescaler Output 01 - Feedback OUTCH9 Output (Zero Delay Mode) 10 - Feedback OUTCH6 Output (Zero Delay Mode)

9.6.2.215 PLL1_HOLDOVER_CTRL0

The PLL1_HOLDOVER_CTRL0 Register selects the GPIO pin to use to force Holdover mode. Back to Register Map.

Table 239. Register - 0x149

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.
[3]	PLL1_CLKINSEL1_ML_HOLDOVER	RW	0	Force holdover by applying mid-level at CLKINSEL1.
[2]	PLL1_SYNC_HOLDOVER	RW	0	Force holdover by applying high-level at SYNC.
[1]	PLL1_STATUS1_HOLDOVER	RW	0	Force holdover by applying high-level at STATUS1.
[0]	PLL1_STATUS0_HOLDOVER	RW	0	Force holdover by applying high-level at STATUS0.

9.6.2.216 IOCTRL_SYNC_1

The IOCTRL_SYNC_1 Register provides control of SYNC Input features. Back to Register Map.

Table 240. Register - 0x14A

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	RSRVD	-	-	Reserved.
[6:2]	SYNC_ANALOGDLY[4:0]	RW	0x0	SYNC input Analog Delay.
[1]	SYNC_ANALOGDLY_EN	RW	0	Enable Analog Delay at SYNC input.
[0]	SYNC_INV	RW	0	SYNC_IN Invert. SYNC_INV - Polarity 0 - Not inverted 1 - Inverted

9.6.2.217 OUTCH_TOP_JESD_CTRL

OUTCH_TOP_JESD_CTRL controls JESD functions for TOP output channels. Back to Register Map.

Table 241. Register - 0x14B

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	DYN_DDLY_CH15_EN	RW	0	Enable CH15 Dynamic Digital Delay.
[6]	DYN_DDLY_CH14_EN	RW	0	Enable CH14 Dynamic Digital Delay.
[5]	DYN_DDLY_CH13_EN	RW	0	Enable CH13 Dynamic Digital Delay.
[4]	DYN_DDLY_CH12_EN	RW	0	Enable CH12 Dynamic Digital Delay.
[3]	DYN_DDLY_CH11_EN	RW	0	Enable CH11 Dynamic Digital Delay.
[2]	DYN_DDLY_CH10_EN	RW	0	Enable CH10 Dynamic Digital Delay.
[1]	DYN_DDLY_CH9_EN	RW	0	Enable CH9 Dynamic Digital Delay.
[0]	DYN_DDLY_CH8_EN	RW	0	Enable CH8 Dynamic Digital Delay.

9.6.2.218 OUTCH_BOT_JESD_CTRL

OUTCH_BOT_JESD_CTRL controls JESD functions for BOTTOM output channels. Back to Register Map.

Table 242. Register - 0x14C

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	DYN_DDLY_CH7_EN	RW	0	Enable CH7 Dynamic Digital Delay.
[6]	DYN_DDLY_CH6_EN	RW	0	Enable CH6 Dynamic Digital Delay.
[5]	DYN_DDLY_CH5_EN	RW	0	Enable CH5 Dynamic Digital Delay.
[4]	DYN_DDLY_CH4_EN	RW	0	Enable CH4 Dynamic Digital Delay.

Table 242. Register - 0x14C (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[3]	DYN_DDLY_CH3_EN	RW	0	Enable CH3 Dynamic Digital Delay.
[2]	DYN_DDLY_CH2_EN	RW	0	Enable CH2 Dynamic Digital Delay.
[1]	DYN_DDLY_CH1_EN	RW	0	Enable CH1 Dynamic Digital Delay.
[0]	DYN_DDLY_CH0_EN	RW	0	Enable CH0 Dynamic Digital Delay.

9.6.2.219 OUTCH_JESD_CTRL1

OUTCH_TOP_JESD_CTRL controls JESD functions for TOP output channels. Back to Register Map.

Table 243. Register - 0x14E

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7]	SYSREF_EN_CH14_15	RW	0	Enable CH14_15 Sysref feature.
[6]	SYSREF_EN_CH12_13	RW	0	Enable CH12_13 Sysref feature.
[5]	SYSREF_EN_CH10_11	RW	0	Enable CH10_11 Sysref feature.
[4]	SYSREF_EN_CH8_9	RW	0	Enable CH8_9 Sysref feature.
[3]	SYSREF_EN_CH6_7	RW	0	Enable CH6_7 Sysref feature.
[2]	SYSREF_EN_CH4_5	RW	0	Enable CH4_5 Sysref feature.
[1]	SYSREF_EN_CH2_3	RW	0	Enable CH2_3 Sysref feature.
[0]	SYSREF_EN_CH0_1	RW	0	Enable CH0_1 Sysref feature.

9.6.2.220 PLL2_CTRL4

PLL2 CTRL4 Register sets PLL2 configuration. Back to Register Map.

Table 244. Register - 0x150

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.
[3]	PLL2_PFD_DIS_SAMPLE	RW	0	Disable PFD Sampling.
[2:0]	PLL2_PROG_PFD_RESET[2:0]	RW	0x0	Programmable PFD reset.

9.6.2.221 PLL2_CTRL5

PLL2 CTRL5 Register sets PLL2 configuration. Back to Register Map.

Table 245. Register - 0x151

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4]	PLL2_RFILT	RW	0	0-> 9.2kOhm 1->4.7kOhm
[3]	RSRVD	-	-	Reserved.
[2]	PLL2_CP_EN_SAMPLE_BYP	RW	0	Bypass PLL2 Chargepump sampling.
[1:0]	PLL2_CPROP[1:0]	RW	0x0	Set Cap prior Sampling.

9.6.2.222 PLL2_CTRL6

PLL2 CTRL6 Register sets PLL2 configuration. Back to Register Map.

Table 246. Register - 0x152

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:4]	RSRVD	-	-	Reserved.

Table 246. Register - 0x152 (continued)

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[3]	PLL2_EN_FILTER	RW	0	Enable PLL2 Chargepump Filter.
[2:0]	PLL2_CSAMPLE[2:0]	RW	0x0	PLL2 Set Cap After sampling.

9.6.2.223 PLL2_CTRL7

PLL2 CTRL7 Register sets PLL2 configuration. Back to Register Map.

Table 247. Register - 0x153

BIT NO.	FIELD	TYPE	RESET	DESCRIPTION
[7:5]	RSRVD	-	-	Reserved.
[4:0]	PLL2_CFILT	RW	0	0 to 124pF in 4pF steps

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

To assist customers in frequency planning and design of loop filters Texas Instrument's provides the Clock Design Tool and Clock Architect.

10.1.1 Digital Lock Detect Frequency Accuracy

The digital lock detect circuit is used to determine PLL1 locked and PLL2 locked. A window size and lock count register are programmed to set a ppm frequency accuracy of reference to feedback signals of the PLL for each event to occur. When a PLL digital lock event occurs the PLL's digital lock detect is asserted true.

EVENT	PLL	WINDOW SIZE	LOCK COUNT
PLL1 Lock	PLL1	PLL1_LD_WNDW_SIZE	PLL1_LOCKDET_CYC_CNT * (1 + (31 * PLL1_LCKDET_BY_32))
PLL2 Lock (Initial)	PLL2	PLL2_LD_WNDW_SIZE_INITIAL = 1 ns	PLL2_LOCKDET_CYC_CNT_INITIAL
PLL2 Lock	PLL2	PLL2_LD_WNDW_SIZE = 1 ns	PLL2_LOCKDET_CYC_CNT

For a digital lock detect event to occur there must be a *lock count* number of a *count frequency* during which the time/phase error of the PLLX_R reference and PLLX_N feedback signal edges are within the user programmable *window size*. Because there must be at least *lock count* number of *count frequency* cycles, a minimum digital lock detect assert time can be calculated as *lock count* / *count frequency* where count frequency = PLL2 phase detector frequency. PLL2 lock time is the sum of the PLL2 Lock (Initial) + PLL2 Lock time.

By using Equation 1, values for a *lock count* and *window size* can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs:

$$\text{ppm} = \frac{1e6 \times \text{WINDOW SIZE} \times \text{COUNT FREQUENCY}}{\text{LOCK COUNT}} \quad (1)$$

The effect of the *lock count* value is that it shortens the effective lock window size by dividing the *window size* by *lock count*.

If at any time the PLLX_R reference and PLLX_N feedback signals are outside the time window set by *window size*, then the *lock count* value is reset to 0.

10.1.1.1 Minimum Lock Time Calculation Example

To calculate the minimum PLL2 digital lock time given a PLL2 phase detector frequency of 245.76 MHz, PLL2_LOCK_DET_CYC_CNT_INITAL = 32768, and PLL2_LOCK_DET_CYC_CNT = 16384. Then the *minimum digital lock time assert time* of PLL2 is PLL2 Lock time (Initial) + PLL2 Lock time = (32768 / 245.76 MHz) + (16384 / 245.76 MHz) = 200 µs.

10.2 Typical Application

Normal use case of the LMK04616 device is as a dual loop jitter cleaner. This section will discuss a design example to illustrate the various functional aspects of the LMK04616 device.

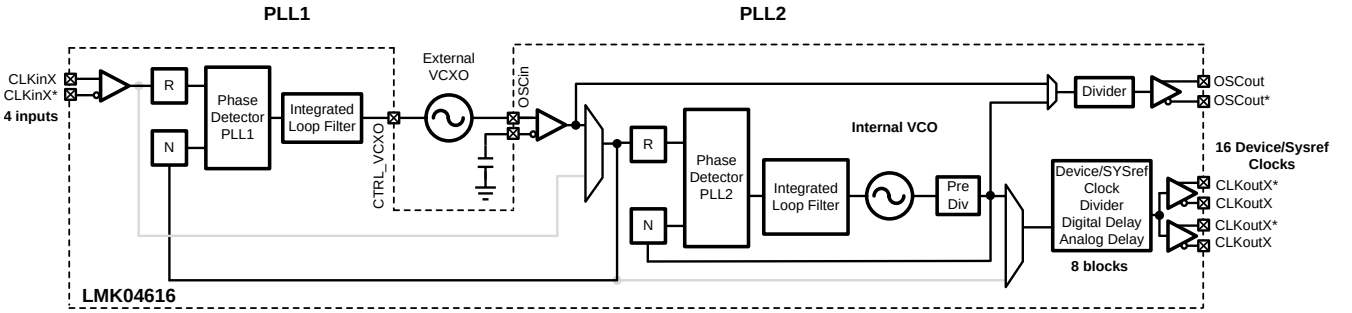


Figure 59. Simplified Functional Block Diagram for Dual-Loop Mode

10.2.1 Design Requirements

Given a remote radio head (RRU) type application which needs to clock some ADCs, DACs, FPGA, SERDES, and an LO. The input clock is a recovered clock which needs jitter cleaning. The FPGA clock should have a clock output on power up. A summary of clock input and output requirements are as follows:

Clock Input:

- 122.88-MHz recovered clock.

Clock Outputs:

- 1x 245.76-MHz clock for ADC
- 2x 983.04-MHz clock for DAC
- 2x 122.88-MHz clock for FPGA
- 1x 122.88-MHz clock for SERDES

It is also desirable to have the holdover feature engage if the recovered clock reference is ever lost. The following information reviews the steps to produce this design.

If JESD204B support is also required for the clock outputs, see *JEDEC JESD204B* for more details.

10.2.2 Detailed Design Procedure

Design of all aspects of the LMK04616 are quite involved and software has been written to assist in part selection and part programming. Contact TI for optimized loop filter settings based on the system requirement. This design procedure gives a quick outline of the process.

NOTE

This information is current as of the date of the release of this data sheet. Design tools receive continuous improvements to add features and improve model accuracy. Refer to software instructions or training for latest features.

1. Device Selection
   - The key to device selection is required VCO frequency given required output frequencies. The device must be able to produce the VCO frequency that can be divided down to required output frequencies.
   - The software design tools take the VCO frequency range into account for specific devices based on the application's required output frequencies.
   - To understand the process better, see the *Detailed Description* which provides more insight into the functional blocks and programming options.

Typical Application (continued)

2. Device Configuration

   There are many possible permutations of dividers and other registers to get same input and output frequencies from a device. However, consider that there are some optimizations and trade-offs. It is possible, although not assured, that some crosstalk and mixing could be created when using some divides.
   – The optimum setting attempts to maximize phase detector frequency and uses the smallest dividers settings.
   – For lowest possible in-band PLL noise, maximize phase detector frequency to minimize N divide value.
   – As rule of thumb, keeping the phase detector frequency approximately between 10 × PLL loop bandwidth and 100 × PLL loop bandwidth. A phase detector frequency less than 5 × PLL bandwidth may be unstable and a phase detector frequency > 100 × loop bandwidth may experience increased lock time due to cycle slipping. However, for clock generation and jitter cleaning applications, lock time is typically not critical and large phase detector frequencies typically result in reduced PLL noise, so cycle-slipping during lock is acceptable.

10.2.2.1 PLL Loop Filter Design

Contact TI with the application requirements to get the optimized loop filter settings.

10.2.2.2 Clock Output Assignment

It is best to consider proximity of each clock output to each other and other PLL circuitry when choosing final clock output locations. Here are some guidelines to help achieve best performance when assigning outputs to specific CLKout/OSCout pins.

- Group common frequencies together.
- Some clock targets require low close-in phase noise. If possible, use a VCXO based PLL1 output from OSCout/OSCout* for such a clock target.
- Some clock targets require excellent noise floor performance. Outputs driven by the internal LC-VCO have the best noise floor performance. An example is an ADC or DAC.

Other device specific configuration. For LMK04616, consider the following:

- Holdover Configuration

  LMK04616 provides the option to have two clock inputs. The clock priority, clock loss detection, holdover, and loss recovery can be programmed. See *Holdover* for more details.
- JESD204B support

  To generate JESD204B compliant clocks, see *JEDEC JESD204B* for more details.
- Digital delay: phase alignment of the output clocks.
- Analog delay: another method to shift phases of clocks with finer resolution with the penalty of increase noise floor.

10.2.2.3 Calculation Using LCM

In this example, the LCM (245.76 MHz, 983.04 MHz, 122.88 MHz) = 983.04 MHz. A valid VCO frequency for LMK04616 is 5898.24 MHz = 6 × 983.04 MHz. Therefore, the LMK04616 may be used to produce these output frequencies.

10.2.2.4 Device Programming

The software tool TICS Pro for EVM programming can be used to set up the device in the desired configuration, then export a hex register map suitable for use in applications.

10.2.2.5 Device Selection

Use the WEBENCH Clock Architect Tool and enter the required frequencies and formats into the tool. To use this device, find a solution using the LMK04616.

Typical Application (continued)

10.2.2.6 Clock Architect

When viewing resulting solutions, it is possible to narrow the parts used in the solution by setting a filter. Filtering of a specific device can be done by selecting the device from the filter combo box. Also, regular expressions can be typed into filter combo box. LMK04616 will only filter for the LMK04616 device.

10.2.3 Application Curves

Table 248 lists the application curves for this device.

Table 248. Table of Graphs

	FIGURE
LMK04616 CLKout2 Phase Noise VCO = 5898.24 MHz CLKout2 Frequency = 122.88 MHz HSDS 8 mA	Figure 2
LMK04616 CLKout2 Phase Noise VCO = 5898.24 MHz CLKout2 Frequency = 245.76 MHz HSDS 8 mA	Figure 4
LMK04616 CLKout2 Phase Noise VCO Frequency = 5898.24 MHz CLKout2 Frequency = 983.04 MHz HSDS 8 mA	Figure 5

10.3 Do's and Don'ts

10.3.1 Pin Connection Recommendations

- **V_{CC} Pins and Decoupling:** all V_{CC} pins must always be connected.
- **Unused Clock Outputs:** leave unused clock outputs floating and powered down.
- **Unused Clock Inputs:** unused clock inputs can be left floating.

11 Power Supply Recommendations

11.1 Recommended Power Supply Connection

Figure 60 shows the recommended power supply connection using a low-noise LDO and a DC-DC converter.

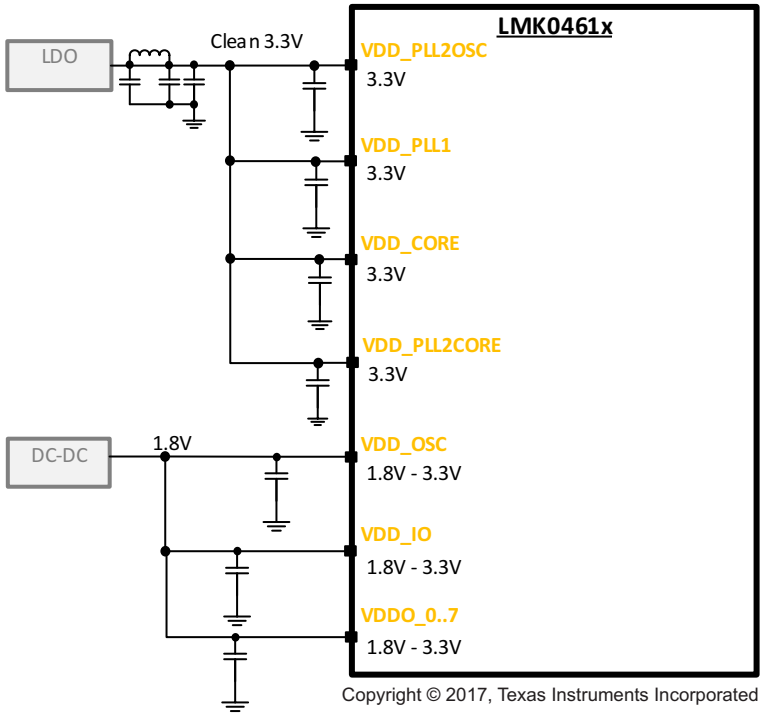


Figure 60. Recommended Power Supply Connection

11.2 Current Consumption / Power Dissipation Calculations

From Table 249 the current consumption can be calculated for any configuration. Data below is typical and not assured.

Table 249. Typical Current Consumption for Selected Functional Blocks (T_A = 25°C, V_{CC} = 3.3 V)

BLOCK	TEST CONDITIONS		TYPICAL I_{CC} (mA)	POWER DISSIPATED IN DEVICE (mW)	POWER DISSIPATED EXTERNALLY (mW)
CORE AND FUNCTIONAL BLOCKS					
PLL1	PLL1 locked		14.5	47.85	-
PLL2	PLL2 locked		44	145.2	
VCO (with VCO divider)	VCO		60	198	-
LOS	LOS enabled		1.8	3.24	
PLL1 Regulation			0.1	0.33	
OSCin Doubler	Doubler is enabled	EN_PLL2_REF_2X = 1	1.5	3.24	-
CLKinX	Any one of the CLKinX is enabled	Single-Ended Mode	1.2	2.16	-
		Differential Mode	1.5	2.7	
Holdover	Holdover is enabled	HOLDOVER_EN = 1	0	0	-
SYNC_EN = 1	Required for SYNC and SYSREF functionality		0	0	-

Current Consumption / Power Dissipation Calculations (continued)

Table 249. Typical Current Consumption for Selected Functional Blocks (T_A = 25°C, V_{CC} = 3.3 V) (continued)

BLOCK	TEST CONDITIONS		TYPICAL I_{CC} (mA)	POWER DISSIPATED IN DEVICE (mW)	POWER DISSIPATED EXTERNALLY (mW)
SYSREF	Enabled	SYSREF_PD = 0	0	0	-
	Dynamic Digital Delay enabled	SYSREF_DDLY_PD = 0	3.5	6.3	-
	Pulser is enabled	SYSREF_PLSR_PD = 0	0	0	
	SYSREF Pulses mode	SYSREF_MUX = 2	0	0	
	SYSREF Continuous mode	SYSREF_MUX = 3	0	0	
Output channel	Static Digital Delay		0	0	
	Static Digital Delay + Half step		0	0	
	Dynamic Digital Delay		3.5	6.3	
	Analog Delay		2.5	4.8	
	Analog Delay per Step		0.2	0.36	
CLOCK OUTPUT BUFFERS					
HCSL	50 Ω to Ground termination		19	34.2	-
HSDS	HSDS 4 mA		5	9	-
	HSDS 6 mA		7	12.6	-
	HSDS 8 mA		9	16.2	-
OSCout BUFFERS					
HCSL	50 Ω to Ground termination		19	34.2	-
HSDS	HSDS 8 mA		9	16.2	
LVCMOS	LVCMOS Pair	150 MHz	5	9	-
	LVCMOS Single	150 MHz	2.5	4.5	-

12 Layout

12.1 Layout Guidelines

Power consumption of the LMK0461x family of devices can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C.

12.1.1 CLKin and OSCin

If differential input (preferred) is used route traces tightly coupled. If single-ended, have at least 3 trace width (of CLKin or OSCin trace) separation from other RF traces. Place terminations close to IC.

12.1.2 CLKout

Normally differential signals must be routed tightly coupled to minimize PCB crosstalk. Trace impedance and terminations must be designed accord to output type being used. Unused outputs must be left open and programmed to power-down state.

12.2 Layout Example

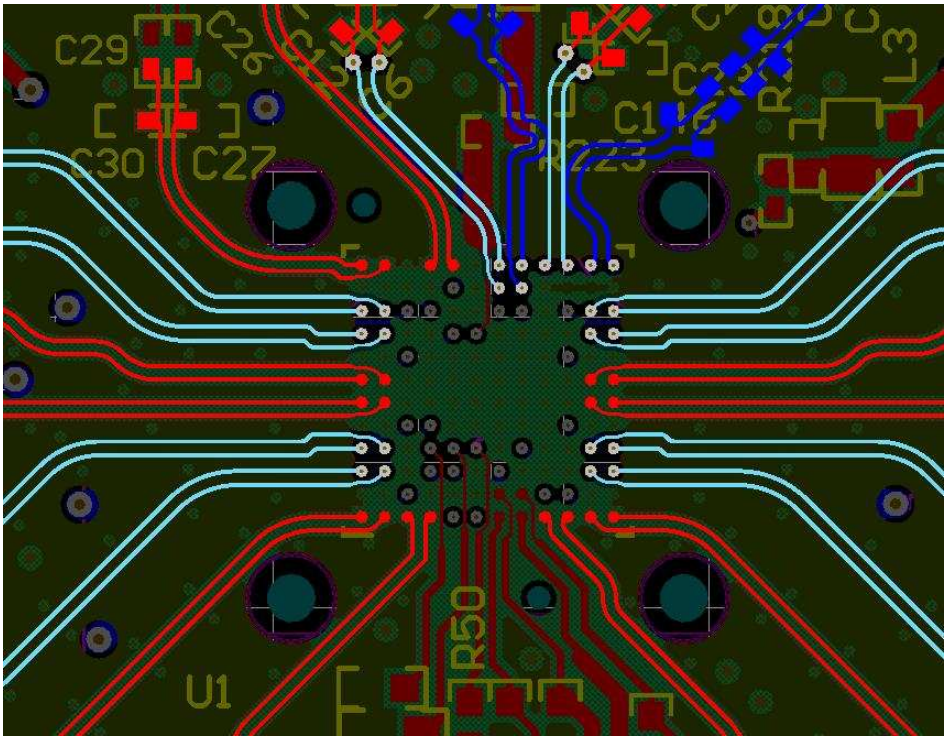


Figure 61. Recommended PCB Layout

1. CLKin and OSCin path:
   – If differential input (preferred), route traces tightly coupled. If single ended, have at least 3 trace width (of CLKin/OSCin trace) separation from other RF traces.
2. CLKouts/OSCout:
   – Normally differential signals should be routed tightly coupled to minimize PCB crosstalk. Trace impedance must be designed according to 100-Ω differential. For optimal isolation place different clock group signals on different layers.
3. VCXO connection
   – Shorter traces are better. Place a resistors and capacitors closer to IC except for a single capacitor and associated resistor, if any, next to VCXO. If any, place loop filter components close to VCXO Vtune pin.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

13.1.1.1 Clock Design Tool

For the Clock Design Tool, go to www.ti.com/tool/clockdesigntool

13.1.1.2 Clock Architect

Part selection, loop filter design, simulation.

For the Clock Architect, go to www.ti.com/clockarchitect.

13.1.1.3 TICS Pro

EVM programming software. Can also be used to generate register map for programming for a specific application.

For TICS Pro, go to www.ti.com/tool/TICSPRO-SW

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK04616ZCRR	Active	Production	NFBGA (ZCR) | 144	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LMK04616
LMK04616ZCRT	Active	Production	NFBGA (ZCR) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	LMK04616

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

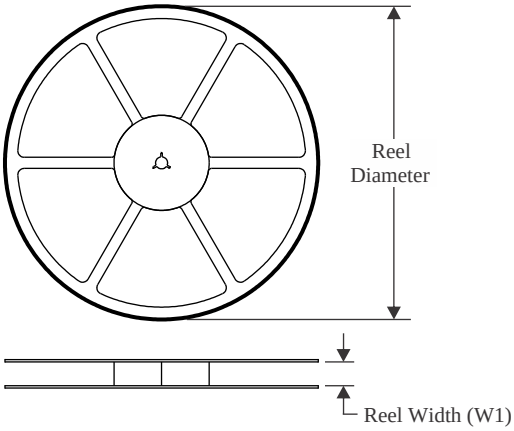
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

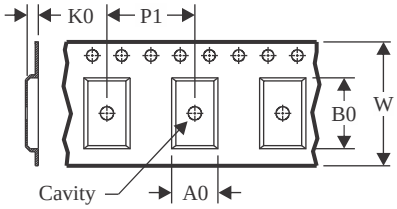
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

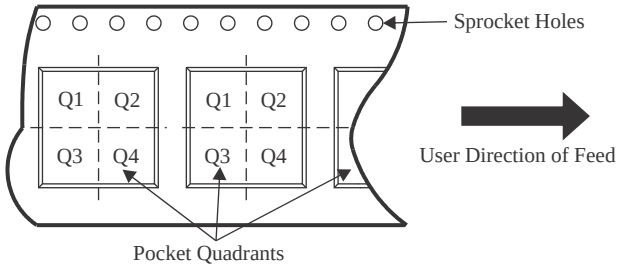


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

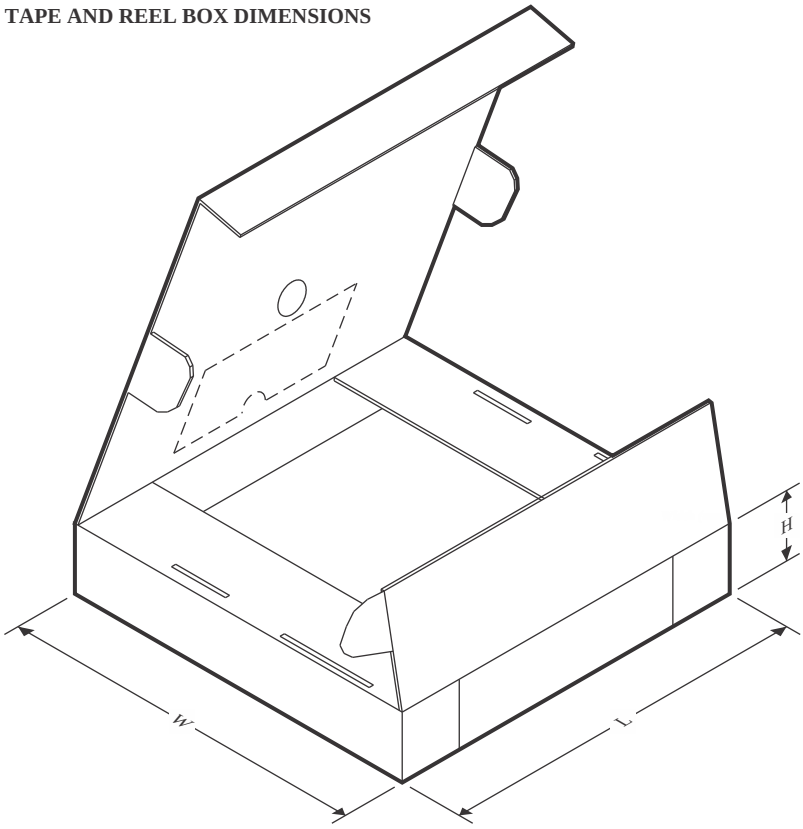
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK04616ZCRR	NFBGA	ZCR	144	1000	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q1
LMK04616ZCRT	NFBGA	ZCR	144	250	178.0	24.4	10.25	10.25	2.25	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

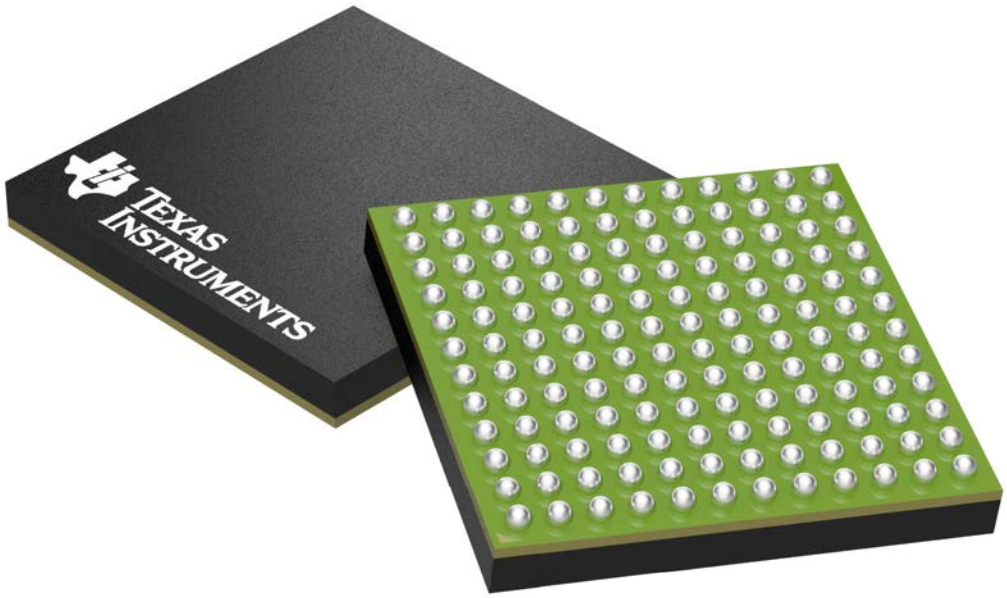
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK04616ZCRR	NFBGA	ZCR	144	1000	356.0	356.0	45.0
LMK04616ZCRT	NFBGA	ZCR	144	250	213.0	191.0	55.0

ZCR 144

NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY

10 x 10 mm, 0.8 mm pitch



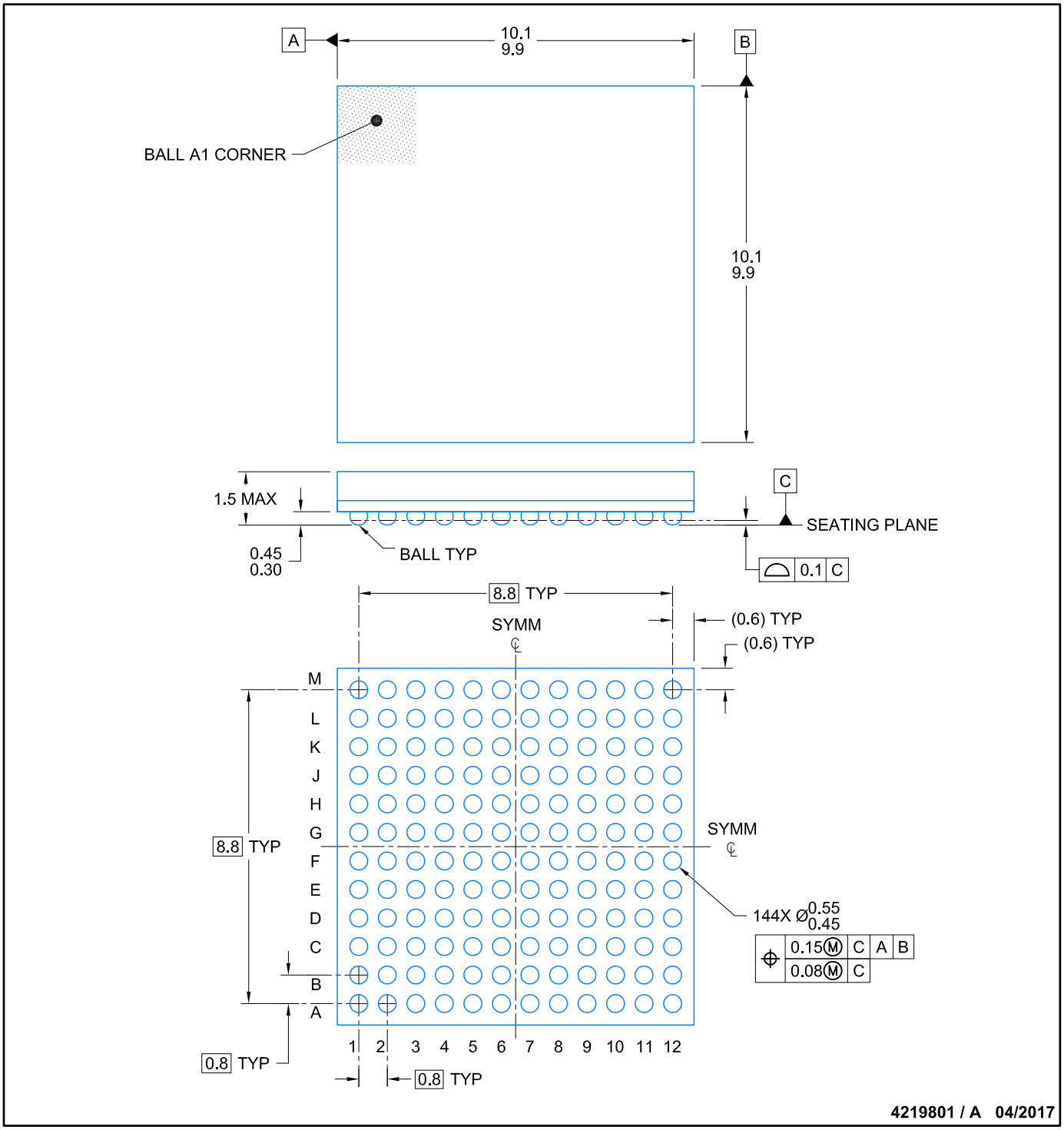
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

ZCR0144A

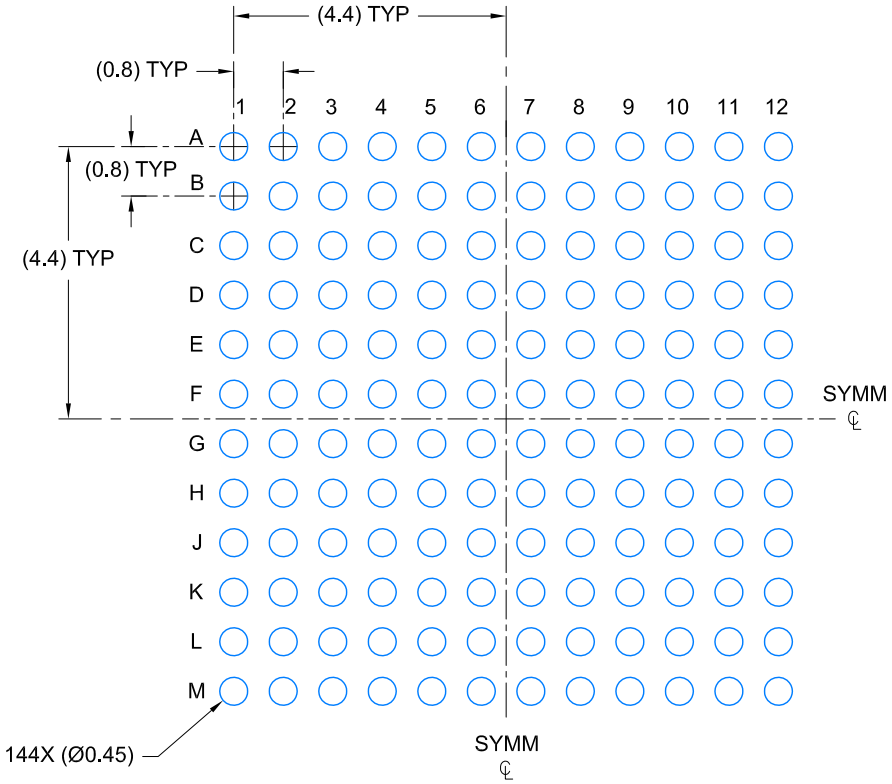
NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY

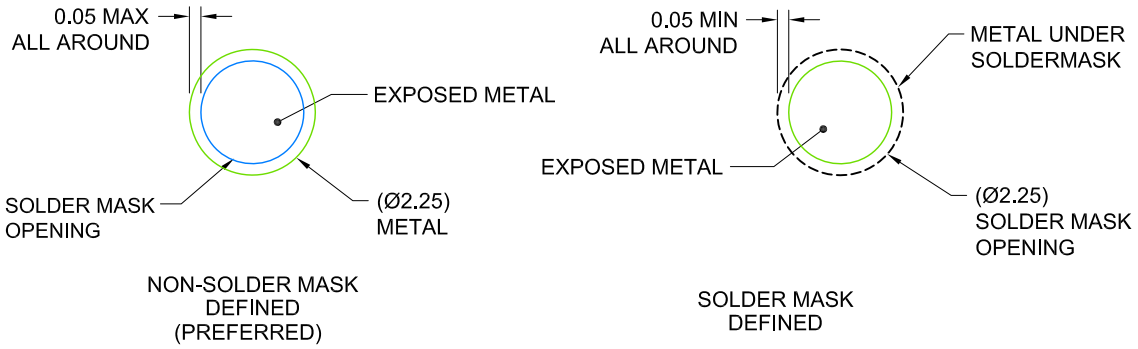


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219801 / A 04/2017

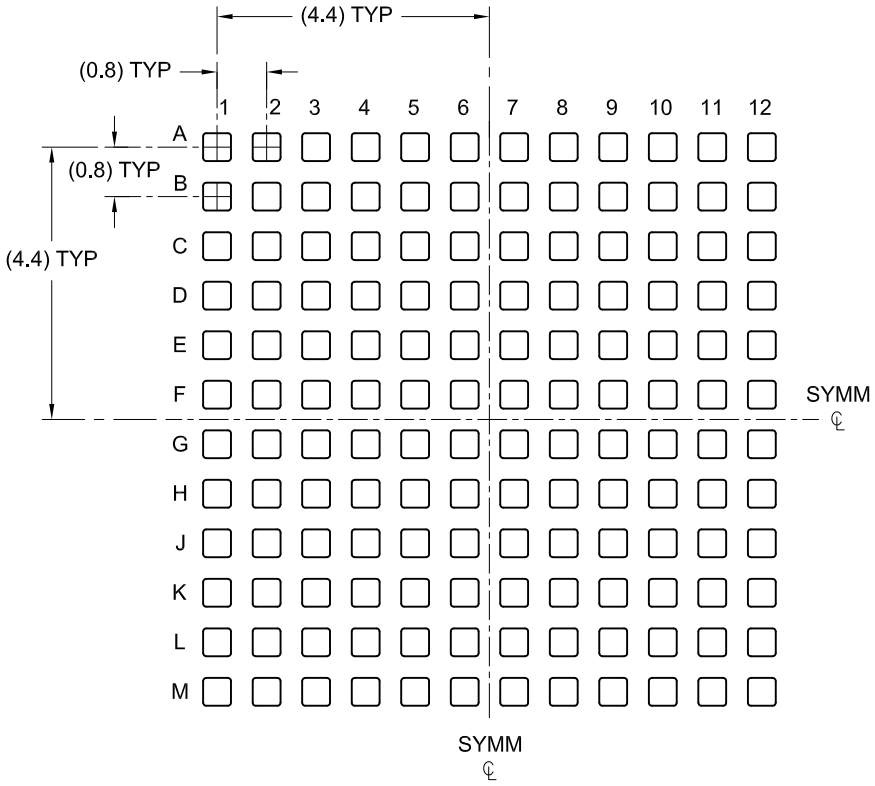
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SPRAA99 (www.ti.com/lit/spraa9).

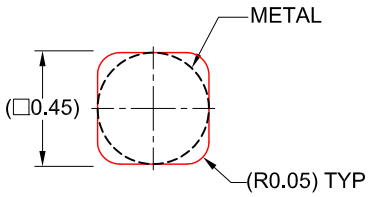
EXAMPLE STENCIL DESIGN

NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 8X



DETAIL
SCALE:32X

4219801 / A 04/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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