

# LMK1D1204P Pin-Controlled OE Low Additive Jitter LVDS Buffer

## 1 Features

- High-performance LVDS clock buffer family with 2 inputs and 4 outputs (2:4)
- Output frequency up to 2 GHz
- Hardware pins for individual output enable/disable
- Supply voltage: 1.8 V / 2.5 V / 3.3 V  $\pm$  5%
- Low additive jitter: < 60 fs rms maximum in 12 kHz to 20 MHz at 156.25 MHz
  - Very low phase noise floor: -164 dBc/Hz (typical)
- Very low propagation delay: < 575 ps maximum
- Output skew: 20 ps maximum
- Fail-safe inputs
- Universal inputs accept LVDS, LVPECL, LVCMOS, HCSL and CML
- LVDS reference voltage,  $V_{AC\_REF}$ , available for capacitive-coupled inputs
- Industrial temperature range:  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$
- Packages available:
  - 5-mm  $\times$  5-mm, 28-pin VQFN (RHD)

## 2 Applications

- [Telecommunications and networking](#)
- [Medical imaging](#)
- [Test and measurement](#)
- [Wireless infrastructure](#)
- [Pro audio, video and signage](#)

## 3 Description

The LMK1D1204P clock buffer distributes one of two selectable clock inputs (IN0 and IN1) to 4 pairs of differential LVDS clock outputs (OUT0 through OUT3) with minimum skew for clock distribution. The inputs can be either LVDS, LVPECL, LVCMOS, HCSL, or CML.

The LMK1D1204P is specifically designed for driving 50- $\Omega$  transmission lines. When driving inputs in single-ended mode, apply the appropriate bias voltage to the unused negative input pin (see [Figure 9-6](#)). The IN\_SEL pin selects the input which is routed to the outputs. The part supports a fail-safe input function. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

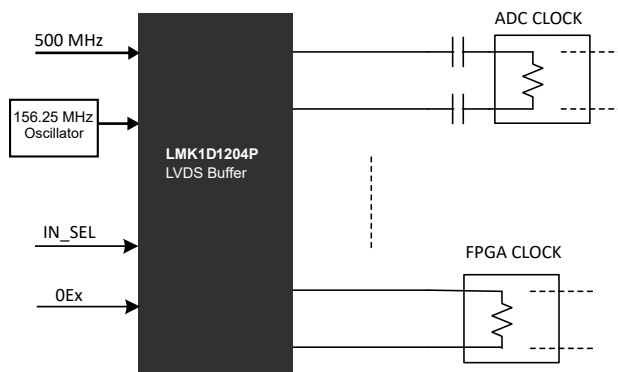
Each LVDS differential output is enabled by setting the corresponding OEx pin to a logic high "1". If this pin is set to a logic low "0", the output is disabled in a high Z state resulting in reduced power consumption.

The device operates in a 1.8-V, 2.5-V, or 3.3-V supply environment and is characterized from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  (ambient temperature).

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE (NOM) <sup>(2)</sup> |
|-------------|------------------------|-----------------------------------|
| LMK1D1204P  | VQFN (28)              | 5.00 mm $\times$ 5.00 mm          |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



**Application Example**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision * (September 2021) to Revision A (June 2023)</b>                                                           | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Updated data sheet formatting to align with the LMK1D1208P data sheet release.....                                                | <b>1</b>    |
| • Changed table title from: Device Information to: Package Information.....                                                         | <b>1</b>    |
| • Added information to the <i>Fail-Safe Input</i> section.....                                                                      | <b>14</b>   |
| • Removed the word 'or' in the phrase 'In this example, the PHY, ASIC, FPGA and CPU'.....                                           | <b>18</b>   |
| • Moved the <i>Power Supply Recommendations</i> and <i>Layout</i> section to the <i>Application and Implementation</i> section..... | <b>20</b>   |
| • Changed 0.1 $\mu$ F (x3) to 0.1 $\mu$ F (x4) in <a href="#">Figure 10-4</a> .....                                                 | <b>20</b>   |

## 5 Device Comparison

**Table 5-1. Device Comparison**

| DEVICE     | DEVICE TYPE | FEATURES                                               | OUTPUT SWING | PACKAGE   | BODY SIZE         |
|------------|-------------|--------------------------------------------------------|--------------|-----------|-------------------|
| LMK1D2108  | Dual 1:8    | Global output enable and swing control via pin control | 350 mV       | VQFN (48) | 7.00 mm × 7.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D2106  | Dual 1:6    | Global output enable and swing control via pin control | 350 mV       | VQFN (40) | 6.00 mm × 6.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D2104  | Dual 1:4    | Global output enable and swing control via pin control | 350 mV       | VQFN (28) | 5.00 mm × 5.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D2102  | Dual 1:2    | Global output enable and swing control via pin control | 350 mV       | VQFN (16) | 3.00 mm × 3.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D1216  | 2:16        | Global output enable control via pin control           | 350 mV       | VQFN (48) | 7.00 mm × 7.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D1212  | 2:12        | Global output enable control via pin control           | 350 mV       | VQFN (40) | 6.00 mm × 6.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D1208P | 2:8         | Individual output enable control via pin control       | 350 mV       | VQGN (40) | 6.00 mm × 6.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D1208I | 2:8         | Individual output enable control via I2C               | 350 mV       | VQFN (40) | 6.00 mm × 6.00 mm |
|            |             |                                                        | 500 mV       |           |                   |
| LMK1D1208  | 2:8         | Global output enable control via pin control           | 350 mV       | VQFN (28) | 5.00 mm × 5.00 mm |
| LMK1D1204P | 2:4         | Individual output enable control via pin control       | 350 mV       | VQGN (28) | 5.00 mm × 5.00 mm |
| LMK1D1204  | 2:4         | Global output enable control via pin control           | 350 mV       | VQFN (16) | 3.00 mm × 3.00 mm |

## 6 Pin Configuration and Functions

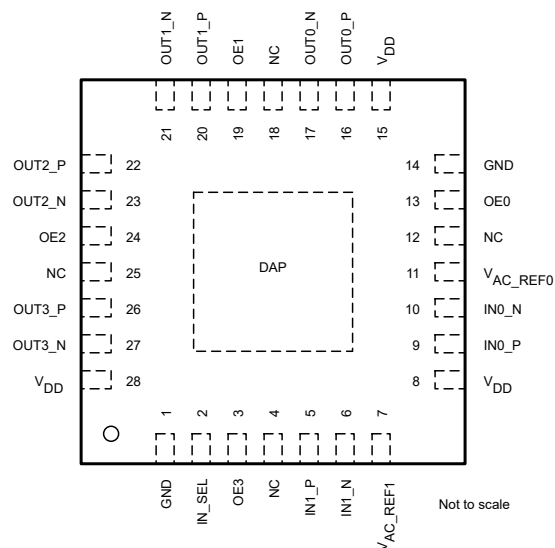


Figure 6-1. LMK1D1204P: RHD Package 28-Pin VQFN Top View

Table 6-1. Pin Functions

| NAME                                  | NO. | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                     |
|---------------------------------------|-----|---------------------|---------------------------------------------------------------------------------------------------------------------------------|
| DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT |     |                     |                                                                                                                                 |
| IN0_P                                 | 9   | I                   | Primary: Differential input pair or single-ended input                                                                          |
| IN0_N                                 | 10  |                     |                                                                                                                                 |
| IN1_P                                 | 5   | I                   | Secondary: Differential input pair or single-ended input.<br>Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N. |
| IN1_N                                 | 6   |                     |                                                                                                                                 |
| INPUT SELECT                          |     |                     |                                                                                                                                 |
| IN_SEL                                | 2   | I                   | Input Selection with an internal 500-kΩ pullup and 320-kΩ pulldown, selects input port. See <a href="#">Table 9-1</a> .         |
| OUTPUT ENABLE                         |     |                     |                                                                                                                                 |
| OE0                                   | 13  | I                   | Output Enable for channel 0<br>HIGH (default): Enable output channel 0<br>LOW: Disable output channel 0 in Hi-Z state           |
| OE1                                   | 19  | I                   | Output Enable for channel 1<br>HIGH (default): Enable output channel 1<br>LOW: Disable output channel 1 in Hi-Z state           |
| OE2                                   | 24  | I                   | Output Enable for channel 2<br>HIGH (default): Enable output channel 2<br>LOW: Disable output channel 2 in Hi-Z state           |
| OE3                                   | 3   | I                   | Output Enable for channel 3<br>HIGH (default): Enable output channel 3<br>LOW: Disable output channel 3 in Hi-Z state           |
| BIAS VOLTAGE OUTPUT                   |     |                     |                                                                                                                                 |
| V <sub>AC_REF0</sub>                  | 11  | O                   | Bias voltage output for capacitive-coupled inputs. If used, TI recommends using a 0.1-μF capacitor to GND on this pin.          |
| V <sub>AC_REF1</sub>                  | 7   |                     |                                                                                                                                 |
| DIFFERENTIAL CLOCK OUTPUT             |     |                     |                                                                                                                                 |
| OUT0_P                                | 16  | O                   | Differential LVDS output pair number 0                                                                                          |
| OUT0_N                                | 17  |                     |                                                                                                                                 |

**Table 6-1. Pin Functions (continued)**

| NAME            | NO.           | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                   |
|-----------------|---------------|---------------------|-----------------------------------------------------------------------------------------------|
| OUT1_P          | 20            | O                   | Differential LVDS output pair number 1                                                        |
| OUT1_N          | 21            |                     |                                                                                               |
| OUT2_P          | 22            | O                   | Differential LVDS output pair number 2                                                        |
| OUT2_N          | 23            |                     |                                                                                               |
| OUT3_P          | 26            | O                   | Differential LVDS output pair number 3                                                        |
| OUT3_N          | 27            |                     |                                                                                               |
| SUPPLY VOLTAGE  |               |                     |                                                                                               |
| V <sub>DD</sub> | 8, 15, 28     | P                   | Device power supply (1.8 V, 2.5 V, or 3.3 V)                                                  |
| GROUND          |               |                     |                                                                                               |
| GND             | 1, 14         | G                   | Ground                                                                                        |
| MISC            |               |                     |                                                                                               |
| DAP             | DAP           | GND                 | Die Attach Pad. Connect to the printed circuit board (PCB) ground plane for heat dissipation. |
| NC              | 4, 12, 18, 25 | NC                  | No Connection. Leave floating                                                                 |

(1) G = Ground, I = Input, O = Output, P = Power

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                    | MIN  | MAX                   | UNIT |
|------------------|------------------------------------|------|-----------------------|------|
| V <sub>DD</sub>  | Supply voltage                     | −0.3 | 3.6                   | V    |
| V <sub>IN</sub>  | Input voltage                      | −0.3 | 3.6                   | V    |
| V <sub>O</sub>   | Output voltage                     | −0.3 | V <sub>DD</sub> + 0.3 | V    |
| I <sub>IN</sub>  | Input current                      | −20  | 20                    | mA   |
| I <sub>O</sub>   | Continuous output current          | −50  | 50                    | mA   |
| T <sub>J</sub>   | Junction temperature               |      | 135                   | °C   |
| T <sub>stg</sub> | Storage temperature <sup>(2)</sup> | −65  | 150                   | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) Device unpowered

### 7.2 ESD Ratings

|                    |                         |                                                                                 | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | ±3000 | V    |
|                    |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                |                                                      | MIN   | NOM | MAX   | UNIT |
|-----------------|--------------------------------|------------------------------------------------------|-------|-----|-------|------|
| V <sub>DD</sub> | Core supply voltage            | 3.3-V supply                                         | 3.135 | 3.3 | 3.465 | V    |
|                 |                                | 2.5-V supply                                         | 2.375 | 2.5 | 2.625 |      |
|                 |                                | 1.8-V supply                                         | 1.71  | 1.8 | 1.89  |      |
| Supply Ramp     | Supply voltage ramp            | Requires monotonic ramp (10-90% of V <sub>DD</sub> ) | 0.1   |     | 20    | ms   |
| T <sub>A</sub>  | Operating free-air temperature |                                                      | −40   |     | 105   | °C   |
| T <sub>J</sub>  | Operating junction temperature |                                                      | −40   |     | 135   | °C   |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | LMK1D1204P | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RHD (VQFN) |      |
|                               |                                              | 28 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 38.9       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 32.1       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 18.7       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1          | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 18.7       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 8.2        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

$V_{DD} = 1.8 \text{ V} \pm 5\%$ ,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ . Typical values are at  $V_{DD} = 1.8 \text{ V}$ ,  $25^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER                                                                                                                                                                        |                                                                            | TEST CONDITIONS                                                                    | MIN                 | TYP                 | MAX                 | UNIT          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|------------------------------------------------------------------------------------|---------------------|---------------------|---------------------|---------------|
| <b>POWER SUPPLY CHARACTERISTICS</b>                                                                                                                                              |                                                                            |                                                                                    |                     |                     |                     |               |
| $I_{DDSTAT}$                                                                                                                                                                     | LMK1D1204P                                                                 | All-outputs enabled and unterminated, $f = 0 \text{ Hz}$ <sup>(1)</sup>            |                     | 50                  |                     | mA            |
| $I_{DD100M}$                                                                                                                                                                     | LMK1D1204P                                                                 | All-outputs enabled, $R_L = 100 \Omega$ , $f = 100 \text{ MHz}$                    |                     | 60                  | 72                  | mA            |
| <b>INPUT CHARACTERISTICS (Applies to <math>V_{DD} = 1.8 \text{ V} \pm 5\%</math>, <math>2.5 \text{ V} \pm 5\%</math> and <math>3.3 \text{ V} \pm 5\%</math>)</b>                 |                                                                            |                                                                                    |                     |                     |                     |               |
| $V_{dI3}$                                                                                                                                                                        | 3-state input                                                              | Open                                                                               |                     | $0.4 \times V_{CC}$ |                     | V             |
| $V_{IH}$                                                                                                                                                                         | Input high voltage                                                         | Minimum input voltage for a logical "1" state                                      | $0.7 \times V_{CC}$ |                     | $V_{CC} + 0.3$      | V             |
| $V_{IL}$                                                                                                                                                                         | Input low voltage                                                          | Maximum input voltage for a logical "0" state                                      | -0.3                |                     | $0.3 \times V_{CC}$ | V             |
| $I_{IH}$                                                                                                                                                                         | Input high current                                                         | $V_{DD}$ can be 1.8V/2.5V/3.3V with $V_{IH} = V_{DD}$                              |                     |                     | 30                  | $\mu\text{A}$ |
| $I_{IL}$                                                                                                                                                                         | Input low current                                                          | $V_{DD}$ can be 1.8V/2.5V/3.3V with $V_{IH} = V_{DD}$                              | -30                 |                     |                     | $\mu\text{A}$ |
| $R_{pull-up(EN)}$                                                                                                                                                                | Input pullup resistor                                                      |                                                                                    |                     | 500                 |                     | k $\Omega$    |
| $R_{pull-down(EN)}$                                                                                                                                                              | Input pulldown resistor                                                    |                                                                                    |                     | 320                 |                     | k $\Omega$    |
| <b>SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to <math>V_{DD} = 1.8 \text{ V} \pm 5\%</math>, <math>2.5 \text{ V} \pm 5\%</math> and <math>3.3 \text{ V} \pm 5\%</math>)</b> |                                                                            |                                                                                    |                     |                     |                     |               |
| $f_{IN}$                                                                                                                                                                         | Input frequency                                                            | Clock input                                                                        | DC                  |                     | 250                 | MHz           |
| $V_{IN\_S-E}$                                                                                                                                                                    | Single-ended Input Voltage Swing                                           | Assumes a square wave input with two levels                                        | 0.4                 |                     | 3.465               | V             |
| $dV_{IN}/dt$                                                                                                                                                                     | Input Slew Rate (20% to 80% of the amplitude)                              |                                                                                    | 0.05                |                     |                     | V/ns          |
| $I_{IH}$                                                                                                                                                                         | Input high current                                                         | $V_{DD} = 3.465 \text{ V}$ , $V_{IH} = 3.465 \text{ V}$                            |                     |                     | 50                  | $\mu\text{A}$ |
| $I_{IL}$                                                                                                                                                                         | Input low current                                                          | $V_{DD} = 3.465 \text{ V}$ , $V_{IL} = 0 \text{ V}$                                | -30                 |                     |                     | $\mu\text{A}$ |
| $C_{IN\_SE}$                                                                                                                                                                     | Input capacitance                                                          | at $25^{\circ}\text{C}$                                                            |                     | 3.5                 |                     | pF            |
| <b>DIFFERENTIAL CLOCK INPUT (Applies to <math>V_{DD} = 1.8 \text{ V} \pm 5\%</math>, <math>2.5 \text{ V} \pm 5\%</math> and <math>3.3 \text{ V} \pm 5\%</math>)</b>              |                                                                            |                                                                                    |                     |                     |                     |               |
| $f_{IN}$                                                                                                                                                                         | Input frequency                                                            | Clock input                                                                        |                     |                     | 2                   | GHz           |
| $V_{IN\_DIFF(P-P)}$                                                                                                                                                              | Differential input voltage peak-to-peak $\{2 \times (V_{INP} - V_{INN})\}$ | $V_{ICM} = 1 \text{ V}$ ( $V_{DD} = 1.8 \text{ V}$ )                               | 0.3                 |                     | 2.4                 | $V_{PP}$      |
|                                                                                                                                                                                  |                                                                            | $V_{ICM} = 1.25 \text{ V}$ ( $V_{DD} = 2.5 \text{ V}/3.3 \text{ V}$ )              | 0.3                 |                     | 2.4                 |               |
| $V_{ICM}$                                                                                                                                                                        | Input common mode voltage                                                  | $V_{IN\_DIFF(P-P)} > 0.4 \text{ V}$ ( $V_{DD} = 1.8 \text{ V}/2.5/3.3 \text{ V}$ ) | 0.25                |                     | 2.3                 | V             |
| $I_{IH}$                                                                                                                                                                         | Input high current                                                         | $V_{DD} = 3.465 \text{ V}$ , $V_{INP} = 2.4 \text{ V}$ , $V_{INN} = 1.2 \text{ V}$ |                     |                     | 30                  | $\mu\text{A}$ |

$V_{DD} = 1.8 \text{ V} \pm 5\%$ ,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ . Typical values are at  $V_{DD} = 1.8 \text{ V}$ ,  $25^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER                             |                                                                                                                                                                | TEST CONDITIONS                                                                                                                                                                                                               | MIN  | TYP  | MAX   | UNIT             |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------|------------------|
| $I_{IL}$                              | Input low current                                                                                                                                              | $V_{DD} = 3.465 \text{ V}$ , $V_{INP} = 0 \text{ V}$ , $V_{INN} = 1.2 \text{ V}$                                                                                                                                              | -30  |      |       | $\mu\text{A}$    |
| $C_{IN\_S-E}$                         | Input capacitance (Single-ended)                                                                                                                               | at $25^{\circ}\text{C}$                                                                                                                                                                                                       |      | 3.5  |       | pF               |
| <b>LVDS DC OUTPUT CHARACTERISTICS</b> |                                                                                                                                                                |                                                                                                                                                                                                                               |      |      |       |                  |
| $ V_{OD} $                            | Differential output voltage magnitude $ V_{OUTP} - V_{OUTN} $                                                                                                  | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$                                                                                                                                                                  | 250  | 350  | 450   | mV               |
| $\Delta V_{OD}$                       | Change in differential output voltage magnitude. Per output, defined as the difference between VOD in logic hi/lo states.                                      | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$                                                                                                                                                                  | -15  |      | 15    | mV               |
| $V_{OC(SS)}$                          | Steady-state common mode output voltage                                                                                                                        | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$ ( $V_{DD} = 1.8 \text{ V}$ )                                                                                                                                     | 1    |      | 1.2   | V                |
|                                       |                                                                                                                                                                | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$ ( $V_{DD} = 2.5 \text{ V}/3.3 \text{ V}$ )                                                                                                                       | 1.1  |      | 1.375 |                  |
| $\Delta V_{OC(SS)}$                   | Change in steady-state common mode output voltage. Per output, defined as the difference in VOC in logic hi/lo states.                                         | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$                                                                                                                                                                  | -15  |      | 15    | mV               |
| <b>LVDS AC OUTPUT CHARACTERISTICS</b> |                                                                                                                                                                |                                                                                                                                                                                                                               |      |      |       |                  |
| $V_{ring}$                            | Output overshoot and undershoot                                                                                                                                | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$ , $f_{OUT} = 491.52 \text{ MHz}$                                                                                                                                 | -0.1 |      | 0.1   | $V_{OD}$         |
| $V_{OS}$                              | Output AC common mode                                                                                                                                          | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$                                                                                                                                                                  |      | 50   | 100   | mV <sub>pp</sub> |
| $I_{OS}$                              | Short-circuit output current (differential)                                                                                                                    | $V_{OUTP} = V_{OUTN}$                                                                                                                                                                                                         | -12  |      | 12    | mA               |
| $I_{OS(cm)}$                          | Short-circuit output current (common-mode)                                                                                                                     | $V_{OUTP} = V_{OUTN} = 0$                                                                                                                                                                                                     | -24  |      | 24    | mA               |
| $t_{PD}$                              | Propagation delay                                                                                                                                              | $V_{IN,DIFF(P-P)} = 0.3 \text{ V}$ , $R_{LOAD} = 100 \Omega$ (2)                                                                                                                                                              | 0.3  |      | 0.575 | ns               |
| $t_{SK, O}$                           | Output skew                                                                                                                                                    | Skew between outputs with the same load conditions                                                                                                                                                                            |      |      | 20    | ps               |
| $t_{SK, PP}$                          | Part-to-part skew                                                                                                                                              | Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.                                                                                                    |      |      | 250   | ps               |
| $t_{SK, P}$                           | Pulse skew                                                                                                                                                     | 50% duty cycle input, crossing point-to-crossing-point distortion (4)                                                                                                                                                         | -20  |      | 20    | ps               |
| $t_{RJIT(ADD)}$                       | Random additive Jitter (rms)                                                                                                                                   | $f_{IN} = 156.25 \text{ MHz}$ with 50% duty-cycle, Input slew rate = $1.5 \text{ V/ns}$ , Integration range = $12 \text{ kHz} - 20 \text{ MHz}$ , with output load $R_{LOAD} = 100 \Omega$                                    |      | 50   | 60    | fs, RMS          |
| Phase noise                           | Phase Noise for a carrier frequency of $156.25 \text{ MHz}$ with 50% duty-cycle, Input slew rate = $1.5 \text{ V/ns}$ with output load $R_{LOAD} = 100 \Omega$ | $PN_{1kHz}$                                                                                                                                                                                                                   |      | -143 |       | dBc/Hz           |
|                                       |                                                                                                                                                                | $PN_{10kHz}$                                                                                                                                                                                                                  |      | -152 |       |                  |
|                                       |                                                                                                                                                                | $PN_{100kHz}$                                                                                                                                                                                                                 |      | -157 |       |                  |
|                                       |                                                                                                                                                                | $PN_{1MHz}$                                                                                                                                                                                                                   |      | -160 |       |                  |
|                                       |                                                                                                                                                                | $PN_{floor}$                                                                                                                                                                                                                  |      | -164 |       |                  |
| $MUX_{ISO}$                           | Mux Isolation                                                                                                                                                  | $f_{IN} = 156.25 \text{ MHz}$ . The difference in power level at $f_{IN}$ when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active. |      | 80   |       | dB               |
| ODC                                   | Output duty cycle                                                                                                                                              | With 50% duty cycle input                                                                                                                                                                                                     | 45   |      | 55    | %                |
| $t_R/t_F$                             | Output rise and fall time                                                                                                                                      | 20% to 80% with $R_{LOAD} = 100 \Omega$                                                                                                                                                                                       |      |      | 300   | ps               |

$V_{DD} = 1.8 \text{ V} \pm 5 \%$ ,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ . Typical values are at  $V_{DD} = 1.8 \text{ V}$ ,  $25^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER                                                          |                                                                  | TEST CONDITIONS                                     | MIN | TYP  | MAX   | UNIT |
|--------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------|-----|------|-------|------|
| V <sub>AC_REF</sub>                                                | Reference output voltage                                         | VDD = 2.5 V, I <sub>LOAD</sub> = 100 μA             | 0.9 | 1.25 | 1.375 | V    |
| POWER SUPPLY NOISE REJECTION (PSNR) V <sub>DD</sub> = 2.5 V/ 3.3 V |                                                                  |                                                     |     |      |       |      |
| PSNR                                                               | Power Supply Noise Rejection (f <sub>carrier</sub> = 156.25 MHz) | 10 kHz, 100 mVpp ripple injected on V <sub>DD</sub> | −70 |      |       | dBc  |
|                                                                    |                                                                  | 1 MHz, 100 mVpp ripple injected on V <sub>DD</sub>  | −50 |      |       |      |

- (1) A typical 4-mA current reduction per disabled output can be expected.
- (2) Measured between single-ended/differential input crossing point to the differential output crossing point.
- (3) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

## 7.6 Typical Characteristics

Figure 7-1 captures the variation of the LMK1D1204P current consumption with input frequency and supply voltage. Figure 7-2 shows the variation of the differential output voltage (VOD) swept across frequency.

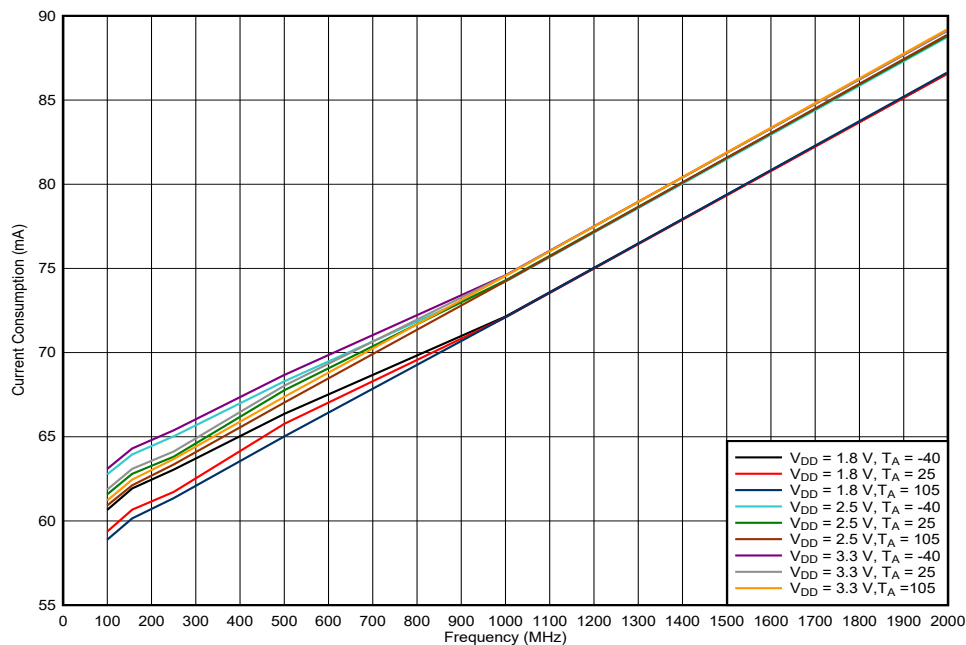


Figure 7-1. LMK1D1204P Current Consumption vs Frequency

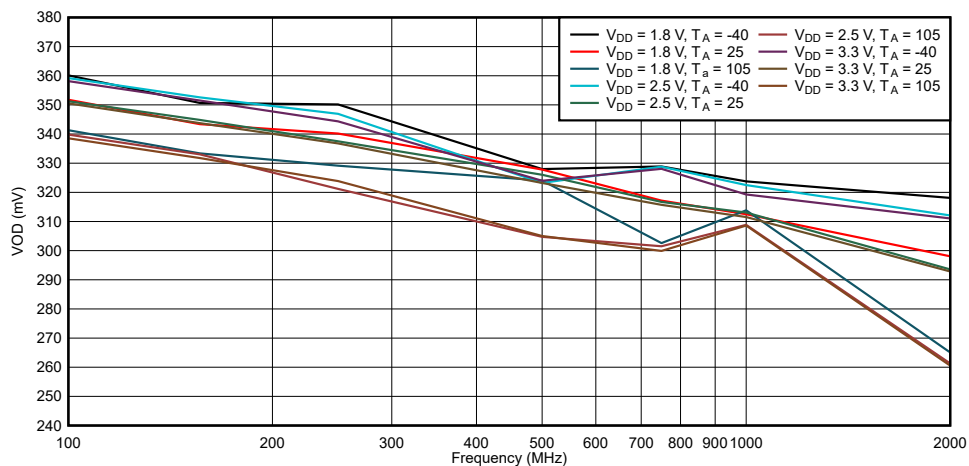


Figure 7-2. LMK1D1204P VOD vs Frequency

## 8 Parameter Measurement Information

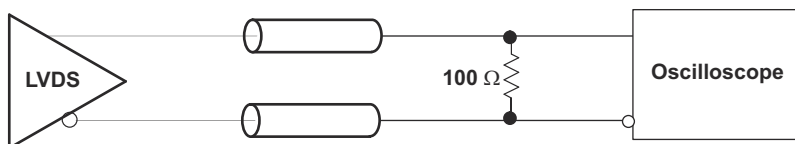


Figure 8-1. LVDS Output DC Configuration During Device Test

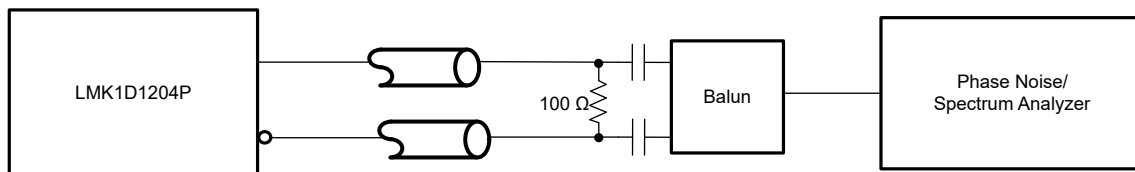


Figure 8-2. LVDS Output AC Configuration During Device Test

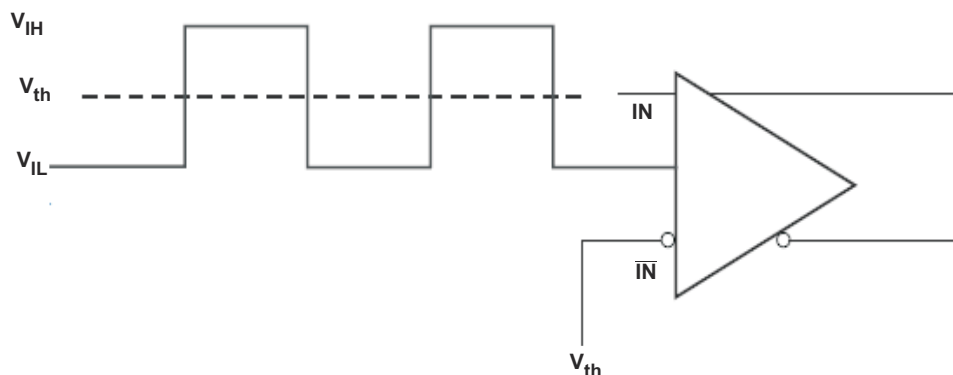


Figure 8-3. DC-Coupled LVCMOS Input During Device Test

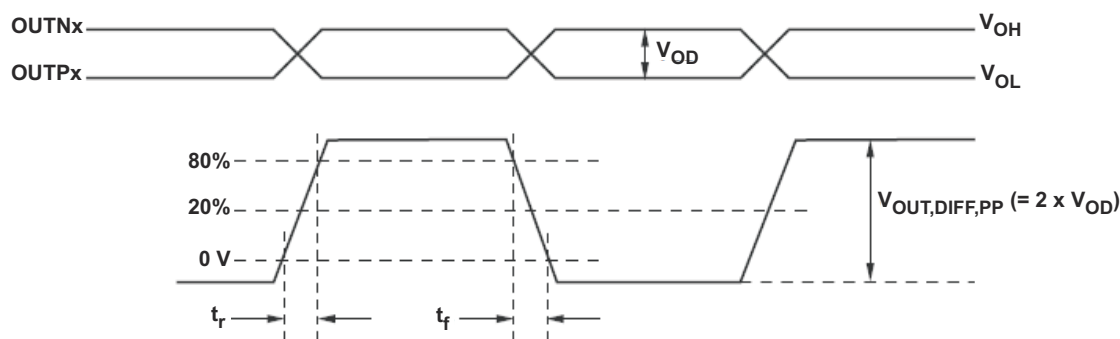
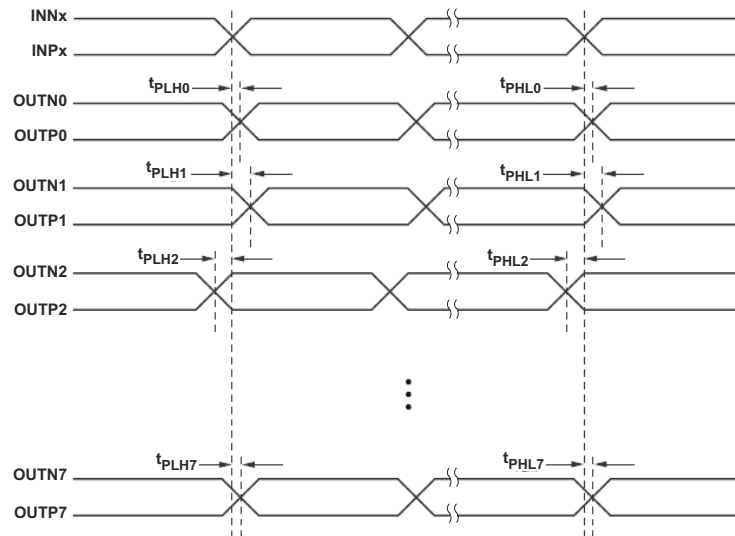
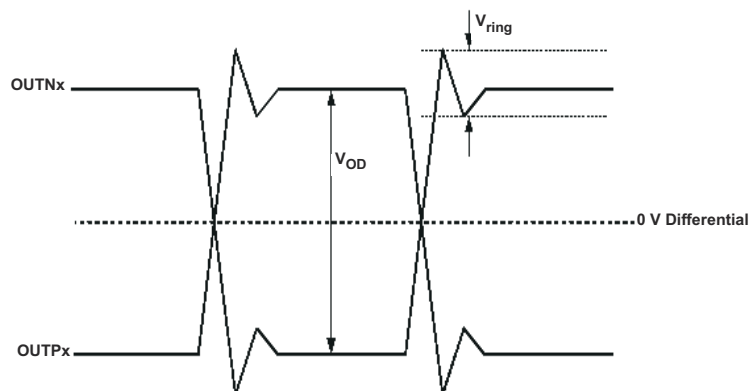


Figure 8-4. Output Voltage and Rise/Fall Time

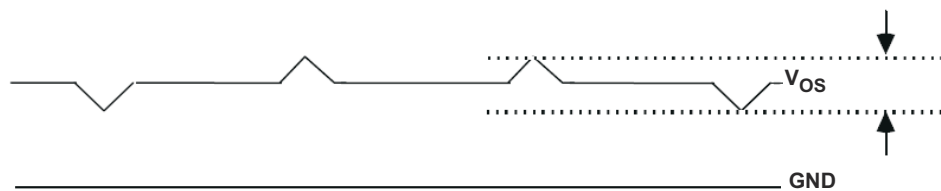


- A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 7$ )
- B. Part to part skew is calculated as the greater of the following: the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  across multiple devices ( $n = 0, 1, 2, \dots, 7$ )

**Figure 8-5. Output Skew and Part-to-Part Skew**



**Figure 8-6. Output Overshoot and Undershoot**



**Figure 8-7. Output AC Common Mode**

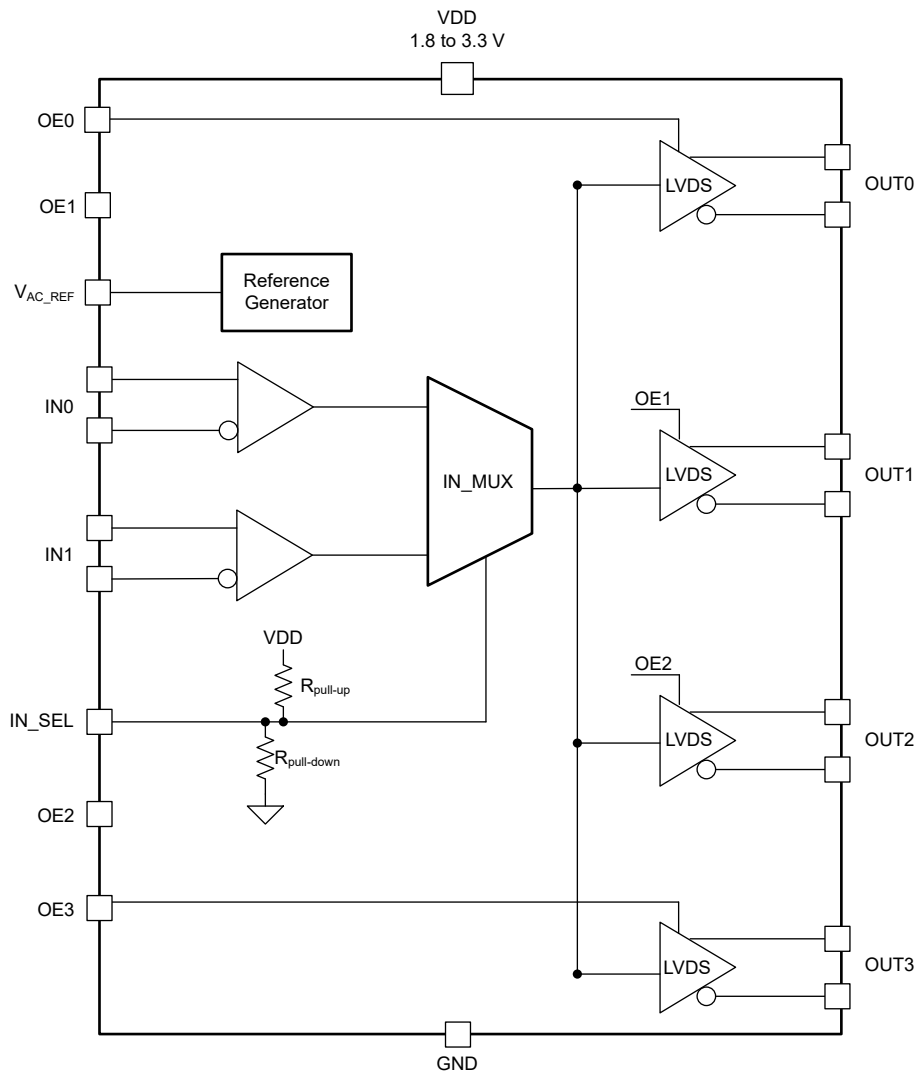
## 9 Detailed Description

### 9.1 Overview

The LMK1D1204P LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D1204P, AC coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

The LMK1D1204P is a low additive jitter LVDS fan-out buffer that can generate up to four copies of two selectable LVPECL, LVDS, HCSL, CML, or LVCMOS inputs. The LMK1D1204P can accept reference clock frequencies up to 2 GHz while providing low output skew.

#### 9.3.1 Fail-Safe Input

The LMK1D120x family of devices is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before  $V_{DD}$  is applied without damaging the device. Refer to [Specifications](#) for more information on the maximum input supported by the device. The user should note that incorporating the fail-safe inputs also results in a slight increase in clock input pin capacitance. The device also incorporates an input hysteresis which prevents random oscillation in absence of an input signal. Furthermore, this feature allows the input pins to be left open.

### 9.4 Device Functional Modes

The two inputs of the LMK1D1204P are internally muxed together and can be selected through the control pin (see [Table 9-1](#)). Unused inputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the LMK1D1204P to provide greater system flexibility.

**Table 9-1. Input Selection Table**

| IN_SEL | ACTIVE CLOCK INPUT  |
|--------|---------------------|
| 0      | IN0_P, IN0_N        |
| 1      | IN1_P, IN1_N        |
| Open   | None <sup>(1)</sup> |

- (1) The input buffers are disabled and the state of the outputs are dependent on the state of OEx (see [Table 9-2](#)). If OEx = 0, the corresponding output will be disabled in Hi-Z state, whereas if OEx = 1 (default), the corresponding output will be logic low.

The outputs of the LMK1D1204P can be individually enabled or disabled using the OEx hardware pins (see [Table 9-2](#)). The disabled state of the outputs is Hi-Z (high impedance) as this reduces the power consumption and also prevents back-biasing of the devices connected to these outputs.

Unused outputs should be disabled to eliminate the need for a termination resistor. In the case of enabled unused outputs, TI recommends a 100-Ω termination for optimal performance.

**Table 9-2. Output Control**

| OEx         | CLOCK OUTPUTS                       |
|-------------|-------------------------------------|
| 0           | OUTPx, OUTNx disabled in Hi-Z state |
| 1 (default) | OUTPx, OUTNx enabled                |

#### 9.4.1 LVDS Output Termination

TI recommends that unused outputs are terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode  $V_{OS}$ ) in the outputs being used.

The LMK1D1204P can be connected to LVDS receiver inputs with DC and AC coupling as shown in [Figure 9-1](#) and [Figure 9-2](#), respectively.

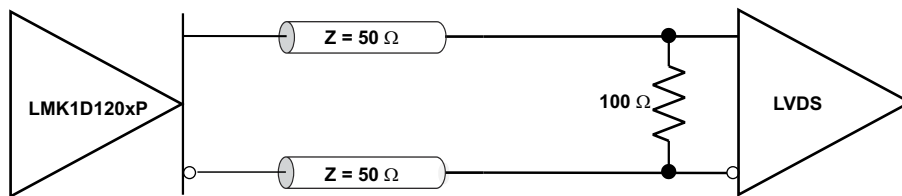


Figure 9-1. Output DC Termination

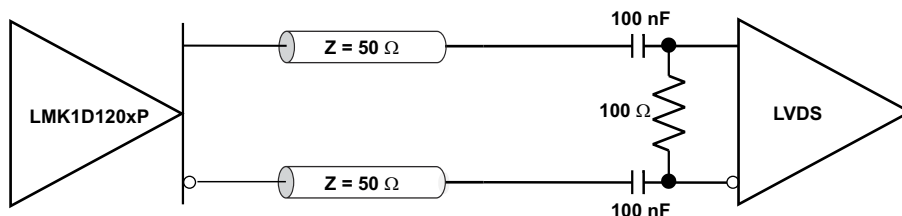


Figure 9-2. Output AC Termination (With the Receiver Internally Biased)

#### 9.4.2 Input Termination

The LMK1D1204P inputs can be interfaced with LVDS, LVPECL, HCSL, or LVCMOS drivers.

LVDS drivers can be connected to LMK1D1204P inputs with DC and AC coupling as shown [Figure 9-3](#) and [Figure 9-4](#), respectively.

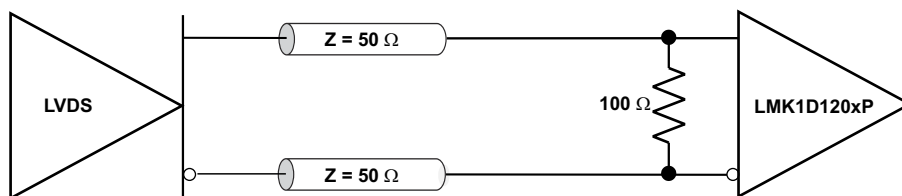


Figure 9-3. LVDS Clock Driver Connected to LMK1D1204P Input (DC-Coupled)

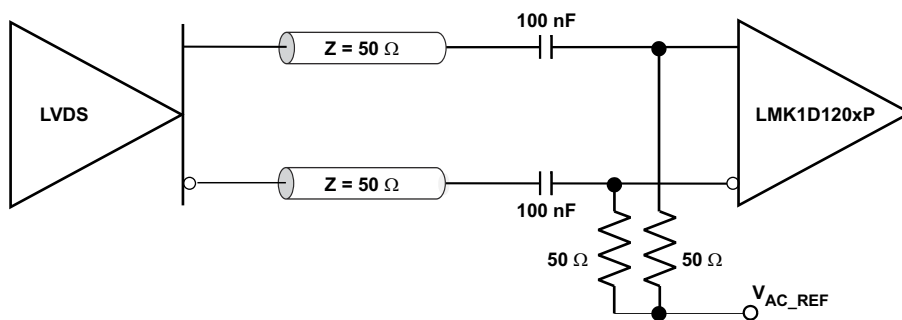


Figure 9-4. LVDS Clock Driver Connected to LMK1D1204P Input (AC-Coupled)

[Figure 9-5](#) shows how to connect LVPECL inputs to the LMK1D1204P. The series resistors are required to reduce the LVPECL signal swing if the signal swing is  $>1.6 V_{PP}$ .

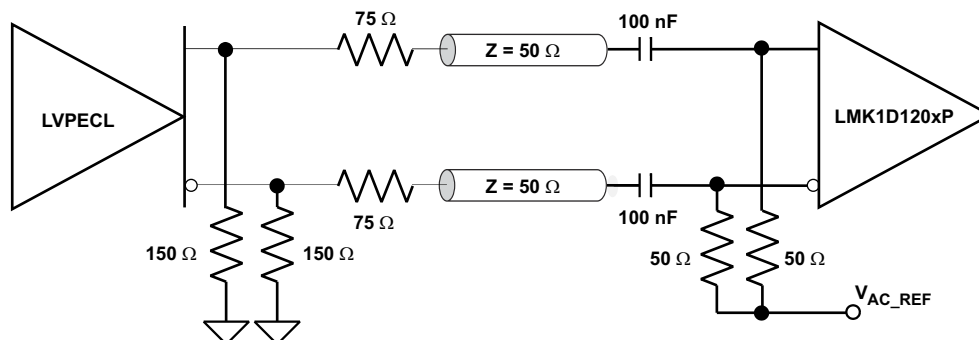


Figure 9-5. LVPECL Clock Driver Connected to LMK1D1204P Input

Figure 9-6 shows how to couple a LVCMOS clock input to the LMK1D1204P directly.

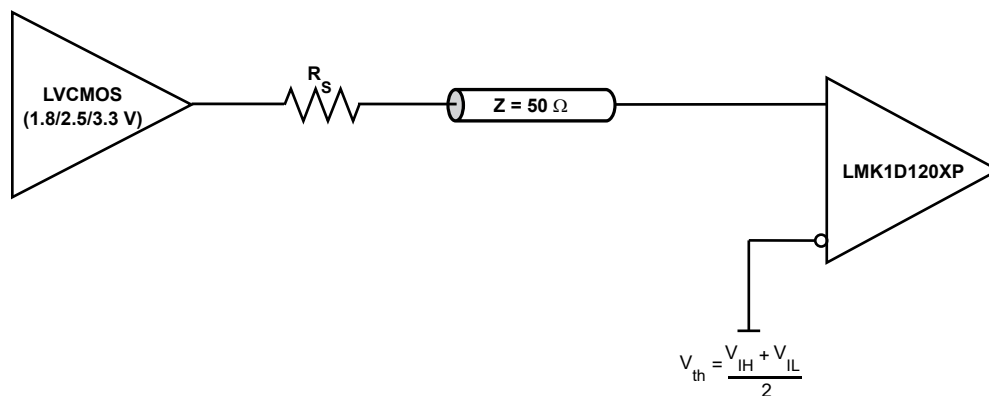


Figure 9-6. 1.8-V, 2.5-V, or 3.3-V LVCMOS Clock Driver Connected to LMK1D1204P Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

The LMK1D1204P is a low additive jitter universal to LVDS fan-out buffer with two selectable inputs and pin controlled output enables. The small package size, low output skew, low propagation delay and low additive jitter of this device is designed for applications that require high-performance clock distribution as well as for low-power and space-constraint applications.

### 10.2 Typical Application

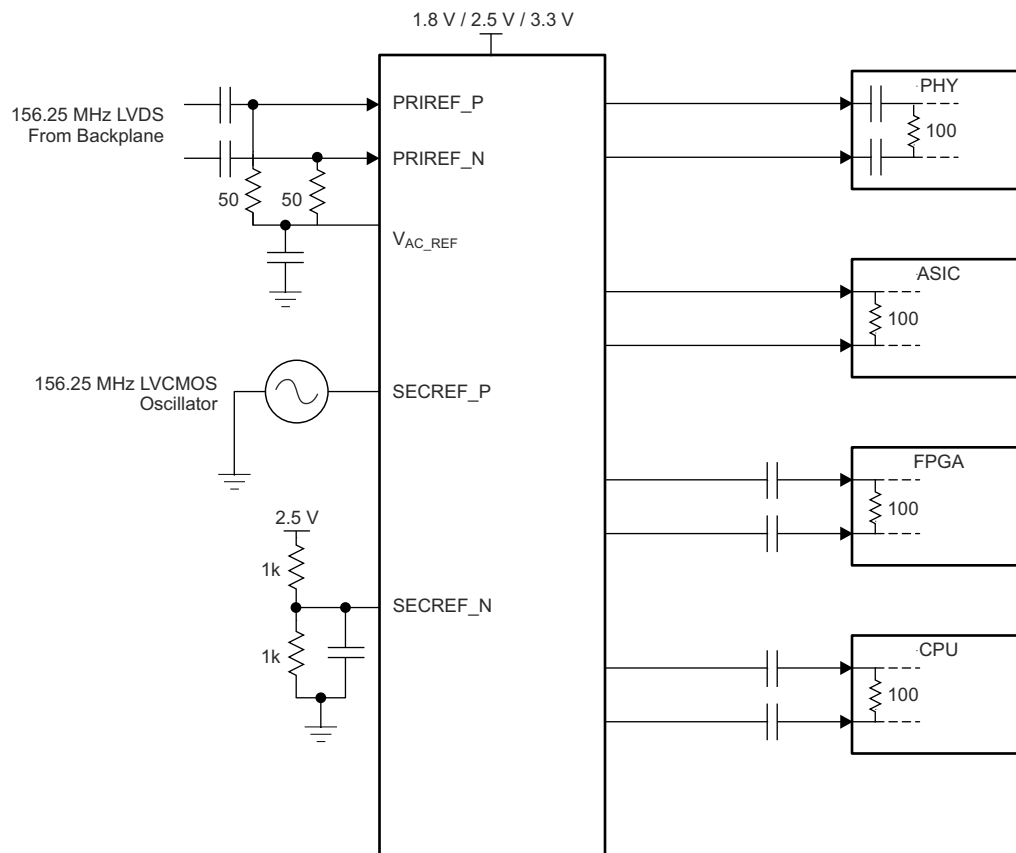


Figure 10-1. Fan-Out Buffer for Line Card Application

### 10.2.1 Design Requirements

The LMK1D1204P shown in [Figure 10-1](#) is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz, LVCMOS, 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1- $\mu$ F capacitors are used to reduce noise on both  $V_{AC\_REF}$  and  $SECREP\_N$ . Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC coupling with an LVDS driver such as the LMK1D1204P. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D1204P. Again, no additional components are required.
- The FPGA requires external AC coupling, but has internal termination. 0.1- $\mu$ F capacitors are placed to provide AC coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- The unused outputs of the LMK1D1204P can be disabled using the corresponding OEx pin. This results in a lower power consumption.

### 10.2.2 Detailed Design Procedure

See [Input Termination](#) for proper input terminations, dependent on single-ended or differential inputs.

See [LVDS Output Termination](#) for output termination schemes depending on the receiver application.

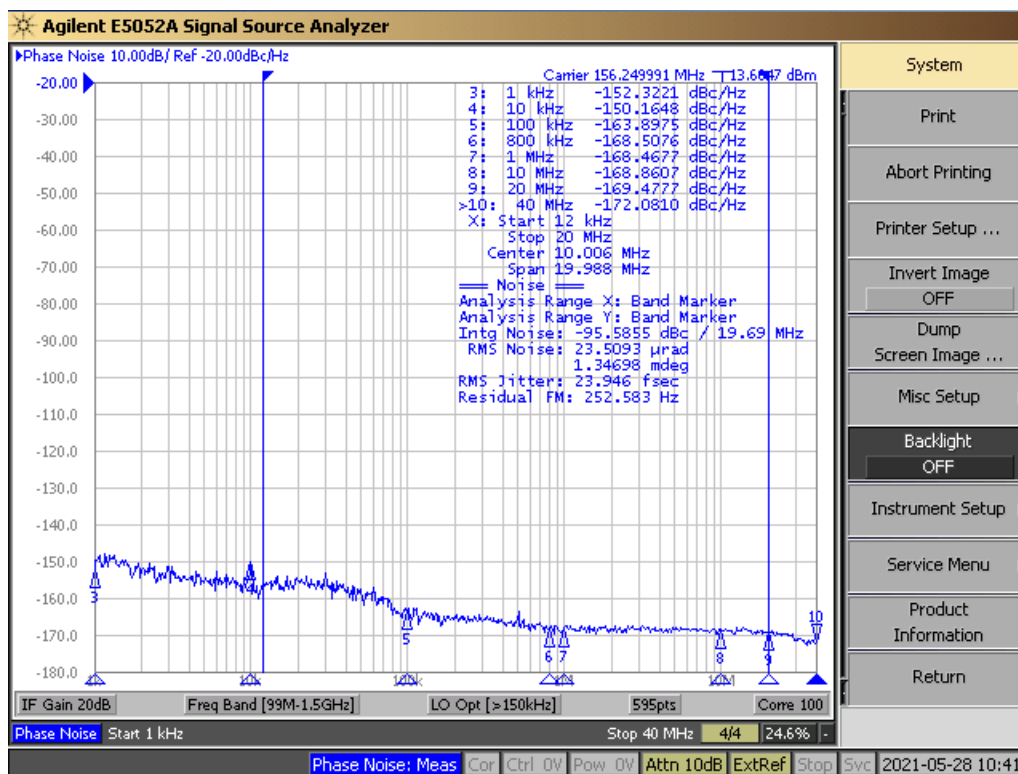
Unused outputs can be disabled using the corresponding OEx pin setting according to [Table 9-2](#). Disabling the outputs also eliminates requirement of termination resistors.

In this example, the PHY, ASIC, FPGA and CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

See [Power Supply Recommendations](#) for recommended filtering techniques. A reference layout is provided in [Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board user's guide](#) (SCAU043).

### 10.2.3 Application Curves

This section shows the low additive noise for the LMK1D1204P. The low noise 156.25-MHz source with 24-fs RMS jitter shown in Figure 10-2 drives the LMK1D1204P, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (see Figure 10-3). The resultant additive jitter is 39.7-fs RMS for this configuration.



Note: Reference signal is a low-noise Rhode and Schwarz SMA100B

Figure 10-2. LMK1D1204P Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)

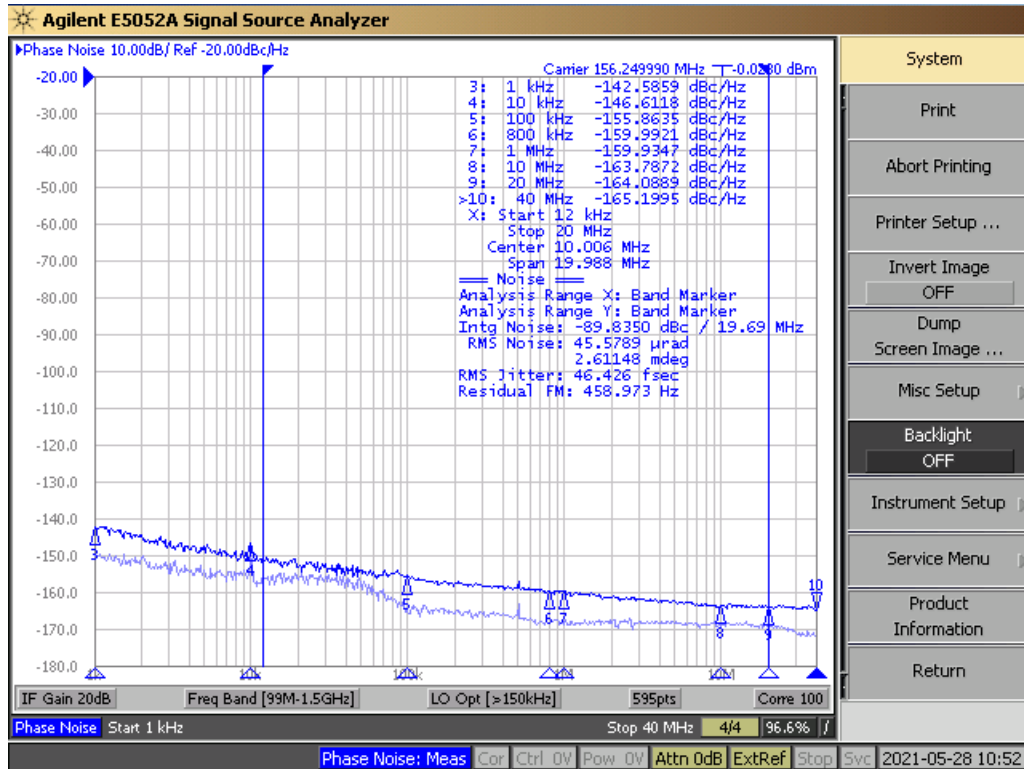


Figure 10-3. LMK1D1204P Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

### 10.3 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1- $\mu$ F) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver. These ferrite beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 10-4 shows this recommended power-supply decoupling method.

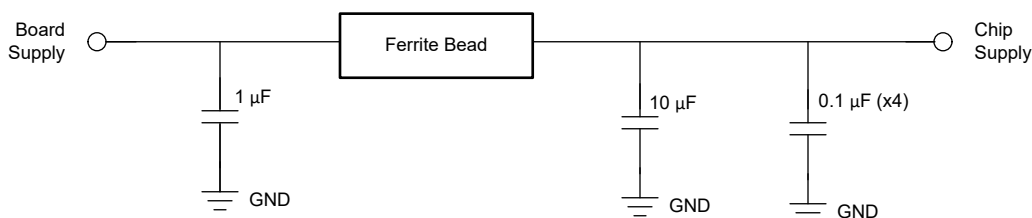


Figure 10-4. Power Supply Decoupling

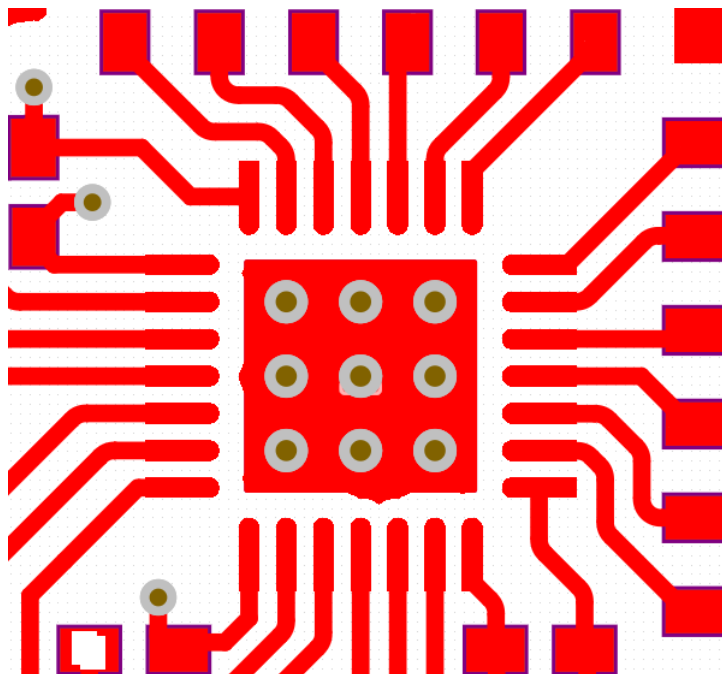
## 10.4 Layout

### 10.4.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the PCB. To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. [Figure 10-5](#) and [Figure 10-6](#) show the recommended land and via patterns for the 28-pin LMK1D1204P device.

### 10.4.2 Layout Examples



**Figure 10-5. Recommended PCB Layout, Top Layer**

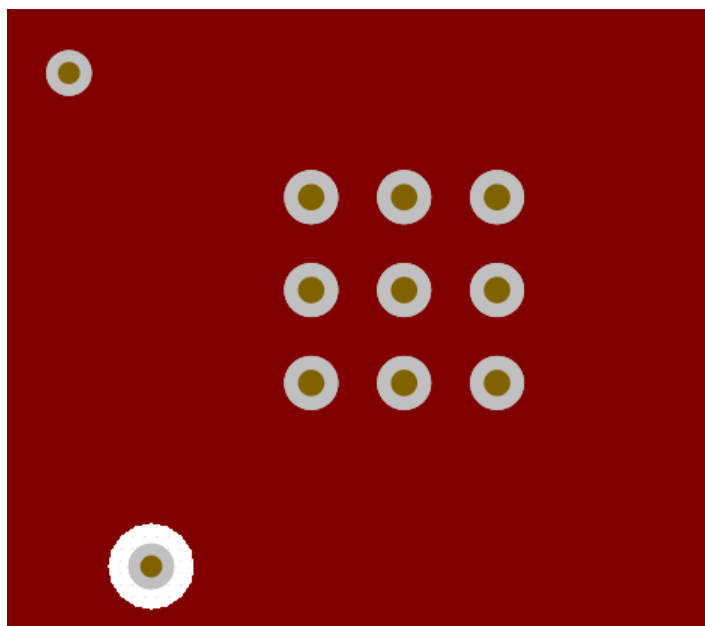


Figure 10-6. Recommended PCB Layout, GND Layer

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board user's guide](#)
- Texas Instruments, [Power Consumption of LVPECL and LVDS Analog Design Journal](#)
- Texas Instruments, [Using Thermal Calculation Tools for Analog Components application note](#)

### 11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LMK1D1204PRHDR</a> | Active        | Production           | VQFN (RHD)   28 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 105   | LMK1D<br>1204P      |
| LMK1D1204PRHDR.B               | Active        | Production           | VQFN (RHD)   28 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 105   | LMK1D<br>1204P      |
| <a href="#">LMK1D1204PRHDT</a> | Active        | Production           | VQFN (RHD)   28 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 105   | LMK1D<br>1204P      |
| LMK1D1204PRHDT.B               | Active        | Production           | VQFN (RHD)   28 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 105   | LMK1D<br>1204P      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK1D1204PRHDR | VQFN         | RHD             | 28   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LMK1D1204PRHDT | VQFN         | RHD             | 28   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK1D1204PRHDR | VQFN         | RHD             | 28   | 3000 | 360.0       | 360.0      | 36.0        |
| LMK1D1204PRHDT | VQFN         | RHD             | 28   | 250  | 210.0       | 185.0      | 35.0        |

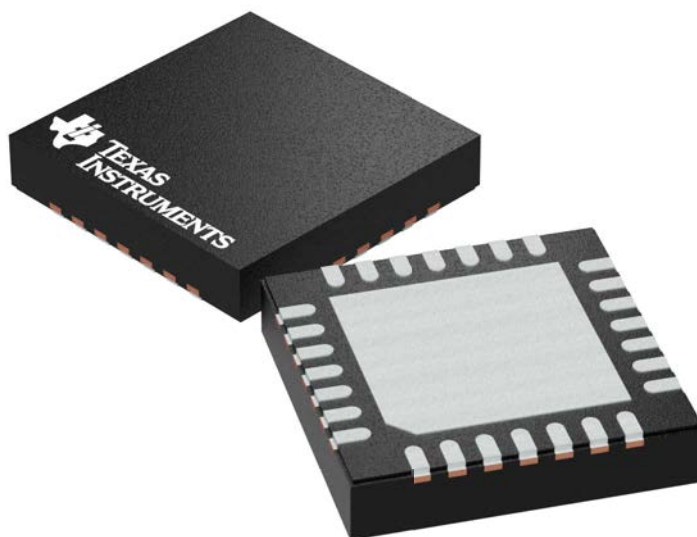
## GENERIC PACKAGE VIEW

**RHD 28**

**VQFN - 1 mm max height**

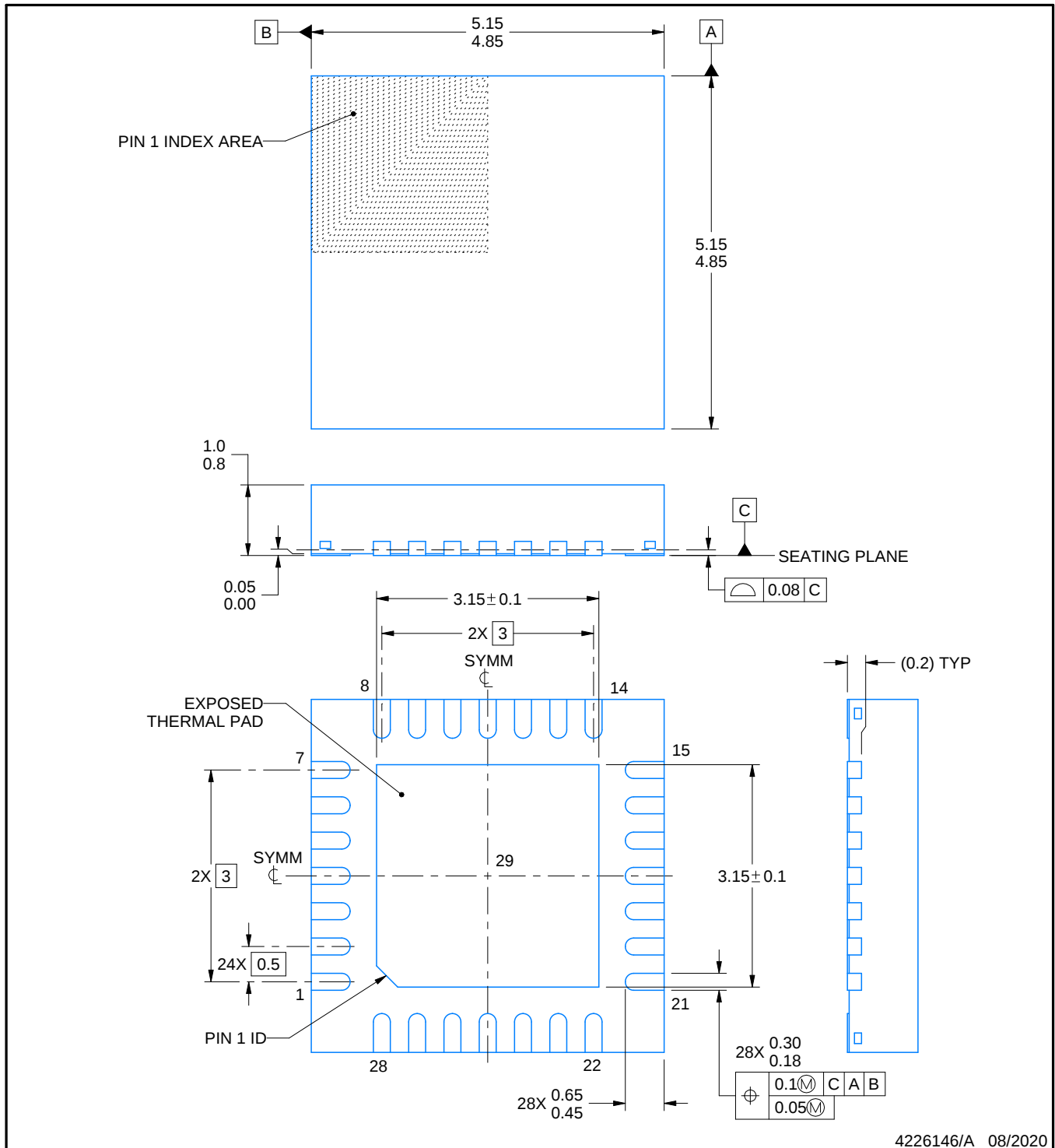
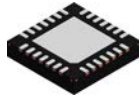
5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204400/G



## NOTES:

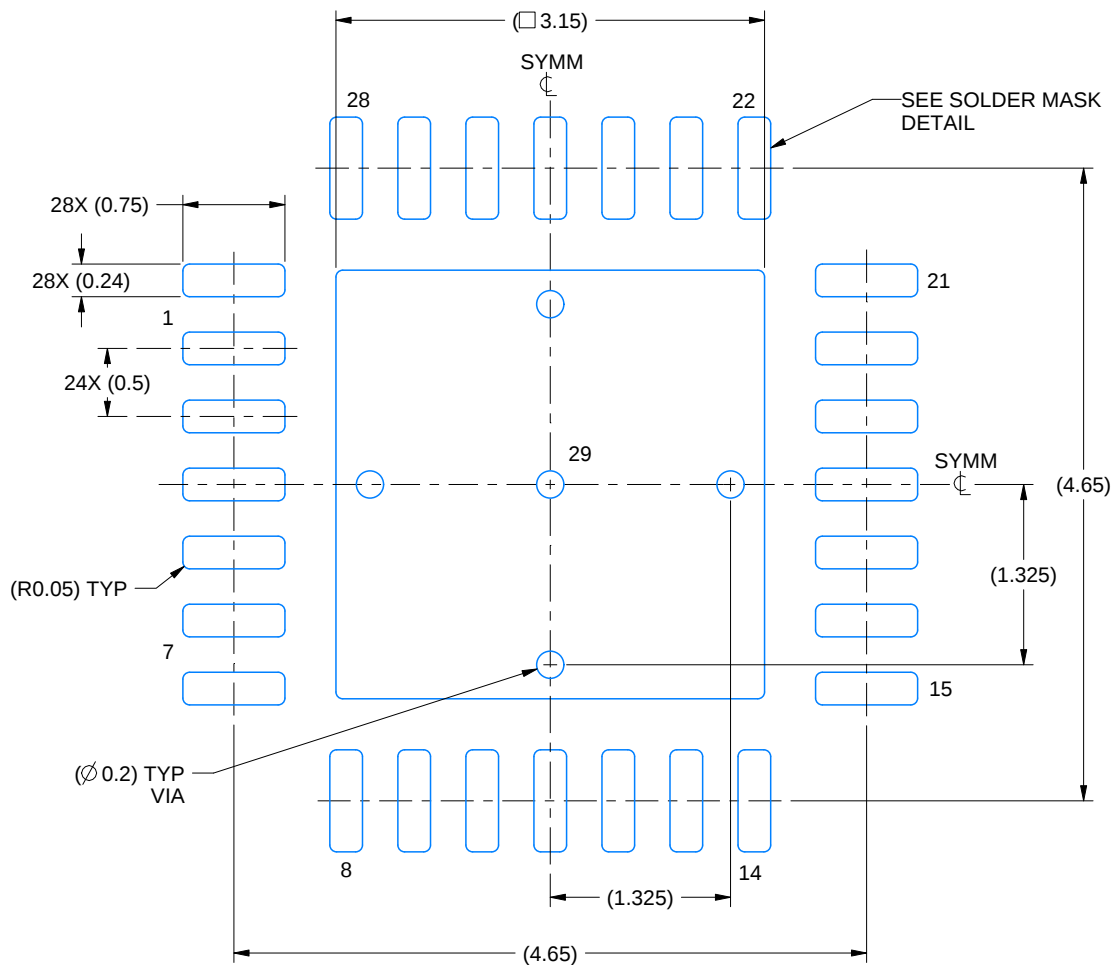
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

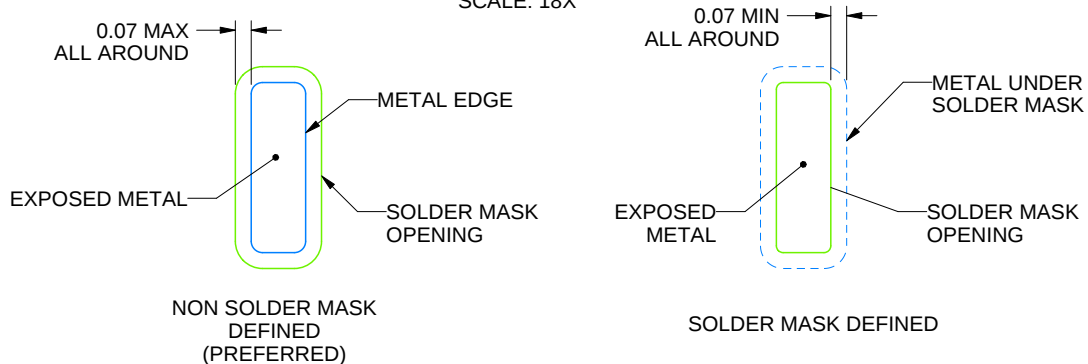
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 18X



SOLDER MASK DETAILS

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NOTES: (continued)

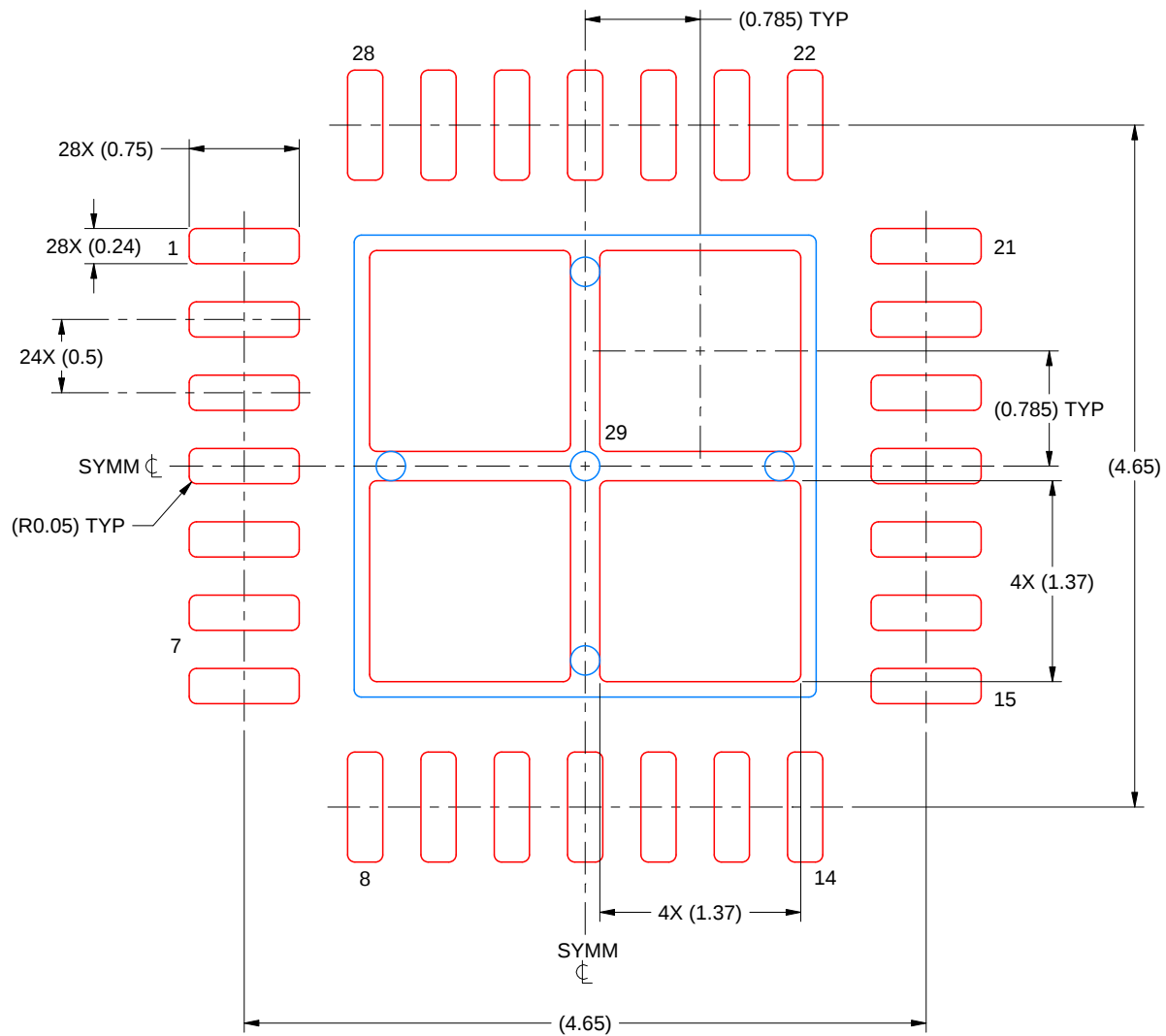
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 29  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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