TEXAS INSTRUMENTS
LMKDB1120, LMKDB1108
SNAS855B – NOVEMBER 2023 – REVISED FEBRUARY 2024

LMKDB1xxx PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX

1 Features

- LP-HCSL clock buffer and clock MUX that support:
  - PCIe Gen 1 to Gen 6
  - CC (Common Clock) and IR (Independent Reference) PCIe architectures
  - Input clock with or without SSC
- DB2000QL compliant:
  - All devices meet DB2000QL specifications
  - LMKDB1120 is pin-compatible to DB2000QL
- Extremely low additive jitter:
  - 31fs maximum 12kHz to 20MHz RMS additive jitter at 156.25MHz
  - 13fs maximum additive jitter for PCIe Gen 4
  - 5fs maximum additive jitter for PCIe Gen 5
  - 3fs maximum additive jitter for PCIe Gen 6
- Fail-safe input
- Flexible power-up sequence
- Automatic output disable
- Individual output enable
- SBI (Side Band Interface) for high-speed output enable or disable
- LOS (Loss of Signal) input detection
- 85Ω or 100Ω output impedance
- 1.8V / 3.3V ± 10% power supply
- –40°C to 105°C ambient temperature

2 Applications

- High Performance Computing
- Server Motherboard
- NIC/SmartNIC
- Hardware Accelerator

3 Description

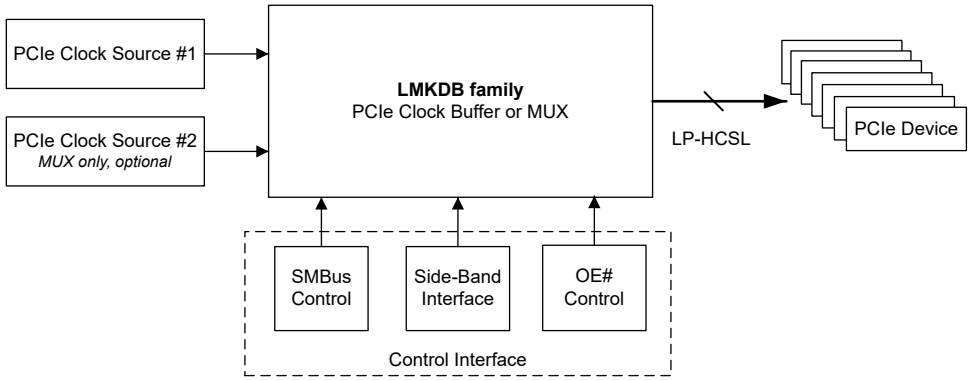
The LMKDB devices are a family of extremely-low-jitter LP-HCSL buffers and MUX that support PCIe Gen 1 to Gen 6 and are DB2000QL compliant. The devices provide flexible power-up sequence, fail-safe inputs, individual output enable and disable pins, loss of input signal (LOS) detection and automatic output disable features, as well as excellent power supply noise rejection performance.

Both 1.8V and 3.3V supply voltages are supported. For LMKDB1120, 1.8V power supply saves 250mW power compared to 3.3V.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMKDB1120	NPP (TLGA, 80)	6mm × 6mm
LMKDB1108	RKP (VQFN, 40)	5mm × 5mm
LMKDB1104(3)	REX (VQFN, 28)	4mm × 4mm
LMKDB1204(3)	REX (VQFN, 28)	4mm × 4mm
LMKDB1202(3)	REY (VQFN, 20)	3mm × 3mm
LMKDB1102(3)	REY (VQFN, 20)	3mm × 3mm

(1) For all available packages, see Section 14.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) This device is in preview only.



Typical Application

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4 Device Comparison

Table 4-1. Device Comparison

PART NUMBER	DESCRIPTION
LMKDB1120Z85	1 input, 20 outputs, 85-Ω output impedance
LMKDB1120Z100	1 input, 20 outputs, 100-Ω output impedance
LMKDB1108Z85	1 input, 8 outputs, 85-Ω output impedance
LMKDB1108Z100	1 input, 8 outputs, 100-Ω output impedance
LMKDB1104Z85(1)	1 input, 4 outputs, 85-Ω output impedance
LMKDB1104Z100(1)	1 input, 4 outputs, 100-Ω output impedance
LMKDB1204(1)	2 inputs, 4 outputs, 85-Ω or 100-Ω output impedance
LMKDB1202(1)	2 inputs, 2 outputs, 85-Ω or 100-Ω output impedance
LMKDB1102(1)	1 input, 2 outputs, 85-Ω or 100-Ω output impedance

(1) This device is in preview only.

5 Pin Configuration and Functions

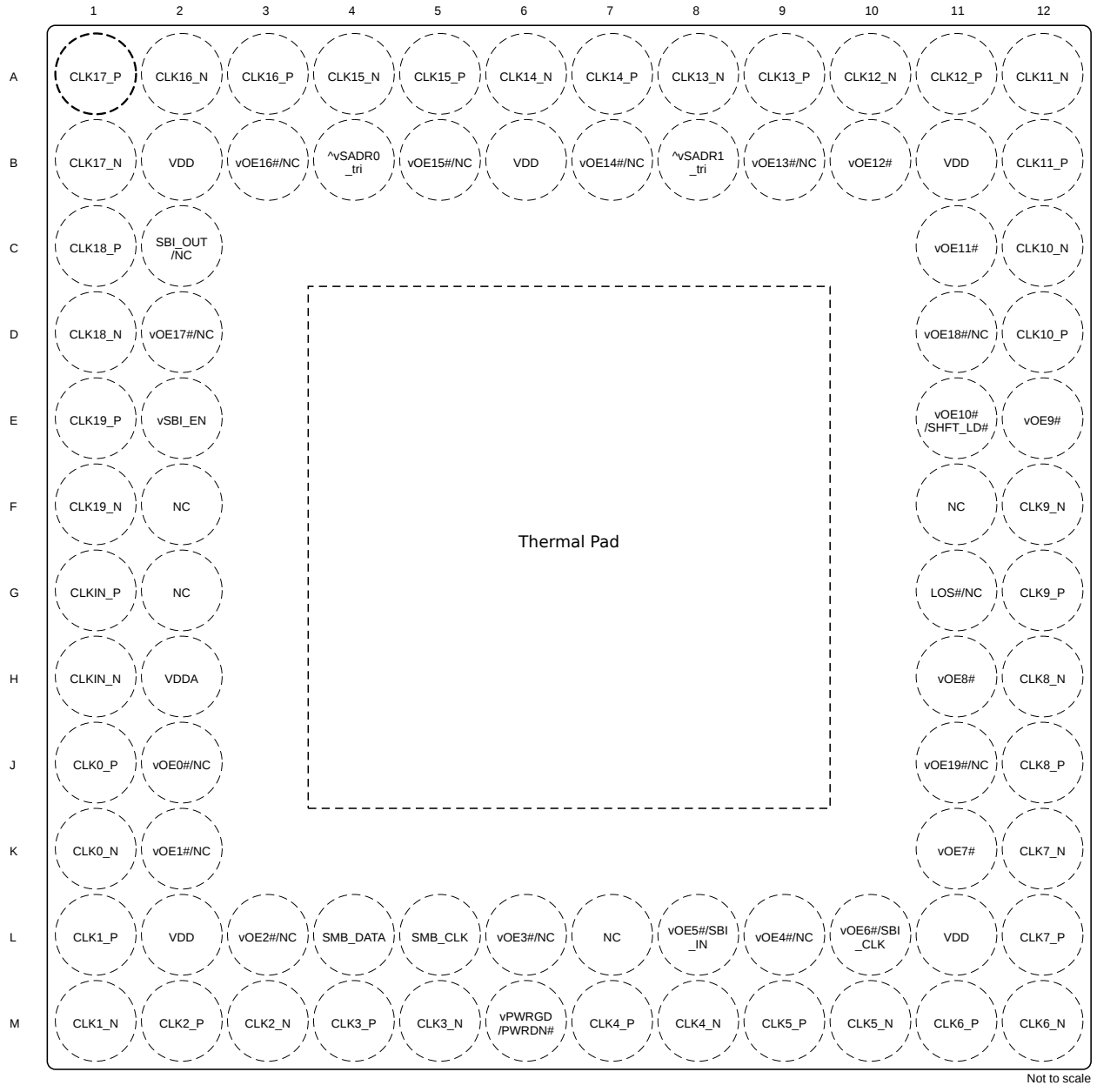


Figure 5-1. LMKDB1120 NPP Package, 80-Pin TLGA (Top View)

Table 5-1. LMKDB1120 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN_P	G1	I	Differential clock input
CLKIN_N	H1	I	Differential clock input
CLK0_P	J1	O	LP-HCSL differential clock output 0. No connect if unused.
CLK0_N	K1	O	LP-HCSL differential clock output 0. No connect if unused.
CLK1_P	L1	O	LP-HCSL differential clock output 1. No connect if unused.
CLK1_N	M1	O	LP-HCSL differential clock output 1. No connect if unused.

Table 5-1. LMKDB1120 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLK2_P	M2	O	LP-HCSL differential clock output 2. No connect if unused.
CLK2_N	M3	O	LP-HCSL differential clock output 2. No connect if unused.
CLK3_P	M4	O	LP-HCSL differential clock output 3. No connect if unused.
CLK3_N	M5	O	LP-HCSL differential clock output 3. No connect if unused.
CLK4_P	M7	O	LP-HCSL differential clock output 4. No connect if unused.
CLK4_N	M8	O	LP-HCSL differential clock output 4. No connect if unused.
CLK5_P	M9	O	LP-HCSL differential clock output 5. No connect if unused.
CLK5_N	M10	O	LP-HCSL differential clock output 5. No connect if unused.
CLK6_P	M11	O	LP-HCSL differential clock output 6. No connect if unused.
CLK6_N	M12	O	LP-HCSL differential clock output 6. No connect if unused.
CLK7_P	L12	O	LP-HCSL differential clock output 7. No connect if unused.
CLK7_N	K12	O	LP-HCSL differential clock output 7. No connect if unused.
CLK8_P	J12	O	LP-HCSL differential clock output 8. No connect if unused.
CLK8_N	H12	O	LP-HCSL differential clock output 8. No connect if unused.
CLK9_P	G12	O	LP-HCSL differential clock output 9. No connect if unused.
CLK9_N	F12	O	LP-HCSL differential clock output 9. No connect if unused.
CLK10_P	D12	O	LP-HCSL differential clock output 10. No connect if unused.
CLK10_N	C12	O	LP-HCSL differential clock output 10. No connect if unused.
CLK11_P	B12	O	LP-HCSL differential clock output 11. No connect if unused.
CLK11_N	A12	O	LP-HCSL differential clock output 11. No connect if unused.
CLK12_P	A11	O	LP-HCSL differential clock output 12. No connect if unused.
CLK12_N	A10	O	LP-HCSL differential clock output 12. No connect if unused.
CLK13_P	A9	O	LP-HCSL differential clock output 13. No connect if unused.
CLK13_N	A8	O	LP-HCSL differential clock output 13. No connect if unused.
CLK14_P	A7	O	LP-HCSL differential clock output 14. No connect if unused.
CLK14_N	A6	O	LP-HCSL differential clock output 14. No connect if unused.
CLK15_P	A5	O	LP-HCSL differential clock output15. No connect if unused.
CLK15_N	A4	O	LP-HCSL differential clock output15. No connect if unused.
CLK16_P	A3	O	LP-HCSL differential clock output 16. No connect if unused.
CLK16_N	A2	O	LP-HCSL differential clock output 16. No connect if unused.
CLK17_P	A1	O	LP-HCSL differential clock output 17. No connect if unused.
CLK17_N	B1	O	LP-HCSL differential clock output 17. No connect if unused.
CLK18_P	C1	O	LP-HCSL differential clock output 18. No connect if unused.
CLK18_N	D1	O	LP-HCSL differential clock output 18. No connect if unused.
CLK19_P	E1	O	LP-HCSL differential clock output 19. No connect if unused.
CLK19_N	F1	O	LP-HCSL differential clock output 19. No connect if unused.
DAP	GND	G	Ground. Thermal Pad
LOS#/NC	G11	O	Loss of Input Clock Signal Active Low/No Connect. Open drain. Requires external pullup resistor. This pin can be left no connect to match with DB2000QL pinout. • Low = Invalid input clock. • High = Valid input clock.
NC	F2	NC	No Connect
NC	F11	NC	No Connect
NC	G2	NC	No Connect

Table 5-1. LMKDB1120 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	L7	NC	No Connect
SBI_OUT/NC	C2	O	SBI Data Output/No Connect. This pin can be left no connect to match with DB2000QL pinout.
SMB_DATA	L4	I/O	SMBus Data. Requires external pullup resistor. No connect if unused.
SMB_CLK	L5	I	SMBus Clock. Requires external pullup resistor. No connect if unused.
VDDA	H2	P	Analog power supply. Additional power supply filtering is recommended. See *Power Supply Recommendations* for details.
VDD	B2	P	Power supply.
VDD	B6	P	Power supply.
VDD	B11	P	Power supply.
VDD	L2	P	Power supply.
VDD	L11	P	Power supply.
vOE0#/NC	J2	I	Output Enable for CLK0 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE1#/NC	K2	I	Output Enable for CLK1 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE2#/NC	L3	I	Output Enable for CLK2 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE3#/NC	L6	I	Output Enable for CLK3 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE4#/NC	L9	I	Output Enable for CLK4 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE5#/SBI_IN	L8	I	Output Enable for CLK5 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. No connect if unused.
vOE6#/SBI_CLK	L10	I	Output Enable for CLK6 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.
vOE7#	K11	I	Output Enable for CLK7 Active Low. Internal pulldown resistor. No connect if unused.
vOE8#	H11	I	Output Enable for CLK8 Active Low. Internal pulldown resistor. No connect if unused.
vOE9#	E12	I	Output Enable for CLK9 Active Low. Internal pulldown resistor. No connect if unused.
vOE10#/SHFT_LD#	E11	I	Output Enable for CLK10 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. No connect if unused.
vOE11#	C11	I	Output Enable for CLK11 Active Low. Internal pulldown resistor. No connect if unused.
vOE12#	B10	I	Output Enable for CLK12 Active Low. Internal pulldown resistor. No connect if unused.
vOE13#/NC	B9	I	Output Enable for CLK13 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE14#/NC	B7	I	Output Enable for CLK14 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE15#/NC	B5	I	Output Enable for CLK15 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE16#/NC	B3	I	Output Enable for CLK16 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE17#/NC	D2	I	Output Enable for CLK17 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE18#/NC	D11	I	Output Enable for CLK18 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.
vOE19#/NC	J11	I	Output Enable for CLK19 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.

Table 5-1. LMKDB1120 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
vPWRGD/PWRDN#	M6	I	Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. • On the first low-to-high transition, functions as Power Good pin which starts up the device • On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. – Low = power-down mode – High = normal operation mode
vSBI_EN	E2	I	SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. • Low at power-up = SBI interface disabled. Pin L8, L10, E11 function as OE pins. • High at power-up = SBI interface enabled. Pin L8, L10, E11 function as SBI interface pins. SMBus and other OE pins remain functional.
^vSADR1_tri	B8	I	SMBus Address 3-level input pin. Internal pullup and pulldown resistors.
^vSADR0_tri	B4	I	SMBus Address 3-level input pin. Internal pullup and pulldown resistors.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

Figure 5-2. LMKDB1108 RKP Package, 40-Pin VQFN (Top View)

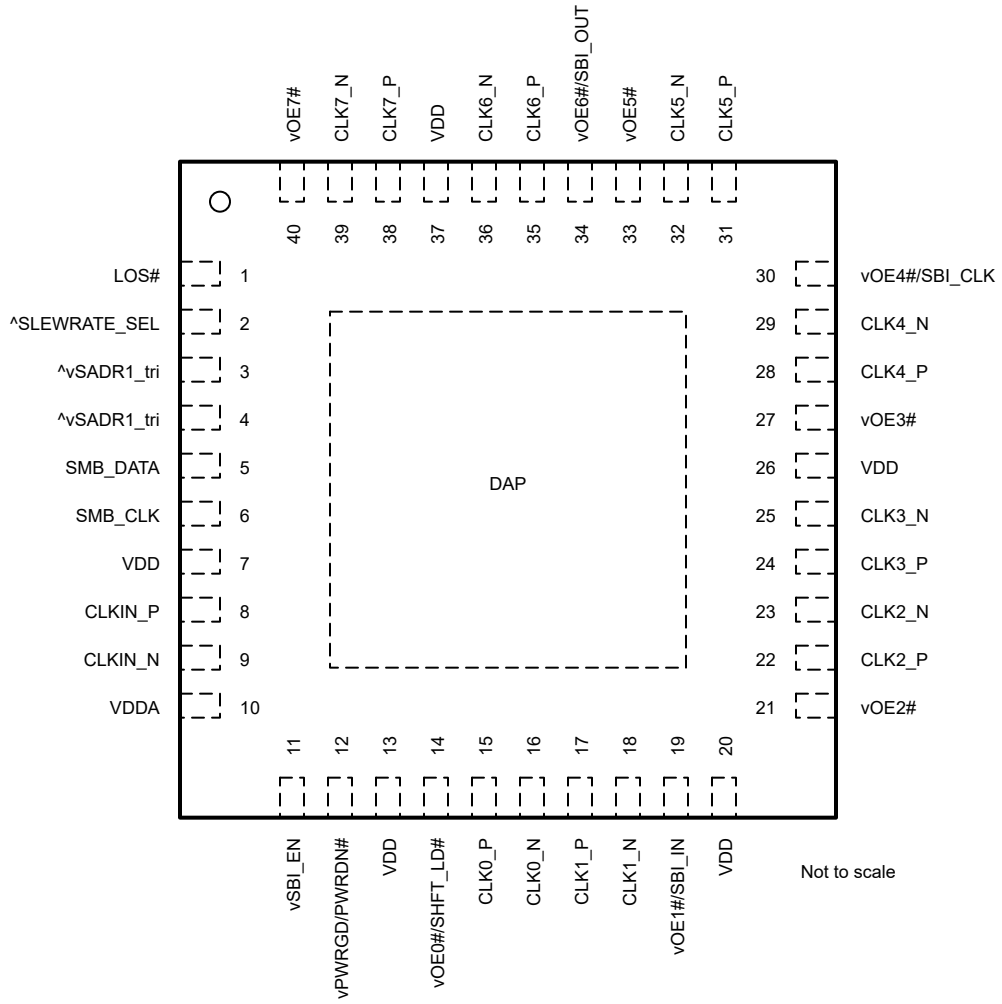


Table 5-2. LMKDB1108 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN_P	8	I	Differential clock input
CLKIN_N	9	I	Differential clock input
CLK0_P	15	O	LP-HCSL differential clock output 0. No connect if unused.
CLK0_N	16	O	LP-HCSL differential clock output 0. No connect if unused.
CLK1_P	17	O	LP-HCSL differential clock output 1. No connect if unused.
CLK1_N	18	O	LP-HCSL differential clock output 1. No connect if unused.
CLK2_P	22	O	LP-HCSL differential clock output 2. No connect if unused.
CLK2_N	23	O	LP-HCSL differential clock output 2. No connect if unused.
CLK3_P	24	O	LP-HCSL differential clock output 3. No connect if unused.
CLK3_N	25	O	LP-HCSL differential clock output 3. No connect if unused.
CLK4_P	28	O	LP-HCSL differential clock output 4. No connect if unused.
CLK4_N	29	O	LP-HCSL differential clock output 4. No connect if unused.
CLK5_P	31	O	LP-HCSL differential clock output 5. No connect if unused.
CLK5_N	32	O	LP-HCSL differential clock output 5. No connect if unused.
CLK6_P	35	O	LP-HCSL differential clock output 6. No connect if unused.

Table 5-2. LMKDB1108 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLK6_N	36	O	LP-HCSL differential clock output 6. No connect if unused.
CLK7_P	38	O	LP-HCSL differential clock output 7. No connect if unused.
CLK7_N	39	O	LP-HCSL differential clock output 7. No connect if unused.
vPWRGD/PWRDN#	12	I	Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. • On the first low-to-high transition, functions as Power Good pin which starts up the device • On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. – Low = power-down mode – High = normal operation mode
vOE0#/SHFT_LD#	14	I	Output Enable for CLK0 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. No connect if unused.
vOE1#/SBI_IN	19	I	Output Enable for CLK1 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. No connect if unused.
vOE2#	21	I	Output Enable for CLK2 Active Low. Internal pulldown resistor. No connect if unused.
vOE3#	27	I	Output Enable for CLK3 Active Low. Internal pulldown resistor. No connect if unused.
vOE4#/SBI_CLK	30	I	Output Enable for CLK4 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.
vOE5#	33	I	Output Enable for CLK5 Active Low. Internal pulldown resistor. No connect if unused.
vOE6#/SBI_OUT	34	I or O	Output Enable for CLK6 Active Low/SBI Data Output. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.
vOE7#	40	I	Output Enable for CLK7 Active Low. Internal pulldown resistor. No connect if unused.
vSBI_EN	11	I	SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. • Low at power-up = SBI interface disabled. Pin 14, 19, 30, 34 function as OE pins. • High at power-up = SBI interface enabled. Pin 14, 19, 30, 34 function as SBI interface pins. SMBus and other OE pins remain functional.
SMB_DATA	5	I/O	SMBus Data. Requires external pullup resistor. No connect if unused.
SMB_CLK	6	I	SMBus Clock. Requires external pullup resistor. No connect if unused.
^vSADR1_tri	3	I	SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.
^vSADR1_tri	4	I	SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.
^SLEWRATE_SEL	2	I	Slew Rate Select for output clocks. Internal pullup resistor. • Low = Slow slew rate • High = Fast slew rate
LOS#	1	O	Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. • Low = Invalid input clock. • High = Valid input clock.
VDD	7	P	Power supply.
VDD	13	P	Power supply.
VDD	20	P	Power supply.
VDD	26	P	Power supply.
VDD	37	P	Power supply.
VDDA	10	P	Analog power supply. Additional power supply filtering is recommended. See Power Supply Recommendations for details.

Table 5-2. LMKDB1108 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DAP	GND	G	Ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

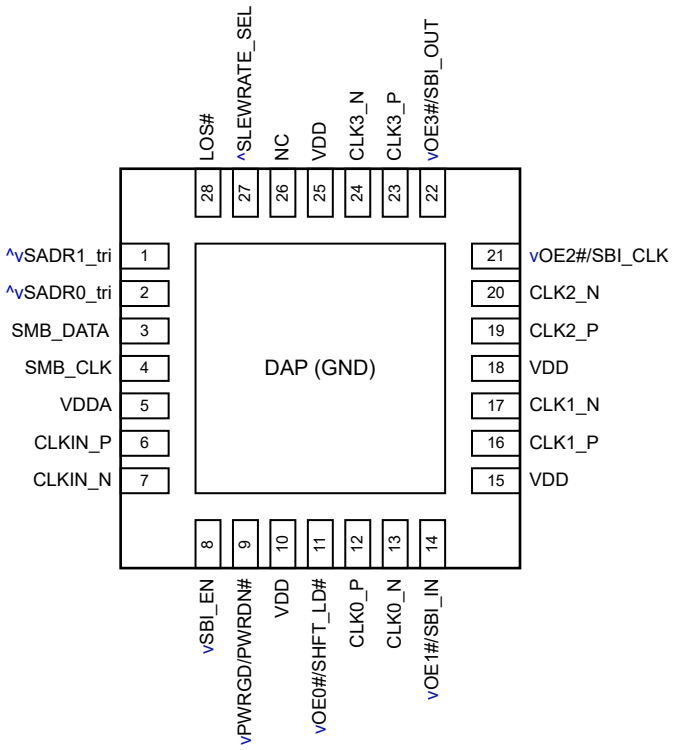


Figure 5-3. LMKDB1104 4 x 4 mm 28-pin QFN

Table 5-3. LMKDB1104 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN_P, CLKIN_N	6, 7	I	Differential clock input
CLK0_P, CLK0_N	12, 13	O	LP-HCSL differential clock output 0
CLK1_P, CLK1_N	16, 17	O	LP-HCSL differential clock output 1
CLK2_P, CLK2_N	19, 20	O	LP-HCSL differential clock output 2
CLK3_P, CLK3_N	23, 24	O	LP-HCSL differential clock output 3
vPWRGD/PWRDN#	9	I	Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. • On the first low-to-high transition, functions as Power Good pin which starts up the device • On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. – Low = power-down mode – High = normal operation mode
vOE0#/SHFT_LD#	11	I	Output Enable for CLK0 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. No connect if unused.
vOE1#/SBI_IN	14	I	Output Enable for CLK1 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. No connect if unused.
vOE2#/SBI_CLK	21	I	Output Enable for CLK2 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.
vOE3#/SBI_OUT	22	I or O	Output Enable for CLK3 Active Low/SBI Data Output. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.

Table 5-3. LMKDB1104 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
vSBI_EN	8	I	SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. • Low at power-up = SBI interface disabled. Pin 11, 14, 21, 22 function as OE pins. • High at power-up = SBI interface enabled. Pin 11, 14, 21, 22 function as SBI interface pins. SMBus and other OE pins remain functional.
SMB_DATA	3	I/O	SMBus Data. Requires external pullup resistor. No connect if unused.
SMB_CLK	4	I	SMBus Clock. Requires external pullup resistor. No connect if unused.
^vSADR1_tri	1	I	SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.
^vSADR0_tri	2	I	SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.
^SLEWRATE_SEL	27	I	Slew Rate Select for output clocks. Internal pullup resistor. • Low = Slow slew rate • High = Fast slew rate
LOS#	28	O	Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. • Low = Invalid input clock. • High = Valid input clock.
VDDA	5	P	Analog power supply. Additional power supply filtering is recommended. See Power Supply Recommendations for details.
VDD	10, 15, 18, 25	P	Power supply.
GND	DAP	G	Ground.
NC	26	NC	No Connect.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

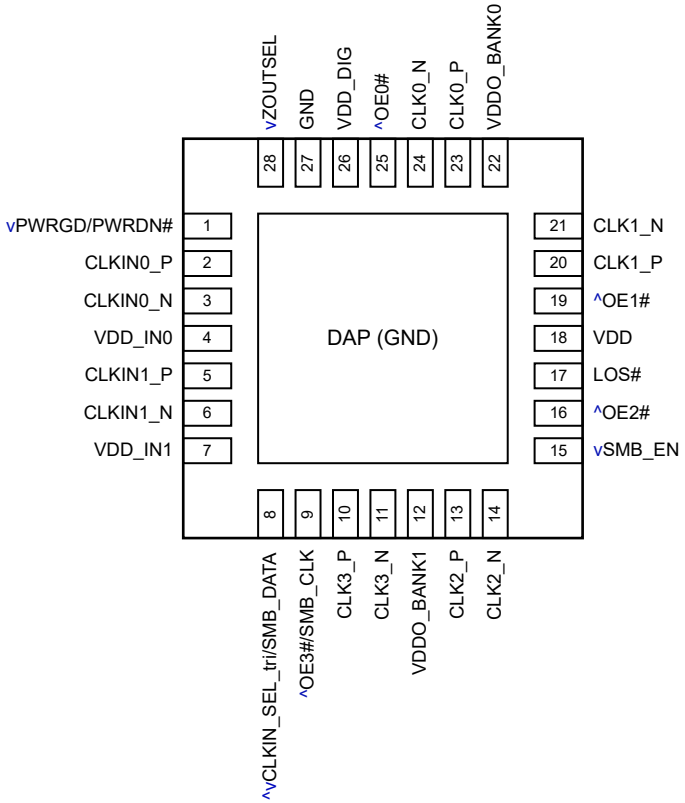


Figure 5-4. LMKDB1204 4 x 4 mm 28-pin QFN

Table 5-4. LMKDB1204 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN0_P, CLKIN0_N	2, 3	I	Differential clock input 0
CLKIN1_P, CLKIN1_N	5, 6	I	Differential clock input 1
CLK3_P, CLK3_N	10, 11	O	LP-HCSL differential clock output 3. Output Bank 1.
CLK2_P, CLK2_N	13, 14	O	LP-HCSL differential clock output 2. Output Bank 1.
CLK1_P, CLK1_N	20, 21	O	LP-HCSL differential clock output 1. Output Bank 0.
CLK0_P, CLK0_N	23, 24	O	LP-HCSL differential clock output 0. Output Bank 0.
vPWRGD/PWRDN#	1	I	Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. • On the first low-to-high transition, functions as Power Good pin which starts up the device • On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. – Low = power-down mode – High = normal operation mode
^OE3#/SMB_CLK	9	I	Output Enable for CLK3 Active Low/SMBus Clock. Internal pullup resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. When used as SMBus Clock pin, external pullup resistor is required. No connect if unused.
^OE2#	16	I	Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.
^OE1#	19	I	Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused.
^OE0#	25	I	Output Enable for CLK0 Active Low. Internal pullup resistor. No connect if unused.

Table 5-4. LMKDB1204 Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
^vCLKIN_SEL_tri/ SMB_DATA	8	I or I/O	3-Level Clock Input Select/SMBus Data. Internal pullup and pulldown resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. • When used as CLKIN_SEL_tri pin: – Low = CLKIN0 goes to all outputs – Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1 – High = CLKIN1 goes to all outputs • When used as SMBus Data pin, external pullup resistor is required.
vSMB_EN	15	I	SMBus Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. • Low at power-up = SMBus disabled. Pin 8 is CLKIN_SEL_tri and Pin 9 is OE5#. • High at power-up = SMBus enabled. Pin 8 is SMB_DATA and Pin 9 is SMB_CLK.
vZOUT_SEL	28	I	LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. • Low = 85 Ω • High = 100 Ω
LOS#	17	O	Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. • Low = Invalid input clock. • High = Valid input clock.
VDD_IN0	4	P	Power supply for CLKIN0.
VDD_IN1	7	P	Power supply for CLKIN1.
VDDO_BANK1	12	P	Power supply for output bank 1 (OUT2 and OUT3)
VDDO_BANK0	22	P	Power supply for output bank 0 (OUT0 and OUT1)
VDD_DIG	26	P	Power supply for digital
VDD	18	P	Power supply
GND	27, DAP	G	Ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

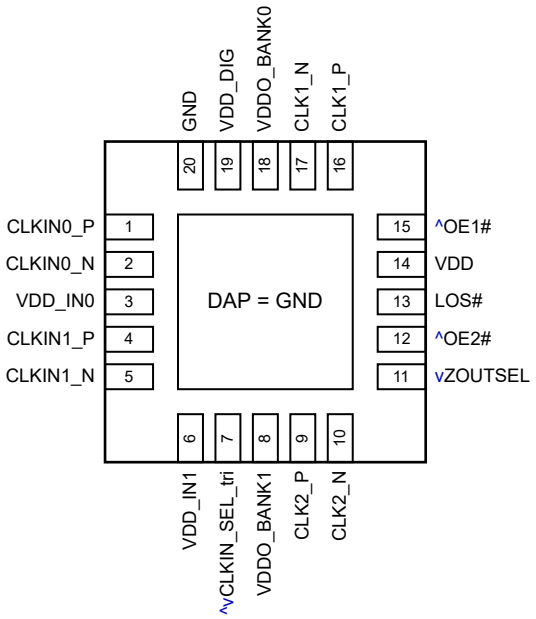


Figure 5-5. LMKDB1202 3 x 3 mm 20-pin QFN

Table 5-5. LMKDB1202 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN0_P, CLKIN0_N	1, 2	I	Differential clock input 0
CLKIN1_P, CLKIN1_N	4, 5	I	Differential clock input 1
CLK2_P, CLK2_N	9, 10	O	LP-HCSL differential clock output 2. Output Bank 1.
CLK1_P, CLK1_N	16, 17	O	LP-HCSL differential clock output 1. Output Bank 0.
^OE2#	12	I	Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.
^OE1#	15	I	Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused. This pin requires either of below conditions to dynamically enable or disable the CLK1 after power-up. If CLK1 stays enabled or disabled after power-up, then below conditions do not need to be met. • This pin is driven low or high at ≥0.1 V/ns slew rate. • The resistance used to drive this pin is ≤1 kΩ. The above requirement is only needed for Pin 15.
^vCLKIN_SEL_tri	7	I	3-Level Clock Input Select • Low = CLKIN0 goes to all outputs • Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1 • High = CLKIN1 goes to all outputs
vZOUT_SEL	11	I	LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. • Low = 85 Ω • High = 100 Ω
LOS#	13	O	Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. • Low = Invalid input clock. • High = Valid input clock.
VDD_IN0	3	P	Power supply for CLKIN0
VDD_IN1	6	P	Power supply for CLKIN1
VDDO_BANK1	8	P	Power supply for output bank 1 (CLK2)

Table 5-5. LMKDB1202 Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VDD	14	P	Power supply
VDDO_BANK0	18	P	Power supply for output bank 0 (CLK1)
VDD_DIG	19	P	Power supply for digital
GND	20, DAP	G	Ground.

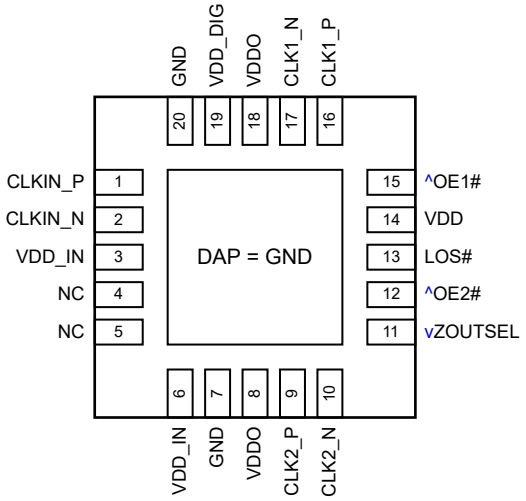


Figure 5-6. LMKDB1102 3 x 3 mm 20-pin QFN

Table 5-6. LMKDB1102 Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLKIN_P,	1	I	Differential clock input
CLKIN_N	2	I	Differential clock input
NC	4, 5	I	No connect. Leave floating
CLK2_P	9	O	LP-HCSL differential clock output 2
CLK2_N	10	O	LP-HCSL differential clock output 2
CLK1_P	16	O	LP-HCSL differential clock output 1
CLK1_N	17	O	LP-HCSL differential clock output 1
^OE2#	12	I	Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.
^OE1#	15	I	Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused. This pin requires either of below conditions to dynamically enable or disable the CLK1 after power-up. If CLK1 stays enabled or disabled after power-up, then below conditions do not need to be met. • This pin is driven low or high at ≥0.1 V/ns slew rate. • The resistance used to drive this pin is ≤1 kΩ. The above requirement is only needed for Pin 15.
GND	7	I or GND	Digital 0 or GND. Tie to GND through pull down resistor or directly tie to GND.
vZOUT_SEL	11	I	LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. • Low = 85 Ω • High = 100 Ω
LOS#	13	O	Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. • Low = Invalid input clock. • High = Valid input clock.
VDD_IN	3, 6	P	Power supply for CLKIN
VDDO	8, 18	P	Power supply for clock output
VDD	14	P	Power supply
VDD_DIG	19	P	Power supply for digital
GND	20, DAP	G	Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DDx}	Supply voltage on any VDD pin	–0.3	3.63	V
V_{IN}	Input voltage on CLKIN and digital input pins	–0.3	3.63	V
I_{OUT}	Output current - continuous (CLKOUT)		30	mA
	Output current - continuous (SMB_DATA, SBI_OUT)		25	mA
	Output current - surge (CLKOUT)		60	mA
	Output current - surge (SMB_DATA, SBI_OUT)		50	mA
T_S	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature			125	°C
T_A	Ambient temperature	–40		105	°C
V_{DD}	Power supply voltage	2.97	3.3	3.6	V
		1.71	1.8	1.89	V
V_{IN}	Input voltage on CLKIN and digital input pins	–0.3		3.6	V
t_{ramp}	Power ramping time	0.05		5	ms

6.4 Thermal Information

THERMAL METRIC(1)		NPP (TLGA)	RKP (VQFN)	UNIT
		80 PINS	40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.9	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	13.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.0	13.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK INPUT REQUIREMENTS						
$V_{IN, cross}$	Clock input crossing point voltage		100		1400	mV
DC_{IN}	Clock input duty cycle		45		55	%
V_{IN}	Differential clock input amplitude (half of differential peak-peak voltage)	$f_0 \le 300$ MHz	200		2000	mV
		300 MHz < $f_0 \le 400$ MHz	250		2000	mV
dV_{IN}/dt	Clock input slew rate	Measured from –150 mV to 150 mV on the differential waveform	0.6			V/ns
CLOCK OUTPUT CHARACTERISTICS - 100 MHz 85 Ω PCIe						
$V_{OH,AC}$	Output voltage high	DB2000QL AC test load(6)	670		820	mV
$V_{OL,AC}$	Output voltage low		–100		100	mV
$V_{max,AC}$	Output max voltage (including overshoot)		670		920	mV
$V_{min,AC}$	Output min voltage (including undershoot)		–100		100	mV
$V_{OH,DC}$	Output voltage high with DC test load	DB2000QL DC test load(2)	225		270	mV
$V_{OL,DC}$	Output voltage low with DC test load		10		150	mV
$V_{ovs,DC}$	Output overshoot voltage with DC test load				75	mV
$V_{uds,DC}$	Output undershoot voltage with DC test load		–75			mV
Z_{diff}	Differential output impedance	Measured at V_{OL}/V_{OH}, V_{DD} = 3.3 V	80.75	85	89.25	Ω
		Measured at V_{OL}/V_{OH}, V_{DD} = 1.8 V	81	85	90	Ω
$Z_{diff-crossing}$	Differential output impedance - crossing	Measured during transition	68	85	102	Ω
dV/dt	Output slew rate	Measured from –150 mV to 150 mV on the differential waveform. Lowest slew rate(6) (7)	1.5		2.2	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. Low slew rate(6) (7)	1.8		2.6	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. High slew rate (default)(6) (7)	2		2.9	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. Highest slew rate(6) (7)	2.4		4	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	DB2000QL AC test load(6)			10	%
DCD	Duty cycle distortion	Measured on the differential waveform. Input duty cycle = 50%(6)	–1		1	%
$V_{cross,AC}$	Absolute crossing point voltage	DB2000QL AC test load(6)	250		550	mV
$V_{cross,DC}$	Absolute crossing point voltage	DB2000QL DC test load(2)	130		200	mV
$\Delta V_{cross,AC}$	Variation of V_{cross} over all clock edges	DB2000QL AC test load(6)			140	mV
$\Delta V_{cross-DC}$	Variation of V_{cross} over all clock edges	DB2000QL DC test load(2)			35	mV
$\lvert V_{RB} \rvert$	Absolute value of ring back voltage as defined in PCIe	DB2000QL AC test load(6)	100			mV
t_{stable}	Time before V_{RB} is allowed	DB2000QL AC test load(6)	500			ps
V_{OH}	Output voltage high	PCIe AC test load(1)	670		820	mV
V_{OL}	Output voltage low	PCIe AC test load(1)	–100		100	mV

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK OUTPUT CHARACTERISTICS - 100 MHz 100 Ω PCIe						
V_{max}	Output voltage high including overshoot	PCIe AC test load(1)	670		920	mV
V_{min}	Output voltage low including undershoot	PCIe AC test load(1)	–100		100	mV
Z_{diff}	Differential output DC impedance	V_{DD} = 3.3 V	95	100	105	Ω
		V_{DD} = 1.8 V	95	100	105	Ω
dV/dt	Output slew rate	Measured from –150 mV to 150 mV on the differential waveform. Lowest slew rate(1) (7)	1.5		2.2	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. Low slew rate(1) (7)	1.8		2.6	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. High slew rate(1) (7)	2		2.9	V/ns
		Measured from –150 mV to 150 mV on the differential waveform. Highest slew rate(1) (7)	2.4		4	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	PCIe AC test load(1)			10	%
DCD	Duty cycle distortion	Measured on the differential waveform. Input duty cycle = 50%(1)	–1		1	%
V_{cross}	Absolute crossing point voltage	PCIe AC test load(1)	250		550	mV
ΔV_{cross}	Variation of V_{cross} over all clock edges	PCIe AC test load(1)			140	mV
$\lvert V_{RB} \rvert$	Absolute value of ring back voltage as defined in PCIe	PCIe AC test load(1)	100			mV
t_{stable}	Time before V_{RB} is allowed	PCIe AC test load(1)	500			ps
CLOCK OUTPUT CHARACTERISTICS - non-PCIe						
V_{OH}	Output voltage high	Output swing programmed to 800 mV. f_0 = 156.25 MHz or 312.5 MHz	720		880	mV
V_{OL}	Output voltage low		–120		120	mV
V_{OH}	Output voltage high	Output swing programmed to 900 mV. f_0 = 156.25 MHz or 312.5 MHz	780		980	mV
V_{OL}	Output voltage low		–120		120	mV
t_R, t_F	Rise/fall time on single-ended waveform, 20% to 80%	Output swing programmed to 800 mV. Fastest slew rate. f_0 = 156.25 MHz or 312.5 MHz			340	ps
		Output swing programmed to 900 mV. Fastest slew rate. f_0 = 156.25 MHz or 312.5 MHz			370	ps
DCD	Duty cycle distortion	Input duty cycle = 50%	–1		1	%
SKEW AND DELAY CHARACTERISTICS						
t_{skew}	Output-to-output skew	Same bank			50	ps
		Regardless of banks			50	ps
	Part-to-part skew				300	ps
t_{PD}	Input-to-output delay				1	ns
Δt_{PD}	Input-to-output delay variation	Single device over temperature and voltage			1.5	ps/°C
FREQUENCY AND TIMING CHARACTERISTICS						
f_0	Operating frequency	Automatic Output Disable functionality is disabled	1		400	MHz
		Automatic Output Disable functionality is enabled	25		400	MHz

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{startup}$	Startup time	Cold start. Measured from VDD valid (90% of final VDD) to output clock stable[3]. Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 \geq 100$ MHz			0.4	ms
		Cold start. Measured from VDD valid (90% of final VDD) to output clock stable[3]. Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 < 100$ MHz			0.8	ms
t_{stable}	Clock stabilization time	VDD is stable. Measured from PWRGD assertion[4] to output clock stable. $f_0 \geq 100$ MHz[3]			0.4	ms
		VDD is stable. Measured from PWRGD assertion[4] to output clock stable. $f_0 < 100$ MHz[3]			0.8	ms
$t_{PD\#}$	Powerdown deassertion time	Measured from PWRDN# deassertion[4] to output clock stable. $f_0 \geq 100$ MHz[3]			0.15	ms
		Measured from PWRDN# deassertion[4] to output clock stable. $f_0 < 100$ MHz[3]			0.5	ms
t_{OE}	Output enable/disable time	Time elapsed from OE assertion/ deassertion[4] to output clock starts/stops	4		10	clk
$t_{LOS\text{-}assert}$	LOS# assertion time	Time elapsed from loss of input clock to LOS# assertion. $f_0 < 100$ MHz			120	ns
		Time elapsed from loss of input clock to LOS# assertion. $f_0 \geq 100$ MHz			120	ns
$t_{LOS\text{-}deassert}$	LOS# deassertion time	Time elapsed from presence of input clock to LOS# deassertion. $f_0 < 100$ MHz			340	ns
		Time elapsed from presence of input clock to LOS# deassertion. $f_0 \geq 100$ MHz			105	ns
t_{AOD}	Automatic output disable time	Time elapsed from LOS# assertion to output disable (both outputs are low/ low). $f_0 < 100$ MHz			0.07	ns
		Time elapsed from LOS# assertion to output disable (both outputs are low/low), $f_0 \geq 100$ MHz			0.07	ns
t_{AOE}	Automatic output enable time	Time elapsed from LOS# deassertion to output clock stable. $f_0 < 100$ MHz[3]			115	ns
		Time elapsed from LOS# deassertion to output clock stable, $f_0 \geq 100$ MHz[3]			22	ns
JITTER CHARACTERISTICS						
$J_{PCIe1\text{-}CC}$	PCIe Gen 1 CC jitter	Single clock input. Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV			442.5	fs
$J_{PCIe2\text{-}CC}$	PCIe Gen 2 CC jitter				39	fs
$J_{PCIe3\text{-}CC}$	PCIe Gen 3 CC jitter				12.3	fs
$J_{PCIe4\text{-}CC}$	PCIe Gen 4 CC jitter				12.3	fs
$J_{PCIe5\text{-}CC}$	PCIe Gen 5 CC jitter				4.9	fs
$J_{PCIe6\text{-}CC}$	PCIe Gen 6 CC jitter				3	fs
$J_{PCIe2\text{-}IR}$	PCIe Gen 2 IR jitter				33.8	fs
$J_{PCIe3\text{-}IR}$	PCIe Gen 3 IR jitter				14.1	fs
$J_{PCIe4\text{-}IR}$	PCIe Gen 4 IR jitter				14.5	fs
$J_{PCIe5\text{-}IR}$	PCIe Gen 5 IR jitter				3.9	fs
$J_{PCIe6\text{-}IR}$	PCIe Gen 6 IR jitter				3	fs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Single clock input. Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV			583.2	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter				51.3	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter				16	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter				16	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter				6.4	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter				3.9	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter				41.9	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter				18.3	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter				18.9	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter				5.1	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter				3.8	fs
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Both inputs (for MUX only) have running clocks. SSC enabled or disabled. Crosstalk included. Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV		443.7	583.2	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter			39	51.3	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter			12.2	16	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter			12.2	16	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter			4.9	6.4	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter			3	3.9	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter			31.9	41.9	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter			13.9	18.3	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter			14.4	18.9	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter			3.9	5.1	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter			2.9	3.8	fs
$J_{PCIe1-CC}$	PCIe Gen 1 CC jitter	Both inputs (for MUX only) have running clocks. SSC enabled or disabled. Crosstalk included. Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV				fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC jitter					fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC jitter					fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC jitter					fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC jitter					fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC jitter					fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR jitter					fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR jitter					fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR jitter					fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR jitter					fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR jitter					fs
$J_{DB2000QL}$	DB2000QL filter	Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV[6]		8.7	11.5	fs
		Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV[6]		6.5	9	fs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{RMS-additive}$	Additive 12 kHz to 20 MHz RMS jitter	f = 100 MHz, slew rate ≥ 3.5 V/ns		27.3	37.5	fs
		f = 100 MHz, slew rate ≥ 1.5 V/ns		37.4	48.5	fs
	Additive 12 kHz to 20 MHz RMS jitter	f = 156.25 MHz, slew rate ≥ 3.5 V/ns		21.9	31	fs
		f = 156.25 MHz, slew rate ≥ 1.5 V/ns		29.4	38.5	fs
	Additive 12 kHz to 70 MHz RMS jitter	f = 156.25 MHz, slew rate ≥ 3.5 V/ns		35.1	48.5	fs
		f = 156.25 MHz, slew rate ≥ 1.5 V/ns		47.1	60.5	fs
	Additive 12 kHz to 20 MHz RMS jitter	f = 312.5 MHz, slew rate ≥ 3.5 V/ns		19.3	28	fs
		f = 312.5 MHz, slew rate ≥ 1.5 V/ns		27.4	39.5	fs
	Additive 12 kHz to 70 MHz RMS jitter	f = 312.5 MHz, slew rate ≥ 3.5 V/ns		29.5	41.5	fs
		f = 312.5 MHz, slew rate ≥ 1.5 V/ns		40.7	58	fs
SUPPLY CURRENT CHARACTERISTICS						
$I_{DD,total}$	LMKDB1104 total supply current	All outputs running, f_0 = 100 MHz			54	mA
$I_{DD,total}$	LMKDB1108 total supply current	All outputs running, f_0 = 100 MHz			85.7	mA
$I_{DD,total}$	LMKDB1120 total supply current	All outputs running, f_0 = 100 MHz			162	mA
$I_{DD,total}$	LMKDB1202 total supply current	All outputs running, f_0 = 100 MHz			41	mA
$I_{DD,total}$	LMKDB1204 total supply current	All outputs running, f_0 = 100 MHz			54	mA
$I_{DD,core}$	LMKDB1104 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled				mA
$I_{DD,core}$	LMKDB1108 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled			36.3	mA
$I_{DD,core}$	LMKDB1120 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled			37.9	mA
$I_{DD,core}$	LMKDB1202 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled, 1 input enabled				mA
$I_{DD,core}$		Pin PWRGD/PWRDN# = high, all outputs disabled, 2 inputs enabled				mA
$I_{DD,core}$	LMKDB1204 core supply current	Pin PWRGD/PWRDN# = high, all outputs disabled, 1 input enabled				mA
$I_{DD,core}$		Pin PWRGD/PWRDN# = high, all outputs disabled, 2 inputs enabled				mA
I_{DDO}	Output supply current per output	f_0 = 100 MHz			6.4	mA
		f_0 = 400 MHz			9.2	mA
I_{PD}	LMKDB1108 or LMKDB1120 power down current	Pin PWRGD/PWRDN# = low			5.6	mA
I_{PD}	LMKDB1104, LMKDB1204, LMKDB1102 or LMKDB1202 power down current	Pin PWRGD/PWRDN# = low			5.6	mA
PSNR CHARACTERISTICS						

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSNR	Power Supply Noise Rejection, V_{DD} = 3.3 V[5]	10 kHz noise ripple			–93	dBc
		50 kHz noise ripple			–91	dBc
		100 kHz noise ripple			–91	dBc
		500 kHz noise ripple			–95	dBc
		1 MHz noise ripple			–96	dBc
		5 MHz noise ripple			–111	dBc
		10 MHz noise ripple			–99	dBc
	Power Supply Noise Rejection, V_{DD} = 1.8 V[5]	10 kHz noise ripple			–85	dBc
		50 kHz noise ripple			–89	dBc
		100 kHz noise ripple			–91	dBc
		500 kHz noise ripple			–93	dBc
		1 MHz noise ripple			–94	dBc
		5 MHz noise ripple			–109	dBc
		10 MHz noise ripple			–97	dBc
I/O CHARACTERISTICS						
V_{IH}	Input voltage high	2-level logic input, V_{DD} = 3.3 V ± 10%	2		V_{DD} + 0.3	V
V_{IL}	Input voltage low		–0.3		0.8	V
V_{IH}	Input voltage high	3-level logic input, V_{DD} = 3.3 V ± 10%	2.4		V_{DD} + 0.3	V
V_{IM}	Input voltage mid		1.2		1.8	V
V_{IL}	Input voltage low		–0.3		0.8	V
V_{IH}	Input voltage high	2-level logic input, V_{DD} = 1.8 V ± 5%	1.3		V_{DD} + 0.3	V
V_{IL}	Input voltage low		–0.3		0.4	V
V_{IH}	Input voltage high	3-level logic input, V_{DD} = 1.8 V ± 5%	1.3		V_{DD} + 0.3	V
V_{IM}	Input voltage mid		0.65		0.95	V
V_{IL}	Input voltage low		–0.3		0.4	V
V_{OH}	Output high voltage	SBI_OUT, I_{OH} = -2 mA	2.4		V_{DD} + 0.3	V
V_{OL}	Output low voltage	SBI_OUT, I_{OL} = 2 mA			0.4	V
I_{IN}	Input leakage current	CLKINx_P	–40		40	µA
		CLKINx_N	–40		40	µA
		single-ended inputs with internal pulldown	–30		30	µA
		single-ended inputs without internal pulldown	–5		5	µA
		3-level logic input	–30		30	µA
$R_{PU,PD}$	Internal pullup/pulldown resistor for single-ended inputs			120		kΩ
SMBUS ELECTRICAL CHARACTERISTICS						
V_{IH}	SMB_CLK, SMB_DATA input high voltage		0.8 × V_{DD}			V
V_{IL}	SMB_CLK, SMB_DATA input low voltage				0.3 × V_{DD}	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05 × V_{DD}			V
V_{OL}	SMB_DATA output low voltage	I_{OL} = 4 mA			0.4	V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	SMB_CLK, SMB_DATA input leakage		–10		10	µA
C_{PIN}	SMB_CLK, SMB_DATA pin capacitance				10	pF

(1) PCIe AC test load
(2) DB2000QL DC test load
(3) First clock edge is used for timing measurements. Clock outputs are muted until stabilized.
(4) For input pins, assertion or deassertion starts when the input voltage reaches the minimum voltage required for a "high" level, or the maximum voltage required for a "low" level
(5) All power supply pins are tied together. A 0.1 uF capacitor is placed close to each power supply pin. 50 mVpp ripple is applied before the decoupling capacitors. Measure the spur level at the clock output
(6) DB2000QL AC test load
(7) Slew rate is highly dependent on PCB trace characteristics

6.6 SMBus Timing Requirements

		100-kHz CLASS		400-kHz CLASS		UNIT
		MIN	MAX	MIN	MAX	
f_{SMB}	SMBus Operating Frequency	10	100	10	400	kHz
f_{BUF}	Bus free time between STOP and START condition	4.7	–	1.3	–	µs
t_{HD_STA}	Hold time after (REPEATED) START condition	4.0	–	0.6	–	µs
t_{SU_STA}	REPEATED START condition setup time	4.7	–	0.6	–	µs
t_{SU_STO}	STOP condition setup time	4.0	–	0.6	–	µs
t_{HD_DAT}	Data hold time	0	–	0	–	ns
t_{SU_DAT}	Data setup time	250	–	100	–	ns
$t_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
t_{LOW}	Clock low period	4.7	–	1.3	–	µs
t_{HIGH}	Clock high period	4.0	50	0.6	50	µs
t_{LOW_SEXT}	Cumulative clock low extend time (secondary device)	–	25	–	25	ms
t_{LOW_PEXT}	Cumulative clock low extend time (primary device)	–	10	–	10	ms
t_F	Clock/Data Fall Time	–	300	–	300	ns
t_R	Clock/Data Rise Time	–	1000	–	300	ns
t_{SPIKE}	Noise spike suppression time	–	–	0	50	ns
t_{POR}	Time in which a device must be operational after power-on reset		500		500	ms

6.7 SBI Timing Requirements

		MIN	MAX	UNIT
t_{PERIOD}	Clock period	40	–	ns
t_{SETUP}	SHFT setup to SBI_CLK rising edge	10	–	ns
t_{DSU}	SBI_IN data setup to SBI_CLK rising edge	5	–	ns
t_{DHOLD}	SBI_IN data hold after SBI_CLK rising edge	2	–	ns
t_{DOUT}	SBI_CLK rising edge to SBI_OUT data valid	2	–	ns
t_{LD}	CLK rising edge to LD# falling edge	10	–	ns
t_{OE}	Delay from LD# falling edge to output enable/disable taking effect	4	10	clocks
t_{SLEW}	SBI_CLK 20% to 80% slew rate	0.7	4	V/ns

6.8 Timing Diagrams

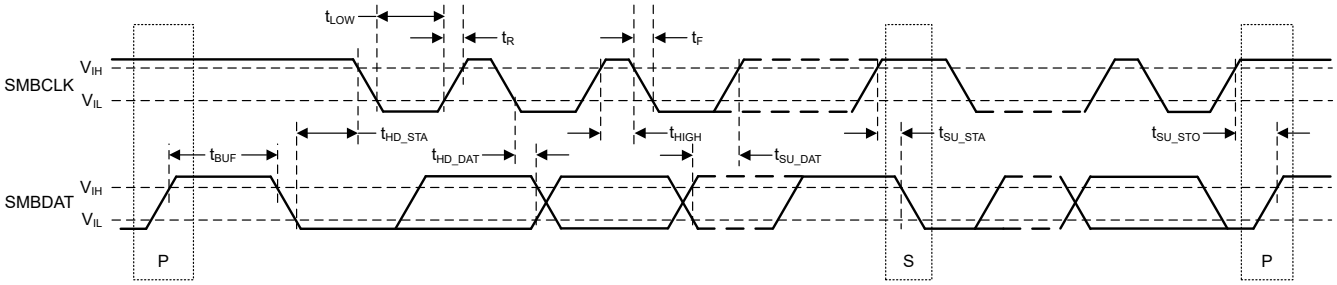


Figure 6-1. SMBus Timing Diagram

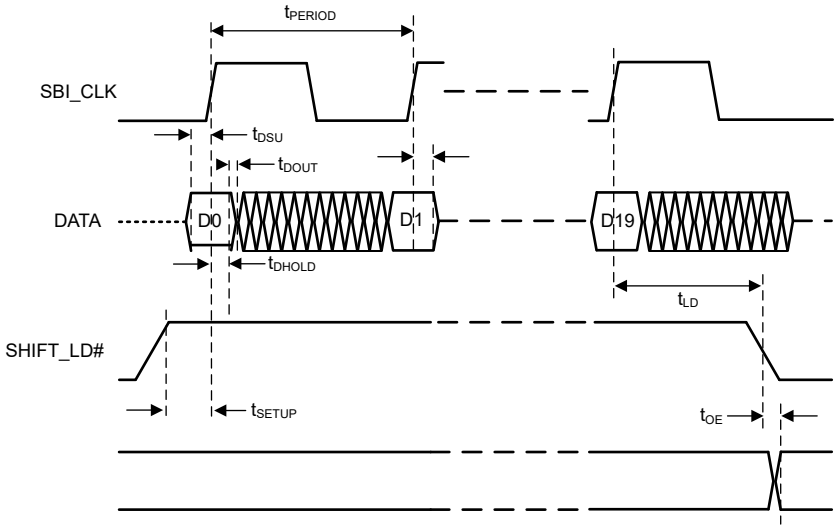


Figure 6-2. SBI Timing Diagram

6.9 Typical Characteristics

Typical 12-kHz to 20-MHz additive RMS jitter at 156.25 MHz = $(33.9^2 – 25.8^2)^{0.5}$ = 22.0 fs

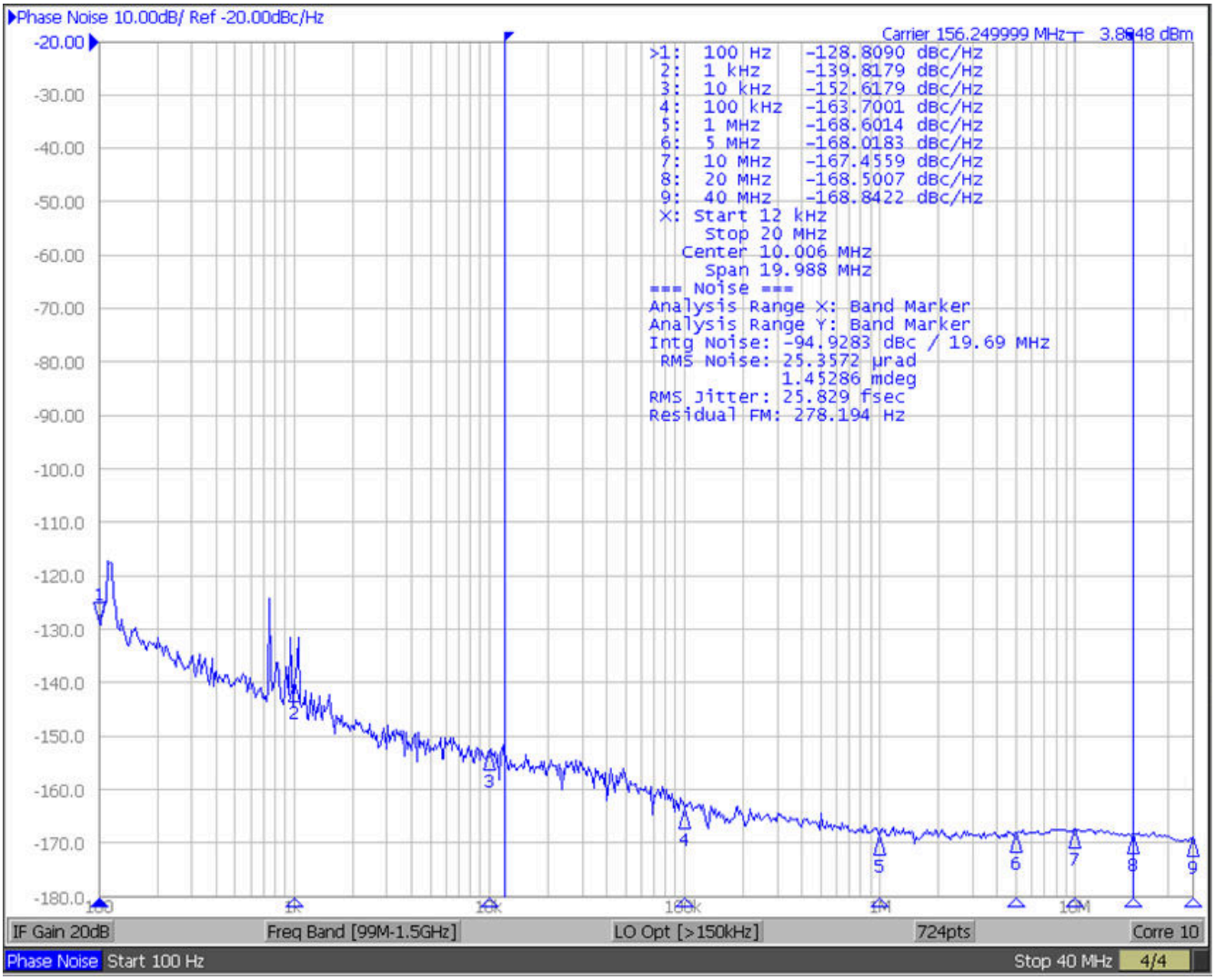


Figure 6-3. LMKDB Input Clock Phase Noise at 156.25 MHz

6.9 Typical Characteristics (continued)

Typical 12-kHz to 20-MHz additive RMS jitter at 156.25 MHz = $(33.9^2 – 25.8^2)^{0.5}$ = 22.0 fs

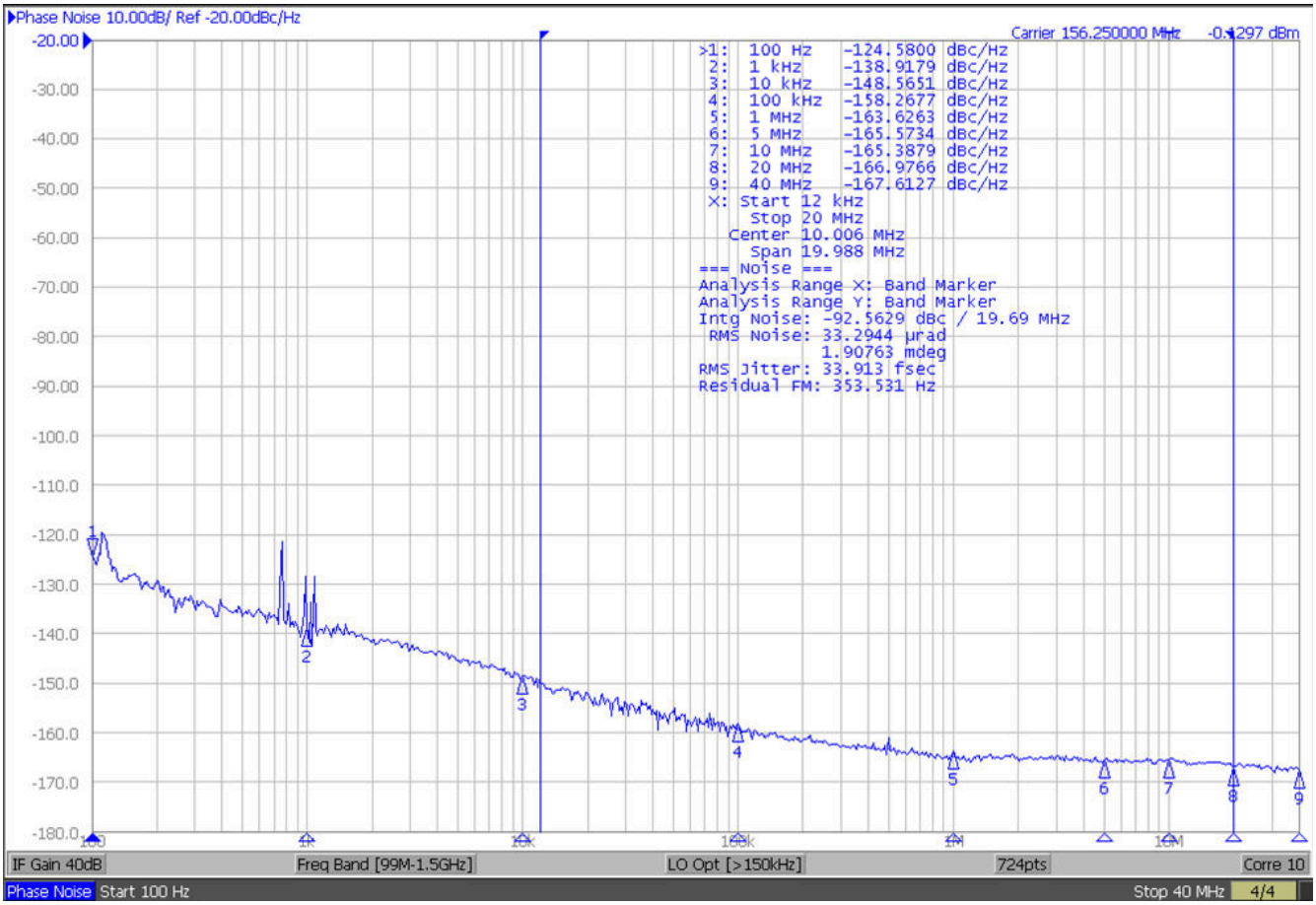


Figure 6-4. LMKDB Output Clock Phase Noise at 156.25 MHz

7 Parameter Measurement Information

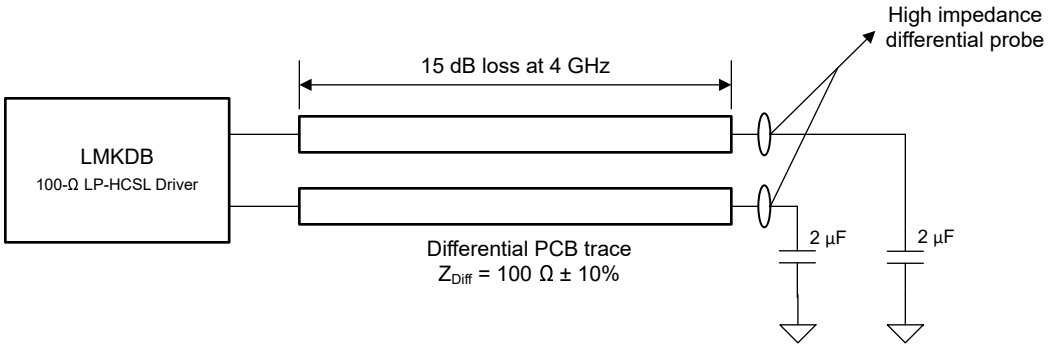


Figure 7-1. PCIe AC Test Load

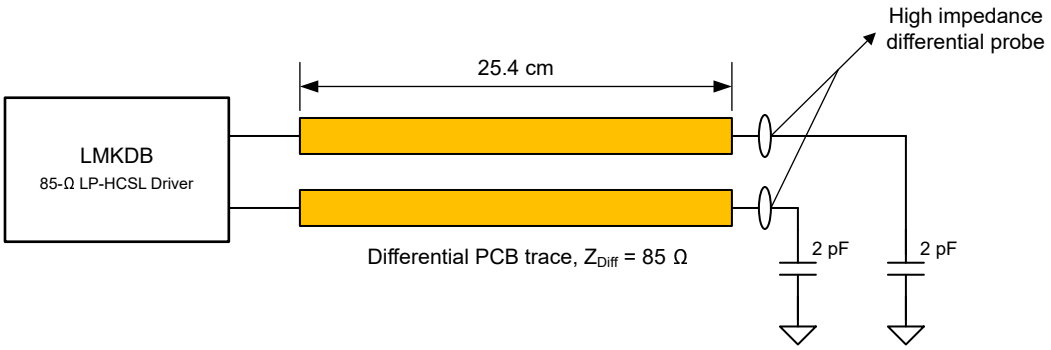


Figure 7-2. DB2000QL AC Test Load

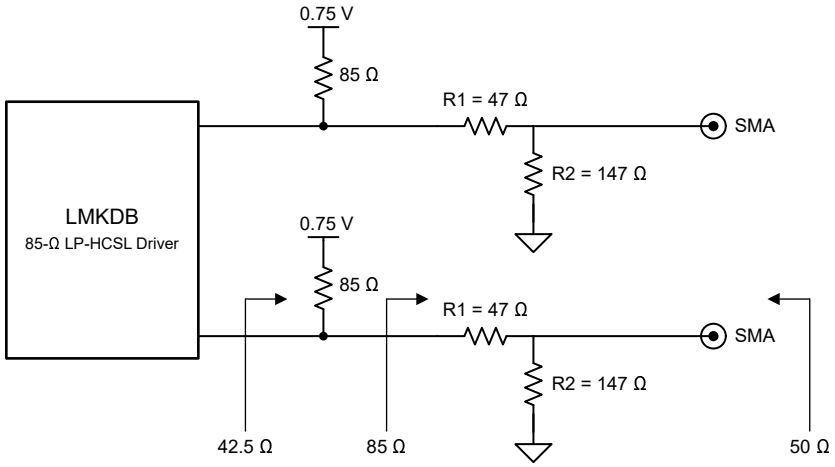


Figure 7-3. DB2000QL DC Test Load

8 Detailed Description

8.1 Overview

LMKDB1120 and LMKDB1108 DB2000QL compliant clock buffers distribute either 20 or 8 LP-HCSL clocks (respectively) designed for PCIe Gen 1 through 6 applications. With ultra-low additive jitter and ultra-low propagation delay, both devices allow for enough jitter margin for the entire clock path mainly required for PCIe Gen 5 and Gen 6 buffer cascading and Ethernet fan-out applications. The LMKDB1120 and LMKDB1108 also support both 1.8 V and 3.3 V supply voltages for better design flexibility.

LMKDB1120 and LMKDB1108 have individual OE controls for all 20 or 8 outputs (respectively), which provides more design flexibility. Each OE pin has an internal pull-down, allowing the pins to be left floating when unused. Each output of each device also has programmable slew rate, programmable output amplitude swing, and automatic output disable. The devices support 100-Ω or 85-Ω LP-HCSL, denoted by the part number as shown in Section 4, with output frequencies of up to 400 MHz.

Both devices have pin mode, SMBus mode, and Side Band Interface (SBI) mode, which can all be used at the same time. SBI enables or disables output clocks at a much faster speeds (up to 25 MHz) as compared to SMBus. Furthermore, because both SBI and SMBus can operate at the same time, SMBus can still be used to take over device control and readback status after power-up. For more details please refer to Section 8.4.

Refer to Section 8 for the detailed descriptions of the devices pins and the *Register Map* for more details on the devices' registers.

8.2 Functional Block Diagram

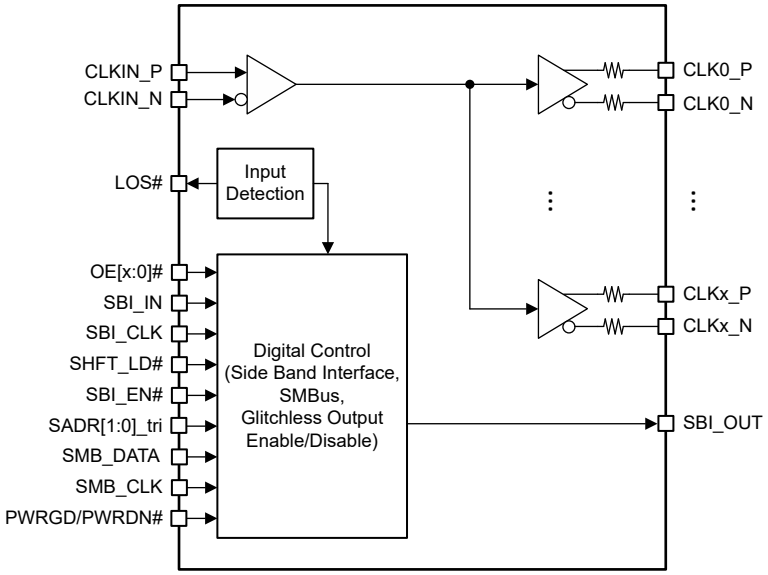


Figure 8-1. LMKDB1120 or LMKDB1108 Block Diagram

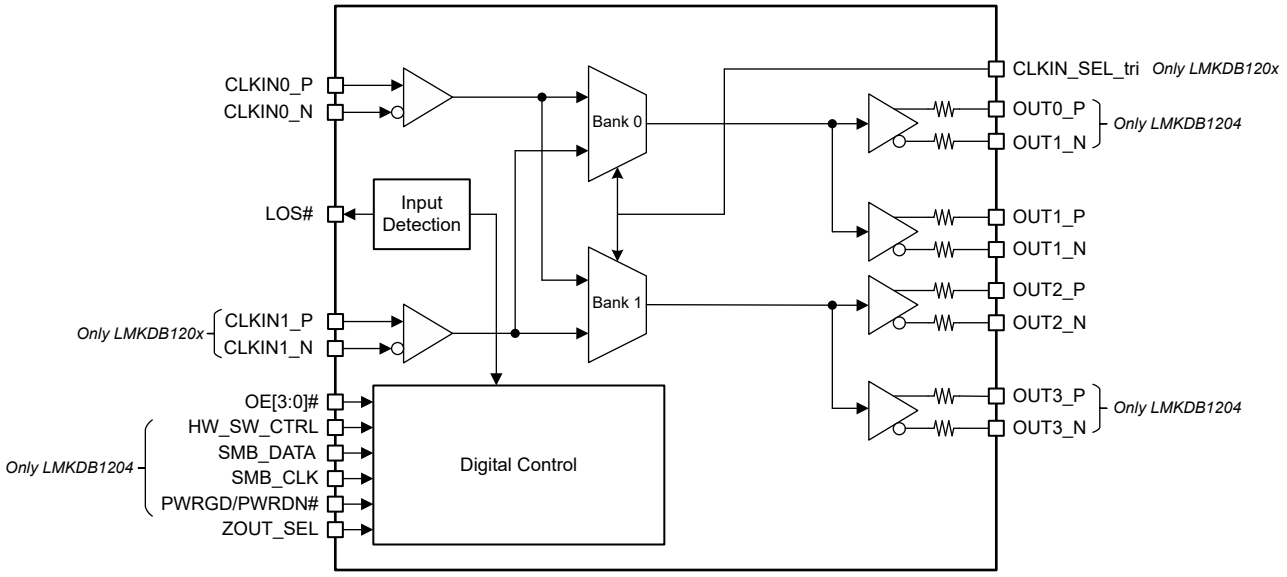


Figure 8-2. LMKDB1204, LMKDB1202, or LMKDB1102 Block Diagram

8.3 Feature Description

8.3.1 Input Features

8.3.1.1 Running Input Clocks When Device is Powered Off

The device supports running input clocks when power is off. This is different than the fail-safe feature where the input can be pulled to static VDD when device power is off. This is useful if clock inputs are available before power is provided to the clock buffer.

8.3.1.2 Fail-Safe Inputs

All clock input pins and digital input pins support fail-safe. Fail-safe means a pin can be driven to VDD when device power is off, without causing any leakage or reliability problem. For example, an OE# pin can be driven to VDD before device power is up so that the output stays muted until the OE# pin goes low, sometime after power-up.

8.3.1.3 Internal Termination for Clock Inputs

There is an option to enable 50-Ω internal termination for differential clock input. For LP-HCSL input, disable the internal termination. For HCSL input, enable internal termination if external termination is not provided. The internal termination is disabled by default.

8.3.1.4 AC-Coupled or DC-Coupled Clock Inputs

Input clocks can be either AC coupled or DC coupled. If the inputs are DC coupled, the input signal swing levels must match those in Specifications under the *CLOCK INPUT REQUIREMENTS*. Also, register RX_EN_AC_INPUT must be set to 0 for DC-coupled inputs or set to 1 for AC-coupled inputs. Refer to the *Register Map* for more information about RX_EN_AC_INPUT.

8.3.2 Flexible Power Sequence

8.3.2.1 PWRDN# Assertion and Deassertion

In the recommended power down sequence, PWRDN# is asserted while input clocks are valid. Make sure to hold the PWRDN# pin at low level for two consecutive rising edges of the input clock cycle. As a result, all clock outputs are muted to low/low (OUTx_P = Low, OUTx_N = Low) without a glitch. Following any other sequence brings the device to an undefined mode and can cause glitches or invalid outputs.

8.3.2.2 OE# Assertion and Deassertion

OE# pins can be asserted and deasserted at anytime, whether:

- Device power supply is on or off
- PWRGD/PWRDN# pin is pulled high or low
- Clock input is valid or invalid

The OE# pins only take effect if all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Otherwise outputs are always muted and OE# assertion and deassertion has no impact.

If OE# pins become low in any of the below conditions:

1. Input clock is invalid
2. PWRGD/PWRDN# pin is low
3. Device power is off

Then when all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Outputs are enabled without any glitch (assuming register OE and SBI OE are active).

8.3.2.3 PWRGD Assertion

The first low-to-high transition of the PWRGD pin after device power is on can occur while input clock is running, floating, low/low or pulled to VDD. The power-up sequence only starts if the PWRGD pin is pulled from low to high while input clock is valid.

If the PWRGD pin is pulled from low to high while input clock is invalid, then the power-up sequence is not initiated and the outputs stay low/low. When this happens, pulling the PWRGD pin back from high to low has no impact and this low-to-high transition on PWRGD pin is not considered a valid Power Good signal. The device is powered up next time when the PWRGD pin is pulled high while input clock is valid. In other words, there is only one valid Power Good signal for every power cycle.

8.3.2.4 Clock Input and PWRGD/PWRDN# Behaviors When Device Power is Off

Input clocks can be running, floating, low/low or pulled to VDD when device power is off, regardless of PWRGD/PWRDN# pin states (low, high, low-to-high transition and high-to-low transition)

8.3.3 LOS and OE

8.3.3.1 Additional OE# Pins for LMKDB1120 and Backward Compatibility

The DB2000QL specification only defines 8 OE# pins. In the LMKDB1120, 12 additional OE# pins are added so that each of the 20 outputs has a dedicated OE# pin. This provides additional design flexibility. The LMKDB1120 is backward pin-compatible with DB2000QL because all OE# pins have internal pulldown resistor. When left floating, these additional OE# pins have no impact (OE# pins are active low), because the three types of OE controls follow the AND logic.

8.3.3.2 Synchronous OE

Outputs are enabled and disabled synchronously. Synchronous OE means when an output is enabled or disabled, there is no glitch or runt pulse at the output.

8.3.3.3 OE Control

OE (Output Enable) can enable or disable a certain output. Three types of OE controls are supported: OE pin, OE register bit through SMBus, and OE control through SBI. The three controls follow the AND logic. An output is enabled only if all three controls enable that output. If any control disables that output, that output is disabled.

8.3.3.4 Automatic Output Disable

Automatic Output Disable (AOD) is enabled by default, and can be disabled through SMBus. When input clock becomes invalid and LOS# is active, output clocks are muted to low/low (OUTx_P = Low, OUTx_N = Low). Before LOS# is active and after input clock becomes invalid (because LOS detection takes time), output clocks stay at a steady state following the last input state. For example, if the input clock stopped at low/high, then output clocks first stay at low/high, then muted to low/low once LOS# is active.

8.3.3.5 LOS Detection

LOS (Loss Of input Signal) detects whether the clock input is valid or not. When input clock is valid, LOS# register bit = 1 and LOS# pin = high. When input clock is invalid, LOS register bit = 0 and LOS# pin = low.

At power-up, the LOS# pin is kept low until input is detected valid. Therefore, the LOS# pin can be used for the timing of OE# insertion and other operations.

The LOS# signal is only effective if PWRGD/PWRDN# pin is high. If this pin is low, then LOS# is low regardless of input validness

8.3.4 Output Features

8.3.4.1 Double Termination

For regular PCIe applications, LP-HCSL outputs do not require external termination, but the LMKDB family does support double termination (this is uncommon). In that case, an external 50-Ω termination is placed and the swing is halved

8.3.4.2 Programmable Output Slew Rate

The LMKDB family supports programmable output slew rate for each individual output. The slew rate can be chosen between 16 different values. There are four register field options, named SLEWRATE_OPT_#, each storing a slew rate value (chosen out of the 16 available slew rate values). A register field assignment of 0x0 is the fastest slew rate setting and a register field assignment of 0xF is the slowest slew rate setting. The SLEWRATE_OPT_# default values are found in Table 8-1. The corresponding ranges for the four default slew rates can be found in Section 6 under *CLOCK OUTPUT CHARACTERISTICS - 100 MHz 85 Ω PCIe* or *CLOCK OUTPUT CHARACTERISTICS - 100 MHz 100 Ω PCIe* for the specification *Output slew rate*. Slew rate is heavily dependent on trace characteristics including trace width, copper thickness, substrate height, dielectric constant, and loss tangent.

Table 8-1. LMKDB Default SLEWRATE_OPT_# Values

Register Field Name	Default Value	Default Slew Rate
SLEWRATE__OPT_1	0x0	Highest
SLEWRATE_OPT_2	0x6	High (default for all outputs)
SLEWRATE_OPT_3	0xA	Low
SLEWRATE_OPT_4	0xF	Lowest

Each of these slew rates can be assigned to each output separately using the register bits SLEWRATE_SEL_CLKX_LSB and SLEWRATE_SEL_CLKX_MSB. Setting these two bits assigns the slew rate for a specific output X, as shown in Table 8-2. By default, all outputs are assigned to SLEWRATE_OPT_2.

Table 8-2. SLEWRATE_SEL_CLKX_LSB & SLEWRATE_SEL_CLKX_MSB Slew Rate Selection

SLEWRATE_SEL_CLKX_LSB	SLEWRATE_SEL_CLKX_MSB	Slew Rate Option Selection
0	0	SLEWRATE_OPT_4
1	0	SLEWRATE_OPT_3

Table 8-2. SLEWRATE_SEL_CLKX_LSB & SLEWRATE_SEL_CLKX_MSB Slew Rate Selection (continued)

SLEWRATE_SEL_CLKX_LSB	SLEWRATE_SEL_CLKX_MSB	Slew Rate Option Selection
0	1	SLEWRATE_OPT_2
1	1	SLEWRATE_OPT_1

To program the slew rate to the desired slew rate, the following sequence needs to be followed:

1. [Optional]: if the default assignments shown in Table 8-1 for each slew rate speed is not as desired, one of the slew rate options value can be changed to another slew rate.
2. Program SLEWRATE_SEL_CLKX_MSB and SLEWRATE_SEL_CLKX_LSB to assign clock output X to desired slew rate speed option, as shown in Table 8-2. The default assignments for each option can be found in Table 8-1.

8.3.4.3 Programmable Output Swing

LMKDB family supports programmable LP-HCSL swings ranging from 600 mV to 975 mV. All outputs are programmed to the same output swing via register AMP_1. To program the outputs to the desired swing refer to the *Register Map*.

8.3.4.4 Accurate Output Impedance

The LMKDB family supports both 100-Ω LP-HCSL and 85-Ω LP-HCSL. The output impedance is accurately trimmed to ±5%. This helps improve impedance matching and clock signal integrity.

8.4 Device Functional Modes

8.4.1 SMBus Mode

In SMBus mode, SMBus registers can be written and read through SMBus pins. Pin SADR1 and SADR0 set the SMBus address.

SADR1	SADR0	8-Bit SMBus Address (R/W Bit = 0)
Low	Low	0xD8
Low	Float	0xDA
Low	High	0xDE
Float	Low	0xC2
Float	Float	0xC4
Float	High	0xC6
High	Low	0xCA
High	Float	0xCC
High	High	0xCE

Table 8-3. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Register address for *Byte* operations, or starting register address for *Block*, operations

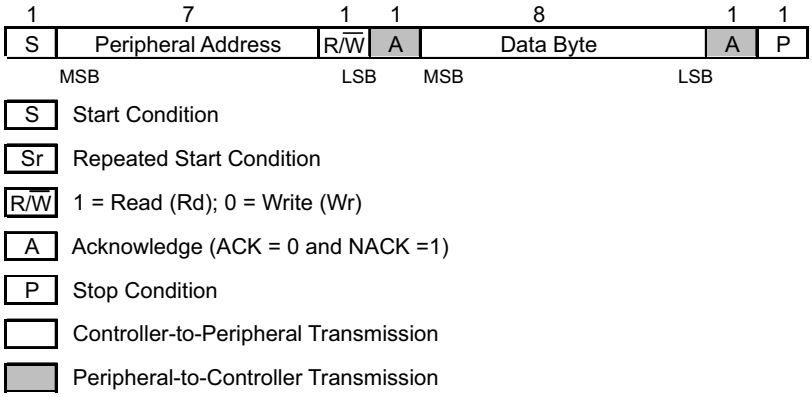


Figure 8-3. Generic Programming Sequence

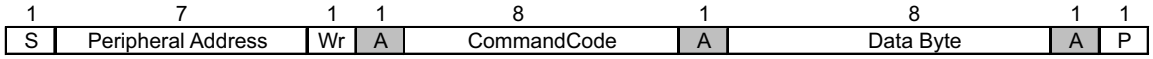


Figure 8-4. Byte Write Protocol

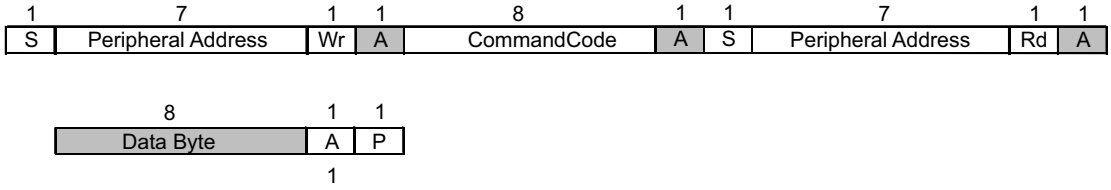


Figure 8-5. Byte Read Protocol

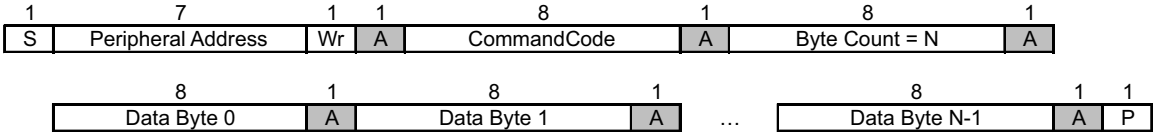


Figure 8-6. Block Write Protocol

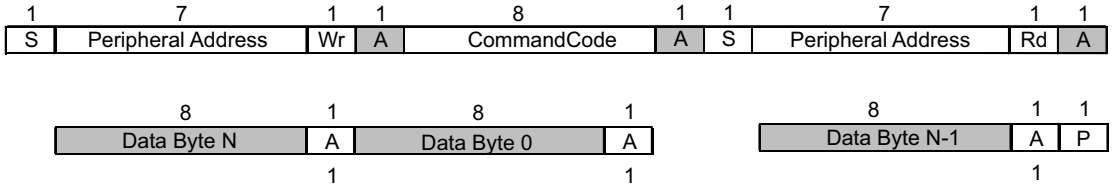


Figure 8-7. Block Read Protocol

8.4.2 SBI Mode

Side-Band Interface (SBI) is a simple 3-wire or 4-wire serial interface which consists of SHFT_LD#, SBI_IN, SBI_CLK and SBI_OUT (optional) pins. When the SHFT_LD# pin is high, the rising edge of SBI_CLK clocks SBI_IN into a shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents into the output register. SBI registers can be shifted out through SBI_OUT pin to form daisy chain topology.

Enabling SBI mode does not disable SMBus. SBI registers can be accessed while PWRGD/PWRDN# pin is low.

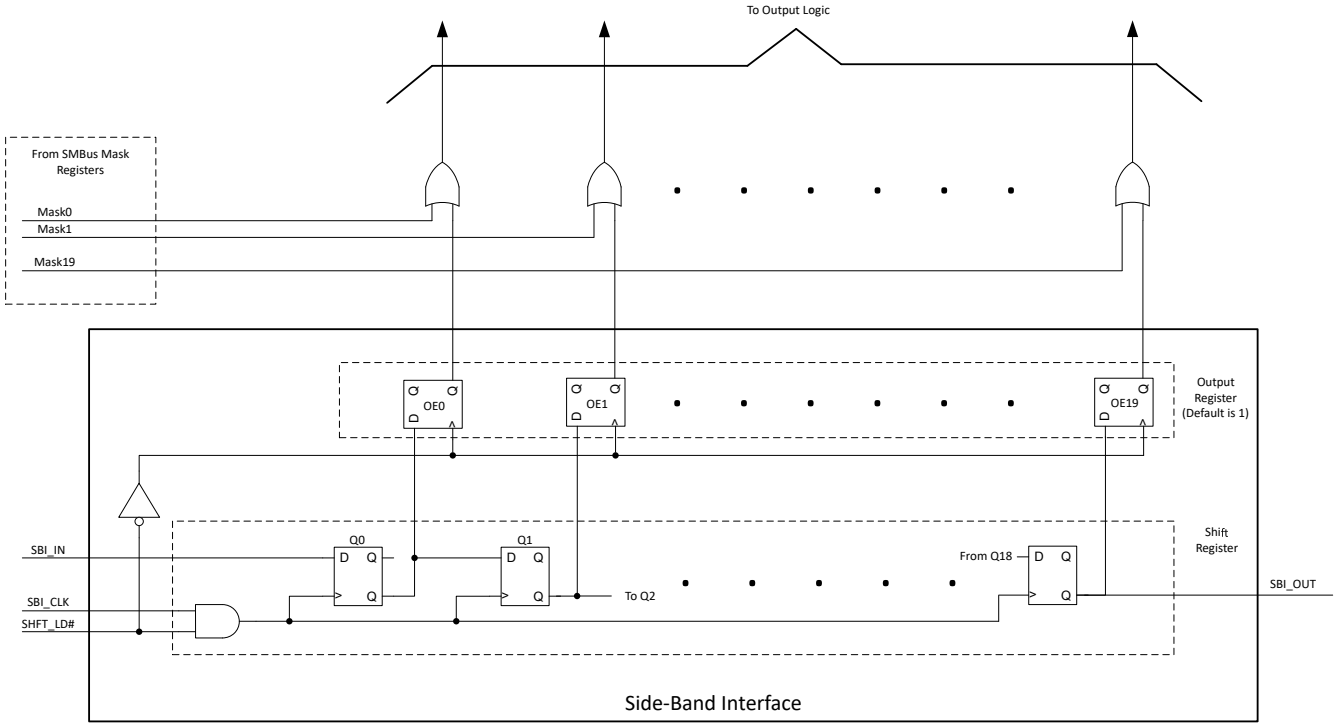


Figure 8-8. SBI Control Logic

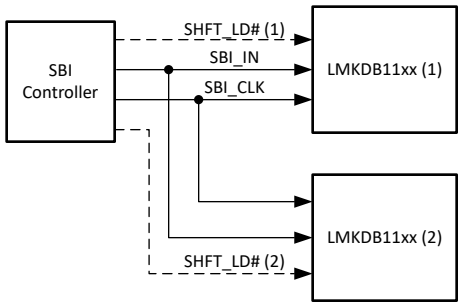


Figure 8-9. SBI Star Topology

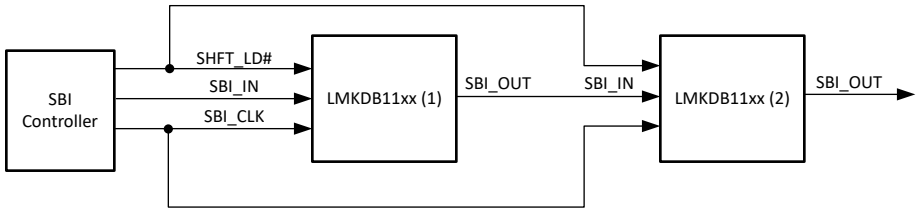


Figure 8-10. SBI Daisy Chain Topology

SBI register sequence:

- LMKDB1120: SBI_IN – CLK0, CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, CLK8, CLK9, CLK10, CLK11, CLK12, CLK13, CLK14, CLK15, CLK16, CLK17, CLK18, CLK19 – SBI_OUT
- LMKDB1108: SBI_IN – CLK7, CLK6, CLK5, CLK4, CLK3, CLK2, CLK1, CLK0 – SBI_OUT
- LMKDB1104: SBI_IN – CLK3, CLK2, CLK1, CLK0

8.4.3 Pin Mode

If the SMBus or SBI interface is not needed, the SMBus pins or SBI pins can be left floating. The device can operate in pin mode and the outputs can be enabled or disabled by OE# pins.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMKDB devices are a family of ultra-low additive jitter LP-HCSL clock buffers and clock MUX. The device can be controlled through SMBus registers, Side Band Interface, and OE# pins.

9.2 Typical Application

This example shows PCIe and Ethernet clock distribution. Provide multiple copies of PCIe clocks (100 MHz) or Ethernet clocks (156.25 MHz) based on the given source.

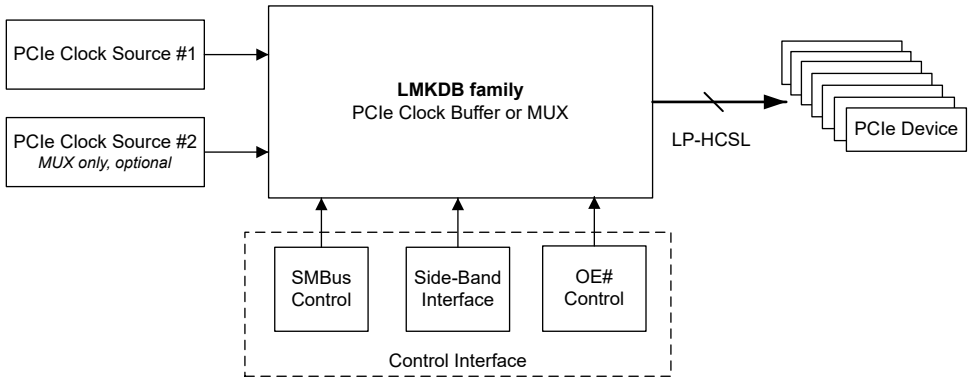


Figure 9-1. Typical Application

9.2.1 Design Requirements

Find two buffers for PCIe clock fan-out and Ethernet clock fan-out separately. Jitter requirements must be met and space must be minimized.

Table 9-1. Design Parameters

PARAMETER	VALUE
Number of PCIe clocks	15
Number of 156.25 MHz Ethernet clocks	7
PCIe architecture	CC (Common Clock)
PCIe reference clock slew rate	≥3.5 V/ns
PCIe Gen 5 reference clock jitter	45 fs maximum
PCIe Gen 5 total jitter	50 fs maximum
156.25-MHz reference clock slew rate	≥3.5 V/ns
156.25-MHz reference clock jitter (12 kHz to 20 MHz)	90 fs maximum
156.25-MHz total jitter (12 kHz to 20 MHz)	100 fs maximum

9.2.2 Detailed Design Procedure

First of all, calculate the jitter budget for the clock buffer using RMS addition. The maximum allowed additive jitter for the clock buffer is square root of the difference between square of reference clock jitter and square of total clock jitter.

The maximum PCIe Gen 5 additive jitter allowed for the buffer is sqrt(50^2 – 45^2) = 21 fs. According to the Specifications under the *Electrical Characteristics* table, the additive PCIe Gen 5 jitter under Common Clock and ≥3.5 V/ns input slew rate test condition is 13 fs maximum, well below 21 fs requirement. Therefore, the LMKDB1120 (20 outputs) can be used for PCIe Gen 5 clock distribution.

Similarly, the maximum 12 kHz to 20 MHz additive jitter allowed at 156.25 MHz is sqrt(100^2 – 90^2) = 43 fs. According to the Specifications under the *Electrical Characteristics* table, the 12 kHz to 20 MHz additive jitter at 156.25 MHz is 31 fs maximum, well below the 43 fs requirement. Therefore, the LMKDB1108 (8 outputs) can be used for Ethernet clock distribution.

9.2.3 Application Curves

Figure 9-2 and Figure 9-3 are example phase noise plots before and after using the LMKDB at 156.25 MHz, respectively. The LMKDB clock buffer adds a 22-fs (typical) jitter from 12 kHz to 20 MHz. All LMKDB devices have very similar performance.

To better understand jitter and how the additive jitter of the LMKDB resulted in 22-fs refer to *Timing is Everything: How to measure additive jitter* TI blog post.

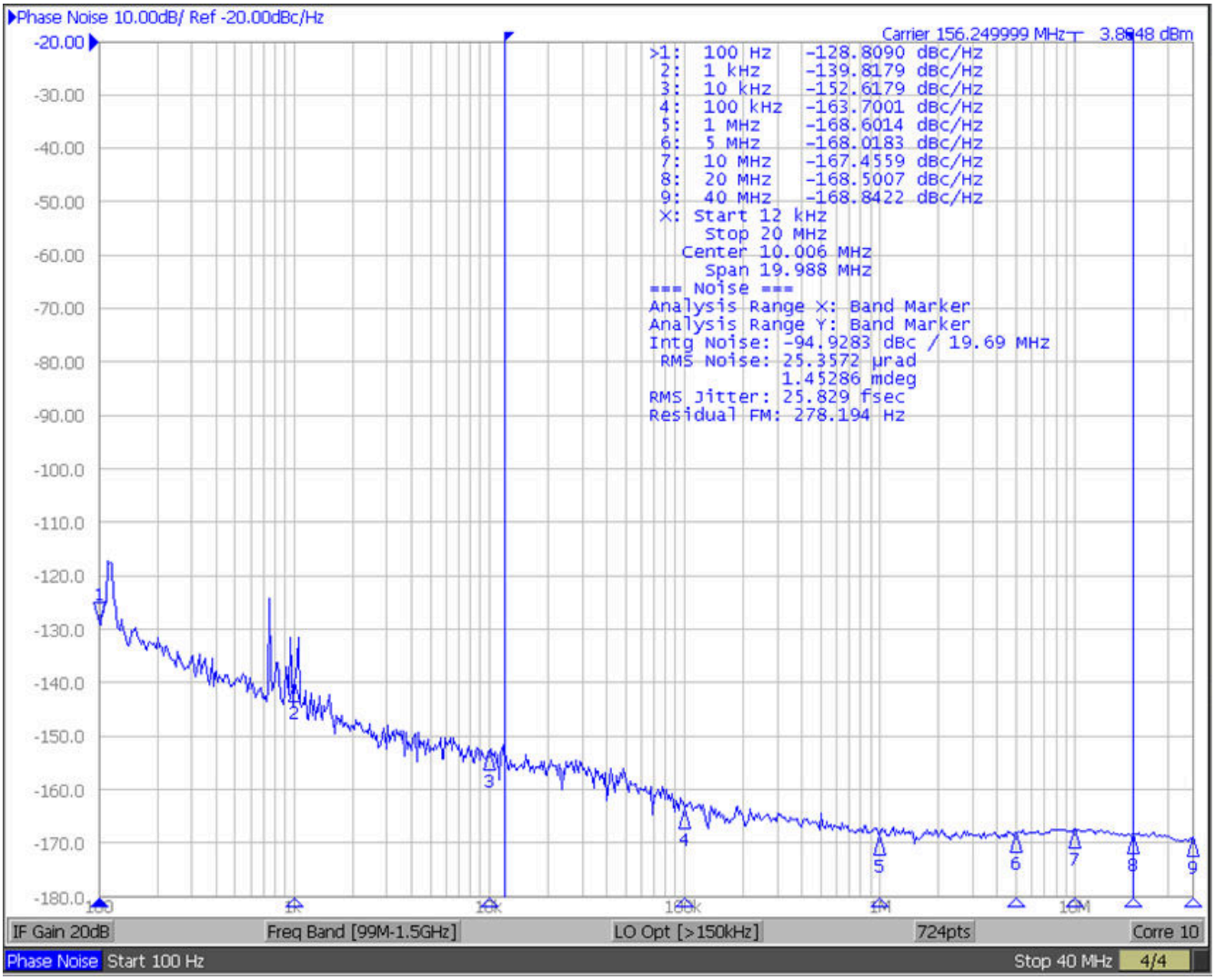


Figure 9-2. Reference Clock Phase Noise

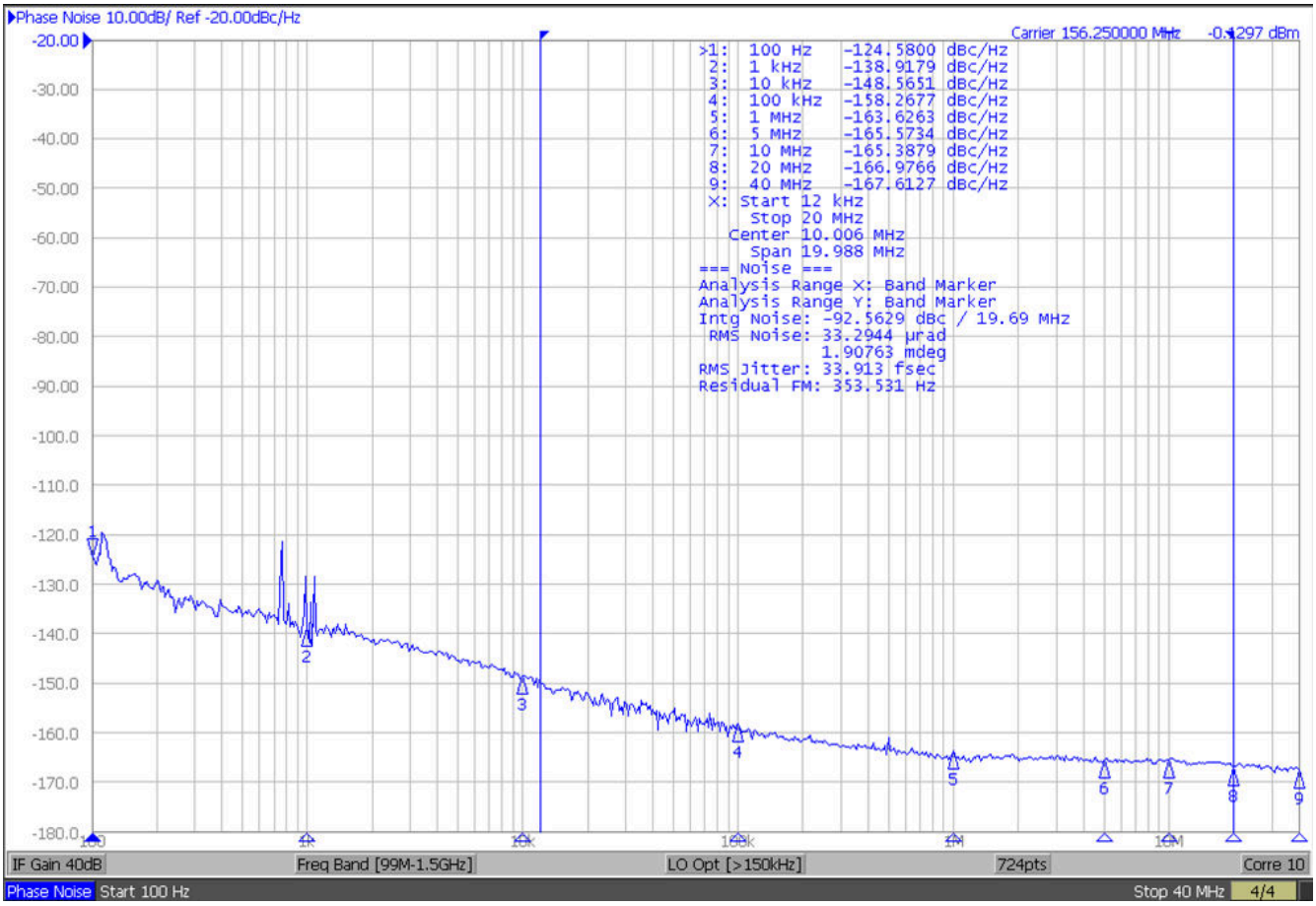


Figure 9-3. Reference Clock + LMKDB Phase Noise

9.3 Power Supply Recommendations

Place a 0.1-µF capacitor close to every power supply pin. To minimize noise on VDDA, place a 2.2-Ω resistor next to the VDDA pin. All supply pins can be grouped onto one power rail. TI recommends a Ferrite Bead and a 10-µF capacitor to GND for the entire chip. Figure 9-4 shows an example power schematic.

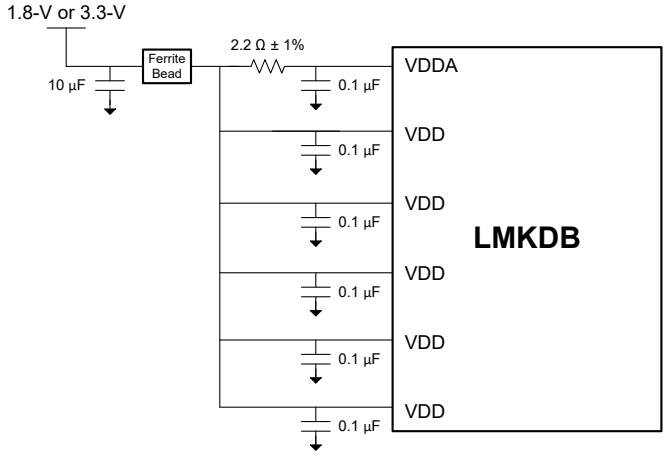


Figure 9-4. Power Supply Recommendation for LMKDB1120 and LMKDB1108

If both inputs are used for a MUX device and the two inputs have different frequencies (including PCIe SSC and PCIe No SSC), then isolate the inputs and corresponding output banks by adding more Ferrite Beads.

9.4 Layout

9.4.1 Layout Guidelines

Use a low-inductance ground connection between the device DAP and the PCB.

Match PCB trace impedance with device output impedance (85-Ω or 100-Ω differential impedance). Eliminate stubs and reduce discontinuity on the transmission lines.

9.4.2 Layout Example

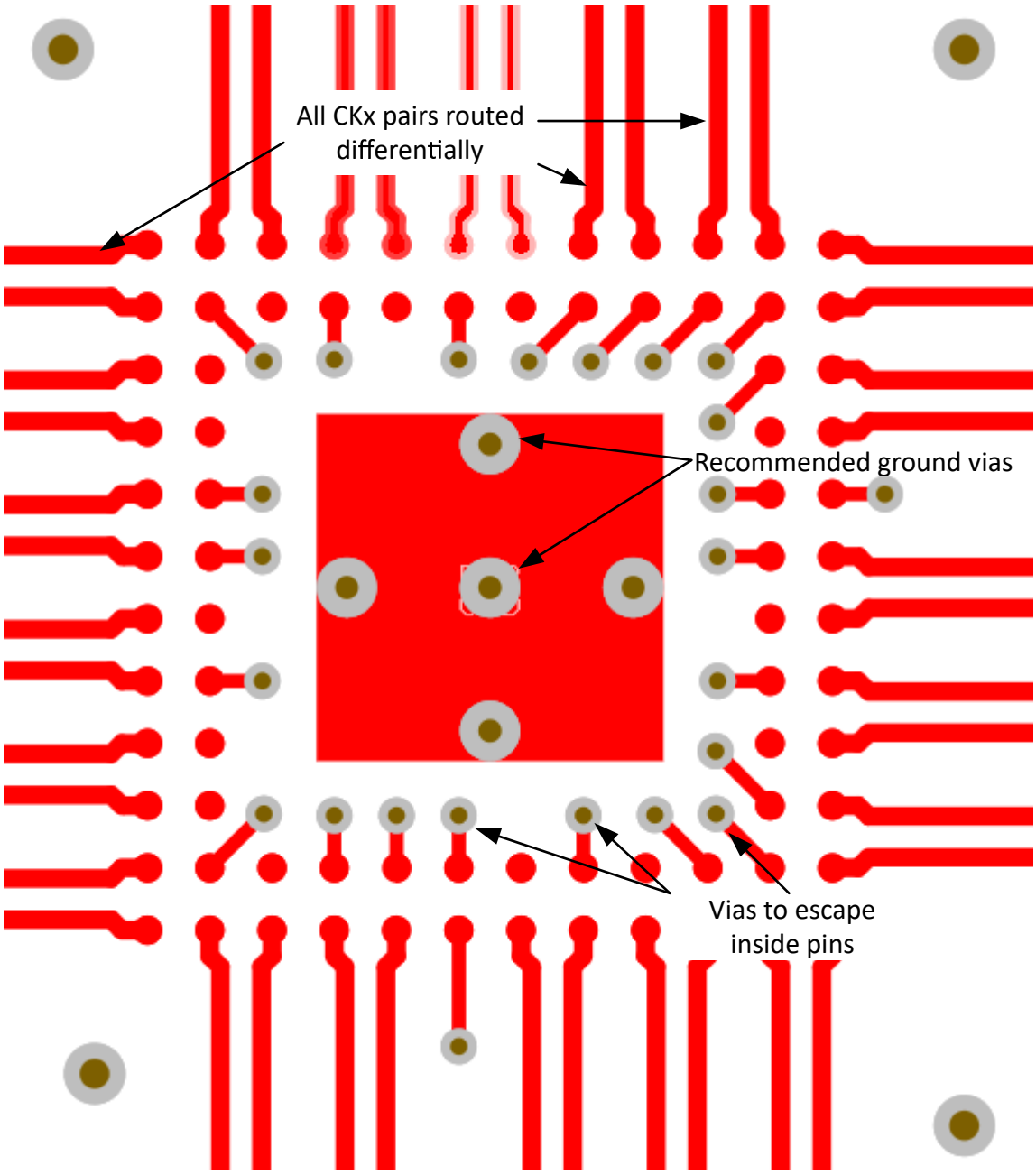


Figure 9-5. Layout Example - Top Layer

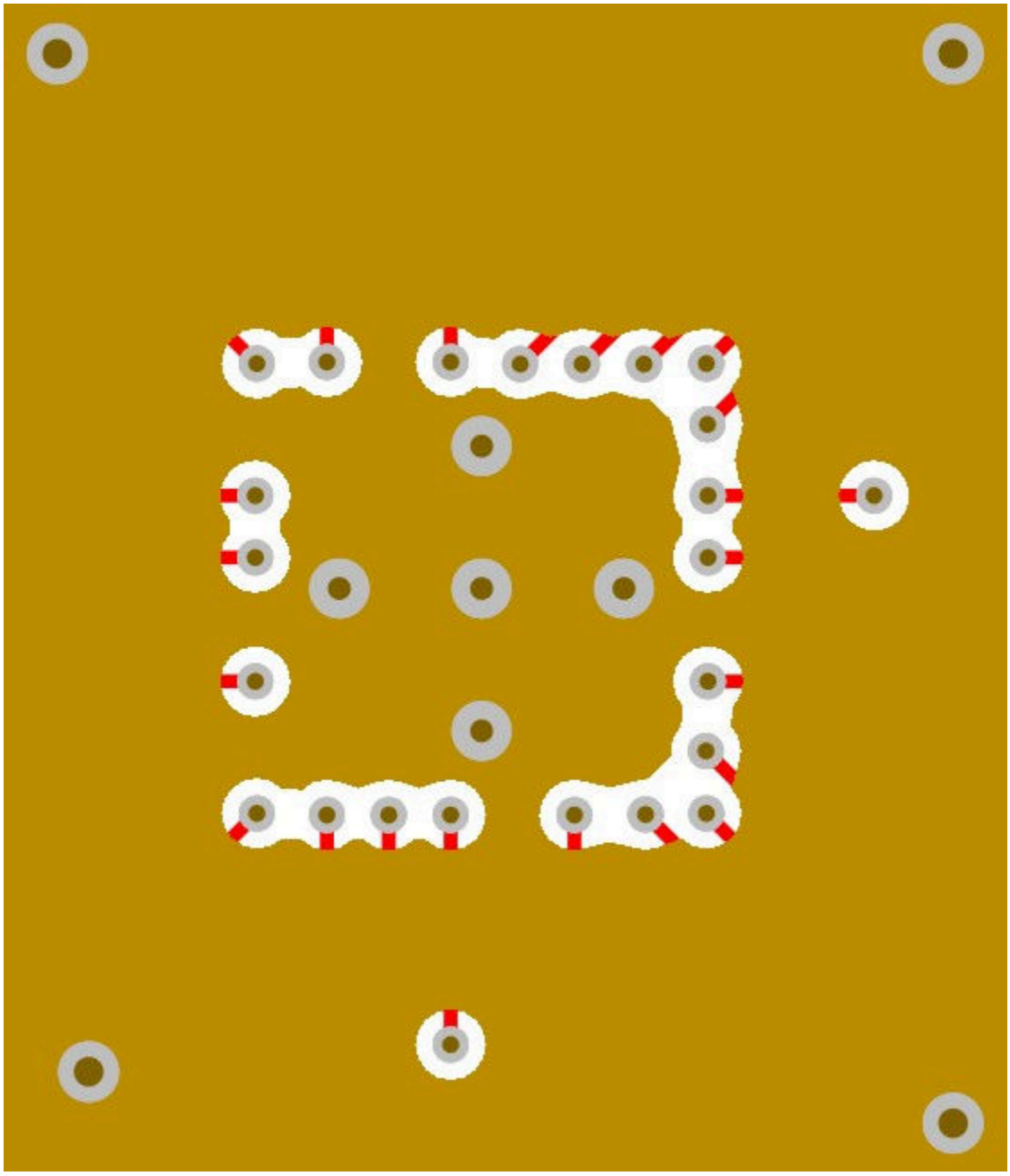


Figure 9-6. Layout Example - GND Layer

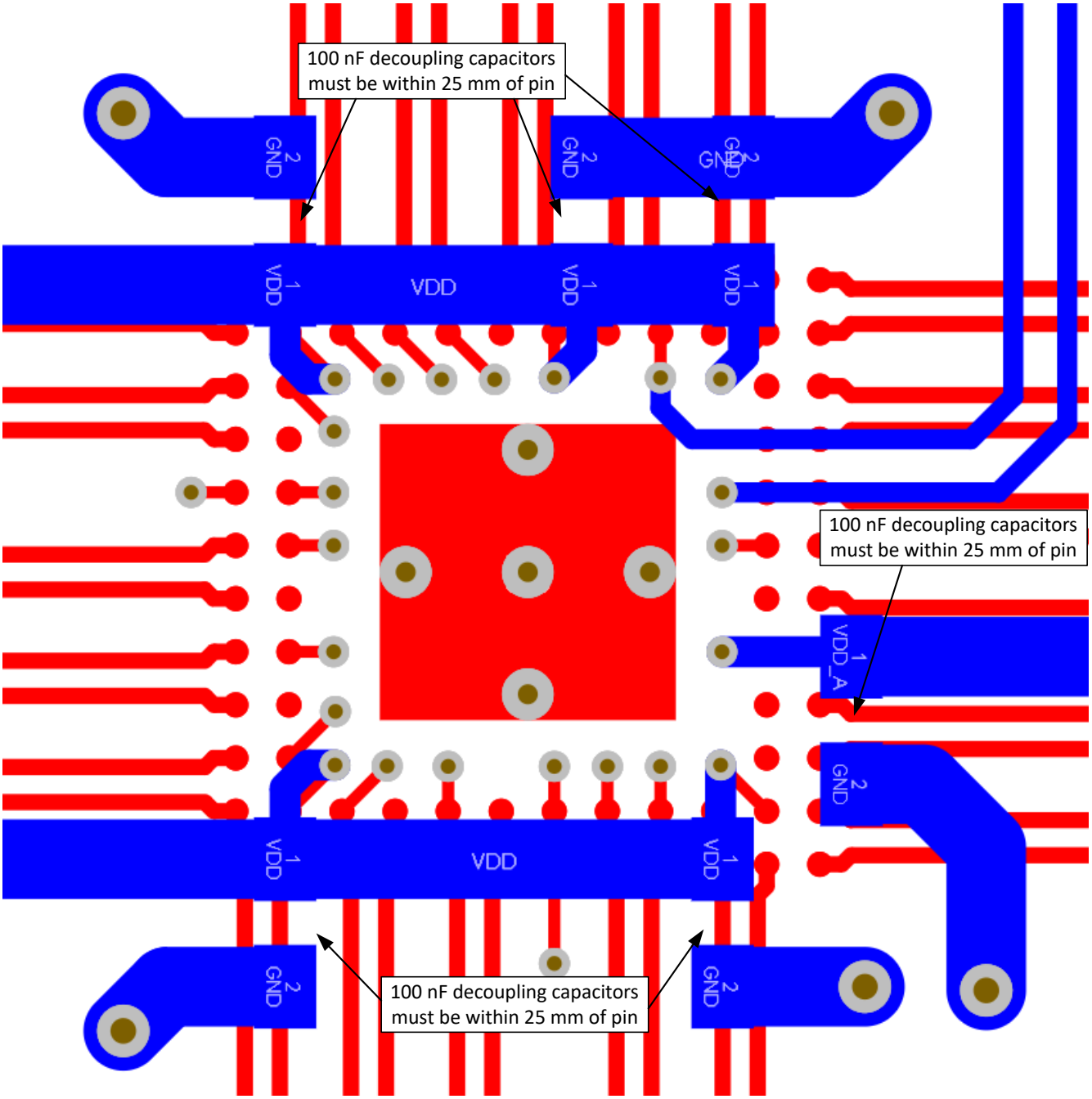


Figure 9-7. Layout Example - Bottom Layer

10 LMKDB1120 Registers

Table 10-1 lists the memory-mapped registers for the LMKDB1120 registers. All register offset addresses not listed in Table 10-1 must be considered as reserved locations and the register contents must not be modified.

Table 10-1. LMKDB1120 Registers

Offset	Acronym	Register Name	Section
0h	R0	Output Enable Control for CLK16 through CLK19	Section 10.1
1h	R1	Output Enable Control for CLK0 through CLK7	Section 10.2
2h	R2	Output Enable Control for CLK8 through CLK15	Section 10.3
3h	R3	OE Pin Readback for CLK5 through CLK12	Section 10.4
4h	R4	AOD Enable Control and SBI_EN Readback	Section 10.5
5h	R5	Device Info	Section 10.6
6h	R6	Device Info (cont.)	Section 10.7
7h	R7	SMBus Byte Counter	Section 10.8
8h	R8	SBI Mask for CLK0 through CLK7	Section 10.9
9h	R9	SBI Mask for CLK8 and CLK15	Section 10.10
Ah	R10	SBI Mask for CLK16 and CLK19	Section 10.11
Bh	R11	Output Slew Rate Select MSB for CLK0 through CLK7	Section 10.12
Ch	R12	Output Slew Rate Select MSB for CLK8 through CLK15	Section 10.13
Dh	R13	Output Slew Rate Select MSB for CLK16 through CLK19	Section 10.14
14h	R20	Output Amplitude	Section 10.15
15h	R21	Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback	Section 10.16
21h	R33	SBI Mask Readback for CLK0 through CLK7	Section 10.17
22h	R34	SBI Mask Readback for CLK8 through CLK15	Section 10.18
23h	R35	SBI Mask Readback for CLK16 through CLK19	Section 10.19
26h	R38	Non-clearable SMBUS Write Lock	Section 10.20
27h	R39	LOS Event Status and Clearable SMBus Write Lock	Section 10.21
5Bh	R91	Slew Rate Speed Options 1 and 2 Assignments	Section 10.22
5Ch	R92	Slew Rate Speed Options 3 and 4 Assignments	Section 10.23
62h	R98	Output Slew Rate Select LSB for CLK0 through CLK7	Section 10.24
63h	R99	Output Slew Rate Select LSB for CLK8 through CLK15	Section 10.25
64h	R100	Output Slew Rate Select LSB for CLK16 through CLK19	Section 10.26

Complex bit access types are encoded to fit into small table cells. Table 10-2 shows the codes that are used for access types in this section.

Table 10-2. LMKDB1120 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WSC	W	Write
Reset or Default Value		

Table 10-2. LMKDB1120 Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

10.1 R0 Register (Offset = 0h) [Reset = 78h]

R0 is shown in Table 10-3.

Return to the Summary Table.

Table 10-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	CLK_EN_19	R/W	1h	Output Enable for CLK19 0h = Output Disabled (low/low) 1h = Output Enabled
5	CLK_EN_18	R/W	1h	Output Enable for CLK18 0h = Output Disabled (low/low) 1h = Output Enabled
4	CLK_EN_17	R/W	1h	Output Enable for CLK17 0h = Output Disabled (low/low) 1h = Output Enabled
3	CLK_EN_16	R/W	1h	Output Enable for CLK16 0h = Output Disabled (low/low) 1h = Output Enabled
2:0	RESERVED	R	0h	Reserved

10.2 R1 Register (Offset = 1h) [Reset = FFh]

R1 is shown in Table 10-4.

Return to the Summary Table.

Table 10-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_EN_7	R/W	1h	Output Enable for CLK7 0h = Output Disabled (low/low) 1h = Output Enabled
6	CLK_EN_6	R/W	1h	Output Enable for CLK6 0h = Output Disabled (low/low) 1h = Output Enabled
5	CLK_EN_5	R/W	1h	Output Enable for CLK5 0h = Output Disabled (low/low) 1h = Output Enabled
4	CLK_EN_4	R/W	1h	Output Enable for CLK4 0h = Output Disabled (low/low) 1h = Output Enabled
3	CLK_EN_3	R/W	1h	Output Enable for CLK3 0h = Output Disabled (low/low) 1h = Output Enabled
2	CLK_EN_2	R/W	1h	Output Enable for CLK2 0h = Output Disabled (low/low) 1h = Output Enabled
1	CLK_EN_1	R/W	1h	Output Enable for CLK1 0h = Output Disabled (low/low) 1h = Output Enabled

Table 10-4. R1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_EN_0	R/W	1h	Output Enable for CLK0 0h = Output Disabled (low/low) 1h = Output Enabled

10.3 R2 Register (Offset = 2h) [Reset = FFh]

R2 is shown in Table 10-5.

Return to the Summary Table.

Table 10-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_EN_15	R/W	1h	Output Enable for CLK15 0h = Output Disabled (low/low) 1h = Output Enabled
6	CLK_EN_14	R/W	1h	Output Enable for CLK14 0h = Output Disabled (low/low) 1h = Output Enabled
5	CLK_EN_13	R/W	1h	Output Enable for CLK13 0h = Output Disabled (low/low) 1h = Output Enabled
4	CLK_EN_12	R/W	1h	Output Enable for CLK12 0h = Output Disabled (low/low) 1h = Output Enabled
3	CLK_EN_11	R/W	1h	Output Enable for CLK11 0h = Output Disabled (low/low) 1h = Output Enabled
2	CLK_EN_10	R/W	1h	Output Enable for CLK10 0h = Output Disabled (low/low) 1h = Output Enabled
1	CLK_EN_9	R/W	1h	Output Enable for CLK9 0h = Output Disabled (low/low) 1h = Output Enabled
0	CLK_EN_8	R/W	1h	Output Enable for CLK8 0h = Output Disabled (low/low) 1h = Output Enabled

10.4 R3 Register (Offset = 3h) [Reset = 00h]

R3 is shown in Table 10-6.

Return to the Summary Table.

Table 10-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RB_OEb_12	R	0h	Status of OEb12
6	RB_OEb_11	R	0h	Status of OEb11
5	RB_OEb_10	R	0h	Status of OEb10
4	RB_OEb_9	R	0h	Status of OEb9
3	RB_OEb_8	R	0h	Status of OEb8
2	RB_OEb_7	R	0h	Status of OEb7
1	RB_OEb_6	R	0h	Status of OEb6
0	RB_OEb_5	R	0h	Status of OEb5

10.5 R4 Register (Offset = 4h) [Reset = 10h]

R4 is shown in Table 10-7.

Return to the Summary Table.

Table 10-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	BANK1_AOD_ENABLE	R/W	1h	Enable automatic output disable to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information. 0h = Disabled 1h = Enabled
3:1	RESERVED	R	0h	Reserved
0	RB_SBI_ENQ	R	0h	Status of SBI_ENQ

10.6 R5 Register (Offset = 5h) [Reset = 0Ah]

R5 is shown in Table 10-8.

Return to the Summary Table.

Table 10-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	REV_ID	R	0h	Silicon revision
3:0	VENDOR_ID	R	Ah	Vendor ID

10.7 R6 Register (Offset = 6h) [Reset = C9h]

R6 is shown in Table 10-9.

Return to the Summary Table.

Table 10-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID	R	C9h	Device ID

10.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in Table 10-10.

Return to the Summary Table.

Table 10-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:0	SMBUS_BC	R/W	7h	SMBus Block Read Byte Count

10.9 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in Table 10-11.

Return to the Summary Table.

Table 10-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_MASK_7	R/W	0h	Mask off Side-Band Disable for CLK7
6	SBI_MASK_6	R/W	0h	Mask off Side-Band Disable for CLK6
5	SBI_MASK_5	R/W	0h	Mask off Side-Band Disable for CLK5
4	SBI_MASK_4	R/W	0h	Mask off Side-Band Disable for CLK4
3	SBI_MASK_3	R/W	0h	Mask off Side-Band Disable for CLK3
2	SBI_MASK_2	R/W	0h	Mask off Side-Band Disable for CLK2
1	SBI_MASK_1	R/W	0h	Mask off Side-Band Disable for CLK1
0	SBI_MASK_0	R/W	0h	Mask off Side-Band Disable for CLK0

10.10 R9 Register (Offset = 9h) [Reset = 00h]

R9 is shown in Table 10-12.

Return to the Summary Table.

Table 10-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_MASK_15	R/W	0h	Mask off Side-Band Disable for CLK15
6	SBI_MASK_14	R/W	0h	Mask off Side-Band Disable for CLK14
5	SBI_MASK_13	R/W	0h	Mask off Side-Band Disable for CLK13
4	SBI_MASK_12	R/W	0h	Mask off Side-Band Disable for CLK12
3	SBI_MASK_11	R/W	0h	Mask off Side-Band Disable for CLK11
2	SBI_MASK_10	R/W	0h	Mask off Side-Band Disable for CLK10
1	SBI_MASK_9	R/W	0h	Mask off Side-Band Disable for CLK9
0	SBI_MASK_8	R/W	0h	Mask off Side-Band Disable for CLK8

10.11 R10 Register (Offset = Ah) [Reset = 00h]

R10 is shown in Table 10-13.

Return to the Summary Table.

Table 10-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	SBI_MASK_19	R/W	0h	Mask off Side-Band Disable for CLK19
2	SBI_MASK_18	R/W	0h	Mask off Side-Band Disable for CLK18
1	SBI_MASK_17	R/W	0h	Mask off Side-Band Disable for CLK17
0	SBI_MASK_16	R/W	0h	Mask off Side-Band Disable for CLK16

10.12 R11 Register (Offset = Bh) [Reset = FFh]

R11 is shown in Table 10-14.

Return to the Summary Table.

Table 10-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK7_MSB	R/W	1h	MSB CLK7 slew rate select

Table 10-14. R11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SLEWRATE_SEL_CLK6_MSB	R/W	1h	MSB CLK6 slew rate select
5	SLEWRATE_SEL_CLK5_MSB	R/W	1h	MSB CLK5 slew rate select
4	SLEWRATE_SEL_CLK4_MSB	R/W	1h	MSB CLK4 slew rate select
3	SLEWRATE_SEL_CLK3_MSB	R/W	1h	MSB CLK3 slew rate select
2	SLEWRATE_SEL_CLK2_MSB	R/W	1h	MSB CLK2 slew rate select
1	SLEWRATE_SEL_CLK1_MSB	R/W	1h	MSB CLK1 slew rate select
0	SLEWRATE_SEL_CLK0_MSB	R/W	1h	MSB CLK0 slew rate select

10.13 R12 Register (Offset = Ch) [Reset = FFh]

R12 is shown in Table 10-15.

Return to the Summary Table.

Table 10-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK15_MSB	R/W	1h	MSB CLK15 slew rate select
6	SLEWRATE_SEL_CLK14_MSB	R/W	1h	MSB CLK14 slew rate select
5	SLEWRATE_SEL_CLK13_MSB	R/W	1h	MSB CLK13 slew rate select
4	SLEWRATE_SEL_CLK12_MSB	R/W	1h	MSB CLK12 slew rate select
3	SLEWRATE_SEL_CLK11_MSB	R/W	1h	MSB CLK11 slew rate select
2	SLEWRATE_SEL_CLK10_MSB	R/W	1h	MSB CLK10 slew rate select
1	SLEWRATE_SEL_CLK9_MSB	R/W	1h	MSB CLK9 slew rate select
0	SLEWRATE_SEL_CLK8_MSB	R/W	1h	MSB CLK8 slew rate select

10.14 R13 Register (Offset = Dh) [Reset = 0Fh]

R13 is shown in Table 10-16.

Return to the Summary Table.

Table 10-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	SLEWRATE_SEL_CLK19_MSB	R/W	1h	MSB CLK19 slew rate select
2	SLEWRATE_SEL_CLK18_MSB	R/W	1h	MSB CLK18 slew rate select

Table 10-16. R13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SLEWRATE_SEL_CLK17_MSB	R/W	1h	MSB CLK17 slew rate select
0	SLEWRATE_SEL_CLK16_MSB	R/W	1h	MSB CLK16 slew rate select

10.15 R20 Register (Offset = 14h) [Reset = 66h]

R20 is shown in Table 10-17.

Return to the Summary Table.

Table 10-17. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	AMP_1	R/W	6h	Global Differential output Control = 0.6 V to approximately 1 V 25mV/step Default = 0.75 V 0h = 600 mV 1h = 625 mV 2h = 650 mV 3h = 675 mV 4h = 700 mV 5h = 725 mV 6h = 750 mV 7h = 775 mV 8h = 800 mV 9h = 825 mV Ah = 850 mV Bh = 875 mV Ch = 900 mV Dh = 925 mV Eh = 950 mV Fh = 975 mV
3:0	RESERVED	R	0h	Reserved

10.16 R21 Register (Offset = 15h) [Reset = 0Ch]

R21 is shown in Table 10-18.

Return to the Summary Table.

Table 10-18. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX1_EN_AC_INPUT	R/W	0h	Enable receiver bias when CLKIN is AC coupled 0h = DC Coupled Input 1h = AC Coupled Input
6	RX1_EN_RTERM_LSB	R/W	0h	Enable termination resistors on CLKIN1 0h = Input Termination R Disabled 1h = Input Termination R Enabled
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	PD_RESTOREB	R/W	1h	Save Configuration in Power Down 1'b0 : config cleared 1'b1: config saved
2	SDATA_TIMEOUT_EN	R/W	1h	Enable SMB SDATA time out monitoring 0h = Disable SDATA Time Out 1h = Enable SDATA Time Out
1	RESERVED	R	0h	Reserved

Table 10-18. R21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOSb_RB	R	0h	Real time read back of loss detect block output 0h = LOS Event Detected 1h = LOS Event Not-Detected

10.17 R33 Register (Offset = 21h) [Reset = FFh]

R33 is shown in Table 10-19.

Return to the Summary Table.

Table 10-19. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_CLK_7	R	1h	Readback of Side-Band Disable for CLK7
6	SBI_CLK_6	R	1h	Readback of Side-Band Disable for CLK6
5	SBI_CLK_5	R	1h	Readback of Side-Band Disable for CLK5
4	SBI_CLK_4	R	1h	Readback of Side-Band Disable for CLK4
3	SBI_CLK_3	R	1h	Readback of Side-Band Disable for CLK3
2	SBI_CLK_2	R	1h	Readback of Side-Band Disable for CLK2
1	SBI_CLK_1	R	1h	Readback of Side-Band Disable for CLK1
0	SBI_CLK_0	R	1h	Readback of Side-Band Disable for CLK0

10.18 R34 Register (Offset = 22h) [Reset = FFh]

R34 is shown in Table 10-20.

Return to the Summary Table.

Table 10-20. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_CLK_15	R	1h	Readback of Side-Band Disable for CLK15
6	SBI_CLK_14	R	1h	Readback of Side-Band Disable for CLK14
5	SBI_CLK_13	R	1h	Readback of Side-Band Disable for CLK13
4	SBI_CLK_12	R	1h	Readback of Side-Band Disable for CLK12
3	SBI_CLK_11	R	1h	Readback of Side-Band Disable for CLK11
2	SBI_CLK_10	R	1h	Readback of Side-Band Disable for CLK10
1	SBI_CLK_9	R	1h	Readback of Side-Band Disable for CLK9
0	SBI_CLK_8	R	1h	Readback of Side-Band Disable for CLK8

10.19 R35 Register (Offset = 23h) [Reset = 0Fh]

R35 is shown in Table 10-21.

Return to the Summary Table.

Table 10-21. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	SBI_CLK_19	R	1h	Readback of Side-Band Disable for CLK19
2	SBI_CLK_18	R	1h	Readback of Side-Band Disable for CLK18
1	SBI_CLK_17	R	1h	Readback of Side-Band Disable for CLK17

Table 10-21. R35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SBI_CLK_16	R	1h	Readback of Side-Band Disable for CLK16

10.20 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in Table 10-22.

Return to the Summary Table.

Table 10-22. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	WRITE_LOCK	W1C	0h	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power. 0h = SMBus Not locked for Writing 1h = SMBus Locked for Writing

10.21 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in Table 10-23.

Return to the Summary Table.

Table 10-23. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0h	Reserved
1	LOS_EVT	R/WSC	0h	LOS Event Status When high, indicates that a LOS event is detected. Can be cleared by writing a 1 to the bit. 0h = LOS Event Not-Detected 1h = LOS Event Detected
0	WRITE_LOCK_RW1C	R/W	0h	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to the bit. 0h = SMBus Not Locked for Writing 1h = SMBus locked for writing

10.22 R91 Register (Offset = 5Bh) [Reset = 00h]

R91 is shown in Table 10-24.

Return to the Summary Table.

Table 10-24. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SLEWRATE_OPT_2	R/W	0h	There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information. 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15
3:0	SLEWRATE_OPT_1	R/W	0h	There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information. 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15

10.23 R92 Register (Offset = 5Ch) [Reset = 00h]

R92 is shown in Table 10-25.

Return to the Summary Table.

Table 10-25. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SLEWRATE_OPT_4	R/W	0h	There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information. 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15
3:0	SLEWRATE_OPT_3	R/W	0h	There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information. 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9 Ah = 10 Bh = 11 Ch = 12 Dh = 13 Eh = 14 Fh = 15

10.24 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in Table 10-26.

Return to the Summary Table.

Table 10-26. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK7_LSB	R/W	0h	LSB CLK7 slew rate select
6	SLEWRATE_SEL_CLK6_LSB	R/W	0h	LSB CLK6 slew rate select
5	SLEWRATE_SEL_CLK5_LSB	R/W	0h	LSB CLK5 slew rate select
4	SLEWRATE_SEL_CLK4_LSB	R/W	0h	LSB CLK4 slew rate select
3	SLEWRATE_SEL_CLK3_LSB	R/W	0h	LSB CLK3 slew rate select

Table 10-26. R98 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SLEWRATE_SEL_CLK2_LSB	R/W	0h	LSB CLK2 slew rate select
1	SLEWRATE_SEL_CLK1_LSB	R/W	0h	LSB CLK1 slew rate select
0	SLEWRATE_SEL_CLK0_LSB	R/W	0h	LSB CLK0 slew rate select

10.25 R99 Register (Offset = 63h) [Reset = 00h]

R99 is shown in Table 10-27.

Return to the Summary Table.

Table 10-27. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK15_LSB	R/W	0h	LSB CLK15 slew rate select
6	SLEWRATE_SEL_CLK14_LSB	R/W	0h	LSB CLK14 slew rate select
5	SLEWRATE_SEL_CLK13_LSB	R/W	0h	LSB CLK13 slew rate select
4	SLEWRATE_SEL_CLK12_LSB	R/W	0h	LSB CLK12 slew rate select
3	SLEWRATE_SEL_CLK11_LSB	R/W	0h	LSB CLK11 slew rate select
2	SLEWRATE_SEL_CLK10_LSB	R/W	0h	LSB CLK10 slew rate select
1	SLEWRATE_SEL_CLK9_LSB	R/W	0h	LSB CLK9 slew rate select
0	SLEWRATE_SEL_CLK8_LSB	R/W	0h	LSB CLK8 slew rate select

10.26 R100 Register (Offset = 64h) [Reset = 00h]

R100 is shown in Table 10-28.

Return to the Summary Table.

Table 10-28. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3	SLEWRATE_SEL_CLK19_LSB	R/W	0h	LSB CLK19 slew rate select
2	SLEWRATE_SEL_CLK18_LSB	R/W	0h	LSB CLK18 slew rate select
1	SLEWRATE_SEL_CLK17_LSB	R/W	0h	LSB CLK17 slew rate select
0	SLEWRATE_SEL_CLK16_LSB	R/W	0h	LSB CLK16 slew rate select

11 LMKDB1108 Registers

Table 11-1 lists the memory-mapped registers for the LMKDB1108 registers. All register offset addresses not listed in Table 11-1 must be considered as reserved locations and the register contents must not be modified.

Table 11-1. LMKDB1108 Registers

Offset	Acronym	Register Name	Section
0h	R0	Output Enable Control for CLK2 through CLK7	Section 11.1
1h	R1	Output Enable Control for CLK0 and CLK1	Section 11.2
2h	R2	OE Pin Readback for CLK2 through CLK7	Section 11.3
3h	R3	OE Pin Readback for CLK0 and CLK1	Section 11.4
4h	R4	AOD Enable Control and SBI_EN Readback	Section 11.5
5h	R5	Device Info	Section 11.6
6h	R6	Device Info (cont.)	Section 11.7
7h	R7	SMBus Byte Counter	Section 11.8
8h	R8	SBI Mask for CLK2 through CLK7	Section 11.9
9h	R9	SBI Mask for CLK0 and CLK1	Section 11.10
Bh	R11	SBI Mask Readback for CLK0 through CLK5	Section 11.11
Ch	R12	SBI Mask Readback for CLK6 and CLK7	Section 11.12
11h	R17	Output Amplitude	Section 11.13
12h	R18	Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback	Section 11.14
14h	R20	Output Slew Rate Select MSB for CLK2 through CLK7	Section 11.15
15h	R21	Output Slew Rate Select MSB for CLK0 and CLK1	Section 11.16
26h	R38	Non-clearable SMBUS Write Lock	Section 11.17
27h	R39	LOS Event Status and Clearable SMBus Write Lock	Section 11.18
35h	R53	Slew Rate Mode Control Selection	Section 11.19
62h	R98	Output Slew Rate Select LSB for CLK0 through CLK7	Section 11.20

Complex bit access types are encoded to fit into small table cells. Table 11-2 shows the codes that are used for access types in this section.

Table 11-2. LMKDB1108 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

11.1 R0 Register (Offset = 0h) [Reset = EEh]

R0 is shown in Table 11-3.

Return to the Summary Table.

Table 11-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_EN_2	R/W	1h	Output Enable for CLK2 0h = Output Disabled (low/low) 1h = Output Enabled
6	CLK_EN_3	R/W	1h	Output Enable for CLK3 0h = Output Disabled (low/low) 1h = Output Enabled
5	CLK_EN_4	R/W	1h	Output Enable for CLK4 0h = Output Disabled (low/low) 1h = Output Enabled
4	RESERVED	R	0h	Reserved
3	CLK_EN_5	R/W	1h	Output Enable for CLK5 0h = Output Disabled (low/low) 1h = Output Enabled
2	CLK_EN_6	R/W	1h	Output Enable for CLK6 0h = Output Disabled (low/low) 1h = Output Enabled
1	CLK_EN_7	R/W	1h	Output Enable for CLK7 0h = Output Disabled (low/low) 1h = Output Enabled
0	RESERVED	R	0h	Reserved

11.2 R1 Register (Offset = 1h) [Reset = 24h]

R1 is shown in Table 11-4.

Return to the Summary Table.

Table 11-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	CLK_EN_0	R/W	1h	Output Enable for CLK0 0h = Output Disabled (low/low) 1h = Output Enabled
4:3	RESERVED	R	0h	Reserved
2	CLK_EN_1	R/W	1h	Output Enable for CLK1 0h = Output Disabled (low/low) 1h = Output Enabled
1:0	RESERVED	R	0h	Reserved

11.3 R2 Register (Offset = 2h) [Reset = 00h]

R2 is shown in Table 11-5.

Return to the Summary Table.

Table 11-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RB_OEb_2	R	0h	Status of OEb2
6	RB_OEb_3	R	0h	Status of OEb3
5	RB_OEb_4	R	0h	Status of OEb4
4	RESERVED	R	0h	Reserved
3	RB_OEb_5	R	0h	Status of OEb5

Table 11-5. R2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RB_OEb_6	R	0h	Status of OEb6
1	RB_OEb_7	R	0h	Status of OEb7
0	RESERVED	R	0h	Reserved

11.4 R3 Register (Offset = 3h) [Reset = 00h]

R3 is shown in Table 11-6.

Return to the Summary Table.

Table 11-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	RB_OEb_0	R	0h	Status of OEb0
4:3	RESERVED	R	0h	Reserved
2	RB_OEb_1	R	0h	Status of OEb1
1:0	RESERVED	R	0h	Reserved

11.5 R4 Register (Offset = 4h) [Reset = 10h]

R4 is shown in Table 11-7.

Return to the Summary Table.

Table 11-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	AOD_ENABLE	R/W	1h	Enable automatic output disable (AOD) to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information. 0h = Disabled (DC Coupled) 1h = Enabled (AC Coupled)
3:1	RESERVED	R	0h	Reserved
0	RB_SBI_ENQ	R	0h	Status of SBI_ENQ

11.6 R5 Register (Offset = 5h) [Reset = 0Ah]

R5 is shown in Table 11-8.

Return to the Summary Table.

Table 11-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	Reserved
3:0	VENDOR_ID	R	Ah	Vendor ID

11.7 R6 Register (Offset = 6h) [Reset = 08h]

R6 is shown in Table 11-9.

Return to the Summary Table.

Table 11-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID	R	8h	Device ID

11.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in Table 11-10.

Return to the Summary Table.

Table 11-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:0	SMBUS_BC	R/W	7h	SMBUS Block Read Byte Count

11.9 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in Table 11-11.

Return to the Summary Table.

Table 11-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_MASK_2	R/W	0h	Mask off Side-Band Disable for CLK2
6	SBI_MASK_3	R/W	0h	Mask off Side-Band Disable for CLK3
5	SBI_MASK_4	R/W	0h	Mask off Side-Band Disable for CLK4
4	RESERVED	R	0h	Reserved
3	SBI_MASK_5	R/W	0h	Mask off Side-Band Disable for CLK5
2	SBI_MASK_6	R/W	0h	Mask off Side-Band Disable for CLK6
1	SBI_MASK_7	R/W	0h	Mask off Side-Band Disable for CLK7
0	RESERVED	R	0h	Reserved

11.10 R9 Register (Offset = 9h) [Reset = 00h]

R9 is shown in Table 11-12.

Return to the Summary Table.

Table 11-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SBI_MASK_0	R/W	0h	Mask off Side-Band Disable for CLK0
4:3	RESERVED	R	0h	Reserved
2	SBI_MASK_1	R/W	0h	Mask off Side-Band Disable for CLK1
1:0	RESERVED	R	0h	Reserved

11.11 R11 Register (Offset = Bh) [Reset = EEh]

R11 is shown in Table 11-13.

Return to the Summary Table.

Table 11-13. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SBI_CLK_2	R	1h	Readback of Side-Band Disable for CLK5
6	SBI_CLK_3	R	1h	Readback of Side-Band Disable for CLK4
5	SBI_CLK_4	R	1h	Readback of Side-Band Disable for CLK3
4	RESERVED	R	0h	Reserved
3	SBI_CLK_5	R	1h	Readback of Side-Band Disable for CLK2
2	SBI_CLK_6	R	1h	Readback of Side-Band Disable for CLK1
1	SBI_CLK_7	R	1h	Readback of Side-Band Disable for CLK0
0	RESERVED	R	0h	Reserved

11.12 R12 Register (Offset = Ch) [Reset = 24h]

R12 is shown in Table 11-14.

Return to the Summary Table.

Table 11-14. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SBI_CLK_0	R	1h	Readback of Side-Band Disable for CLK7
4:3	RESERVED	R	0h	Reserved
2	SBI_CLK_1	R	1h	Readback of Side-Band Disable for CLK6
1:0	RESERVED	R	0h	Reserved

11.13 R17 Register (Offset = 11h) [Reset = 66h]

R17 is shown in Table 11-15.

Return to the Summary Table.

Table 11-15. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	AMP_1	R/W	6h	Global Differential output Control 0.6V~1V 25mV/step Default = 0.8V 0h = 600 mV 1h = 625 mV 2h = 650 mV 3h = 675 mV 4h = 700 mV 5h = 725 mV 6h = 750 mV 7h = 775 mV 8h = 800 mV 9h = 825 mV Ah = 850 mV Bh = 875 mV Ch = 900 mV Dh = 925 mV Eh = 950 mV Fh = 975 mV
3:0	RESERVED	R	0h	Reserved

11.14 R18 Register (Offset = 12h) [Reset = 08h]

R18 is shown in Table 11-16.

Return to the Summary Table.

Table 11-16. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_EN_AC_INPUT	R/W	0h	Enable receiver bias when CLKIN is AC coupled 0h = DC Coupled Input 1h = AC Coupled Input
6	RX_EN_RTERM_LSB	R/W	0h	Enable/Disables termination resistors on CLKIN1 0h = Disabled 1h = Enabled
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	PD_RESTOREB	R/W	1h	Save Configuration in Power Down 0h = Config Cleared 1h = Config Saved
2:1	RESERVED	R	0h	Reserved
0	LOSb_RB	R	0h	Real time read back of loss detect block output 0h = LOS Event Detected 1h = LOS Event Not-Detected

11.15 R20 Register (Offset = 14h) [Reset = EEh]

R20 is shown in Table 11-17.

Return to the Summary Table.

Table 11-17. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK2_MSB	R/W	1h	MSB CLK2 slew rate select
6	SLEWRATE_SEL_CLK3_MSB	R/W	1h	MSB CLK3 slew rate select
5	SLEWRATE_SEL_CLK4_MSB	R/W	1h	MSB CLK4 slew rate select
4	RESERVED	R	0h	Reserved
3	SLEWRATE_SEL_CLK5_MSB	R/W	1h	MSB CLK5 slew rate select
2	SLEWRATE_SEL_CLK6_MSB	R/W	1h	MSB CLK6 slew rate select
1	SLEWRATE_SEL_CLK7_MSB	R/W	1h	MSB CLK7 slew rate select
0	RESERVED	R	0h	Reserved

11.16 R21 Register (Offset = 15h) [Reset = 24h]

R21 is shown in Table 11-18.

Return to the Summary Table.

Table 11-18. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SLEWRATE_SEL_CLK0_MSB	R/W	1h	MSB CLK0 slew rate select
4:3	RESERVED	R	0h	Reserved

Table 11-18. R21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SLEWRATE_SEL_CLK1_MSB	R/W	1h	MSB CLK1 slew rate select
1:0	RESERVED	R	0h	Reserved

11.17 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in Table 11-19.

Return to the Summary Table.

Table 11-19. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0h	Reserved
0	WRITE_LOCK	R	0h	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power. 0h = SMBus Not Locked for Writing 1h = SMBus Locked for Writing

11.18 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in Table 11-20.

Return to the Summary Table.

Table 11-20. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0h	Reserved
1	LOS_EVT	R/W	0h	LOS Event Status. When high, indicates that a LOS event is detected. Can be cleared by writing a 1 to the bit. 0h = Not LOS Event Detected 1h = LOS Event Detected
0	WRITE_LOCK_RW1C	R	0h	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to the bit. 0h = SMBus Not Locked for Writing 1h = SMBus Locked for Writing

11.19 R53 Register (Offset = 35h) [Reset = 00h]

R53 is shown in Table 11-21.

Return to the Summary Table.

Table 11-21. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5	SLEWRATE_CTRL_MODE	R/WSC	0h	Sets which mode is used to change the outputs slew rates 0h = Pin mode 1h = SMBus mode
4:0	RESERVED	R	0h	Reserved

11.20 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in Table 11-22.

Return to the Summary Table.

Table 11-22. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEWRATE_SEL_CLK7_LSB	R/W	0h	LSB CLK7 Slew Rate Control
6	SLEWRATE_SEL_CLK6_LSB	R/W	0h	LSB CLK6 Slew Rate Control
5	SLEWRATE_SEL_CLK5_LSB	R/W	0h	LSB CLK5 Slew Rate Control
4	SLEWRATE_SEL_CLK4_LSB	R/W	0h	LSB CLK4 Slew Rate Control
3	SLEWRATE_SEL_CLK3_LSB	R/W	0h	LSB CLK3 Slew Rate Control
2	SLEWRATE_SEL_CLK2_LSB	R/W	0h	LSB CLK2 Slew Rate Control
1	SLEWRATE_SEL_CLK1_LSB	R/W	0h	LSB CLK1 Slew Rate Control
0	SLEWRATE_SEL_CLK0_LSB	R/W	0h	LSB CLK0 Slew Rate Control

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMKDB1120 Evaluation Module*, user's guide
- Texas Instruments, *LMKDB1108 Evaluation Module*, user's guide
- Texas Instruments, *Timing is Everything: How to measure additive jitter*, blog post

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2023) to Revision B (February 2024)	Page
• Updated the number format for tables, figures, and cross-references throughout the document	1
• Added additional explanations for recommended PWRDN# assertion/deassertion sequences and effects when not followed properly in the *PWRDN# Assertion and Deassertion* section	31

Changes from Revision * (November 2023) to Revision A (December 2023)	Page
• Updated the number format for tables, figures, and cross-references throughout the document	1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMKDB1120Z100NPPR	ACTIVE	TLGA	NPP	80	2500	RoHS & Green	Call TI	Call TI	-40 to 105	LMKDB 1120Z100	Samples
LMKDB1120Z100NPPT	ACTIVE	TLGA	NPP	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	LMKDB 1120Z100	Samples
LMKDB1120Z85NPPR	ACTIVE	TLGA	NPP	80	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	LMKDB 1120Z85	Samples
LMKDB1120Z85NPPT	ACTIVE	TLGA	NPP	80	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	LMKDB 1120Z85	Samples
PLMKDB1108RKPT	ACTIVE	VQFN	RKP	40	250	TBD	Call TI	Call TI	-40 to 85		Samples
PLMKDB1120NPPT	ACTIVE	TLGA	NPP	80	250	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

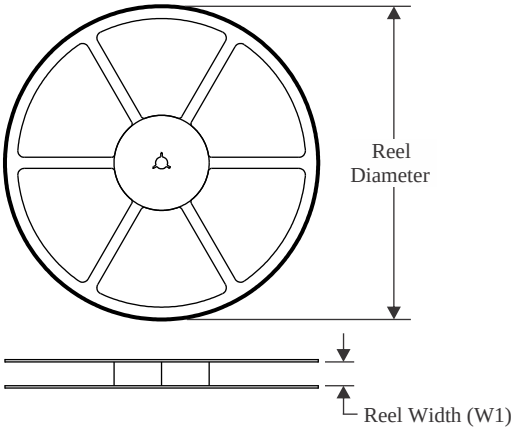
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

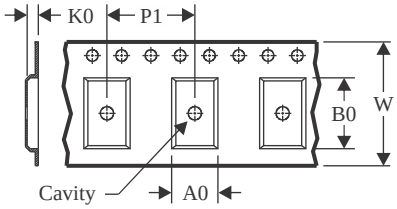
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

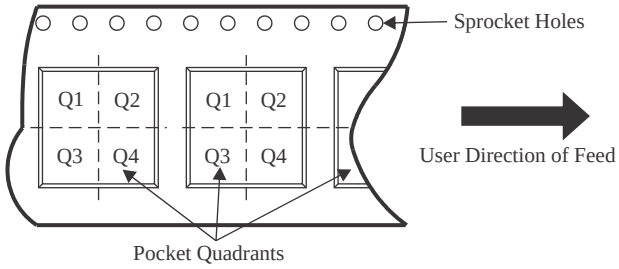


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

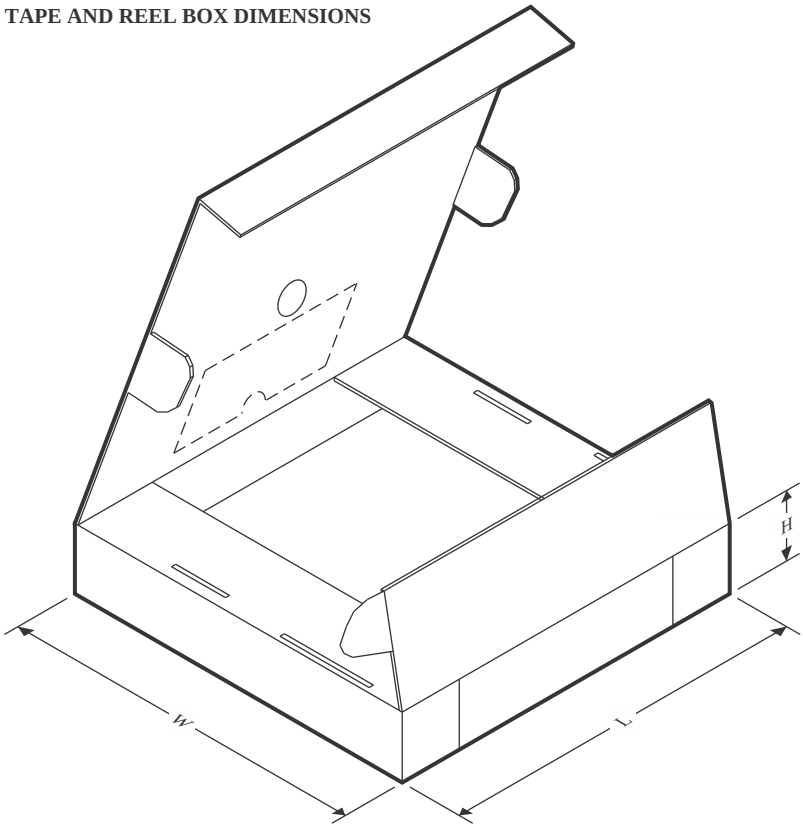
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMKDB1120Z85NPPR	TLGA	NPP	80	2500	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

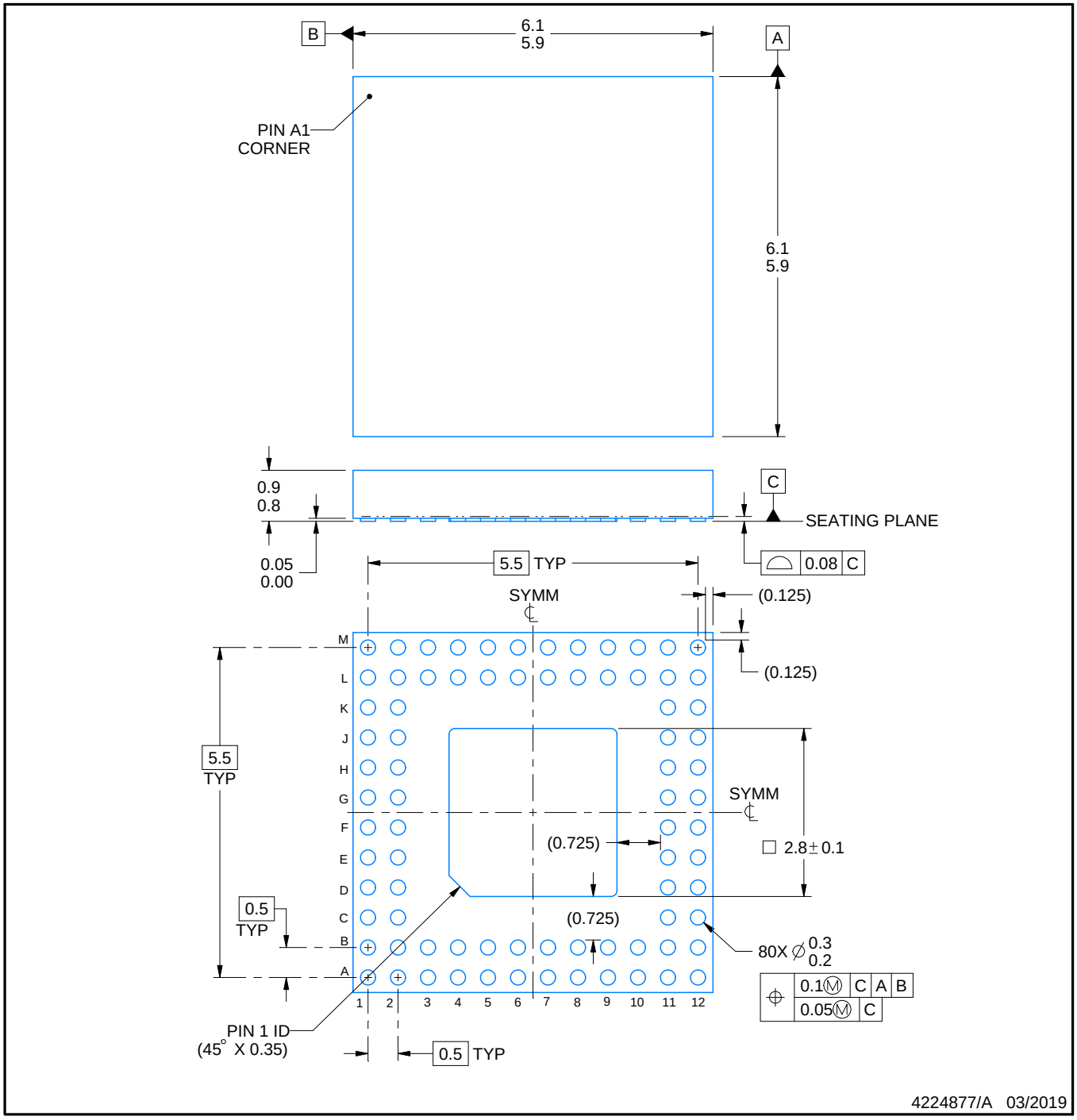
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMKDB1120Z85NPPR	TLGA	NPP	80	2500	210.0	185.0	35.0

PACKAGE OUTLINE

NPP0080A

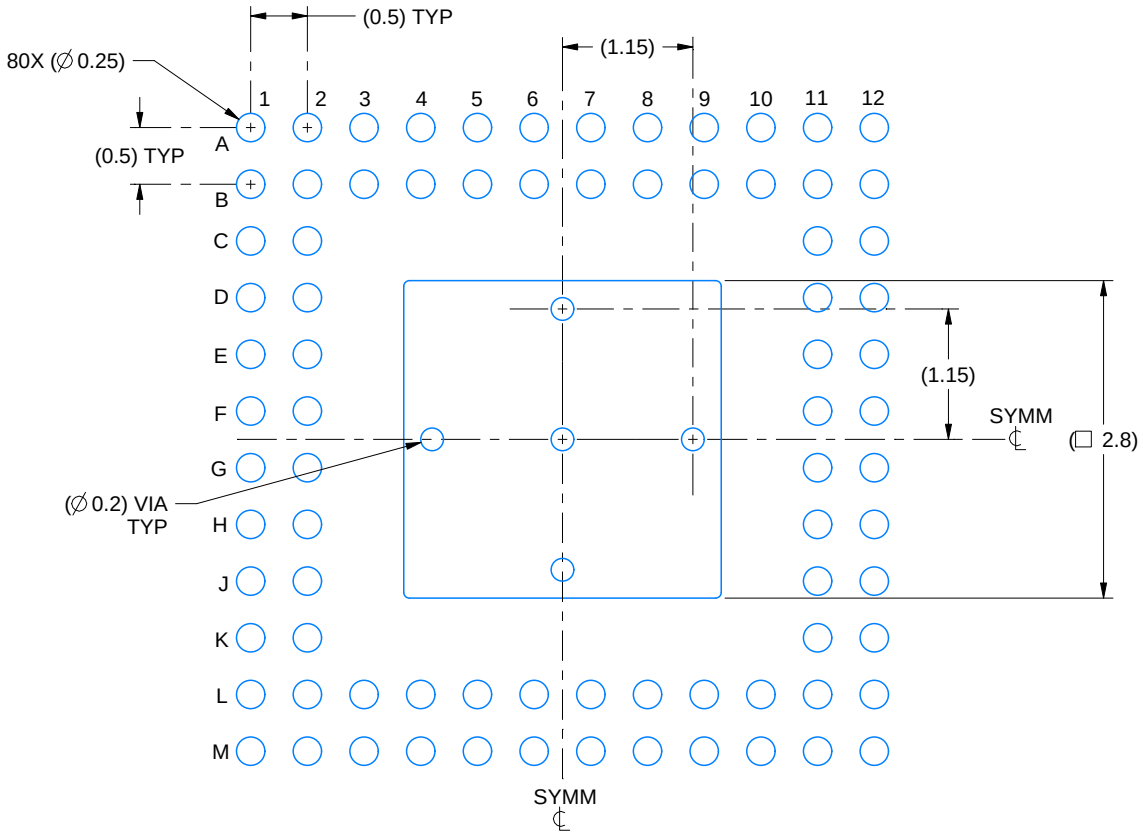
TLGA - 0.9 mm max height

THIN LAND GRID ARRAY

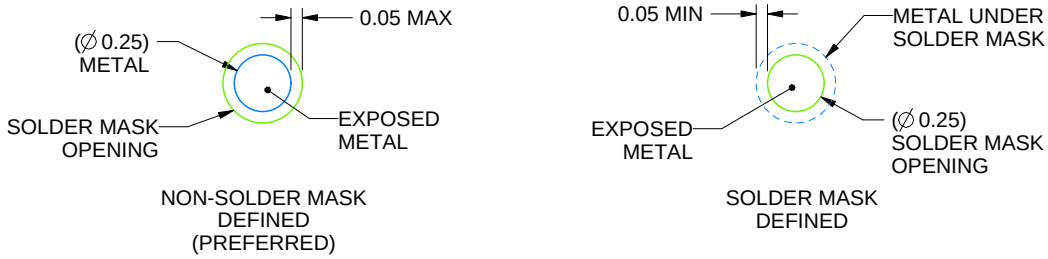


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

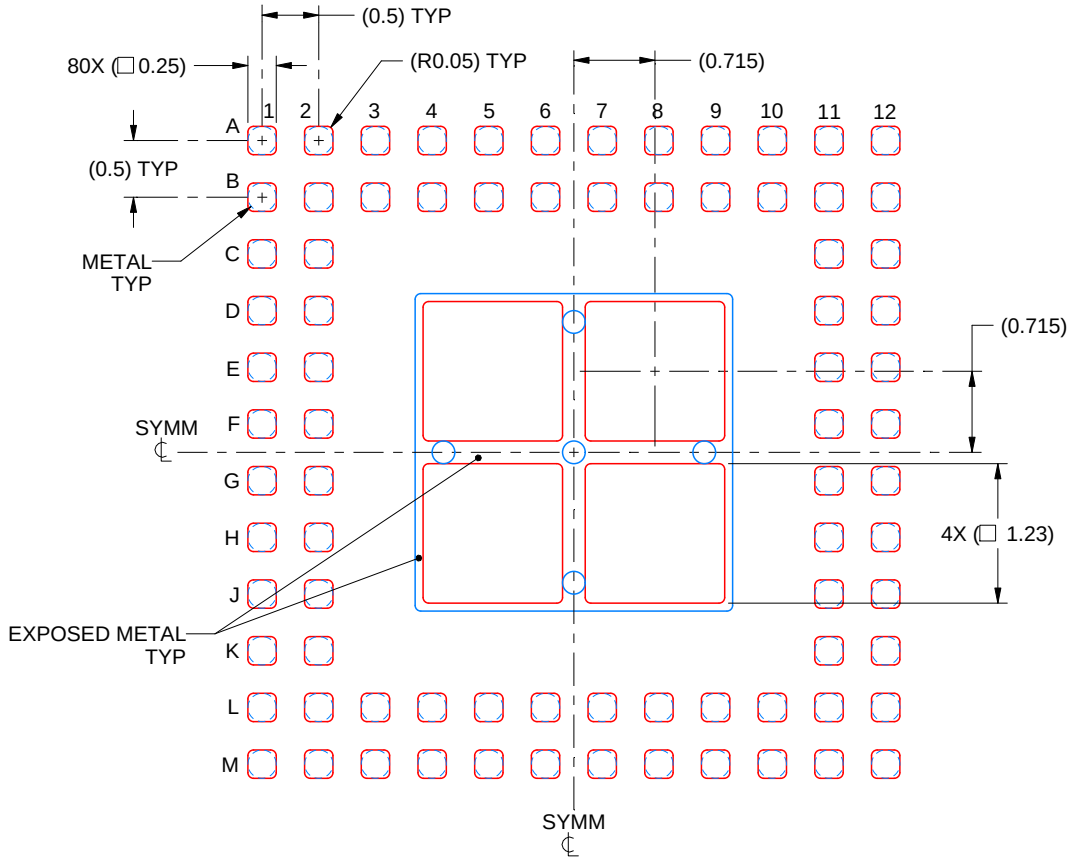


SOLDER MASK DETAILS
NOT TO SCALE

4224877/A 03/2019

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 15X

4224877/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GENERIC PACKAGE VIEW

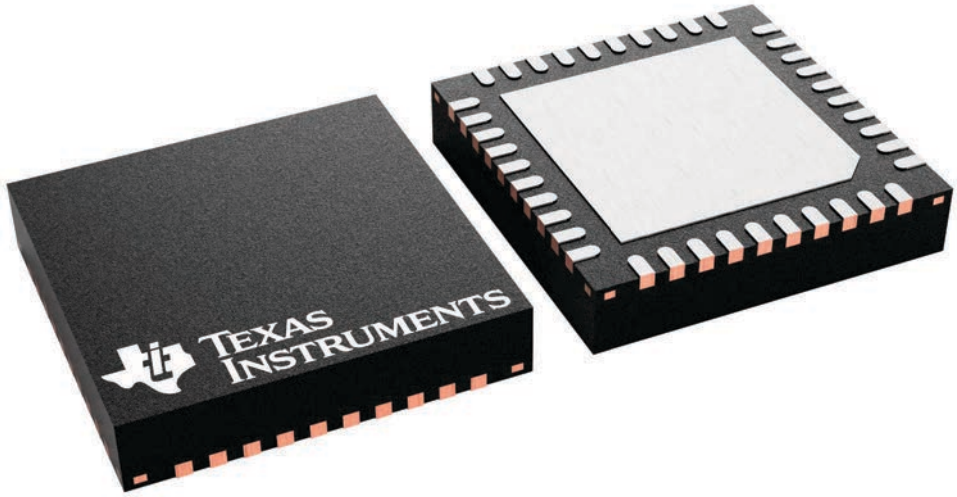
RKP 40

VQFN - 1 mm max height

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



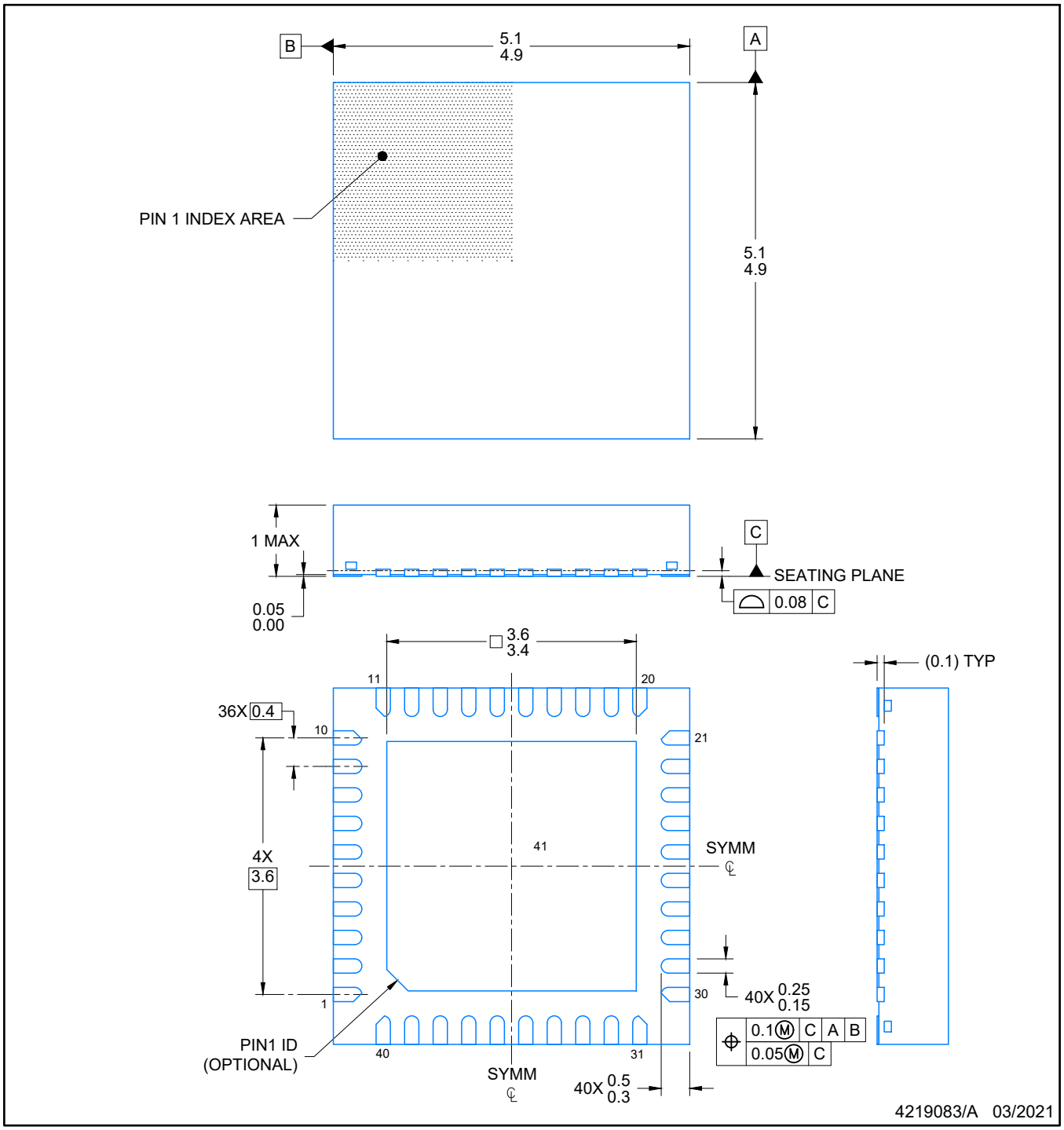
4229305/A

PACKAGE OUTLINE

RKP0040B

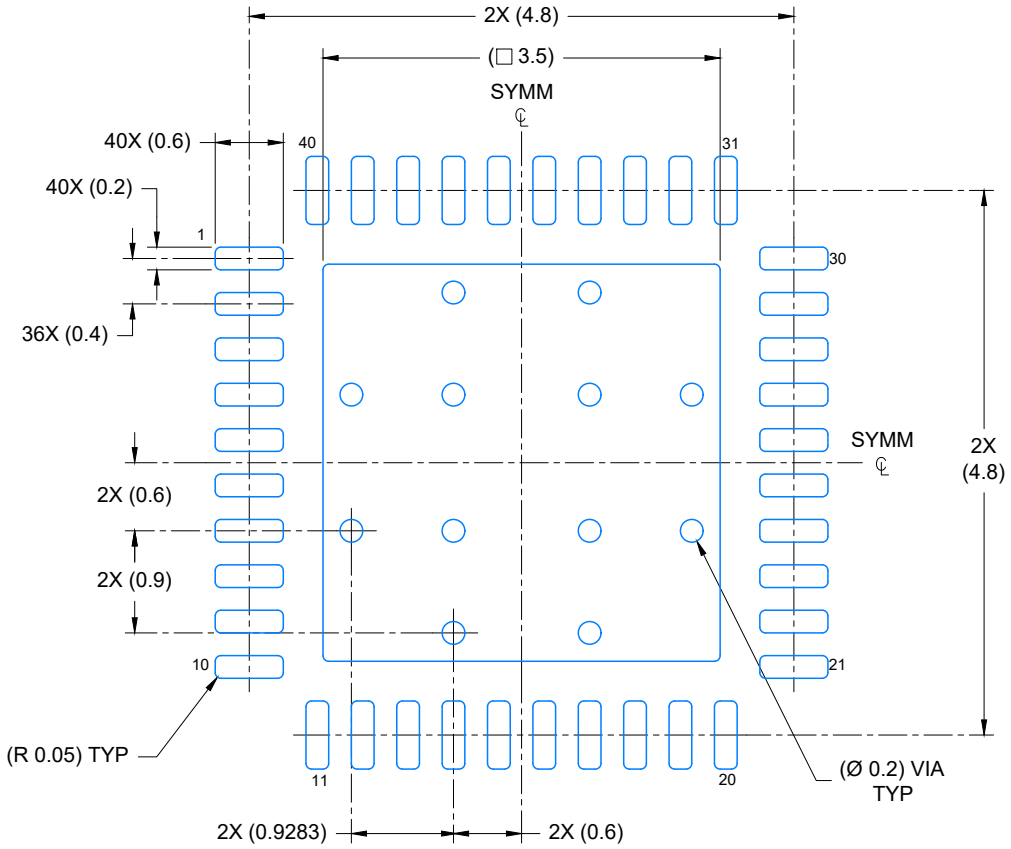
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

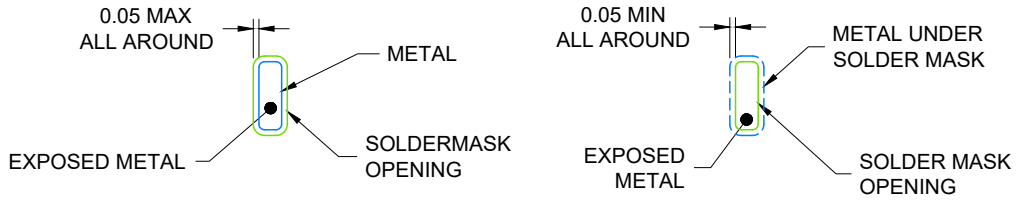


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK DEFINED (PREFERRED)

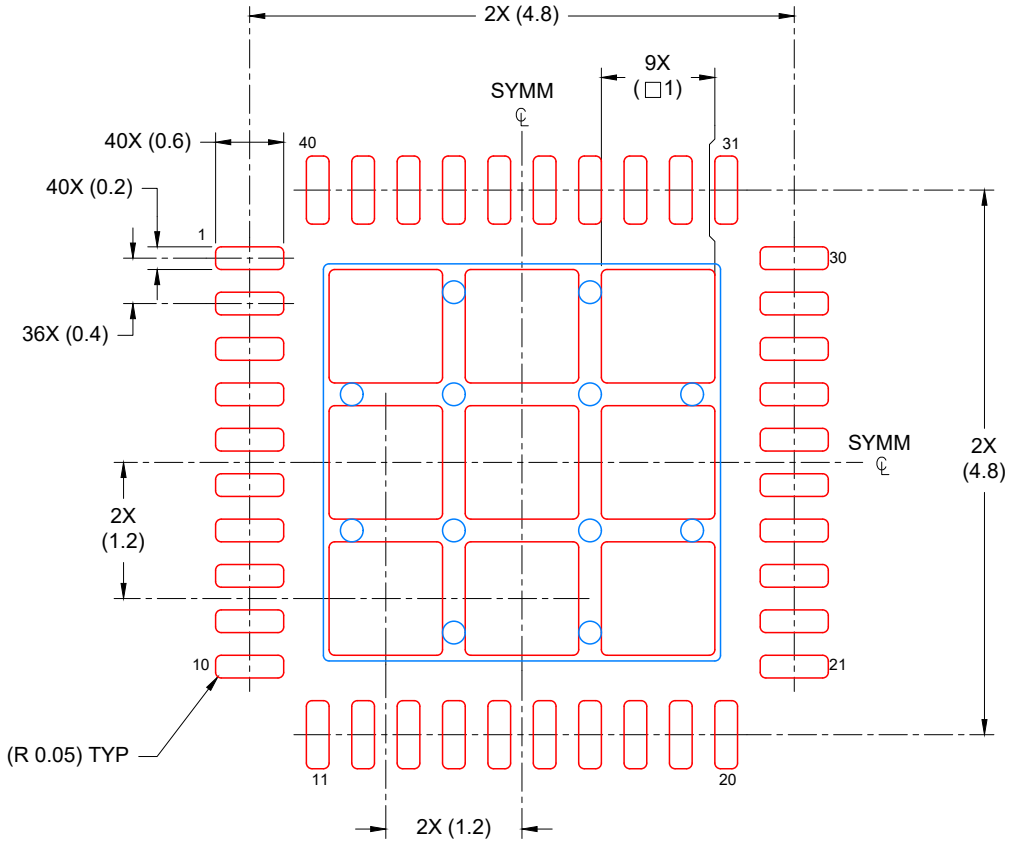
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219083/A 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 15X

4219083/A 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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