LMQ61460-Q1 Automotive 3-V to 36-V, 6 A, Low EMI Synchronous Step-Down Quiet Converter

1 Features

- Functional safety capable
  - Documentation available to aid functional safety system design
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: -40°C to +150°C, $T_J$
- Optimized for ultra-low EMI requirements
  - Meets CISPR25 class 5 standard
  - Hotrod™ package minimizes switch node ringing
  - Internal bypass capacitors reduce EMI
  - Parallel input path minimizes parasitic inductance
  - Spread spectrum reduces peak emissions
  - Adjustable SW node rise time
- Designed for rugged Automotive applications
  - Supports 42-V load dump
  - 0.4-V dropout with 4-A load (typical)
- High efficiency power conversion at all loads
  - 7-µA no load current at 13.5 $V_{IN}$, 3.3 $V_{OUT}$
  - 83% PFM efficiency at 1-mA, 13.5 $V_{IN}$, 5 $V_{OUT}$
- External bias option for improved efficiency
- Suitable for scalable power supplies
  - Pin compatible with:
    - LM61460-Q1 (36 V, 6 A)

2 Applications

- Automotive infotainment and cluster: head unit, media hub, USB charge, display
- Automotive ADAS and body electronics

3 Description

The LMQ61460-Q1 is a high-performance, DC-DC synchronous step-down quiet converter. With integrated high-side and low-side MOSFETs, up to 6 A of output current is delivered over a wide input range of 3.0 V to 36 V; 42-V tolerance supports load dump for durations of 400 ms. The device implements soft recovery from dropout eliminating overshoot on the output.

The device is specifically designed for minimal EMI. The device incorporates pseudo-random spread spectrum, integrated bypass capacitors, adjustable SW node rise time, low-EMI VQFN-HR package featuring low switch node ringing, and optimized pinout for ease of use. The switching frequency can be synchronized between 200 kHz and 2.2 MHz to avoid noise sensitive frequency bands. In addition the frequency can be selected for improved efficiency at low operating frequency or smaller solution size at high operating frequency.

Auto-mode enables frequency foldback when operating at light loads, allowing an unloaded current consumption of only 7 µA (typical) and high light load efficiency. Seamless transition between PWM and PFM modes, along with very low MOSFET ON resistances and an external bias input, ensures exceptional efficiency across the entire load range.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMQ61460-Q1</td>
<td>VQFN-HR (14)</td>
<td>4.00 mm × 3.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency: $V_{OUT} = 5$ V, $F_{SW} = 2.1$ MHz
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2020) to Revision A

<table>
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<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Added functional safety bullet to the Features</td>
</tr>
<tr>
<td>• Updated Device Comparison Table</td>
</tr>
</tbody>
</table>

5 Description (continued)

The device is available in a 14-pin VQFN-HR package with wettable flanks. Electrical characteristics are specified over a junction temperature range of –40°C to +150°C. Find additional resources in the Related Documentation.
## 6 Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>ORDERABLE PART NUMBER</th>
<th>REFERENCE PART NUMBER</th>
<th>LIGHT LOAD MODE</th>
<th>SPREAD SPECTRUM</th>
<th>OUTPUT VOLTAGE</th>
<th>SWITCHING FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMQ61460-Q1</td>
<td>PLMQ61460AASQRJTQ1</td>
<td>LMQ61460AAS-Q1</td>
<td>Auto Mode</td>
<td>Yes</td>
<td>Adjustable</td>
<td>Adjustable</td>
</tr>
<tr>
<td></td>
<td>PLMQ61460AFSQRJTQ1</td>
<td>LMQ61460AFS-Q1</td>
<td>FPWM</td>
<td>Yes</td>
<td>Adjustable</td>
<td>Adjustable</td>
</tr>
</tbody>
</table>
7 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>NAME</th>
<th>NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIAS</td>
<td>P</td>
<td>1</td>
<td>BIAS</td>
<td>Input to internal LDO. Connect to output voltage point to improve efficiency. Connect an optional high-quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If output voltage is above 12 V, connect this pin to ground.</td>
</tr>
<tr>
<td>VCC</td>
<td>O</td>
<td>2</td>
<td>VCC</td>
<td>Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-µF capacitor from this pin to AGND.</td>
</tr>
<tr>
<td>AGND</td>
<td>G</td>
<td>3</td>
<td>AGND</td>
<td>Analog ground for internal circuitry. Feedback and VCC are measured with respect to this pin. Must connect AGND to both PGND1 and PGND2 on PCB.</td>
</tr>
<tr>
<td>FB</td>
<td>I</td>
<td>4</td>
<td>FB</td>
<td>Output voltage feedback input to the internal control loop. Connect to output voltage sense point for fixed 3.3 V or 5 V output voltage factory options. Connect to feedback divider tap point for adjustable output voltage. Do not float or connect to ground.</td>
</tr>
<tr>
<td>PGOOD</td>
<td>O</td>
<td>5</td>
<td>PGOOD</td>
<td>Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PGOOD output goes low when EN = low, $V_{IN} &gt; 1$ V.</td>
</tr>
<tr>
<td>RT</td>
<td>I/O</td>
<td>6</td>
<td>RT</td>
<td>Connect this pin to ground through a resistor with value between 5.76 kΩ and 66.5 kΩ to set switching frequency between 200 kHz and 2200 kHz. Do not float or connect to ground.</td>
</tr>
<tr>
<td>EN/SYNC</td>
<td>I</td>
<td>7</td>
<td>EN/SYNC</td>
<td>Precision enable input. High = on, Low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. See the Application and Implementation section. Do not float. EN/SYNC also functions as a synchronization input pin. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock. A capacitor can be used to ACS couple the synchronization signal to this pin. When synchronized to external clock, the device functions in forced PWM and disables the PFM light load efficiency mode. See the Detailed Description.</td>
</tr>
<tr>
<td>VIN1</td>
<td>P</td>
<td>8</td>
<td>VIN1</td>
<td>Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.</td>
</tr>
<tr>
<td>PGND1</td>
<td>G</td>
<td>9</td>
<td>PGND1</td>
<td>Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.</td>
</tr>
<tr>
<td>SW</td>
<td>O</td>
<td>10</td>
<td>SW</td>
<td>Switch node of the converter. Connect to output inductor.</td>
</tr>
<tr>
<td>PGND2</td>
<td>G</td>
<td>11</td>
<td>PGND2</td>
<td>Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.</td>
</tr>
<tr>
<td>VIN2</td>
<td>P</td>
<td>12</td>
<td>VIN2</td>
<td>Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.</td>
</tr>
<tr>
<td>RBOOT</td>
<td>I/O</td>
<td>13</td>
<td>RBOOT</td>
<td>Connect to CBOOT through a resistor. This resistance must be between 0 Ω and open and determines SW node rise time.</td>
</tr>
<tr>
<td>CBOOT</td>
<td>I/O</td>
<td>14</td>
<td>CBOOT</td>
<td>High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and CBOOT. An internal diode connects to VCC and allows CBOOT to charge while SW node is low.</td>
</tr>
</tbody>
</table>
8 Specifications

8.1 Absolute Maximum Ratings
Over the recommended operating junction temperature range of -40°C to +150°C (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(VIN1, VIN2) to AGND, PGND</td>
<td>-0.3</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>(RBOOT) to SW</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(CBOOT) to SW</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>BIAS to AGND, PGND</td>
<td>-0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>EN to AGND, PGND</td>
<td>-0.3</td>
<td>42</td>
<td>V</td>
</tr>
<tr>
<td>SYNC/MODE to AGND, PGND</td>
<td>-0.3</td>
<td>lower of 36 and (V_{}\text{IN}+5)</td>
<td>V</td>
</tr>
<tr>
<td>(FB) to AGND, PGND</td>
<td>-0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>(PGOOD) to AGND, PGND</td>
<td>0</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>PGND to AGND(^{(2)})</td>
<td>-1</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>(SW) to AGND, PGND(^{(3)})</td>
<td>-0.3</td>
<td>(V_{\text{IN}}+0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(VCC) to AGND, PGND</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(PGOOD) sink current(^{(4)})</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) This specification applies to voltage durations of 100 ns or less. The maximum D.C. voltage should not exceed ± 0.3 V.

\(^{(3)}\) A voltage of 2 V below GND and 2 V above \(V_{\text{IN}}\) can appear on this pin for \(\leq 200\) ns with a duty cycle of \(\leq 0.01\%\).

\(^{(4)}\) Do not exceed pin’s voltage rating.

8.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}}) Electrostatic discharge</td>
<td>±2000</td>
</tr>
<tr>
<td>Human body model (HBM), per AEC Q100-002(^{(1)}) Device HBM Classification Level 2</td>
<td>±2000</td>
</tr>
<tr>
<td>Charged device model (CDM), per AEC Q100-011 Device CDM Classification Level CS</td>
<td>±750</td>
</tr>
</tbody>
</table>

\(^{(1)}\) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions
Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>Input voltage range after start-up</td>
<td>3</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>Output voltage range for adjustable version(^{(2)})</td>
<td>1</td>
<td>0.95 * (V_{\text{IN}})</td>
<td>V</td>
</tr>
<tr>
<td>Frequency</td>
<td>Free running frequency</td>
<td>2.1</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Sync frequency</td>
<td>Synchronization frequency range</td>
<td>200</td>
<td>2200</td>
<td>kHz</td>
</tr>
<tr>
<td>Load current</td>
<td>Output DC current range(^{(3)})</td>
<td>0</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>Temperature</td>
<td>Operating junction temperature (T_J) range(^{(4)})</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics table.

\(^{(2)}\) Under no conditions should the output voltage be allowed to fall below zero volts.

\(^{(3)}\) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. See Application section for details.

\(^{(4)}\) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
### 8.4 Thermal Information

The value of $R_{\text{th JA}}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 4-layer PCB, a $R_{\text{th JA}} = 25 \degree\text{C/W}$ can be achieved. For design information see Maximum Ambient Temperature versus Output Current.

<table>
<thead>
<tr>
<th>THERMAL METRIC (1) (2)</th>
<th>LMQ61460-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{th JA}}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>59</td>
</tr>
<tr>
<td>$R_{\text{th JC(top)}}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>19</td>
</tr>
<tr>
<td>$R_{\text{th JB}}$</td>
<td>Junction-to-board thermal resistance</td>
<td>19.2</td>
</tr>
<tr>
<td>$\Psi_{\text{JT}}$</td>
<td>Junction-to-top characterization parameter</td>
<td>1.4</td>
</tr>
<tr>
<td>$\Psi_{\text{JB}}$</td>
<td>Junction-to-board characterization parameter</td>
<td>19</td>
</tr>
<tr>
<td>$R_{\text{th JC(bot)}}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>-</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) The value of $R_{\text{th JA}}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

### 8.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25\degree\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{\text{IN}} = 13.5\ \text{V}$, VIN1 shorted to VIN2 = $V_{\text{IN}}$, $V_{\text{OUT}}$ is converter output voltage.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{IN,OPERATE}}$</td>
<td>Input operating voltage (1) Needed to start up</td>
<td>3.95</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Once operating</td>
<td>3.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IN,OPERATE}_H}$</td>
<td>Hysteresis (1)</td>
<td></td>
<td></td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{Q}}$</td>
<td>Operating quiescent current (not switching); measured at VIN pin (2)</td>
<td>$V_{FB} = +5%, V_{BIAS} = 5\ \text{V}$</td>
<td>0.6</td>
<td>6</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{Bias}}$</td>
<td>Current into BIAS pin (not switching, maximum at $T_J = 125\degree\text{C}$) (5)</td>
<td>$V_{FB} = +5%, V_{BIAS} = 5\ \text{V}$, Auto Mode</td>
<td>24</td>
<td>31.2</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{\text{SD}}$</td>
<td>Shutdown quiescent current; measured at VIN pin</td>
<td>$EN = 0\ \text{V}$, $T_J = 25\degree\text{C}$</td>
<td>0.6</td>
<td>6</td>
<td>µA</td>
</tr>
</tbody>
</table>

**ENABLE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{EN}}$</td>
<td>Enable input threshold voltage - rising</td>
<td></td>
<td></td>
<td>1.263</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{EN-ACC}}$</td>
<td>Enable input threshold voltage - rising deviation from typical</td>
<td></td>
<td>-8.1</td>
<td>8.1</td>
<td>%</td>
</tr>
<tr>
<td>$V_{\text{EN-HYST}}$</td>
<td>Enable threshold hysteresis as percentage of $V_{\text{EN}}$ (TYP)</td>
<td></td>
<td>24</td>
<td>28</td>
<td>32</td>
</tr>
<tr>
<td>$V_{\text{EN-WAKE}}$</td>
<td>Enable wake-up threshold</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{EN}}$</td>
<td>Enable pin input current</td>
<td>$V_{\text{IN}} = EN = 13.5\ \text{V}$</td>
<td></td>
<td>2.3</td>
<td></td>
</tr>
</tbody>
</table>

**LDO - VCC**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CC}}$</td>
<td>Internal $V_{\text{CC}}$ voltage</td>
<td>$V_{\text{BIAS}} &gt; 3.4\ \text{V}$, CCM Operation (1)</td>
<td>3.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{BIAS}} = 3.1\ \text{V}$, Non-switching</td>
<td>3.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{CC_UVLLO}}$</td>
<td>Internal $V_{\text{CC}}$ input under voltage lock-out</td>
<td>$V_{\text{CC}}$ rising under voltage threshold</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters.

(2) This is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. It does not represent the total input current to the system while regulating. For additional information, reference the Systems Characteristics Table and the Input Supply Current Section.
Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at \( T_J = 25°C \), and are provided for reference purposes only. Unless otherwise stated the following conditions apply: \( V_N = 13.5 \) V, VIN1 shorted to VIN2 = \( V_N \). VOUT is converter output voltage.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VCC_UVLO_HYST</strong></td>
<td>Internal VCC input under voltage lock-out</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>FEEDBACK</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{FB_{acc}} ) Initial reference voltage accuracy for 5-V, 3.3-V and adjustable (1 V FB) versions</td>
<td>( V_BN = 3.3 ) V to 36 V, ( T_J = 25°C ), FPWM Mode</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>%</td>
</tr>
<tr>
<td>( V_{OUT_{acc}} ) Reference voltage accuracy for Fixed 3.3-V VOUT trim option</td>
<td>( V_BN = 13.5 ) V, FPWM Mode</td>
<td>3.2587</td>
<td>3.3</td>
<td>3.3413</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUT_{acc}} ) Reference voltage accuracy for Fixed 5-V VOUT trim option</td>
<td>( V_BN = 13.5 ) V, FPWM Mode</td>
<td>4.9375</td>
<td>5</td>
<td>5.0625</td>
<td>V</td>
</tr>
<tr>
<td>( R_{FB} ) Resistance from FB to AGND</td>
<td>5-V Option</td>
<td>7.4</td>
<td></td>
<td></td>
<td>MO</td>
</tr>
<tr>
<td></td>
<td>3.3-V Option</td>
<td>8.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{FB} ) Input current from FB to AGND</td>
<td>Adjustable versions only, FB = 1 V</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{ADJ} ) Minimum adjustable frequency by ( R_T ) or SYNC</td>
<td>( R_T = 66.5 ) kΩ</td>
<td>0.18</td>
<td>0.2</td>
<td>0.22</td>
<td>MHz</td>
</tr>
<tr>
<td>Adjusted frequency by ( R_T ) or SYNC with 400 kHz setting</td>
<td>( R_T = 33.2 ) kΩ</td>
<td>0.36</td>
<td>0.4</td>
<td>0.44</td>
<td>MHz</td>
</tr>
<tr>
<td>Maximum adjustable frequency by ( R_T ) or SYNC</td>
<td>( R_T = 5.76 ) kΩ</td>
<td>1.98</td>
<td>2.2</td>
<td>2.42</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{SW} ) Switching frequency</td>
<td>( V_BN = 13.5 ) V, Center frequency with or without spread spectrum, PWM operation</td>
<td>1.9</td>
<td>2.1</td>
<td>2.3</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{SSS} ) Frequency span of spread spectrum operation - largest deviation from center frequency</td>
<td>Spread spectrum active</td>
<td>2</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>( f_{PSS} ) Spread spectrum pattern frequency(^{(1)})</td>
<td>Spread spectrum active, ( f_{SW} = 2.1 ) MHz</td>
<td>1.5</td>
<td></td>
<td></td>
<td>Hz</td>
</tr>
<tr>
<td><strong>MODE/SYNC PIN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{MODE/SYNC} ) MODE/SYNC pin leakage current after startup</td>
<td>( V_BN = 13.5 ) V, ( V_{SYNC/MODE} = 3.3 ) V</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>( V_BN = 13.5 ) V, ( V_{SYNC/MODE} = 5.5 ) V</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{MODE_L} ) MODE/SYNC input voltage low</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{MODE_H} ) MODE/SYNC input voltage high</td>
<td></td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{SYNC_HYST} ) MODE/SYNC input voltage hysteresis</td>
<td></td>
<td>0.185</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{MODE_H2} ) Spread spectrum on if MODE/SYNC voltage is below this voltage and above ( V_{SYNC_H} )</td>
<td>Level dependent operation</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{MODE_H3} ) Spread spectrum off if MODE/SYNC is above this voltage</td>
<td>Level dependent operation</td>
<td>4.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{MODE_DELT__A} ) Difference between MODE/SYNC voltage and VCC voltage needed to turn off spread spectrum</td>
<td>Level dependent operation</td>
<td>0.5</td>
<td>1.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>MOSFETS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{DS_ON_HS} ) Power switch on-resistance</td>
<td>High side MOSFET ( R_{DS_ON} )</td>
<td>41</td>
<td>82</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>( R_{DS_ON_LS} ) Power switch on-resistance</td>
<td>Low side MOSFET ( R_{DS_ON} )</td>
<td>21</td>
<td>45</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>( V_{BOOT_UVLO} ) Voltage on CBOOT pin compared to SW which will turn off high-side switch</td>
<td></td>
<td>2.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Spread spectrum pattern frequency is specified within \( f_{SW} = 1 \) to 2 MHz.
### Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 13.5 \text{ V}$. \( V_{IN1} \) shorted to \( V_{IN2} = V_{IN} \). \( V_{OUT} \) is converter output voltage.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{LHS}$</td>
<td>High side switch current limit(^{(3)})</td>
<td></td>
<td>6</td>
<td>7</td>
<td>8.1</td>
</tr>
<tr>
<td>$I_{LWS}$</td>
<td>Low side switch current limit</td>
<td>3.7</td>
<td>4.8</td>
<td>5.4</td>
<td>A</td>
</tr>
<tr>
<td>$I_{LZC}$</td>
<td>Zero-cross current limit. Positive current direction is out of SW pin</td>
<td></td>
<td>0.25</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{LNEG}$</td>
<td>Negative current limit FPWM and SYNC Modes. Positive current direction is out of SW pin</td>
<td></td>
<td>-2</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{PK_MIN_0}$</td>
<td>Minimum peak command in Auto Mode / device current rating</td>
<td>Pulse duration &lt; 100 ns</td>
<td>25</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$I_{PK_MIN_100}$</td>
<td>Minimum peak command in Auto Mode / device current rating</td>
<td>Pulse duration &gt; 1 ( \mu )s</td>
<td>12.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$V_{HICCUP}$</td>
<td>Ratio of FB voltage to in-regulation FB voltage</td>
<td>Not during soft start</td>
<td>40</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

**POWER GOOD**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN(PGD_VALID)}$</td>
<td>Input voltage for proper PGOOD function (^{(3)})</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PGD(LOW)}$</td>
<td>Low level PGOOD function output voltage</td>
<td>46 ( \mu )A pullup to PGOOD pin, $V_{IN} = 1.0 \text{ V}$, $EN = 0 \text{ V}$</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 mA pullup to PGOOD pin, $V_{IN} = 13.5 \text{ V}$, $EN = 0 \text{ V}$</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 mA pullup to PGOOD pin, $V_{IN} = 13.5 \text{ V}$, $EN = 3.3 \text{ V}$</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$R_{PGD}$</td>
<td>17</td>
<td>40</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td>1 mA pullup to PGOOD pin, $EN = 0 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 mA pullup to PGOOD pin, $EN = 3.3 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OV}$</td>
<td>0.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**THERMAL SHUTDOWN**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{SD_R}$</td>
<td>158</td>
<td>168</td>
<td>180</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{SD_HYST}$</td>
<td></td>
<td></td>
<td>10</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(3)}\) High side current limit is a function of duty factor. High side current limit value is highest at small duty factor and less at higher duty factors.

#### 8.6 Timing Characteristics

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 13.5 \text{ V}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ON_MIN}$</td>
<td>Minimum HS switch on time (^{(3)}) ( V_{IN} = 20 \text{ V}, I_{OUT} = 2 \text{ A}, \text{RBOOT short to CBOOT} )</td>
<td>55</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$I_{ON_MAX}$</td>
<td>Maximum HS switch on time</td>
<td>9</td>
<td></td>
<td></td>
<td>( \mu )s</td>
</tr>
</tbody>
</table>
Timing Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 13.5$ V.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{OFF_MIN}$</td>
<td>Minimum LS switch on time</td>
<td>65</td>
<td>85</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SS}$</td>
<td>Time from first SW pulse to $V_{ref}$ at 90%, of set point.</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{SS2}$</td>
<td>Time from first SW pulse to release of FPWM lockout if output not in regulation</td>
<td>4.5</td>
<td>6.5</td>
<td>8.5</td>
<td>ms</td>
</tr>
<tr>
<td>$t_w$</td>
<td>Short circuit wait time (&quot;Hiccup&quot; time)</td>
<td>40</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Turn-on delay$^{(1)}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_B$</td>
<td>Blanking of EN after rising or falling edges</td>
<td></td>
<td>4</td>
<td>8</td>
<td>µs</td>
</tr>
</tbody>
</table>

**SYNC**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PULSE_H_THRES}$</td>
<td>Analog information used to generate $t_{PULSE_H}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PULSE_H}$</td>
<td>High duration needed to be recognized as a pulse</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PULSE_L_THRES}$</td>
<td>Analog information used to generate $t_{PULSE_L}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PULSE_L}$</td>
<td>Low duration needed to be recognized as a pulse</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SYNC_THRES}$</td>
<td>Analog information used to generate $t_{MODE}$, $t_{SYNC}$</td>
<td>8</td>
<td>16.5</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{MODE}$</td>
<td>Time at one level needed to indicate FPWM or Auto Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SYNC}$</td>
<td>High or low signal duration in a valid synchronization signal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{MEAS}$</td>
<td>SYNC/MODE pin duration of resistance test upon entering Auto Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER GOOD**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PGD_FLT_rise}$</td>
<td>Delay time to PGOOD high signal</td>
<td>1.5</td>
<td>2</td>
<td>2.5</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{PGD_FLT_fall}$</td>
<td>Glitch filter time constant for PGOOD function</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

(1) Parameter specified using design, statistical analysis and production testing of correlated parameters; not tested in production.
8.7 Systems Characteristics

The following values are specified by design provided that the component values in the typical application circuit are used. Limits apply over the junction temperature range of -40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are derived using test, design or statistical correlation. Typical values represent the most likely parametric norm at T\textsubscript{J} = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V\textsubscript{IN} = 13.5 V. VIN1 shorted to VIN2 = V\textsubscript{IN}. V\textsubscript{OUT} is output setting. These parameters are not tested in production.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>η\textsubscript{5V_2p1MHz}</td>
<td>Typical 2.1 MHz efficiency</td>
<td>5V, I\textsubscript{OUT} = 4 A, R\textsubscript{BOOT} = 0 Ω</td>
<td>93</td>
<td>%</td>
</tr>
<tr>
<td>η\textsubscript{3p3V_2p1MHz}</td>
<td>Typical 2.1 MHz efficiency</td>
<td>3.3V, I\textsubscript{OUT} = 4 A, R\textsubscript{BOOT} = 0 Ω</td>
<td>91</td>
<td>%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RANGE OF OPERATION</th>
<th>\textsubscript{VIN_MIN1}</th>
<th>\textsubscript{VIN} for full functionality at reduced load, after start-up.</th>
<th>V\textsubscript{OUT} set to 3.3 V</th>
<th>3.0</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>\textsubscript{VIN_MIN2}</td>
<td>\textsubscript{VIN} for full functionality at 100% of maximum rated load, after start-up.</td>
<td>V\textsubscript{OUT} set to 3.3 V</td>
<td>3.95</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{Q-VIN}</td>
<td>Operating quiescent current(^{(1)})</td>
<td>V\textsubscript{IN} = 5.8 V to 36 V, I\textsubscript{OUT} = 4 A</td>
<td>4.9</td>
<td>5</td>
<td>5.1</td>
</tr>
<tr>
<td>V\textsubscript{OUT5}</td>
<td>Output voltage for 5V factory option</td>
<td>V\textsubscript{IN} = 5.8 V to 36 V, I\textsubscript{OUT} = 4 A, Auto mode, R\textsubscript{FBT}=1 MΩ</td>
<td>4.9</td>
<td>5.05</td>
<td>5.125</td>
</tr>
<tr>
<td>V\textsubscript{OUT3}</td>
<td>Output voltage for 3.3V factory option</td>
<td>V\textsubscript{IN} = 3.9 V to 36 V, I\textsubscript{OUT} = 4 A, Auto mode factory option, V\textsubscript{IN} = 5.8 V to 36 V, I\textsubscript{OUT} = 100 μA to 100 mA</td>
<td>3.24</td>
<td>3.3</td>
<td>3.35</td>
</tr>
<tr>
<td>V\textsubscript{DROP1}</td>
<td>Input to output voltage differential to maintain regulation accuracy without inductor DCR drop</td>
<td>V\textsubscript{IN} = 5.8 V to 36 V, I\textsubscript{OUT} = 4 A, -3% output accuracy at 25°C</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{DROP2}</td>
<td>Input to output voltage differential to maintain (f\textsubscript{SW} \geq 1.85\text{MHz}, ) without DCR drop</td>
<td>V\textsubscript{IN} = 5.8 V to 36 V, I\textsubscript{OUT} = 4 A, -3% regulation accuracy at 25°C</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D\textsubscript{MAX}</td>
<td>Maximum switch duty cycle</td>
<td>I\textsubscript{SW} = 1.85 MHz</td>
<td>87</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RBOOT</th>
<th>\textsubscript{R\textsubscript{RISE}}</th>
<th>SW node rise time</th>
<th>R\textsubscript{BOOT} = 0 Ω, I\textsubscript{OUT} = 2 A (10% to 80%)</th>
<th>2.15</th>
<th>ns</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R\textsubscript{BOOT} = 100 Ω, I\textsubscript{OUT} = 2 A (10% to 80%)</td>
<td>2.7</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) See detailed description for the meaning of this specification and how it can be calculated.
8.8 Typical Characteristics

Unless otherwise specified, $V_{IN} = 13.5\, V$ and $f_{SW} = 2100\, kHz$. 

![Figure 1. Non-Switching Input Supply Current](image1)

![Figure 2. Shutdown Supply Current](image2)

![Figure 3. Feedback Voltage](image3)

![Figure 4. Switching Frequency Set by RT Resistor](image4)

![Figure 5. High-Side and Low-Side Switches $R_{DS\_ON}$](image5)

![Figure 6. Enable Thresholds](image6)
Typical Characteristics (continued)

Unless otherwise specified, $V_{IN} = 13.5$ V and $f_{SW} = 2100$ kHz.

![Figure 7. PGOOD Thresholds](image-url)
9 Detailed Description

9.1 Overview

The LMQ61460-Q1 is a wide input, synchronous peak-current mode buck regulator designed for a wide variety of automotive applications. The regulator can operate over a wide range of switching frequencies including sub-AM band at 400 kHz and above the AM band at 2.1 MHz. This device operates over a wide range of conversion ratios. If minimum on-time or minimum off-time does not support the desired conversion ratio, frequency is reduced automatically, allowing output voltage regulation to be maintained during input voltage transients with a high operating-frequency setting.

The device has been designed for low EMI and is optimized for both above and below AM band operation:

• Meets CISPR25 class 5 standard
• Hotrod™ package minimizes switch node ringing
• Parallel input path minimizes parasitic inductance
• Internal bypass capacitors reduce EMI
• Spread spectrum reduces peak emissions
• Adjustable SW node rise time

These features together can eliminate shielding and other expensive EMI mitigation measures.

This device is designed to minimize end-product cost and size while operating in demanding automotive environments. The LMQ61460-Q1 can be set to operate in the range of 200 kHz through 2.2 MHz using its RT pin. Operation at 2.1 MHz allows for the use of small passive components. State-of-the-art current limit function allows the use of inductors that are optimized for 4-A and 6-A regulators. In addition, this device has low unloaded current consumption, desirable for off-battery, always on applications. The low shutdown current and high maximum operating voltage also allows for the elimination of an external load switch and input transient protection. To further reduce system cost, an advanced PGOOD output is provided, which can often eliminate the use of an external reset or supervisory device.

The LMQ61460-Q1 devices are AEC-Q100-qualified and have electrical characteristics ensured up to a maximum junction temperature of 150°C.
9.2 Functional Block Diagram
9.3 Feature Description

9.3.1 EN/SYNC Uses for Enable and \( V_{IN} \) UVLO

Start-up and shutdown are controlled by the EN/SYNC input and \( V_{IN} \) UVLO. For the device to remain in shutdown mode, apply a voltage below \( V_{EN, WAKE} \) (0.4 V) to the EN pin. In shutdown mode, the quiescent current drops to 0.6 µA (typical). At a voltage above \( V_{EN, WAKE} \) and below \( V_{EN} \), VCC is active and the SW node is inactive. Once the EN voltage is above \( V_{EN} \), the chip begins to switch normally provided the input voltage is above 3 V.

The EN/SYNC pin cannot be left floating. The simplest way to enable the operation is to connect the EN/SYNC pin to \( V_{IN} \), allowing self-start-up of the device when \( V_{IN} \) drives the internal VCC above its UVLO level. However, many applications benefit from the employment of an enable divider network as shown in Figure 8, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, preventing re-triggering the device when used with long input cables, or reducing the occurrence of deep discharge of a battery power source. Note that the precision enable threshold \( V_{EN} \) has a 8.1% tolerance. Hysteresis must be enough to prevent re-triggering. External logic output of another IC can also be used to drive the EN/SYNC pin, allowing system power sequencing.

![Figure 8. VIN UVLO Using the EN pin](image)

Resistor values can be calculated using Equation 1.

\[
R_{ENB} = R_{ENT} \cdot \frac{V_{EN}}{V_{ON} - V_{EN}}
\]

where
- \( V_{ON} \) is the desired typical start-up input voltage for the circuit being designed

Note that since the EN/SYNC pin can also be used as an external synchronization clock input. A blanking time, \( t_{B} \), is applied to the enable logic after a clock edge is detected. Any logic change within the blanking time is ignored. Blanking time is not applied when the device is in shutdown mode. The blanking time ranges from 4 µs to 28 µs. To effectively disable the output, the EN/SYNC input must stay low for longer than 28 µs.

9.3.2 EN/SYNC Pin Uses for Synchronization

The LMQ61460-Q1 EN/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive clock edge into the EN pin, as shown in Figure 9. It is recommended to keep the parallel combination value of \( R_{ENT} \) and \( R_{ENB} \) in the 100-kΩ range. \( R_{ENT} \) is required for synchronization, but \( R_{ENB} \) can be left unmounted. Switching action can be synchronized to an external clock ranging from 200 kHz to 2.2 MHz. The external clock must be off before start-up to allow proper start-up sequencing.
Feature Description (continued)

![Diagram](image)

**Figure 9. Typical Implementation Allowing Synchronization Using the EN Pin**

Referring to Figure 10, the AC-coupled voltage edge at the EN pin must exceed the SYNC amplitude threshold, $V_{EN\_SYNC\_MIN}$, to trip the internal synchronization pulse detector. In addition, the minimum EN/SYNC rising pulse and falling pulse durations must be longer than $t_{SYNC\_EDGE\_MIN}$ and shorter than the blanking time $t_B$. A 3.3-V or higher amplitude pulse signal coupled through a 1-nF capacitor, $C_{SYNC}$, is suggested to use.

![Waveform](image)

**Figure 10. Typical SYNC/EN Waveform**

After a valid synchronization signal is applied for 2048 cycles, the clock frequency abruptly changes to that of the applied signal. Also, if the device in use has the spread-spectrum feature, the valid synchronization signal overrides spread spectrum, turning it off, and the clock switches to the applied clock frequency.

### 9.3.3 Clock Locking

Once a valid synchronization signal is detected, a clock locking procedure is initiated. LMQ61460-Q1 devices receive this signal over the EN/SYNC pin. After approximately 2048 pulses, the clock frequency changes to the frequency of the synchronization signal. Note that while the frequency is adjusted suddenly, phase is maintained so the clock cycle that lies between operation at the default frequency and at the synchronization frequency is of intermediate length. This eliminates very long or very short pulses. Once frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising SW node pulses. See Figure 12.
Feature Description (continued)

Pulses four and synchronization signal is detected. After the pulse, approximately 2048 ready to synchronize and frequency is adjusted using a glitch free technique. Later, phase is locked.

9.3.4 Adjustable Switching Frequency

A resistor tied from the device RT pin to AGND is used to set operating frequency. Use Equation 2 or refer to Figure 13 for resistor values. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, refer to the EN/SYNC Pin Uses for Synchronization section.

\[ R_{RT}(\text{k}\Omega) = \left( \frac{1}{f_{SW}(\text{kHz})} - 3.3 \times 10^{-5} \right) \times 1.346 \times 10^4 \]  

(2)
Feature Description (continued)

9.3.5 PGOOD Output Operation

The PGOOD function is implemented to replace a discrete reset device, reducing BOM count and cost. The PGOOD pin voltage goes low when the feedback voltage is outside of the specified PGOOD thresholds (see Figure 7). This can occur in current limit and thermal shutdown, as well as while disabled and during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions shorter than $t_{PGDFLT(fall)}$ do not trip the power-good flag. Power-good operation can be best understood by referring to Figure 14.

The power-good output consists of an open-drain NMOS, requiring an external pullup resistor to a suitable logic supply or $V_{OUT}$. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is $\geq 1$ V (typical).

![Figure 14. PGOOD Timing Diagram (Excludes OV Events)](image)

Table 1. Conditions That Cause PGOOD to Signal a Fault (Pull Low)

<table>
<thead>
<tr>
<th>FAULT CONDITION INITIATED</th>
<th>FAULT CONDITION ENDS (AFTER WHICH $t_{PGDFLT(fall)}$ MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT} &lt; V_{OUT-target} \times PGD_{UV}$ AND $t &gt; t_{PGDFLT(fall)}$</td>
<td>Output voltage in regulation: $V_{OUT-target} \times (PGD_{UV} + PGD_{HYST}) &lt; V_{OUT} &lt; V_{OUT-target} \times (PGD_{OV} - PGD_{HYST})$ (See Figure 7.)</td>
</tr>
<tr>
<td>$V_{OUT} &gt; V_{OUT-target} \times PGD_{OV}$ AND $t &gt; t_{PGDFLT(fall)}$</td>
<td>Output voltage in regulation</td>
</tr>
<tr>
<td>$T_J &gt; T_{SD_R}$</td>
<td>$T_J &lt; T_{SD_F}$ AND output voltage in regulation</td>
</tr>
<tr>
<td>$EN &lt; EN$ Falling</td>
<td>$EN &gt; EN$ Rising AND output voltage in regulation</td>
</tr>
<tr>
<td>$V_{CC} &lt; V_{CC_UVLO} - V_{CC_UVLO_HYST}$</td>
<td>$V_{CC} &gt; V_{CC_UVLO}$ AND output voltage in regulation</td>
</tr>
</tbody>
</table>

(1) As an additional operational check, PGOOD remains low during soft start, defined as until the lesser of either full output voltage reached or $t_{SS2}$ has passed since initiation.

9.3.6 Internal LDO, VCC UVLO, and BIAS Input

The VCC pin is the output of the internal LDO used to supply the control circuits of the device. The nominal output is 3 V to 3.3 V. The BIAS pin is the input to the internal LDO. This input can be connected to $V_{OUT}$ to provide the lowest possible input supply current. If the BIAS voltage is less than 3.1 V, VIN1 and VIN2 directly powers the internal LDO.

To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See $V_{CC\_UVLO}$ and $V_{CC\_UVLO\_HYST}$ in the Electrical Characteristics. Note that these UVLO values and the dropout of the LDO are used to derive minimum $V_{IN\_OPERATE}$ and $V_{IN\_OPERATE\_H}$ values.
9.3.7 Bootstrap Voltage and $V_{\text{CBOOT-UVLO}}$ (CBOOT Pin)

The driver of the High-Side (HS) switch requires bias higher than $V_{\text{IN}}$. The capacitor, CBOOT, connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT pin to SW+VCC. A boot diode is integrated on the device die to minimize external component count. It is recommended that a 100-nF capacitor rated for 10-V or higher is used. The $V_{\text{BOOT-UVLO}}$ threshold (2.1 V typ) is designed to maintain proper HS switch operation. If the CBOOT capacitor voltage drops below $V_{\text{BOOT-UVLO}}$, then the device initiates a charging sequence turning on the low-side switch before attempting to turn on the HS switch.

9.3.8 Adjustable SW Node Slew Rate

To allow optimization of EMI with respect to efficiency, the device is designed to allow a resistor to select the strength of the driver of the high-side FET during turn on. See Figure 15. The current drawn through the RBOOT pin (the dotted loop) is magnified and drawn through from CBOOT (the dashed line). This current is used to turn on the high-side power MOSEFT.

![Figure 15. Simplified Circuit Showing How RBOOT Functions](image)

With RBOOT short circuited to CBOOT, rise time is very fast. As a result SW node harmonics do not "roll off" until above 150 MHz. A boot resistor of 100 Ω corresponds to approximately 2.7 ns SW node rise, and this 100-Ω boot resistor virtually eliminates SW node overshoot. The slower rise time allows energy in SW node harmonics to roll off near 100 MHz under most conditions. Rolling off harmonics eliminates the need for shielding and common mode chokes in many applications. Note that rise time increases with increasing input voltage. Noise due to stored charge is also greatly reduced with higher RBOOT resistance. Switching with slower slew rate also decreases the efficiency.

9.3.9 Spread Spectrum

Spread spectrum is pin-controlled. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than a part with fixed frequency operation. In most systems containing the chip, low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The device uses a ±2% spread of frequencies which can spread energy smoothly across the FM and TV bands but is small enough to limit subharmonic emissions below the device switching frequency. Peak emissions at the switching frequency of the part are only reduced slightly, by less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The device uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats at less than 1.5 Hz, which is below the audio band.
The spread spectrum is only available while the clock of the device is free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed during dropout.
- The clock is slowed at light load in auto mode. In FPWM mode, spread spectrum is active even if there is no load.
- At high input voltage/low output voltage ratio when the device operates at minimum on time the internal clock is slowed disabling spread spectrum. See the Timing Characteristics.
- The clock is synchronized with an external clock.

### 9.3.10 Soft Start and Recovery From Dropout

The device uses a reference-based soft start that prevents output voltage overshoots and large inrush currents during start-up. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the IC, releasing UVLO.
- EN is used to turn on the device.
- Recovery from a hiccup waiting period.
- Recovery from shutdown due to overtemperature protection.

Once soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped. The net result is that output voltage takes t\(_{\text{SS}}\) to reach 90% of its desired value.
- Operating mode is set to auto, activating diode emulation. This allows start-up without pulling output low if there is a voltage already present on output.

Together, these actions provide start-up with limited inrush currents and also allow the use of larger output capacitors and higher loading conditions that cause current to border on current limit during start-up without triggering hiccup. See Figure 16.

**Figure 16. Soft-Start Operation**

Any time the output voltage falls more than a few percent, the output voltage will ramp up slowly. This condition is called recovery from dropout and differs from soft start in three important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- Hiccup is allowed if output voltage is less than 0.4 times its set point. Note that during dropout regulation itself, hiccup is inhibited.
- FPWM mode is allowed during recovery from dropout. If the output voltage were to suddenly be pulled up by an external supply, the device can pull down on the output.
Despite being called recovery from dropout, this feature is active whenever output voltage drops to a few percent lower than the set point. This primarily occurs under the following conditions:

- **Dropout**: When there is insufficient input voltage for the desired output voltage to be generated
- **Overcurrent**: When there is an overcurrent event that is not severe enough to trigger hiccup

Whether output voltage falls due to high load or low input voltage, once the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, it can in principle be triggered during recovery if output voltage is below 0.4 times the output set point for more than 128 clock cycles.

**Figure 17. Recovery From Dropout**

**Figure 18. Recovery From Dropout (V_{OUT} = 5 \, V, I_{OUT} = 4 \, A, V_{IN} = 13.5 \, V \text{ to } 4 \, V \text{ to } 13.5 \, V)**

### 9.3.11 Output Voltage Setting

If the LMQ61460-Q1 has fixed 5-V or fixed 3.3-V output, simply connect FB to the output. See the *Application Information* section for layout information.

For versions of the LMQ61460-Q1 with adjustable output voltage, a feedback resistor divider network between the output voltage and the FB pin is used to set output voltage level. See *Figure 19*.
Figure 19. Setting Output Voltage of Adjustable Versions

The device uses a 1-V reference voltage for the feedback (FB) pin. The FB pin voltage is regulated by the internal controller to be the same as the reference voltage. The output voltage level is then set by the ratio of the resistor divider. Equation 3 can be used to determine $R_{FBB}$ for a desired output voltage and a given $R_{FBT}$. Usually $R_{FBT}$ is between 10 kΩ and 1 MΩ. 100 kΩ is recommended for $R_{FBT}$ for improved noise immunity compared to 1 MΩ and reduced current consumption compared to lower resistance values.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1}$$

(3)

In addition, a feedforward capacitor, $C_{FF}$, connected in parallel with $R_{FBT}$ can be required to optimize the transient response.

9.3.12 Overcurrent and Short Circuit Protection

The device is protected from overcurrent conditions with cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. Every switching cycle, the HS switch current is compared to either the minimum of a fixed current set point or the output of the voltage regulation loop minus slope compensation. Because the voltage loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty cycle when duty cycle is above 35%. See Figure 20.

Figure 20. Maximum Current Allowed Through the HS FET - Function of Duty Cycle for LMQ61460-Q1
When the LS switch is turned on, the switch current is also sensed and monitored. Like the high-side device, the low-side device turns off as commanded by the voltage control loop, low-side current limit. If the LS switch current is higher than $I_{LS\_Limit}$ at the end of a switching cycle, the switching cycle is extended until the LS current reduces below the limit. The LS switch is turned off once the LS current falls below its limit, and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

Figure 21. Current Limit Waveforms

Since the current waveform assumes values between $I_{L\_HS}$ and $I_{L\_LS}$, the maximum output current is very close to the average of these two values. Hysteric control is used and current does not increase as output voltage approaches zero.

The device employs hiccup overcurrent protection if there is an extreme overload, and the following conditions are met for 128 consecutive switching cycles:

- Output voltage is below approximately 0.4 times the output voltage set point.
- Greater than $t_{SS2}$ has passed since soft start has started; see the Soft Start and Recovery From Dropout section.
- The part is not operating in dropout, which is defined as having minimum off-time controlled duty cycle.

In hiccup mode, the device shuts itself down and attempts to soft start after $t_W$. Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits. See Figure 22.

Once the overload is removed, the device recovers as though in soft start; see Figure 23.
9.3.13 Thermal Shutdown

Thermal shutdown prevents the device from extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 165°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 155°C. When the junction temperature falls below 155°C (typical), the device attempts to soft start.

While the device is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The VCC current limit is reduced to a few milliamperes during thermal shutdown.

9.3.14 Input Supply Current

The device is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input pin to the output of the regulator, a small amount of current drawn from the output. This current is reduced at the input by the ratio of $V_{OUT}$ / $V_{IN}$.

$$I_{Q\_VIN} = I_Q + I_{EN} + (I_{BIAS} + I_{DIV}) \frac{Output\ Voltage}{\eta_{eff} \times Input\ Voltage}$$

where

- $I_{Q\_VIN}$ is the current consumed by the operating (switching) buck converter while unloaded.
- $I_Q$ is the current drawn from the $V_{IN}$ terminal. See $I_Q$ in the Electrical Characteristics.
- $I_{EN}$ is current drawn by the EN terminal. Include this current if EN is connected to VIN. See $I_{EN}$ in the Electrical Characteristics. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- $I_{BIAS}$ is bias current drawn by the BIAS input. See $I_{BIAS}$ in the Electrical Characteristics.
- $I_{DIV}$ is the current drawn by the feedback voltage divider used to set output voltage.
- $\eta_{eff}$ is the light load efficiency of the buck converter with $I_{Q\_VIN}$ removed from the input current of the buck converter. $\eta_{eff} = 0.8$ is a conservative value that can be used under normal operating conditions. (4)

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4 V, both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.6 µA.

9.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1.1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The precision enable circuitry is ON once VCC is above its UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The device also employs UVLO protection. If the VCC voltage is below its UVLO level, the output of the converter is turned off.

9.4.3 Active Mode

The device is in active mode whenever the EN pin is above $V_{EN}$, $V_{IN}$ is high enough to satisfy $V_{IN\_OPERATE}$, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to $V_{IN}$ which allows self start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the device is in one of six modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the inductor current ripple.
- Auto Mode - Light Load Operation: PFM when switching frequency is decreased at very light load.
- FPWM Mode - Light Load Operation: Discontinuous conduction mode (DCM) when the load current is lower
Device Functional Modes (continued)

- Minimum on-time: At high input voltage, low output voltages the switching frequency is reduced to maintain regulation.
- Dropout mode: When switching frequency is reduced to minimize voltage drop out.

9.4.3.1 CCM Mode

The following operating description of the device refers to the Functional Block Diagram and to the waveforms in Figure 24. In CCM, the device supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, $V_{SW}$, swings up to approximately $V_{IN}$, and the inductor current, $i_L$, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, $t_{OFF}$, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the $V_{SW}$ to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period:

$$D = \frac{T_{ON}}{T_{SW}}$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = \frac{V_{OUT}}{V_{IN}}$$

![Figure 24. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)](image)

9.4.3.2 Auto Mode - Light Load Operation

The device can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM Mode, maintains full frequency even when unloaded. Which mode the device operates in depends on which factory option is employed, see the Device Comparison Table. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

In auto mode, light load operation is employed in the device at load lower than approximately a tenth of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, they operate independently of each other.
Device Functional Modes (continued)

9.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current though the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.

\[
D = \frac{I_{ON}}{I_{SW}} < \frac{V_{OUT}}{V_{IN}}
\]

\[
I_{LPK} \quad I_{OUT}
\]

In auto mode, the low-side device is turned off once SW node current is near zero. As a result, once output current is less than half of what inductor ripple would be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

**Figure 25. PFM Operation**

The device has a minimum peak inductor current setting while in auto mode. Once current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

9.4.3.2.2 Frequency Reduction

The device reduces frequency whenever output voltage is high. This function is enabled whenever Comp, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.

**Figure 26. Steady State Output Voltage versus Output Current in Auto Mode**

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on \( V_{OUT} \). If the DC offset on \( V_{OUT} \) is not acceptable, a dummy load at \( V_{OUT} \) or FPWM Mode can be used to reduce or eliminate this offset.
Device Functional Modes (continued)

9.4.3.3 FPWM Mode - Light Load Operation

Like auto mode operation, FPWM mode operation during light load operation is selected as a factory option. In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see the Electrical Characteristics for reverse current limit values.

\[ D = \frac{t_{ON}}{t_{SW}} = \frac{V_{OUT}}{V_{IN}} \]

In FPWM mode, Continuous Conduction (CCM) is possible even if \( I_{OUT} \) is less than half of \( I_{ripple} \).

![Figure 27. FPWM Mode Operation](image)

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

9.4.3.4 Minimum On-time (High Input Voltage) Operation

The device continues to regulate output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. Once a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on-time is fixed at its minimum value, this type of operation resembles that of a device using a COT control scheme; see Figure 28.
Device Functional Modes (continued)

9.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off-time. Once this limit is reached, if clock frequency were maintained, output voltage would fall. Instead of allowing the output voltage to drop, the device extends on-time past the end of the clock cycle until needed peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, $t_{ON \_MAX}$, of approximately 9 µs passes. As a result, once the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough so that output voltage cannot be regulated even with an on-time of $t_{ON \_MAX}$, output voltage drops to slightly below input voltage, $V_{DROP1}$. For additional information on recovery from dropout, reference Figure 17.

Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

Figure 29. Frequency and Output Voltage in Dropout
Device Functional Modes (continued)

Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by $t_{\text{ON}_{\text{MAX}}}$.

**Figure 30. Dropout Waveforms**
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
The LMQ61460-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 6 A. Using a 4-layer LMQ61460EVM, at 400 kHz, the device can sustain a continuous 6 A load up to an ambient temperature of approximately 95°C; see Figure 32. The following design procedure can be used to select components for the LMQ61460-Q1.

10.2 Typical Application
Figure 31 shows a typical application circuit for the device. This device is designed to function with a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, Table 3 provides typical component values for some of the common configurations.

Figure 31. Example Application Circuit

10.2.1 Design Requirements
Table 2 provides the parameters for our detailed design procedure example:

Table 2. Detailed Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>13.5 V (5 V to 36 V)</td>
</tr>
<tr>
<td>Input voltage for constant fSW</td>
<td>8 V to 18 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>0 A to 6 A</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>400 kHz</td>
</tr>
</tbody>
</table>
### 10.2.2 Detailed Design Procedure

The following design procedure applies to Figure 31 and Table 2.

#### 10.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows for the use of smaller inductors and output capacitors, hence, a more compact design.

When choosing operating frequency, the most important consideration is thermal limitations. This constraint typically dominates frequency selection. See Figure 32 for circuits running at 400 kHz and Figure 33 for circuits running at 2.1 MHz. These curves show how much output current can be supported at a given ambient temperature given these switching frequencies. Note that power dissipation is layout dependent so while these curves are a good starting point, thermal resistance in any design will be different from the estimates used to generate Figure 32 and Figure 33. The maximum temperature ratings are based on the LMQ61460EVM, which is approximately 100 mm x 80 mm in board area. Unless a larger copper area or cooling is provided to reduce the effective $R_{\theta JA}$, if ambient temperature is 105°C and the switching frequency is set to 2.1 MHz, the load current should typically be limited to 4 A.

![Figure 32. Maximum Ambient Temperature versus Output Current](image)

![Figure 33. Maximum Ambient Temperature versus Output Current](image)

Two other considerations are what maximum and minimum input voltage the part must maintain for the frequency setting. Since the device adjusts its frequency under conditions in which regulation would normally be prevented by minimum on-time or minimum off-time, these constraints are only important for input voltages requiring constant frequency operation.

If foldback is undesirable at high input voltage, use Equation 7:

$$f_{SW} \leq \frac{V_{OUT}}{V_{IN} (MAX2) \cdot t_{ON\_MIN} (MAX)}$$  \hspace{1cm} (7)

If foldback at low input voltage is a concern, use Equation 8:

$$f_{SW} \leq \frac{V_{OUT}}{V_{IN} (MIN2)}$$
The saturation current rating of the inductor must be at least as large as the high-side switch current limit, $I_{L-HS}$ (see the Electrical Characteristics). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{L-LS}$, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1 MHz. In any case, the inductor saturation current must not be less than the device high-side current limit, $I_{L-HS}$ (see the Electrical Characteristics). To avoid subharmonic oscillation, the inductance value must not be less than that given in Equation 10. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \cdot K \cdot I_{OUT}(MAX)} \cdot \frac{V_{OUT}}{V_{IN}}$$  

(9)
\[ L \geq 0.32 \cdot \frac{V_{OUT}}{f_{SW}} \]  

Equation 10 assumes that this design must operate with input voltage near or in dropout. If minimum operating voltage for this design is high enough to limit duty factor to below 50%, Equation 11 can be used in place of Equation 10.

\[ L \geq 0.2 \cdot \frac{V_{OUT}}{f_{SW}} \]  

Note that choosing an inductor that is larger than the minimum inductance calculated using Equation 9 through Equation 11 results in less output capacitance being needed to limit output ripple but more output capacitance being needed to manage large load transients. See the Output Capacitor Selection section.

### 10.2.2.4 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor is usually determined by the load transient requirements rather than the output voltage ripple. Table 4 can be used to find the output capacitor and \( C_{FF} \) selection for a few common applications. Note that a 1-k\( \Omega \) \( R_{FF} \) must be used in series with \( C_{FF} \). In this example, improved transient performance is desired giving 2 x 47 \( \mu \F \) ceramic as the output capacitor and 22 pF as \( C_{FF} \).

<table>
<thead>
<tr>
<th>FREQUENCY</th>
<th>TRANSIENT PERFORMANCE</th>
<th>3.3-V OUTPUT</th>
<th>5-V OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 MHz</td>
<td>Minimum</td>
<td>3 x 22 ( \mu \F )</td>
<td>2 x 22 ( \mu \F )</td>
</tr>
<tr>
<td>2.1 MHz</td>
<td>Better Transient</td>
<td>2 x 47 ( \mu \F )</td>
<td>3 x 22 ( \mu \F )</td>
</tr>
<tr>
<td>400 kHz</td>
<td>Minimum</td>
<td>3 x 47 ( \mu \F )</td>
<td>2 x 47 ( \mu \F )</td>
</tr>
<tr>
<td>400 kHz</td>
<td>Better Transient</td>
<td>4 x 47 ( \mu \F )</td>
<td>3 x 47 ( \mu \F )</td>
</tr>
</tbody>
</table>

To minimize ceramic capacitance, a low-ESR electrolytic capacitor can be used in parallel with minimal ceramic capacitance. As a starting point for designing with an output electrolytic capacitor, Table 5 shows the recommended output ceramic capacitance \( C_{FF} \) values when using an electrolytic capacitor.

<table>
<thead>
<tr>
<th>FREQUENCY</th>
<th>TRANSIENT PERFORMANCE</th>
<th>3.3-V OUTPUT</th>
<th>5-V OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 kHz</td>
<td>Minimum</td>
<td>2 x 47 ( \mu \F ) ceramic + 1 x 470 ( \mu \F ), 100 m( \Omega ) electrolytic</td>
<td>3 x 22 ( \mu \F ) ceramic + 1 x 470 ( \mu \F ), 100 m( \Omega ) electrolytic</td>
</tr>
<tr>
<td>400 kHz</td>
<td>Better Transient</td>
<td>3 x 47 ( \mu \F ) ceramic + 2 x 280 ( \mu \F ), 100 m( \Omega ) electrolytic</td>
<td>4 x 22 ( \mu \F ) ceramic + 1 x 560 ( \mu \F ), 100 m( \Omega ) electrolytic</td>
</tr>
</tbody>
</table>

Most ceramic capacitors deliver far less capacitance than the capacitor’s rating indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating and voltage derating. Table 4 and Table 5 have been generated assuming typical derating for 16 V, X7R Automotive grade capacitors. If lower voltage, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed will likely be needed.

### 10.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 \( \mu \F \) of ceramic capacitance is required on the input of the device. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at each input/ground pin pair, VIN1/PGND1 and VIN2/PGND2, immediately adjacent to the converter. This provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and
EMI. The two 100 nF must also be rated at 50 V with an X7R or better dielectric. The VQFN-HR (RJR) package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, two 4.7-μF and two 100-nF ceramic capacitors are used, one at each VIN/PGND location. A single 10-μF can also be used on one side of the package.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the converter. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated from Equation 12 and must be checked against the manufacturers’ maximum ratings.

\[ I_{\text{RMS}} \approx \frac{I_{\text{OUT}}}{2} \]  

(12)

10.2.2.6 BOOT Capacitor

The device requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100 nF and at least 10 V is required.

10.2.2.7 BOOT Resistor

A BOOT resistor can be connected between the CBOOT and RBOOT pins. Unless EMI for the application being designed is critical, these two pins can be shorted. A 100 Ω resistor between these pins eliminates overshoot. Even with 0 Ω, overshoot and ringing are minimal, less than 2 V if input capacitors are placed correctly. A boot resistor of 100 Ω, which corresponds to approximately 2.7 ns SW node rise time and decreases efficiency by approximately 0.5% at 2 MHz. To maximize efficiency, 0 Ω is chosen for this example. Under most circumstances, selecting an RBOOT resistor value above 100 Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

10.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 1-μF, 16-V ceramic capacitor connected from VCC to AGND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see the PGOOD Output Operation section). A pullup resistor with a value of 100 kΩ is a good choice in this case. Note, VCC will remain high when V_{\text{EN_WAKE}} < EN < V_{\text{EN}}. The nominal output voltage on VCC is 3.3 V. Do not short this output to ground or any other external voltage.

10.2.2.9 BIAS

Because \( V_{\text{OUT}} = 5 \) V in this design, the BIAS pin is tied to \( V_{\text{OUT}} \) to reduce LDO power loss. The output voltage is supplying the LDO current instead of the input voltage. The power saving is \( I_{\text{LDO}} \times (V_{\text{IN}} - V_{\text{OUT}}) \). The power saving is more significant when \( V_{\text{IN}} >> V_{\text{OUT}} \) and with higher frequency operation. To prevent \( V_{\text{OUT}} \) noise and transients from coupling to BIAS, a series resistor, 1 Ω to 10 Ω, can be added between \( V_{\text{OUT}} \) and BIAS. A bypass capacitor with a value of 1 μF or higher can be added close to the BIAS pin to filter noise. Note, the maximum allowed voltage on the BIAS pin is 16 V.

10.2.2.10 \( C_{\text{FF}} \) and \( R_{\text{FF}} \) Selection

A feedforward capacitor, \( C_{\text{ff}} \), is used to improve phase margin and transient response of circuits which have output capacitors with low ESR. Since this capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 1-kΩ resistor, \( R_{\text{ff}} \), must be placed in series with \( C_{\text{ff}} \). If the ESR zero of the output capacitor is below 200 kHz, no \( C_{\text{ff}} \) should be used.

If output voltage is less than 2.5 V, \( C_{\text{ff}} \) has little effect so can be omitted. If output voltage is greater than 14 V, \( C_{\text{ff}} \) must not be used since it will introduce too much gain at higher frequencies.
10.2.2.11 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in Figure 34. The input voltage at which the device turns on is designated $V_{ON}$ while the turnoff voltage is $V_{OFF}$. First, a value for $R_{ENB}$ is chosen in the range of 10 kΩ to 100 kΩ, then Equation 14 is used to calculate $R_{ENT}$ and $V_{OFF}$. $R_{ENB}$ is typically set based on how much current this voltage divider must consume. $R_{ENB}$ can be calculated using Equation 13.

$$R_{ENB} = \frac{V_{EN} \cdot V_{IN}}{I_{DIVIDER} \cdot V_{ON}}$$

(13)

$$R_{ENT} = \left( \frac{V_{ON}}{V_{EN}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot (1 - V_{EN-HYST})$$

(14)

where

- $V_{ON} = V_{IN}$ turnon voltage
- $V_{OFF} = V_{IN}$ turnoff voltage
- $I_{DIVIDER} =$ voltage divider current

![Figure 34. UVLO Using EN](image)
10.2.3 Application Curves

Unless otherwise specified, the following conditions apply: $V_{IN} = 13.5\, \text{V}$, $T_A = 25\, ^\circ\text{C}$. The circuit is shown in Figure 31, with the appropriate BOM from Table 6.
Output Current (A)
Output Voltage (V)
0 1 2 3 4 5 6 7
3.29 3.31 3.33 3.35 3.37
SNVS
VIN = 8 V
VIN = 13.5 V
VIN = 24 V

Load Current (A)
Efficiency (%)
0.001 0.01 0.02 0.05 0.1 0.2 0.5 1 2 3 4 5 7 10
60% 65% 70% 75% 80% 85% 90% 95% 100%
LM61
VIN = 8 V
VIN = 13.5 V
VIN = 24 V

Figure 41. Efficiency
Figure 42. Efficiency
Figure 43. Load and Line Regulation
Figure 44. Load and Line Regulation
Figure 45. Load and Line Regulation
Figure 46. Load and Line Regulation

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Product Folder Links: LMQ61460-Q1
### Input Voltage (V) vs. Switching Frequency (Hz)
<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>5.25</td>
<td>5.5</td>
</tr>
<tr>
<td>5.5</td>
<td>5.75</td>
</tr>
<tr>
<td>5.75</td>
<td>6</td>
</tr>
</tbody>
</table>

### SNVS
- **I\text{OUT} = 0.01 A**
- **I\text{OUT} = 3 A**
- **I\text{OUT} = 6 A**

#### Figures
- **Figure 53. Dropout Curve**
- **Figure 54. Dropout Curve**
- **Figure 55. Frequency Dropout**
- **Figure 56. Frequency Dropout Curve**
- **Figure 57. Frequency Dropout Curve**
- **Figure 58. Frequency Dropout Curve**
$V_{OUT} = 5 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} AUTO Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 50 \text{ mA}

Figure 59. Switching Waveform and $V_{OUT}$ Ripple

$V_{OUT} = 5 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} FPWM Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 50 \text{ mA}

Figure 60. Switching Waveform and $V_{OUT}$ Ripple

$V_{OUT} = 5 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} AUTO Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 50 \text{ mA}

Figure 61. Start-up with 50-mA Load

$V_{OUT} = 5 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} AUTO Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 50 \text{ mA}

Figure 62. Start-up with 50-mA Load

$V_{OUT} = 3.3 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} FPWM Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 3.25 \text{ A}

Figure 63. Start-up with 3.25-A

$V_{OUT} = 5 \text{ V}$  \hspace{1cm} F_{SW} = 2100 \text{ kHz}  \hspace{1cm} FPWM Mode

$V_{IN} = 13.5 \text{ V}$  \hspace{1cm} I_{OUT} = 5 \text{ A to Short Circuit}

Figure 64. Short Circuit Protection
Figure 65. Short Circuit Recovery

V_{OUT} = 5 V  \quad F_{SW} = 2100 kHz  \quad FPWM Mode
I_{OUT} = Short Circuit to 5 A  \quad V_{IN} = 13.5 V

Figure 66. Short Circuit Performance

V_{OUT} = 5 V  \quad F_{SW} = 2100 kHz  \quad FPWM Mode
I_{OUT} = Short Circuit  \quad V_{IN} = 13.5 V

Figure 67. Graceful Recovery from Dropout

V_{OUT} = 5 V  \quad F_{SW} = 2100 kHz  \quad FPWM Mode
I_{OUT} = 4 A  \quad V_{IN} = 13.5 V to 4 V to 13.5 V

Figure 68. Load Transient

V_{OUT} = 5 V  \quad F_{SW} = 400 kHz  \quad AUTO Mode
I_{OUT} = 0 A to 6 A to 0 A  \quad V_{IN} = 13.5 V  \quad T_{R} = T_{F} = 6 \mu s

Figure 69. Load Transient

V_{OUT} = 5 V  \quad F_{SW} = 400 kHz  \quad FPWM Mode
I_{OUT} = 0 A to 6 A to 0 A  \quad V_{IN} = 13.5 V  \quad T_{R} = T_{F} = 6 \mu s

Figure 70. Load Transient

V_{OUT} = 5 V  \quad F_{SW} = 400 kHz  \quad AUTO Mode
I_{OUT} = 2 A to 5 A to 2 A  \quad V_{IN} = 13.5 V  \quad T_{R} = T_{F} = 3 \mu s
**Figure 71. Load Transient**

- $V_{\text{OUT}} = 5\, \text{V}$
- $I_{\text{OUT}} = 50\, \text{mA}$ to $6\, \text{A}$ to $50\, \text{mA}$
- $F_{\text{SW}} = 400\, \text{kHz}$
- $V_{\text{IN}} = 13.5\, \text{V}$
- $T_R = T_F = 6\, \mu\text{s}$

**Figure 72. Load Transient**

- $V_{\text{OUT}} = 3.3\, \text{V}$
- $I_{\text{OUT}} = 0\, \text{A}$ to $6\, \text{A}$ to $0\, \text{A}$
- $F_{\text{SW}} = 400\, \text{kHz}$
- $V_{\text{IN}} = 13.5\, \text{V}$
- $T_R = T_F = 6\, \mu\text{s}$

**Figure 73. Load Transient**

- $V_{\text{OUT}} = 3.3\, \text{V}$
- $I_{\text{OUT}} = 2\, \text{A}$ to $4\, \text{A}$ to $2\, \text{A}$
- $F_{\text{SW}} = 400\, \text{kHz}$
- $V_{\text{IN}} = 13.5\, \text{V}$
- $T_R = T_F = 2\, \mu\text{s}$

**Figure 74. Load Transient**

- $V_{\text{OUT}} = 5\, \text{V}$
- $I_{\text{OUT}} = 0\, \text{A}$ to $6\, \text{A}$ to $0\, \text{A}$
- $F_{\text{SW}} = 2100\, \text{kHz}$
- $V_{\text{IN}} = 13.5\, \text{V}$
- $T_R = T_F = 6\, \mu\text{s}$

**Figure 75. Load Transient**

- $V_{\text{OUT}} = 5\, \text{V}$
- $I_{\text{OUT}} = 0\, \text{A}$ to $6\, \text{A}$ to $0\, \text{A}$
- $F_{\text{SW}} = 2100\, \text{kHz}$
- $V_{\text{IN}} = 13.5\, \text{V}$
- $T_R = T_F = 6\, \mu\text{s}$
- $F_{\text{SW}} = 400\, \text{kHz}$
- $V_{\text{OUT}} = 5\, \text{V}$
- $I_{\text{OUT}} = 5\, \text{A}$
- Frequency Tested: 150 kHz to 30 MHz

**Figure 76. Conducted EMI versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)**
$V_{OUT} = 5 \text{ V} \quad F_{SW} = 400 \text{ kHz} \quad I_{OUT} = 5 \text{ A}$
Frequency Tested: 30 MHz to 108 MHz

Figure 77. Conducted EMI versus CISPR25 Limits (Yellow: Peak Signal, Blue: Average Signal)

$V_{OUT} = 5 \text{ V} \quad F_{SW} = 400 \text{ kHz} \quad I_{OUT} = 5 \text{ A}$
Frequency Tested: 150 kHz to 30 MHz

Figure 78. Radiated EMI Rod versus CISPR25 Limits

$V_{OUT} = 5 \text{ V} \quad F_{SW} = 400 \text{ kHz} \quad I_{OUT} = 5 \text{ A}$
Frequency Tested: 30 MHz to 300 MHz

Figure 79. Radiated EMI Bicon Vertical versus CISPR25 Limits

$V_{OUT} = 5 \text{ V} \quad F_{SW} = 400 \text{ kHz} \quad I_{OUT} = 5 \text{ A}$
Frequency Tested: 300 MHz to 1 GHz

Figure 81. Radiated EMI Log Vertical versus CISPR25 Limits

$V_{OUT} = 5 \text{ V} \quad F_{SW} = 400 \text{ kHz} \quad I_{OUT} = 5 \text{ A}$
Frequency Tested: 300 MHz to 1 GHz

Figure 82. Radiated EMI Log Horizontal versus CISPR25 Limits
Table 6. BOM for Typical Application Curves

<table>
<thead>
<tr>
<th>V_{OUT}</th>
<th>FREQUENCY</th>
<th>R_{FB}</th>
<th>R_{T}</th>
<th>C_{OUT}</th>
<th>C_{IN} + C_{HF}</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td>400 kHz</td>
<td>43.2 kΩ</td>
<td>33.2 kΩ</td>
<td>6 x 22 µF</td>
<td>2 x 4.7 µF + 2 x 100 nF</td>
<td>4.7 µH (XHMI6060)</td>
</tr>
<tr>
<td>3.3 V</td>
<td>2100 kHz</td>
<td>43.2 kΩ</td>
<td>6.04 kΩ</td>
<td>3 x 22 µF</td>
<td>2 x 4.7 µF + 2 x 100 nF</td>
<td>1 µH (XEL5030)</td>
</tr>
<tr>
<td>5 V</td>
<td>400 kHz</td>
<td>24.9 kΩ</td>
<td>33.2 kΩ</td>
<td>4 x 22 µF</td>
<td>2 x 4.7 µF + 2 x 100 nF</td>
<td>4.7 µH (XHMI6060)</td>
</tr>
<tr>
<td>5 V</td>
<td>2100 kHz</td>
<td>24.9 kΩ</td>
<td>6.04 kΩ</td>
<td>3 x 22 µF</td>
<td>2 x 4.7 µF + 2 x 100 nF</td>
<td>1 µH (XEL5030)</td>
</tr>
</tbody>
</table>
11 Power Supply Recommendations

The characteristics of the input supply must be compatible with the Absolute Maximum Ratings and Recommended Operating Conditions in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. The average input current can be estimated with Equation 15.

\[ I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \]

where

- \( \eta \) is the efficiency

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter or tripping UVLO. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the converter to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the converter and use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A value in the range of 20 \( \mu \)F to 100 \( \mu \)F is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of converters. One class of this device has a snap-back characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the converter, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the TVS and cause large input transients.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.
12 Layout

12.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 87. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 88 shows a recommended layout for the critical components for the circuit of the device.

- **Place the input capacitor or capacitors as close as possible input pin pairs**: VIN1 to PGND1 and VIN2 to PGND2. Each pair of pins are adjacent, simplifying the input capacitor placement. With the VQFN-HR package, there are two VIN/PGND pairs on either side of the package. This provides for a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a lower layer to connect both of the VIN pairs together to the input supply.

- **Place bypass capacitor for VCC close to the VCC pin and AGND pins**: This capacitor must routed with short, wide traces to the VCC and AGND pins.

- **Use wide traces for the CBOOT capacitor**: Place the CBOOT capacitor as close to the device with short, wide traces to the CBOOT and SW pins. It is important to route the SW connection under the device through the gap between VIN2 and RBOOT pins, reducing exposed SW node area. If an RBOOT resistor is used, place as close as possible to CBOOT and RBOOT pins. If high efficiency is desired, RBOOT and CBOOT pins can be shorted. This short must be placed as close as possible to RBOOT and CBOOT pins as possible.

- **Place the feedback divider as close as possible to the FB pin of the device**: Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and AGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the converter.

- **Layer 2 of the PCB must be a ground plane**: This plane acts as a noise shield and a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.

- **Provide wide paths for V_{IN}, V_{OUT}, and GND**: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter and maximizes efficiency.

- **Provide enough PCB area for proper heat sinking**: Enough copper area must be used to ensure a low R_{thJA}, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces must be used for all pins except where noise considerations dictate minimization of area.

- **Keep switch area small**: Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.
Layout Guidelines (continued)

![Figure 87. Input Current Loop](image)

12.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using vias near ground and $V\text{IN}$ to connect to the system ground plane or $V\text{IN}$ strap, both of which dissipate heat. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.
12.2 Layout Example

![Layout Example Diagram](image_url)

**Figure 88. Layout Example**
13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation
For related documentation see the following:

- Texas Instruments, Designing High Performance, Low-EMI, Automotive Power Supplies Application Report
- Texas Instruments, LMQ61460-Q1 EVM User’s Guide
- Texas Instruments, 30 W Power for Automotive Dual USB Type-C Charge Port Reference Design
- Texas Instruments, EMI Filter Components and Their Nonidealities for Automotive DC/DC Regulators Technical Brief
- Texas Instruments, AN-2020 Thermal Design by Insight, Not Hindsight Application Report
- Texas Instruments, Optimizing the Layout for the TPS54424/TPS54824 HotRod QFN Package for Thermal Performance Application Report
- Texas Instruments, AN-2162 Simple Success With Conducted EMI From DC-DC Converters Application Report
- Texas Instruments, Practical Thermal Design With DC/DC Power Modules Application Report

13.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

Hotrod, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMQ61460AASQRJRTQ1</td>
<td>ACTIVE</td>
<td>VQFN-HR</td>
<td>RJR</td>
<td>14</td>
<td>250</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 150</td>
<td>Samples</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.
NOTES: (continued)

3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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