FEATURES

• Input Voltage Range of 2.7V to 14V
• Output Voltage up to 20V
• Switch Current up to 1.4A
• 1.6 MHz Switching Frequency
• Low Shutdown Iq, <1 µA
• Cycle-by-Cycle Current Limiting
• Internally Compensated
• 5-Pin SOT-23 Packaging (2.92 x 2.84 x 1.08mm)
• Fully Enabled for WEBENCH® Power Designer

DESCRIPTION

The LMR62014 switching regulator is a current-mode boost converter operating at fixed frequency of 1.6 MHz.

The use of SOT-23 package, made possible by the minimal power loss of the internal 1.4A switch, and use of small inductors and capacitors result in the industry's highest power density. The LMR62014 is capable of greater than 90% duty cycle, making it ideal for boosting to voltages up to 20V.

These parts have a logic-level shutdown pin that can be used to reduce quiescent current and extend battery life.

Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies design and reduces component count.

PERFORMANCE BENEFITS

• Extremely Easy to Use
• Tiny Overall Solution Reduces System Cost

APPLICATIONS

• Boost Conversions from 3.3V, 5V, and 12V Rails
• Space Constrained Applications
• Embedded Systems
• LCD Displays
• LED Applications

System Performance

![Efficiency vs Load Current](image1)

![Efficiency vs Load Current](image2)
Connection Diagram

PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW</td>
<td>Drain of the internal FET switch.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Analog and power ground.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Feedback point that connects to external resistive divider.</td>
</tr>
<tr>
<td>4</td>
<td>SHDN</td>
<td>Shutdown control input. Connect to Vin if the feature is not used.</td>
</tr>
<tr>
<td>5</td>
<td>V_IN</td>
<td>Analog and power input.</td>
</tr>
</tbody>
</table>
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Lead Temp. (Soldering, 5 sec.)</td>
<td>300°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Internally Limited</td>
</tr>
<tr>
<td>FB Pin Voltage</td>
<td>−0.4V to +6V</td>
</tr>
<tr>
<td>SW Pin Voltage</td>
<td>−0.4V to +22V</td>
</tr>
<tr>
<td>Input Supply Voltage</td>
<td>−0.4V to VIN + 0.3V</td>
</tr>
<tr>
<td>SHDN Pin Voltage</td>
<td>−0.4V to VIN + 0.3V</td>
</tr>
<tr>
<td>θ_J-A (SOT-23)</td>
<td>265°C/W</td>
</tr>
<tr>
<td>ESD Rating Human Body Model</td>
<td>2 kV</td>
</tr>
</tbody>
</table>

For soldering specifications see SNOA549

1. Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of the limits set forth under the operating ratings which specify the intended range of operating conditions.
2. If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
3. The maximum power dissipation which can be safely dissipated for any application is a function of the maximum junction temperature, T_J (MAX) = 125°C, the junction-to-ambient thermal resistance for the SOT-23 package, θ_J-A = 265°C/W, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature for designs using this device can be calculated using the formula: P (MAX) = T_J (MAX) - T_A / θ_J-A = 125 - T_A / 265. If power dissipation exceeds the maximum specified above, the internal thermal protection circuitry will protect the device by reducing the output voltage as required to maintain a safe junction temperature.
4. The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
Electrical Characteristics

Limits in standard typeface are for $T_J = 25^\circ C$, and limits in **boldface type** apply over the full operating temperature range ($-40^\circ C \leq T_J \leq +125^\circ C$). Unless otherwise specified: $V_{IN} = 5V$, $V_{SHDN} = 5V$, $I_L = 0A$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min$^{(1)}$</th>
<th>Typical$^{(2)}$</th>
<th>Max$^{(1)}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td>$R_L = 43\Omega$ $^{(3)}$</td>
<td>$V_{IN} = 2.7V$</td>
<td>5.4</td>
<td>7</td>
<td>V</td>
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<td></td>
<td></td>
<td></td>
<td>$V_{IN} = 3.3V$</td>
<td>8</td>
<td>10</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{IN} = 5V$</td>
<td>13</td>
<td>17</td>
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<tr>
<td></td>
<td>Minimum Output Voltage Under Load</td>
<td>$R_L = 15\Omega$ $^{(3)}$</td>
<td>$V_{IN} = 2.7V$</td>
<td>3.75</td>
<td>5</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{IN} = 3.3V$</td>
<td>5</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{IN} = 5V$</td>
<td>8.75</td>
<td>11</td>
<td></td>
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<tr>
<td>$I_{SW}$</td>
<td>Switch Current Limit</td>
<td>See $^{(4)}$</td>
<td>1.8</td>
<td>1.4</td>
<td>2</td>
<td>A</td>
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<tr>
<td>$R_{DS(ON)}$</td>
<td>Switch ON Resistance</td>
<td>$I_{SW} = 100mA$, $V_{IN} = 5V$</td>
<td>260</td>
<td>400</td>
<td></td>
<td>mΩ</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$I_{SW} = 100mA$, $V_{IN} = 3.3V$</td>
<td>300</td>
<td>450</td>
<td>550</td>
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<td>$SHDN_{TH}$</td>
<td>Shutdown Threshold</td>
<td>Device ON</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Device OFF</td>
<td>0.50</td>
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<td></td>
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<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown Pin Bias Current</td>
<td>$V_{SHDN} = 0$</td>
<td>0</td>
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<td></td>
<td>μA</td>
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<td></td>
<td></td>
<td>$V_{SHDN} = 5V$</td>
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<td>2</td>
<td></td>
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<tr>
<td>$V_{FB}$</td>
<td>Feedback Pin Reference Voltage</td>
<td>$V_{FB} = 1.23V$</td>
<td>1.205</td>
<td>1.230</td>
<td>1.255</td>
<td>V</td>
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<tr>
<td>$I_{FB}$</td>
<td>Feedback Pin Bias Current</td>
<td>$V_{SHDN} = 5V$, Switching</td>
<td>60</td>
<td>500</td>
<td></td>
<td>nA</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{SHDN} = 0$, Not Switching</td>
<td>400</td>
<td>500</td>
<td></td>
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<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>$V_{SHDN} = 5V$, Switching</td>
<td>2</td>
<td>3.0</td>
<td></td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{SHDN} = 0$, Not Switching</td>
<td>400</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{FB}$</td>
<td>FB Voltage Line Regulation</td>
<td>$2.7V \leq V_{IN} \leq 14V$</td>
<td>0.02</td>
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<td></td>
<td>%/V</td>
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<tr>
<td>$F_{SW}$</td>
<td>Switching Frequency$^{(5)}$</td>
<td></td>
<td>1</td>
<td>1.6</td>
<td>1.85</td>
<td>MHz</td>
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<tr>
<td>$D_{MAX}$</td>
<td>Maximum Duty Cycle$^{(5)}$</td>
<td></td>
<td>86</td>
<td>93</td>
<td></td>
<td>%</td>
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<tr>
<td>$I_L$</td>
<td>Switch Leakage</td>
<td>Not Switching $V_{SW} = 5V$</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

(1) Limits are ensured by testing, statistical correlation, or design.
(2) Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.
(3) $L = 10 \mu H$, $C_{OUT} = 4.7 \mu F$, duty cycle = maximum
(4) Switch current limit is dependent on duty cycle (see Typical Performance Characteristics).
(5) Specified limits are the same for $V_{IN} = 3.3V$ input.
Typical Performance Characteristics

Unless otherwise specified: \( V_{IN} = 5V \), SHDN pin tied to \( V_{IN} \).

- **Figure 2.** 
  \( Iq_{Vin} \) (Active) vs Temperature

- **Figure 3.** 
  Oscillator Frequency vs Temperature

- **Figure 4.** 
  Max. Duty Cycle vs Temperature

- **Figure 5.** 
  \( Iq_{Vin} \) (Idle) vs Temperature

- **Figure 6.** 
  Feedback Bias Current vs Temperature

- **Figure 7.** 
  Feedback Voltage vs Temperature

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Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{IN} = 5V$, SHDN pin tied to $V_{IN}$.

**Figure 8.**

**Figure 9.**

**Figure 10.**

**Figure 11.**

**Figure 12.**

**Figure 13.**
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{\text{IN}} = 5V$, SHDN pin tied to $V_{\text{IN}}$.

Efficiency vs Load Current
$V_{\text{IN}} = 2.7V$, $V_{\text{OUT}} = 12V$

Efficiency vs Load Current
$V_{\text{IN}} = 3.3V$, $V_{\text{OUT}} = 12V$

Efficiency vs Load Current
$V_{\text{IN}} = 5V$, $V_{\text{OUT}} = 12V$

Efficiency vs Load Current
$V_{\text{IN}} = 5V$, $V_{\text{OUT}} = 18V$

Figure 14.

Figure 15.

Figure 16.

Figure 17.
THEORY OF OPERATION

The LMR62014 is a switching converter IC that operates at a fixed frequency (1.6 MHz) for fast transient response over a wide input voltage range and incorporates pulse-by-pulse current limiting protection. Because this is current mode control, a 33 mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Since the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output voltage in regulation.

Q1 and Q2 along with R3 - R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 and Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node “multiplied up” by the ratio of the output resistive divider.

The current limit comparator feeds directly into the flip-flop that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminated until the next clock pulse. The current limit input terminates the pulse regardless of the status of the output of the PWM comparator.

Application Hints

SELECTING THE EXTERNAL CAPACITORS

The best capacitors for use with the LMR62014 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer’s data curves before selecting a capacitor.

SELECTING THE OUTPUT CAPACITOR

A single ceramic capacitor of value 4.7 µF to 10 µF will provide sufficient output capacitance for most applications. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used. Aluminum electrolytics with ultra low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical AI electrolytic capacitors are not suitable for switching frequencies above 500 kHz due to significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

In general, if electrolytics are used, it is recommended that they be paralleled with ceramic capacitors to reduce ringing, switching losses, and output voltage ripple.

SELECTING THE INPUT CAPACITOR

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. We recommend a nominal value of 2.2 µF, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.
FEED-FORWARD COMPENSATION

Although internally compensated, the feed-forward capacitor \( C_f \) is required for stability (see Basic Application Circuit). Adding this capacitor puts a zero in the loop response of the converter. The recommended frequency for the zero \( f_z \) should be approximately 6 kHz. \( C_f \) can be calculated using the formula:

\[
C_f = \frac{1}{(2 \times \pi \times R_1 \times f_z)} \tag{1}
\]

SELECTING DIODES

The external diode used in the typical application should be a Schottky diode. The diode must be rated to handle the maximum output voltage and load current. A 20V diode such as the MBR0520 is recommended.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5A. For applications exceeding 0.5A average, a Toshiba CRS08 can be used.

LAYOUT HINTS

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LMR62014 device. It is recommended that a 4-layer PCB be used so that internal ground planes are available.

As an example, a recommended layout of components is shown:

![Figure 18. Recommended PCB Component Layout](image)

Some additional guidelines to be observed:

1. Keep the path between \( L_1 \), \( D_1 \), and \( C_2 \) extremely short. Parasitic trace inductance in series with \( D_1 \) and \( C_2 \) will increase noise and ringing.
2. The feedback components \( R_1 \), \( R_2 \) and \( C_F \) must be kept close to the FB pin of \( U_1 \) to prevent noise injection on the FB pin trace.
3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of \( U_1 \), as well as the negative sides of capacitors \( C_1 \) and \( C_2 \).
SETTING THE OUTPUT VOLTAGE

The output voltage is set using the external resistors R1 and R2 (see Basic Application Circuit). A value of approximately 13.3 kΩ is recommended for R2 to establish a divider current of approximately 92 µA. R1 is calculated using the formula:

\[ R1 = R2 \times \left( \frac{V_{\text{OUT}}}{1.23} - 1 \right) \]  

(2)

![Figure 19. Basic Application Circuit](image)

DUTY CYCLE

The maximum duty cycle of the switching regulator determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

\[ \text{Duty Cycle} = \frac{V_{\text{OUT}} + V_{\text{DIODE}} - V_{\text{IN}}}{V_{\text{OUT}} + V_{\text{DIODE}} - V_{\text{SW}}} \]  

(3)

This applies for continuous mode operation.

INDUCTANCE VALUE

The first question we are usually asked is: “How small can I make the inductor?” (because they are the largest sized component and usually the most costly). The answer is not simple and involves trade-offs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

\[ E = \frac{1}{2} L \times (lp)^2 \]  

where

- “lp” is the peak inductor current.  

(4)

An important point to observe is that the LMR62014 will limit its switch current based on peak current. This means that since \(lp_{(\text{max})}\) is fixed, increasing \(L\) will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays “continuous” over a wider load current range.
To better understand these trade-offs, a typical application circuit (5V to 12V boost with a 10 µH inductor) will be analyzed. We will assume:

\[ V_{IN} = 5\text{V}, \quad V_{OUT} = 12\text{V}, \quad V_{DIODE} = 0.5\text{V}, \quad V_{SW} = 0.5\text{V} \]  

(5)

Since the frequency is 1.6 MHz (nominal), the period is approximately 0.625 µs. The duty cycle will be 62.5%, which means the ON time of the switch is 0.390 µs. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5V.

Using the equation:

\[ V = L \frac{di}{dt} \]  

(6)

We can then calculate the \( \frac{di}{dt} \) rate of the inductor which is found to be 0.45 A/µs during the ON time. Using these facts, we can then show what the inductor current will look like during operation:

During the 0.390 µs ON time, the inductor current ramps up 0.176A and ramps down an equal amount during the OFF time. This is defined as the inductor “ripple current”. It can also be seen that if the load current drops to about 33 mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.

![Figure 20. 10 µH Inductor Current, 5V–12V Boost (LMR62014X)]
MAXIMUM SWITCH CURRENT
The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in the graphs below which show typical values of switch current as a function of effective (actual) duty cycle:

CALCULATING LOAD CURRENT
As shown in Figure 20 which depicts inductor current, the load current is related to the average inductor current by the relation:

\[ I_{LOAD} = I_{IND}(AVG) \times (1 - DC) \]

where

- "DC" is the duty cycle of the application.

The switch current can be found by:

\[ I_{SW} = I_{IND}(AVG) + \frac{1}{2} \left( I_{RIPPLE} \right) \]

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

\[ I_{RIPPLE} = DC \times \left( V_{IN} - V_{SW} \right) / (f \times L) \]

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

\[ I_{LOAD}(max) = (1 - DC) \times (I_{SW}(max) - DC \left( V_{IN} - V_{SW} \right)) \]

which is

\[ I_{LOAD}(max) = \frac{(1 - DC) \times (I_{SW}(max)) - DC \left( V_{IN} - V_{SW} \right)}{2fL} \]

Figure 21. Switch Current Limit vs Duty Cycle

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode. For actual load current in typical applications, we took bench data for various input and output voltages that displayed the maximum load current available for a typical device in graph form:
Figure 22. Max. Load Current (typ) vs $V_{\text{IN}}$

**DESIGN PARAMETERS $V_{\text{SW}}$ AND $I_{\text{SW}}$**

The value of the FET “ON” voltage (referred to as $V_{\text{SW}}$ in the equations) is dependent on load current. A good approximation can be obtained by multiplying the “ON Resistance” of the FET times the average inductor current.

FET on resistance increases at $V_{\text{IN}}$ values below 5V, since the internal N-FET has less gate voltage in this input voltage range (see Typical Performance Characteristics curves). Above $V_{\text{IN}} = 5V$, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. For higher duty cycles, see Typical Performance Characteristics curves.

**THERMAL CONSIDERATIONS**

At higher duty cycles, the increased ON time of the FET means the maximum output current will be determined by power dissipation within the LMR62014 FET switch. The switch power dissipation from ON-state conduction is calculated by:

$$P_{(\text{SW})} = DC \times I_{\text{IND}}(\text{AVE})^2 \times R_{\text{DS} \text{(ON)}}$$

(11)

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

**INDUCTOR SUPPLIERS**

Recommended suppliers of inductors for this product include, but are not limited to Sumida, Coilcraft, Panasonic, TDK and Murata. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

**SHUTDOWN PIN OPERATION**

The device is turned off by pulling the shutdown pin low. If this function is not going to be used, the pin should be tied directly to $V_{\text{IN}}$. If the SHDN function will be needed, a pull-up resistor must be used to $V_{\text{IN}}$ (approximately 50k-100kΩ recommended). The SHDN pin must not be left unterminated.
Efficiency vs Load Current

Figure 23. Flash LED Application
<table>
<thead>
<tr>
<th>Changes from Revision A (April 2013) to Revision B</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Data Sheet to TI format</td>
<td>15</td>
</tr>
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Submit Documentation Feedback

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Product Folder Links: LMR62014
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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<tbody>
<tr>
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<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SH1B</td>
<td>Samples</td>
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<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SH1B</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
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<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

#### REEL DIMENSIONS

*All dimensions are nominal.*

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMR62014XMF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMR62014XMFE/NOPB</td>
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<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
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<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMR62014XMXF/NOPB</td>
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<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
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<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
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</tbody>
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*Device names and other information are not provided.*
TAPE AND REEL BOX DIMENSIONS

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
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<td>DBV</td>
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<td>5</td>
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<td>LMR62014XMFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
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<td>3000</td>
<td>208.0</td>
<td>191.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
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