LMV7271, LMV7272, LMV7275

1 Features
• \(V_S = 1.8\) V, \(T_A = 25^\circ\)C, Typical Values Unless Specified).
• Single or Dual Supplies
• Ultra Low Supply Current 9 \(\mu\)A Per Channel
• Low Input Bias Current 10 nA
• Low Input Offset Current 200 pA
• Low Ensured \(V_{OS} \) 4 mV
• Propagation Delay 880 ns (20-mV Overdrive)
• Input Common Mode Voltage Range 0.1 V
• Beyond Rails
• LMV7272 is Available in DSBGA Package

2 Applications
• Wearable Devices
• Mobile Phones and Tablets
• Battery-Powered Electronics
• General Purpose Low Voltage Applications

3 Description
The LMV727x devices are rail-to-rail input low power comparators, characterized at supply voltages 1.8 V, 2.7 V, and 5 V. They consume as little as 9-\(\mu\)A supply current per channel while achieving a 800-ns propagation delay.

The LMV7271 and LMV7275 (single) are available in SC70 and SOT-23 packages. The LMV7272 (dual) is available in the DSBGA package. With these tiny packages, the PCB area can be significantly reduced. They are ideal for low voltage, low power, and space-critical designs.

The LMV7271 and LMV7272 both feature a push-pull output stage which allows operation with minimum power consumption when driving a load.

The LMV7275 features an open-drain output stage that allows for wired-OR configurations. The open-drain output also offers the advantage of allowing the output to be pulled to any voltage up to 5.5 V, regardless of the supply voltage of the LMV7275, which is useful for level-shifting applications.

The LMV727x devices are built with Texas Instruments’ advance submicron silicon-gate BiCMOS process. They all have bipolar inputs for improved noise performance, and CMOS outputs for rail-to-rail output swing.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMV7271,</td>
<td>SC70 (5)</td>
<td>1.25 mm × 2.00 mm</td>
</tr>
<tr>
<td>LMV7275</td>
<td>SOT-23 (5)</td>
<td>1.60 mm × 2.90 mm</td>
</tr>
<tr>
<td>LMV7272</td>
<td>DSBGA (8)</td>
<td>1.50 mm × 1.50 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit

![Typical Circuit Diagram](image-url)
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (February 2013) to Revision I Page
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1
• Removed Soldering Information from Absolute Maximum Ratings table ................................................................. 4

Changes from Revision G (February 2013) to Revision H Page
• Changed layout of National Data Sheet to TI format ................................................................. 19
## Pin Configuration and Functions

### DBV or DGK Package
5-Pin SOT-23 or SC70
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>+IN</td>
<td>I</td>
<td>Noninverting Input</td>
</tr>
<tr>
<td>GND</td>
<td>P</td>
<td>Negative Supply Voltage</td>
</tr>
<tr>
<td>-IN</td>
<td>I</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>VOUT</td>
<td>O</td>
<td>Output</td>
</tr>
</tbody>
</table>

### YZR Package
8-Pin DSBGA
Top View

See DSBGA Light Sensitivity and DSBGA Mounting in the Layout Guidelines section for mounting precautions.

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>+IN</td>
<td>I</td>
<td>Noninverting Input</td>
</tr>
<tr>
<td>GND</td>
<td>P</td>
<td>Negative Supply Voltage</td>
</tr>
<tr>
<td>-IN</td>
<td>I</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>VOUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V+</td>
<td>P</td>
<td>Positive Supply Voltage</td>
</tr>
<tr>
<td>OUT A</td>
<td>O</td>
<td>Output, Channel A</td>
</tr>
<tr>
<td>-IN A</td>
<td>O</td>
<td>Inverting Input, Channel A</td>
</tr>
<tr>
<td>+IN A</td>
<td>O</td>
<td>Noninverting Input, Channel A</td>
</tr>
<tr>
<td>V-</td>
<td>P</td>
<td>Negative Supply Voltage</td>
</tr>
<tr>
<td>+IN B</td>
<td>O</td>
<td>Noninverting Input, Channel B</td>
</tr>
<tr>
<td>-IN B</td>
<td>O</td>
<td>Inverting Input, Channel B</td>
</tr>
<tr>
<td>OUT B</td>
<td>O</td>
<td>Output, Channel B</td>
</tr>
</tbody>
</table>

---

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6 Specifications

6.1 Absolute Maximum Ratings \(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}}) Differential</td>
<td>±Supply Voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage ((V^+) - (V^-))</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Voltage at Input/Output pins</td>
<td>((V^+) + 0.1)</td>
<td>((V^-) - 0.1)</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature (^{(3)})</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature, (T_{\text{stg}})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.

(3) The maximum power dissipation is a function of \(T_{J(\text{MAX})}\), \(R_{\theta JA}\), and \(T_A\). The maximum allowable power dissipation at any ambient temperature is \(P_D = \frac{T_{J(\text{MAX})} - T_A}{R_{\theta JA}}\). All numbers apply for packages soldered directly into a PCB.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Package Type</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT-23, SC70 PACKAGE</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)(2)})</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Machine Model (MM) (^{(3)})</td>
<td>±200</td>
</tr>
<tr>
<td>DSBGA PACKAGE</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)(2)})</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Machine Model (MM) (^{(3)})</td>
<td>±200</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) Human body model, 1.5 k\(\Omega\) in series with 100 pF.

(3) Machine Model, 0 \(\Omega\) in series with 200 pF.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Temperature (^{(1)})</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) The maximum power dissipation is a function of \(T_{J(\text{MAX})}\), \(R_{\theta JA}\), and \(T_A\). The maximum allowable power dissipation at any ambient temperature is \(P_D = \frac{T_{J(\text{MAX})} - T_A}{R_{\theta JA}}\). All numbers apply for packages soldered directly into a PCB.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LMV7271, LMV7272</th>
<th>LMV7275</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBV (SOT-23)</td>
<td>DGK (SC70)</td>
<td>YZR (DSBGA)</td>
</tr>
<tr>
<td>5 PINS</td>
<td>5 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>(R_{\theta JA}) Junction-to-ambient thermal resistance (^{(2)})</td>
<td>325</td>
<td>265</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(2) The maximum power dissipation is a function of \(T_{J(\text{MAX})}\), \(R_{\theta JA}\), and \(T_A\). The maximum allowable power dissipation at any ambient temperature is \(P_D = \frac{T_{J(\text{MAX})} - T_A}{R_{\theta JA}}\). All numbers apply for packages soldered directly into a PCB.
6.5 1.8-V Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25^\circ C, V^+ = 1.8 \text{ V}, V^- = 0 \text{ V} \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TC ( V_{OS} )</td>
<td>Input Offset Temperature Drift</td>
<td>20</td>
<td></td>
<td></td>
<td>( \mu \text{V/}^\circ \text{C} )</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>200</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>9</td>
<td>12</td>
<td>14</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td>LMV7271/LMV7275</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LMV7272</td>
<td>18</td>
<td>25</td>
<td>28</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>3.5</td>
<td>6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Sourcing, ( V_O = 0.9 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(LMV7271/LMV7272 only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sinking, ( V_O = 0.9 \text{ V} )</td>
<td>4</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Voltage High</td>
<td>1.7</td>
<td>1.74</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(LMV7271/LMV7272 only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_O = 0.5 \text{ mA} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_O = 1.5 \text{ mA} )</td>
<td>1.47</td>
<td>1.63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Voltage Low</td>
<td>52</td>
<td>100</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>( I_O = -0.5 \text{ mA} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_O = -1.5 \text{ mA} )</td>
<td>166</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>1.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>CMRR &gt; 45 dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{CMRR} )</td>
<td>Common-Mode Rejection Ratio</td>
<td>46</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( \text{PSRR} )</td>
<td>Power Supply Rejection Ratio</td>
<td>55</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( I_{LEAKAGE} )</td>
<td>Output Leakage Current</td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td>( V_O = 1.8 \text{ V} ) (LMV7275 only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in \( V_{OS} \) at temperature extremes into the total temperature change.

6.6 1.8-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25^\circ C, V^+ = 1.8 \text{ V}, V^- = 0 \text{ V}, V_{CM} = 0.5 \text{ V}, V_O = V^+/2 \) and \( R_L > 1 \text{ M} \Omega \) to \( V^- \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay (High to Low)</td>
<td>880</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 20 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 50 mV Load = 50 pF/5 kΩ</td>
<td>570</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay (Low to High)</td>
<td>1100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 20 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 50 mV Load = 50 pF/5 kΩ</td>
<td>800</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
6.7 2.7-V Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25°C, V^+ = 2.7 \text{ V}, V^- = 0 \text{ V} \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN(^{(1)})</th>
<th>TYP(^{(2)})</th>
<th>MAX(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} ) Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{OS} ) Input Offset Temperature Drift</td>
<td>( V_{CM} = 1.35 \text{ V} )(^{(3)})</td>
<td>20</td>
<td></td>
<td>10</td>
<td>( \mu \text{V/°C} )</td>
</tr>
<tr>
<td>( I_B ) Input Bias Current</td>
<td></td>
<td>10</td>
<td></td>
<td>200</td>
<td>pA</td>
</tr>
<tr>
<td>( I_{OS} ) Input offset Current</td>
<td></td>
<td>9</td>
<td>13</td>
<td>15</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LMV7271/LMV7275</td>
<td>18</td>
<td>25</td>
<td>28</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_S ) Supply Current</td>
<td></td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LMV7272</td>
<td>10</td>
<td>15</td>
<td>15</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{SC} ) Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 1.35 \text{ V} ) (LMV7271/LMV7272 only)</td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Sinking, ( V_O = 1.35 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OH} ) Output Voltage High (LMV7271/LMV7272 only)</td>
<td>( I_O = 0.5 \text{ mA} )</td>
<td>2.63</td>
<td>2.66</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_O = 2.0 \text{ mA} )</td>
<td>2.48</td>
<td>2.55</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} ) Output Voltage Low</td>
<td>( I_O = -0.5 \text{ mA} )</td>
<td>50</td>
<td>70</td>
<td>155</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>( I_O = -2 \text{ mA} )</td>
<td>155</td>
<td>220</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>( V_{CM} ) Input Common Voltage Range</td>
<td>CMRR &gt; 45 dB</td>
<td>-0.1</td>
<td></td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td>( \text{CMRR} ) Common-Mode Rejection Ratio</td>
<td>( 0 &lt; V_{CM} &lt; 2.7 \text{ V} )</td>
<td>46</td>
<td>78</td>
<td>18</td>
<td>dB</td>
</tr>
<tr>
<td>( \text{PSRR} ) Power Supply Rejection Ratio</td>
<td>( V^+ = 1.8 \text{ V} \text{ to } 5 \text{ V} )</td>
<td>55</td>
<td>80</td>
<td>20</td>
<td>dB</td>
</tr>
<tr>
<td>( I_{LEAKAGE} ) Output Leakage Current</td>
<td>( V_O = 2.7 \text{ V} ) (LMV7275 only)</td>
<td>2</td>
<td></td>
<td>2</td>
<td>pA</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in \( V_{OS} \) at temperature extremes into the total temperature change.

6.8 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25°C, V^+ = 2.7 \text{ V}, V^- = 0 \text{ V}, V_{CM} = 0.5 \text{ V}, V_O = V^+/2 \text{ and } R_L > 1 \text{ MΩ to } V^- \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN(^{(1)})</th>
<th>TYP(^{(2)})</th>
<th>MAX(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay (High to Low)</td>
<td>1200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 20 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 50 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay (Low to High)</td>
<td>810</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 20 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 50 mV Load = 50 pF/5 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
6.9 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 5\, V$, $V^- = 0\, V$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN$^{(1)}$</th>
<th>TYP$^{(2)}$</th>
<th>MAX$^{(1)}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$ Input Offset Voltage</td>
<td>At the temperature extremes</td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td>$TC , V_{OS}$ Input Offset Temperature Drift</td>
<td>$V_{CM} = 2.5, V^{(3)}$</td>
<td>20</td>
<td>μV$/^\circ C$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_B$ Input Bias Current</td>
<td></td>
<td>10</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$ Input Offset Current</td>
<td>LMV7271/LMV7275</td>
<td>200</td>
<td>14</td>
<td>16</td>
<td>μA</td>
</tr>
<tr>
<td>$I_S$ Supply Current</td>
<td>LMV7272</td>
<td>20</td>
<td>27</td>
<td>30</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{SC}$ Output Short Circuit Current</td>
<td>Sourcing, $V_O = 2.5, V$ (LMV7271/LMV7272 only)</td>
<td>18</td>
<td>34</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OH}$ Output Voltage High (LMV7271/LMV7272 only)</td>
<td></td>
<td>4.93</td>
<td>4.96</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Output Voltage Low</td>
<td></td>
<td>27</td>
<td>70</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{CM}$ Input Common Voltage Range</td>
<td>CMRR &gt; 45 dB</td>
<td>225</td>
<td>315</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$CMRR$ Common-Mode Rejection Ratio</td>
<td>$0 &lt; V_{CM} &lt; 5.0, V$</td>
<td>46</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$PRSS$ Power Supply Rejection Ratio</td>
<td>$V^+ = 1.8, V$ to 5, V</td>
<td>55</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_{LEAKAGE}$ Output Leakage Current</td>
<td>$V_O = 5, V$ (LMV7275 only)</td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in $V_{OS}$ at temperature extremes into the total temperature change.

6.10 5-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 5.0\, V$, $V^- = 0\, V$, $V_{CM} = 0.5\, V$, $V_O = V^+/2$ and $R_L > 1\, M\Omega$ to $V^-$.  

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN$^{(1)}$</th>
<th>TYP$^{(2)}$</th>
<th>MAX$^{(1)}$</th>
<th>UNIT</th>
</tr>
</thead>
</table>
| $t_{PHL}$       | Propagation Delay (High to Low)  
|                 | Input Overdrive = 20 mV 
|                 | Load = 50 pF/5 kΩ | 2100        | ns          |             |      |
|                 | Input Overdrive = 50 mV 
|                 | Load = 50 pF/5 kΩ | 1380        | ns          |             |      |
| $t_{PLH}$       | Propagation Delay (Low to High) 
|                 | Input Overdrive = 20 mV 
|                 | Load = 50 pF/5 kΩ | 1800        | ns          |             |      |
|                 | Input Overdrive = 50 mV 
|                 | Load = 50 pF/5 kΩ | 1100        | ns          |             |      |

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
6.11 Typical Characteristics

$T_A = 25^\circ C$, Unless otherwise specified.
Typical Characteristics (continued)

$T_A = 25^\circ C$, Unless otherwise specified.

**Figure 7. Supply Current vs. Supply Voltage (LMV7272)**

**Figure 8. Output Positive Swing vs. $V_{\text{SUPPLY}}$**

**Figure 9. Output Negative Swing vs. $V_{\text{SUPPLY}}$**

**Figure 10. Output Positive Swing vs. $I_{\text{SOURCE}}$**

**Figure 11. Output Negative Swing vs. $I_{\text{SINK}}$**

**Figure 12. Output Positive Swing vs. $I_{\text{SOURCE}}$**

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Typical Characteristics (continued)

$T_A = 25°C$, Unless otherwise specified.

- Figure 13. Output Negative Swing vs. $I_{\text{SINK}}$
- Figure 14. Output Negative Swing vs. $I_{\text{SINK}}$
- Figure 15. Output Positive Swing vs. $I_{\text{SOURCE}}$
- Figure 16. Propagation Delay ($t_{\text{PLH}}$)
- Figure 17. Propagation Delay ($t_{\text{PHL}}$)
Typical Characteristics (continued)

\( T_A = 25°C, \text{ Unless otherwise specified.} \)

Figure 19. Propagation Delay (\( t_{PHL} \))

Figure 20. Propagation Delay (\( t_{PLH} \))

Figure 21. Propagation Delay (\( t_{PHL} \))

Figure 22. \( t_{PHL} \) vs. Overdrive

Figure 23. \( t_{PLH} \) vs. Overdrive
7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 24, the comparator compares an input voltage \( V_{\text{IN}} \) to a reference voltage \( V_{\text{REF}} \). If \( V_{\text{IN}} \) is less than \( V_{\text{REF}} \), the output \( V_{O} \) is low. However, if \( V_{\text{IN}} \) is greater than \( V_{\text{REF}} \), the output voltage \( V_{O} \) is high.

![Figure 24. LMV7271 Basic Comparator](image)

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Rail-to-Rail Input Stage

The LMV727X has an input common mode voltage range \( (V_{\text{CM}}) \) of \(-0.1\) V below the \( V^-\) to \( 0.1\) V above \( V^+\). This is achieved by using paralleled PNP and NPN differential input pairs. When the \( V_{\text{CM}} \) is near \( V^+\), the NPN pair is on and the PNP pair is off. When the \( V_{\text{CM}} \) is near \( V^-\), the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from \( V^+\). Because each input stage has its own offset voltage \( (V_{\text{OS}}) \), the \( V_{\text{OS}} \) of the comparator becomes a function of the \( V_{\text{CM}} \). See curves for \( V_{\text{OS}} \) vs. \( V_{\text{CM}} \) in the Typical Characteristics section. In application design, it is recommended to keep the \( V_{\text{CM}} \) away from the crossover point to avoid problems. The wide input voltage range makes LMV727X ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.
Feature Description (continued)

7.3.2 Output Stage, LMV7271 and LMV7272

![Figure 25. LMV7271 and LMV7272 Push-Pull Output Stage](image)

The LMV7271 and LMV7272 have a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum by eliminating the need for a pullup resistor. The only current consumed is the low supply current and the current going directly into the load.

When the output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V+ and V− through output transistors. The result is a short spike of current (called shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See *Circuit Techniques for Avoiding Oscillations in Comparator Applications* for supply bypassing for details.

7.3.3 Output Stage, LMV7275

![Figure 26. LMV7275 Open-Drain Output](image)

The LMV7275 has an open-drain output that requires a pullup resistor to a positive supply voltage for the output to operate properly. The internal circuitry is identical to the LMV7271 except that the upper P-channel output device is absent. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage by the external pullup resistor. This allows the output to be OR'ed with other open-drain outputs on the same bus. The output pullup resistor may be connected to any voltage level between V- and V+ for level shifting applications.

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay is not affected by capacitive loads at the output of the LMV7271 or LMV7272. However, resistive loads slightly effect the propagation delay on the falling edge depending on the load resistance value.

The propagation delay on the rising edge of the LMV7275 depends on the load resistance and capacitance values.
Device Functional Modes (continued)

7.4.2 Noise

Most comparators have rather low gain. This allows the output to alternate between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero and triggers on noise. The high gain of this comparator eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See Hysteresis.)

7.4.3 Hysteresis

It is a standard procedure to use hysteresis (positive feedback) around a comparator to prevent oscillation due to the comparator triggering its own noise on slowly ramping signals. The following sections will describe various ways to apply hysteresis.

7.4.3.1 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference ($V_{REF}$) at the inverting input. When $V_{IN}$ is low, the output is also low. For the output to switch from low to high, $V_{IN}$ must rise up to $V_{IN1}$ where $V_{IN1}$ is calculated by:

$$\Delta V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2}$$  \hspace{1cm} (1)

As soon as $V_{O}$ switches to $V_{CC}$, $V_{A}$ steps to a value greater than $V_{REF}$ which is given by:

$$V_{A} = V_{IN} + \frac{(V_{CC} - V_{IN})R_1}{R_1 + R_2}$$  \hspace{1cm} (2)

To make the comparator switch back to its low state, $V_{IN}$ must equal $V_{REF}$ before $V_{A}$ will again equal $V_{REF}$. $V_{IN2}$ can be calculated by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC} R_1}{R_2}$$  \hspace{1cm} (3)

The hysteresis of this circuit is the difference between $V_{IN1}$ and $V_{IN2}$.

$$\Delta V_{IN} = \frac{V_{CC} R_1}{R_2}$$  \hspace{1cm} (4)

Figure 27. Noninverting Comparator With Hysteresis

Figure 28. Noninverting Comparator Thresholds
Device Functional Modes (continued)

7.4.3.2 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage \( V_{CC} \) of the comparator (Figure 29). When \( V_{IN} \) at the inverting input is less than \( V_A \), the voltage at the noninverting node of the comparator (\( V_{IN} < V_A \)), the output voltage is high (for simplicity assume \( V_O \) switches as high as \( V_{CC} \)). The three network resistors can be represented as \( R_1 || R_3 \) in series with \( R_2 \). The lower input trip voltage \( V_{A1} \) is defined as

\[
V_{A1} = \frac{V_{CC} R_2}{(R_1 || R_3) + R_2}
\]

When \( V_{IN} \) is greater than \( V_A \) (\( V_{IN} > V_A \)), the output voltage is low and very close to ground. In this case the three network resistors can be presented as \( R_2 // R_3 \) in series with \( R_1 \). The upper trip voltage \( V_{A2} \) is defined as

\[
V_{A2} = \frac{V_{CC} (R_2 || R_3)}{R_1 + (R_2 || R_3)}
\]

The total hysteresis provided by the network is defined as

\[
\Delta V_A = V_{A1} - V_{A2}
\]

A good typical value of \( \Delta V_A \) would be in the range of 5 to 50 mV. This is easily obtained by choosing \( R_3 \) as 1000 to 100 times \( (R_1 || R_2) \) for 5-V operation, or as 300 to 30 times \( (R_1 || R_2) \) for 1.8-V operation.
Device Functional Modes (continued)

7.4.4 Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100 mV<sub>PP</sub> AC signal. As the signal at the noninverting input crosses 0 V, the output of the comparator changes state.

7.4.4.1 Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider $R_4$ and $R_5$ establishes a reference voltage, $V_1$, at the positive input. By making the series resistance, $R_1$ plus $R_2$ equal to $R_5$, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

The positive feedback resistor, $R_6$, is made very large with respect to $R_5 || R_6 = 2000 R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions.

Diode $D_1$ is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, $D_1$ will forward bias, clamping the node between $R_1$ and $R_2$ to approximately −700 mV. This sets up a voltage divider with $R_2$ and $R_3$ preventing $V_2$ from going below ground. The maximum negative input overdrive is limited by the current handling ability of $D_1$.

7.4.5 Threshold Detector

Diode $D_1$ is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, $D_1$ will forward bias, clamping the node between $R_1$ and $R_2$ to approximately −700 mV. This sets up a voltage divider with $R_2$ and $R_3$ preventing $V_2$ from going below ground. The maximum negative input overdrive is limited by the current handling ability of $D_1$. 

Figure 31. Zero Crossing Detector With Hysteresis

Figure 32. Threshold Detector
Device Functional Modes (continued)

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the $V_{REF}$ threshold, the output of the comparator changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

7.4.6 Universal Logic Level Shifter (LMV7275 only)

The output of LMV7275 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level within the permitted power supply range. Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

For example, $V_A$ could be the 5-V analog supply voltage, where $V_B$ could be the 3.3-V supply of the processor. The output will now be compatible with the 3.3-V logic.

7.4.7 OR'ING the Output (LMV7275 only)

Because the LMV7275 output is an unconnected NMOS drain, many open-drain outputs can be tied together, pulled up to $V^*$ by a common resistor to provide an output OR'ing function. If any of the comparator outputs goes low, the output $V_O$ goes low.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LMV727x devices are single-supply comparators with 880 ns of propagation delay and only 12 µA of supply current.

8.2 Typical Applications

8.2.1 Square Wave Oscillator

8.2.1.1 Design Requirements
A typical application for a comparator is as a square wave oscillator. Figure 35 generates a square wave whose period is set by the RC time constant of the capacitor C1 and resistor R4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

8.2.1.2 Detailed Design Procedure
To analyze the circuit, consider it when the output is high. That implies that the inverted input (VC) is lower than the noninverting input (VA).

![Figure 35. Square Wave Oscillator Application](image)

![Figure 36. Squarewave Oscillator Timing Thresholds](image)
Typical Applications (continued)

This causes the \( C_1 \) to get charged through \( R_4 \), and the voltage \( V_C \) increases till it is equal to the noninverting input. The value of \( V_A \) at this point is

\[
V_{A1} = \frac{V_{CC}R_2}{R_2 + R_1||R_3}
\]

If \( R_1 = R_2 = R_3 \), then \( V_{A1} = 2V_{CC}/3 \)

At this point the comparator switches pulling down the output to the negative rail. The value of \( V_A \) at this point is

\[
V_{A2} = \frac{V_{CC}(R_2||R_3)}{R_1 + (R_2||R_3)}
\]

If \( R_1 = R_2 = R_3 \), then \( V_{A2} = V_{CC}/3 \)

The capacitor \( C_1 \) now discharges through \( R_4 \), and the voltage \( V_C \) decreases till it is equal to \( V_{A2} \), at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge \( C_1 \) from \( 2V_{CC}/3 \) to \( V_{CC}/3 \), which is given by \( R_4C_1\ln2 \). Hence the formula for the frequency is:

\[
F = \frac{1}{2(R_4C_1\ln2)}
\]

8.2.1.3 Application Curve

Figure Figure 37 shows the simulated results of an oscillator using the following values:

1. \( R_1 = R_2 = R_3 = R_4 = 100 \, \text{k}\Omega \)
2. \( C_1 = 750 \, \text{pF}, \, C_L = 20 \, \text{pF} \)
3. \( V_+ = 5 \, \text{V}, \, V_- = \text{GND} \)
4. \( C_{STRAY} \) (not shown) from \( V_a \) to \( \text{GND} = 10 \, \text{pF} \)

![Figure 37. Square Wave Oscillator Output Waveforms](image-url)
Typical Applications (continued)

8.2.2 Positive Peak Detector

Figure 38. Positive Peak Detector

The positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to store the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the pullup resistor. When the input $V_{IN}$ increases, the inverting input of the comparator follows it, thus charging the capacitor. When the input voltage decreases, the cap discharges through the 1-MΩ resistor.

The decay time can be modified by changing $R_2$. The output should be accessed through a high-impedance input follower circuit to prevent loading. Upper output swing headroom is determined by the forward voltage of the diode ($V_{MAX} = V_{CC} - V_F$). A Shottky signal diode can be used to reduce the required headroom to around 300 mV.

This circuit can use any of the LMV727x devices, but $R_1$ is not required for the LMV7271 or LMV7272.

8.2.3 Negative Peak Detector

Figure 39. Negative Peak Detector (LMV7275 Only)

The Negative Peak Detector circuit will store the peak negative voltage below ground (0 V to $-V_{CC}$). For the negative detector, the LMV7275 must be used because the output transistor acts as a low-impedance current sink. Because there is no pullup resistor, the only discharge path will be the 1-MΩ resistor and any load impedance used. Decay time is changed by varying the 1-MΩ resistor.

NOTE

The negative peak detector does require a negative supply voltage! $+V_{CC}$ can be grounded to save dynamic range because the output does not swing above ground.
Typical Applications (continued)

8.2.4 Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$.

\[ V_{REF1} = \frac{R_3}{R_1 + R_2 + R_3} \times V^+ \]
\[ V_{REF2} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V^+ \]

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The LMV7275 with an open-drain output should be used if the outputs are to be tied together for a common logic output.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.
9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-\(\mu\)F ceramic capacitor in parallel with a 10-\(\mu\)F capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to ring due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV727x as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the \(V^+\) and \(V^-\) pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

10.1.1 Circuit Techniques for Avoiding Oscillations in Comparator Applications

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1-\(\mu\)F ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8 \(\mu\)F or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In a dual-supply application, a 0.1-\(\mu\)F capacitor is recommended to be placed across \(V^+\) and \(V^-\) pins.

2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).

3. It is a good practice to use an unbroken ground plane on a printed-circuit-board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.

4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in Figure 43.

5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.

6. All pins of any unused comparators should be tied to the negative supply.

10.1.2 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight will cause mis-operation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device. The wavelengths, which have the most detrimental effect, are reds and infrareds. Be aware of internal light sources, such as keyboard or display backlights, that may pass through a PCB. A copper plane should be placed on a lower layer under the DSBGA to block light. Be careful using vias under the device, as they may pass light.
Layout Guidelines (continued)

10.1.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Application Note AN-1112 (SNVA009).

10.1.4 LMV7272 DSBGA to DIP Conversion Board

To facilitate characterization and testing, a DSBGA to DIP conversion board, LMV7272TLCONV, is available. It is a 2-layer board, with the LMV7272 mounted on the bottom layer, and a capacitor (C1, between the positive and negative supplies) added to the top layer.

![LMV7272 TLCONV Diagram](image)

**Figure 42. LMV7272TLCONV Diagram**

10.2 Layout Example

![Typical PCB Layout](image)

**Figure 43. Typical PCB Layout**
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For developmental support, see the following:

• LMV7271 PSPICE Model (can also be used for LMV7272), SNOM052
• LMV7275 PSPICE Model, SNOM555
• TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

• AN-74 A Quad of Independently Functioning Comparators, SNOA654
• AN-1112 Micro SMD Wafer Level Chip Scale Package, SNVA009

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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</table>

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™ Online Community  **TI’s Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  **TI’s Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Device Marking (4/5)</th>
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</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.
RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000 ppm threshold requirement.

MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMV7275:
- Automotive : LMV7275-Q1

NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- **Device**: LMV7271MF
  - **Package Type**: SOT-23
  - **Drawing**: DBV
  - **Pins**: 5
  - **SPQ**: 1000
  - **Reel Diameter (mm)**: 178.0
  - **Reel Width (W1) (mm)**: 8.4

**TAPE DIMENSIONS**

- **Device**: LMV7271MF/NOPB
  - **Package Type**: SOT-23
  - **Drawing**: DBV
  - **Pins**: 5
  - **SPQ**: 1000
  - **Reel Diameter (mm)**: 178.0
  - **Reel Width (W1) (mm)**: 8.4

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<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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<td>0.76</td>
<td>4.0</td>
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</table>

*All dimensions are nominal.*

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Pocket Quadrants**: Q1, Q2, Q3, Q4
- **User Direction of Feed**
- **Sprocket Holes**

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*www.ti.com 25-Sep-2019*
<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
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*All dimensions are nominal.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7526 for other stencil recommendations.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
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