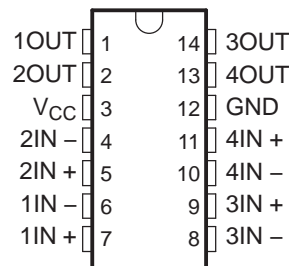


LOW-POWER QUAD DIFFERENTIAL COMPARATOR

FEATURES

- Qualified for Automotive Applications
- Wide Supply-Voltage Range . . . 3 V to 30 V
- Ultra-Low Power-Supply Current
Drain . . . 60 μ A Typ
- Low Input Biasing Current . . . 3 nA
- Low Input Offset Current . . . ± 0.5 nA
- Low Input Offset Voltage . . . ± 2 mV
- Common-Mode Input Voltage Includes Ground
- Output Voltage Compatible With MOS and CMOS Logic
- High Output Sink-Current Capability
(30 mA at $V_O = 2$ V)
- Power-Supply Input Reverse Voltage Protected
- Single Power-Supply Operation
- Pin-for-Pin Compatible With LM239, LM339, LM2901

**D PACKAGE
(TOP VIEW)**


DESCRIPTION/ORDERING INFORMATION

The LP2901 is a low-power quadruple differential comparator. The device consists of four independent voltage comparators designed specifically to operate from a single power supply and, typically, to draw 60- μ A drain current over a wide range of voltages. Operation from split power supplies also is possible, and the ultra-low power-supply drain current is independent of the power-supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, square-wave generators, time-delay generators, voltage-controlled oscillators, multivibrators, and high-voltage logic gates. The LP2901 is designed specifically to interface with the CMOS logic family. The ultra-low power-supply current makes these products desirable in battery-powered applications.

The LP2901 is characterized for operation from -40°C to 85°C .

ORDERING INFORMATION⁽¹⁾

T_A	$V_{IO\text{MAX}}$ AT 25°C	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	± 5 mV	SOIC – D Reel of 2500	LP2901IDRQ1	LP2901IQ1

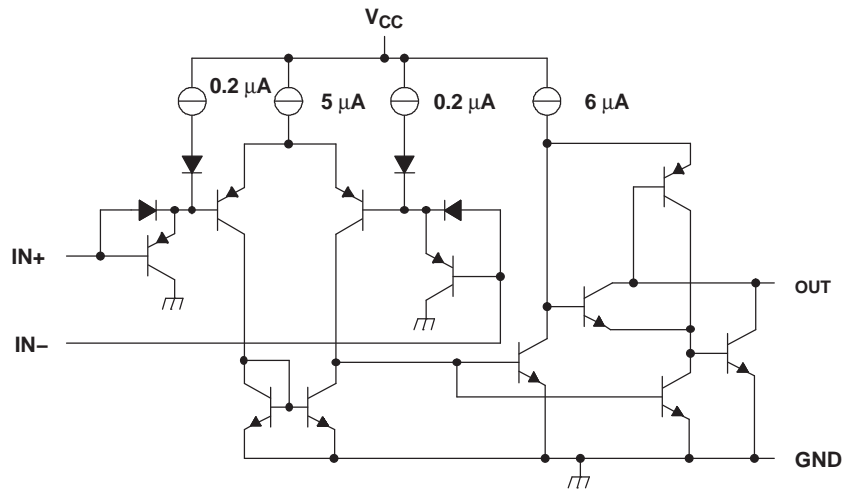
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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SCHEMATIC DIAGRAM (EACH COMPARATOR)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾		36	V
V_{ID}	Differential input voltage range ⁽³⁾		±36	V
V_I	Input voltage range (either input)	-0.3	36	V
I_I	Input current ⁽⁴⁾	$V_I \leq -0.3$ V		-50 mA
	Duration of output short-circuit to ground ⁽⁵⁾	Unlimited		
	Continuous total power dissipation ⁽⁶⁾	See Dissipation Rating Table		
θ_{JA}	Package thermal impedance ⁽⁷⁾⁽⁸⁾		133.5	°C/W
T_A	Operating free-air temperature range	-40	85	°C
T_J	Operating virtual junction temperature		150	°C
T_{lead}	Lead temperature range	1,6 mm (1/16 in) from case for 60 s		300 °C
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) This input current exists only when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive, and normal output states are reestablished when the input voltage returns to a value more positive than -0.3 V at $T_A = 25^\circ\text{C}$.
- (5) Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
- (6) If the output transistors are allowed to saturate, the low-bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).
- (7) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
- (8) The package thermal impedance is calculated in accordance with JESD 51 (low-K board).

Dissipation Ratings

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	936 mW	7.49 mW/°C	599 mW	486 mW

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	30	V
V_{IC}	Common-mode input voltage	$V_{CC} = 5\text{ V}$	0	3	V
		$V_{CC} = 30\text{ V}$	0	28	
V_I	Input voltage	$V_{CC} = 5\text{ V}$	0	3	V
		$V_{CC} = 30\text{ V}$	0	28	
T_A	Operating free-air temperature		-40	85	°C

Electrical Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A ⁽¹⁾	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC} = 5\text{ V to } 30\text{ V}$, $V_O = 2\text{ V}$ ⁽²⁾ , $R_S = 0$	25°C		±2	±5	mV
			Full range			±9	
I_{IO}	Input offset current		25°C		±0.5	±5	nA
			Full range			±1	
I_{IB}	Input bias current ⁽³⁾		25°C		-2.5	-25	nA
			Full range			-4	
V_{ICR}	Common-mode input voltage range	Single supply	25°C	0 to $V_{CC} - 1.5$		V	
			Full range	0 to $V_{CC} - 2$			
A_{VD}	Large-signal differential voltage amplification	$V_{CC} = 15\text{ V}$, $R_L = 15\text{ k}\Omega$		500		V/mV	
Output sink current	$V_{I-} = 1\text{ V}$, $V_{I+} = 0$	$V_O = 2\text{ V}$ ⁽⁴⁾	25°C	20	30	mA	
			Full range	15			
Output leakage current	$V_{I+} = 1\text{ V}$, $V_{I-} = 0$	$V_O = 0.4\text{ V}$	25°C	0.2	0.7	nA	
		$V_O = 5\text{ V}$	25°C	0.1		nA	
I_{CC}	Supply current	$R_L = \infty$, All comparators	Full range			1	μA
						36	V
V_{ID}	Differential input voltage	$V_I \leq 0$ (or V_{CC-} on split supplies)				36	V
I_{CC}	Supply current	$R_L = \infty$, All comparators		60	100	μA	

(1) Full range is -40°C to 125°C .

(2) V_{IO} is measured over the full common-mode input voltage range.

(3) Because of the p-n-p input stage, the direction of the current is out of the device. This current essentially is constant (i.e., independent of the output state). No loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.

(4) The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V and smaller currents at output voltages less than 1.5 V.

Switching Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	TYP	UNIT
Large-signal response time	TTL logic swing, $V_{ref} = 1.4\text{ V}$	1.3	μs
Response time		8	

APPLICATION INFORMATION

Figure 1 shows the basic configuration for using the LP2901 comparator. Figure 2 shows the diagram for using it as a CMOS driver.

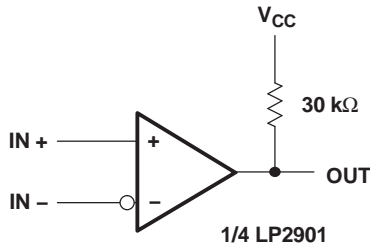


Figure 1. Basic Comparator

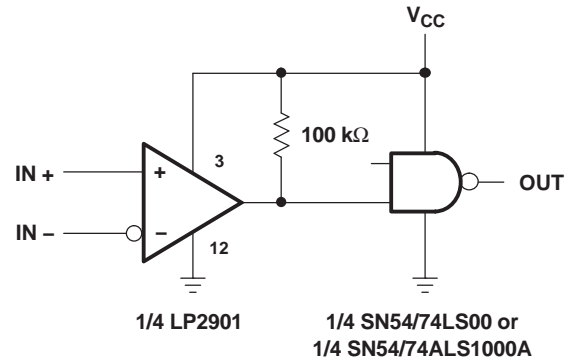


Figure 2. CMOS Driver

All pins of any unused comparators should be grounded. The bias network of the LP2901 establishes a drain current that is independent of the magnitude of the power-supply voltage over the range of 2 V to 30 V. It usually is necessary to use a bypass capacitor across the power-supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than -0.3 V. The output section has two distinct modes of operation, the Darlington mode and the ground-emitter mode. This unique drive circuit permits the device to sink 30 mA at $V_O = 2$ V in the Darlington mode and 700 μ A at $V_O = 0.4$ V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). If the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I_1 and the 60- Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc. in this mode while maintaining an ultra-low power-supply current of 60 μ A typical.

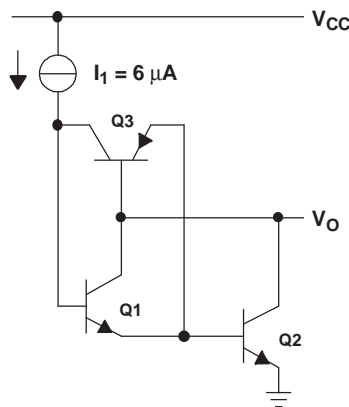


Figure 3. Output-Section Schematic Diagram

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate, and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I_1 directly to the base of Q2. The output sink current now is approximately I_1 times the h_{FE} of Q2 (700 μ A at $V_O = 0.4$ V). The output of the devices exhibits a bimodal characteristic, with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Several outputs can be tied together to provide a dot logic function. An output pullup resistor can be connected to any available power-supply voltage within the permitted power-supply range, and there is no restriction on this voltage, based on the magnitude of the voltage that is supplied to V_{CC} of the package.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2901IDRG4Q1	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LP2901IQ1
LP2901IDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP2901IQ1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LP2901-Q1 :

- Catalog : [LP2901](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2901IDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2901IDRQ1	SOIC	D	14	2500	353.0	353.0	32.0

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

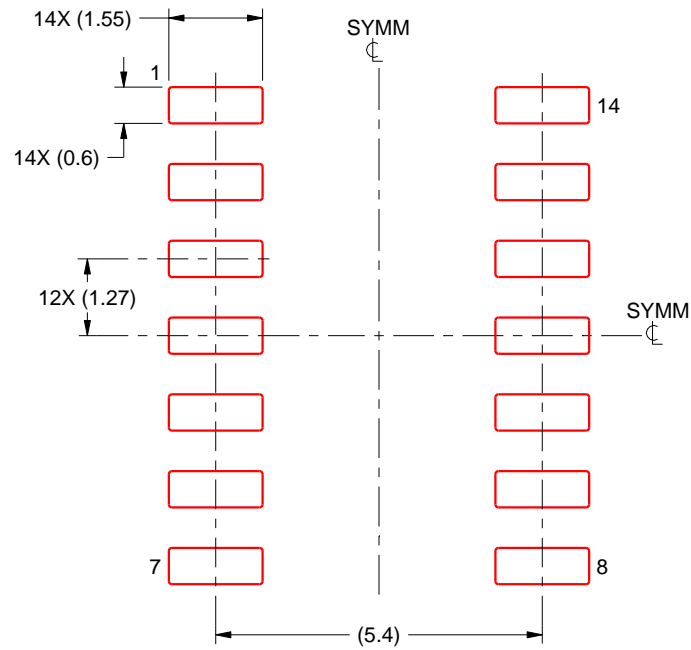
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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