

Programmable LED Driver

Check for Samples: [LP5522](#)

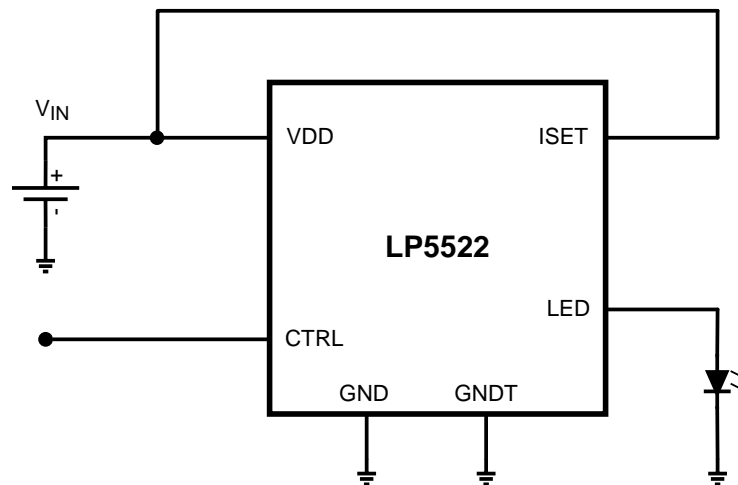
FEATURES

- **Programmable Blinking Sequence**
 - 1 to 3 Programmable Pulses
 - 1 ms to 255 ms LED on Time
 - 10 ms to 2500 ms LED Off Time
 - Single or Continuous Run of Programmed Blinking Sequence
- **Constant Current High Side Output Driver**
- **Adjustable Current with External Resistor**
- **0.2 μ A Typical Shutdown Current**
- **Autonomous Operation without External Clock**
- **DSBGA-6 Package with 0.4 mm Pitch:**
 - 1.215 mm x 0.815 mm x 0.6 mm (LxWxH)

APPLICATIONS

- Indicator Lights
- Phone Cosmetics
- Toys

Typical Application



DESCRIPTION

The LP5522 is a simple single wire programmable LED controller in six bump DSBGA package. It provides constant current flow through high side driver. Output current can be set from 1 mA to 20 mA by using an external resistor on the ISET pin. If no external resistor is used, output current is set to 5 mA default current. The LP5522 is controlled using only one signal. The signal controls either directly the LED driver or it launches previously programmed blinking sequence.

The LP5522 works autonomously without a clock signal from the master device. Very low LED driver headroom voltage makes possible to use supply voltages close to LED forward voltage. Current consumption of the LP5522 is minimized when LED is turned off and once controller is disabled all supporting functions are also shut down. Very small DSBGA package together with minimum number of external components is a best fit for handheld devices.



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Connection Diagrams

DSBGA-6 package, 0.815 x 1.215 x 0.60 mm body size, 0.4 mm pitch, Package Number YFQ0006

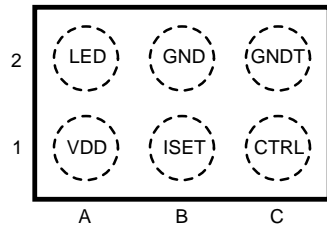


Figure 1. Top View

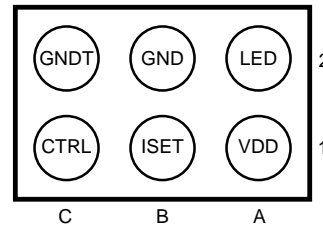


Figure 2. Bottom View

PIN DESCRIPTIONS⁽¹⁾

Pin	Name	Type	Description
A1	VDD	P	Power supply pin
B1	ISET	AI	Current set input
C1	CTRL	DI	Digital control input
A2	LED	AO	Current source output
B2	GND	G	Ground
C2	GNDT	G	Ground

(1) A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

V (VDD, LED, ISET)	-0.3V to +6.0V
Voltage on logic pin (CTRL)	-0.3V to VDD +0.3V with 6.0V max
Continuous Power Dissipation ⁽⁴⁾	Internally Limited
Junction Temperature (T _{J-MAX})	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Reflow soldering, 3 times) ⁽⁵⁾	260°C
ESD Rating ⁽⁶⁾ Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.

(2) All voltages are with respect to the potential at the GND pins.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Office/ Distributors for availability and specifications.

(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typ.) and disengages at T_J=140°C (typ.).

(5) For detailed soldering specifications and information, please refer to Application Note AN1112 : DSBGA Wafer Level Chip Scale Package [SNVA009](#).

(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. MIL-STD-883 3015.7

Operating Ratings ⁽¹⁾⁽²⁾

Voltage on power pin (VDD)	2.7V to 5.5V
Recommended Load Current	1 mA to 20 mA
Junction Temperature (T _J) Range	-30°C to +125°C
Ambient Temperature (T _A) Range ⁽³⁾	-30°C to +85°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (θ_{JA} × P_{D-MAX}).

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ _{JA}) ⁽¹⁾	87°C/W
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- (1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

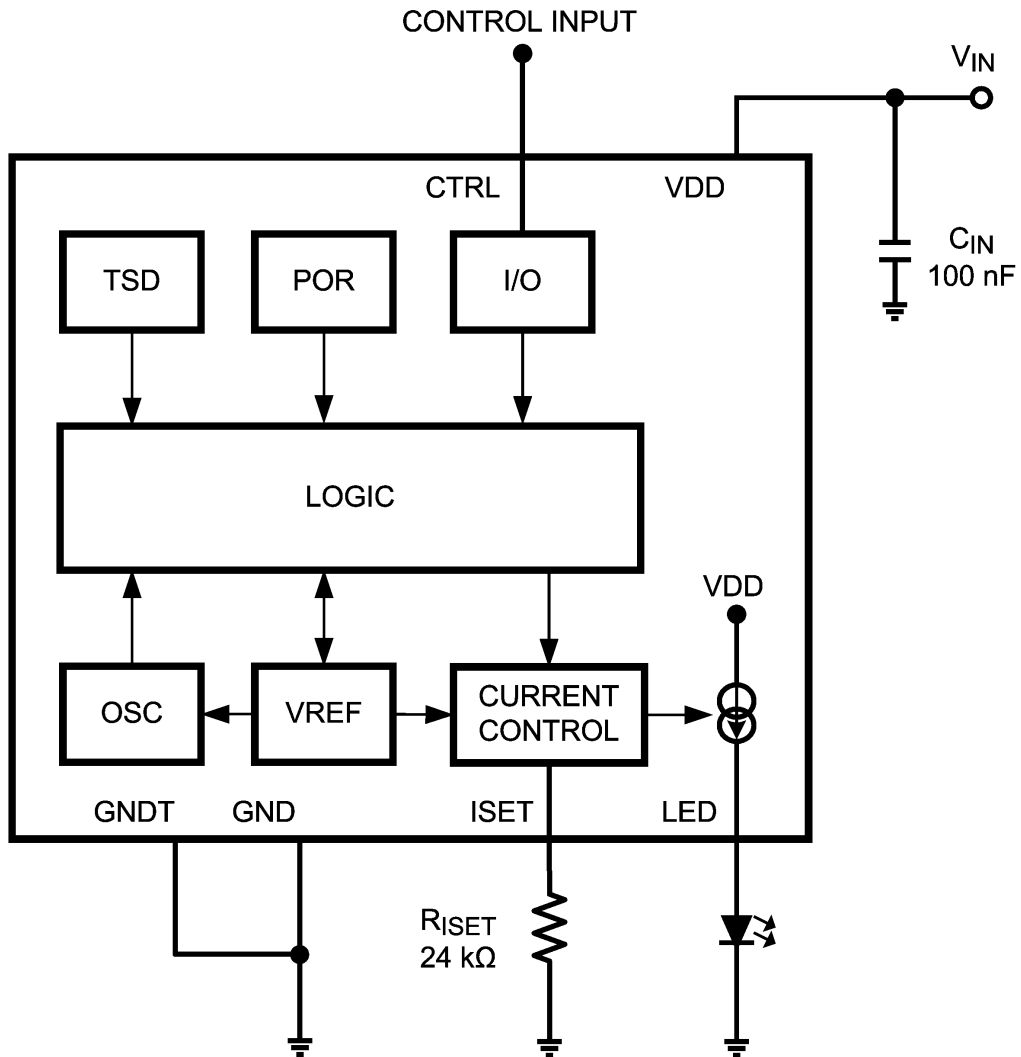
Electrical Characteristics ⁽¹⁾⁽²⁾

Limits in standard typeface are for $T_J = 25^\circ\text{C}$. Limits in **boldface** type apply over the operating ambient temperature range ($-30^\circ\text{C} < T_A < +85^\circ\text{C}$). Unless otherwise noted, specifications apply to [LP5522 Block Diagram](#) with: $V_{IN} = 3.6\text{V}$, $R_{ISET} = 24\text{k}\Omega$, $C_{IN} = 100\text{nF}$.

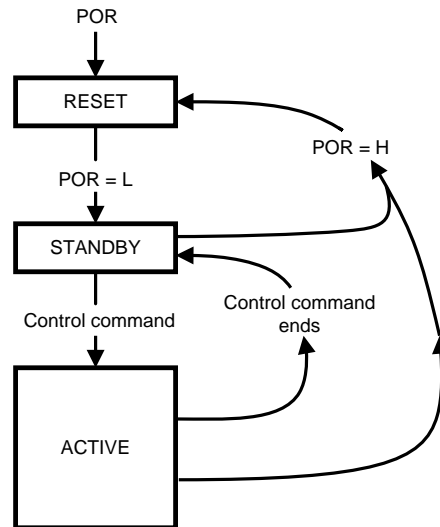
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Standby supply current	CTRL = L		0.2	1	μA
	Active Mode Supply Current	CTRL = H, LED = off		40	55	μA
$I_{LEAKAGE}$	LED Pin Leakage Current				1	μA
I_{OUT}	LED Output Current	Without external resistor	-8	5	+8	mA %
	LED Output Current	With external 24k Ω 0.04% resistor	-8	20	+8	mA %
I_{MIRROR}	External R_{ISET} Mirroring Ratio			1:400		
V_{ISET}	ISET Reference Voltage			1.23		V
V_{HR}	Minimum Headroom Voltage ($V_{IN} - V_{LED}$) ⁽³⁾	I_{OUT} set to 10 mA		35	50	mV
		I_{OUT} set to 20 mA		70	100	mV
T_{CYCLE_H}	Minimum LED On Time		0.9	1.0	1.1	ms
T_{CYCLE_L}	Minimum LED Off Time		9	10	11	ms
$ON_{RESOLUTION}$	LED On Time Resolution			1		ms
$OFF_{RESOLUTION}$	LED Off Time Resolution			10		ms
$T_{Timeout_H}$	LED Timeout On Time		287	319	351	ms
$T_{Timeout_L}$	LED Timeout Off Time		2.87	3.19	3.51	s
V_{IL}	Logic Input Low Level				0.5	V
V_{IH}	Logic Input High Level		1.2			V
I_{IN}	CTRL Input Current		-1		1	μA
t_{ON}	CTRL Pulse ON Time		15			μs
t_{OFF}	CTRL Pulse OFF Time		30			μs
t_{ENTER}	Command Entering Period		500			μs
$t_{ENTER} + t_{BLANK}$	Command Entering Period + Blank Period				1500	μs

- (1) All voltages are with respect to the potential at the GND pins.
- (2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
- (3) The current source is connected internally between V_{IN} and V_{LED} . The voltage across the current source, ($V_{IN} - V_{LED}$), is referred to a headroom voltage (V_{HR}). Minimum headroom voltage is defined as the V_{HR} voltage when the LED current has dropped 10% from the value measured at $V_{LED} = V_{IN} - 1\text{V}$.

LP5522 BLOCK DIAGRAM



Modes of Operation



RESET In the reset mode all functions are off and all registers are reset to the default values. Reset is entered always if internal Power On Reset (POR) is active. Power On Reset will activate during the device startup or when the supply voltage V_{IN} falls below 1.5V (typ.).

STANDBY: After Power On Reset device is in Standby mode. This is the low power consumption mode, when all circuit functions are disabled.

ACTIVE: Once rising edge of CTRL signal is detected device goes into Active mode. In Active mode four sub modes are present:

RUN: Run mode is divided into two sub modes depending on whether a blinking sequence is programmed into memory or not.

Non-programmed mode: No blinking sequence programmed to memory. LED output follows CTRL input

Programmed mode: Blinking sequence programmed to memory. LED output follows the programmed blinking sequence

RUN ONCE: In Run once mode, programmed blinking sequence is performed once and after that device returns into Standby mode. Run once mode is available only if a blinking sequence is programmed into memory.

TRAINING: In Training mode new blinking sequence can be programmed. LED output follows CTRL signal during the programming

TSD: If chip temperature rises above 160°C (typ.) device goes into Thermal Shut Down (TSD) mode. In TSD mode output is disabled but supporting functions are on.

LED Driver Operational Description

The LP5522 LED driver is constant current source. Current can be set with external resistor (R_{ISET}) so that the current ratio between resistor and LED is 1:400. R_{ISET} current correlates to ISET reference voltage (V_{ISET}). Consequently, current through LED can be adjusted using equation $I_{OUT} = 480/R_{ISET}$.

Use of external resistor is optional. If external resistor is not connected, default output current is 5 mA. When external resistor is not used ISET pin should be connected to VDD.

LED Driver Typical Performance Characteristics

$T_J = 25^\circ\text{C}$. Unless otherwise noted, typical performance characteristics apply to [LP5522 Block Diagram](#) with: $V_{IN} = 3.6\text{V}$, $R_{ISET} = 24\text{ k}\Omega$, $C_{IN} = 100\text{ nF}$.

Output Current vs R_{ISET} (Expanded Range)

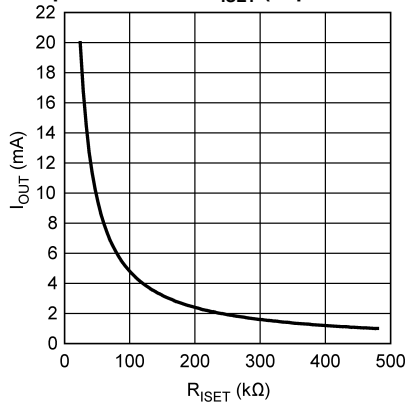


Figure 3.

Output Current vs R_{ISET}

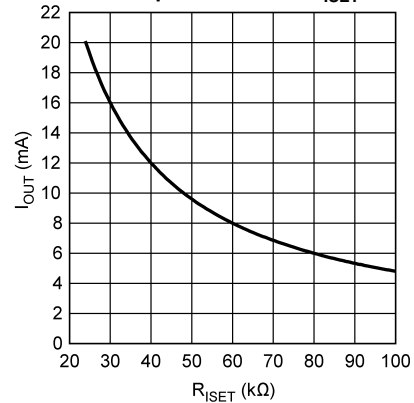


Figure 4.

Output Current vs Input Voltage (ISET Connected To VDD)

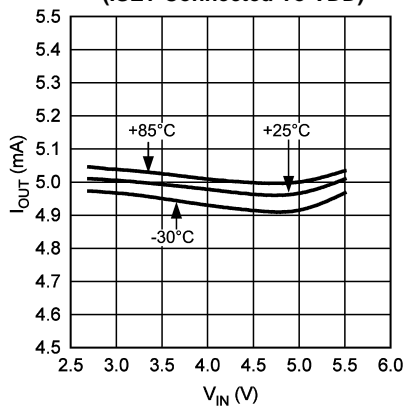


Figure 5.

Output Current vs Headroom Voltage

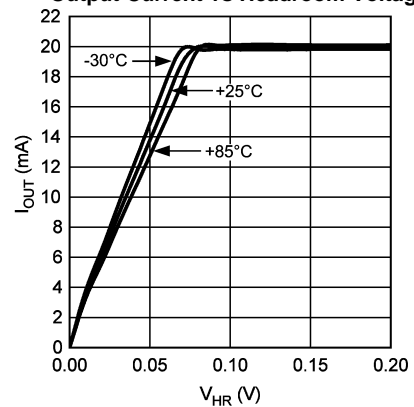


Figure 6.

Line Regulation

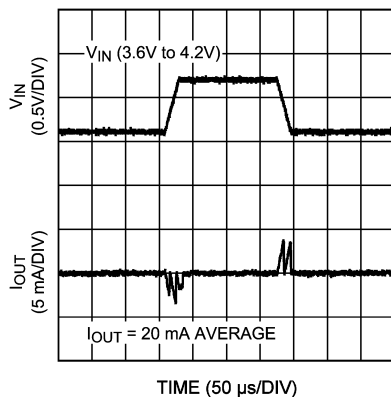


Figure 7.

LED Startup

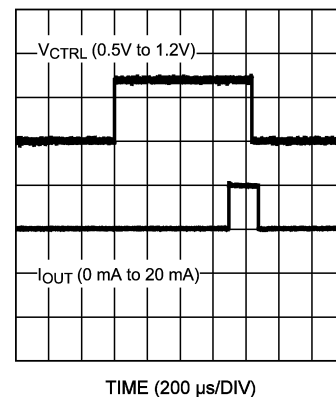
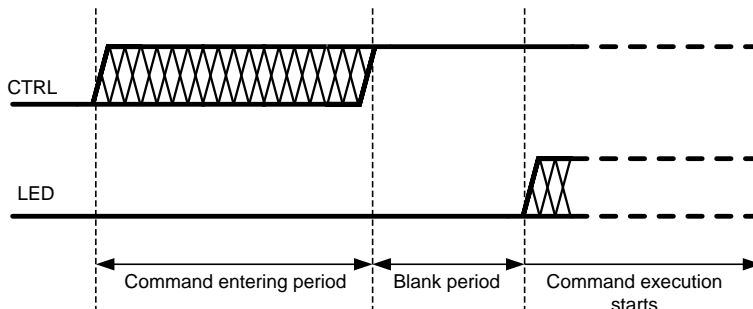


Figure 8.

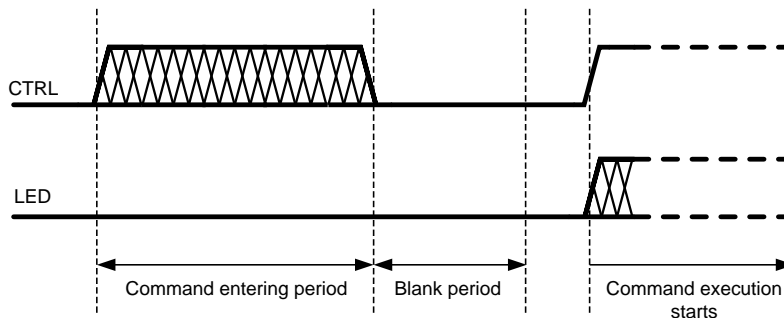
CONTROL INTERFACE OPERATIONAL DESCRIPTION

LP5522 has one digital control input, CTRL. Threshold levels of CTRL input are fixed to enable control from low voltage controller. CTRL signal is used to control the mode of the circuit. A rising edge of the CTRL signal activates the circuit and starts a command entering period. During the command entering period all rising edges are counted. After command entering period there is a blank period when no rising edges are allowed. If CTRL is left high after command entering period, the consequent command is performed right after the blank period.

Note that timing diagrams are not on scale!



If CTRL signal is low after command entering period, command execution starts when CTRL is pulled high. This does not apply to Run command. With Run command CTRL must be high. Note that no rising edges are allowed during blank period.



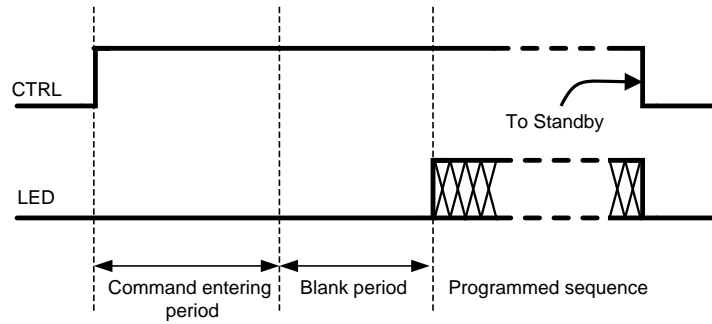
LED Controller Commands and Operation

There are four commands available for LP5522.

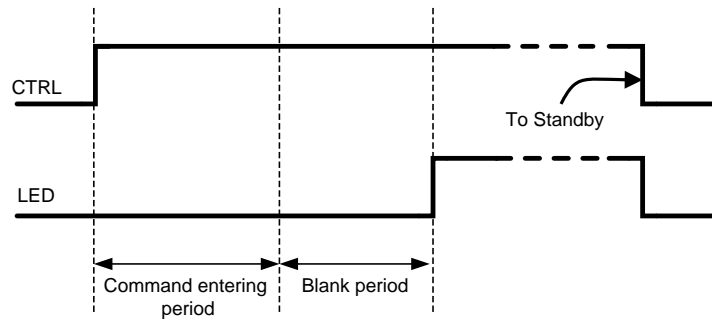
Command	Number of rising edges during command entering period
Run	One rising edge
Training start	Two rising edges
Training end	Three rising edges
Run once	Four rising edges

RUN COMMAND

One rising edge of CTRL signal within command entering period is interpreted as Run command. In programmed mode blinking sequence is started right after Blank period and it is repeated as long as CTRL signal is kept high. When CTRL signal is set low device goes into Standby mode.

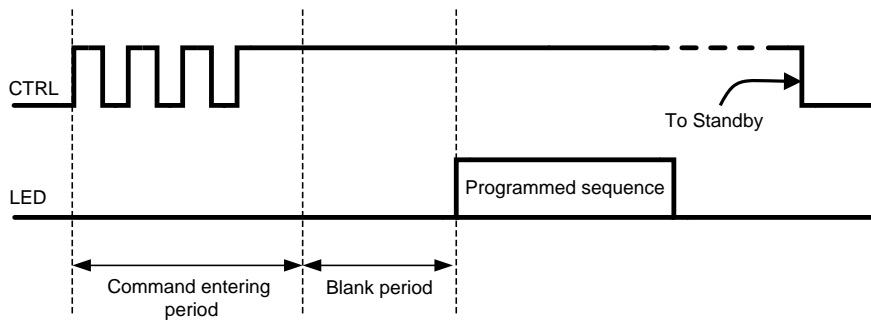


In non-programmed mode LED is on as long as CTRL is kept high. When CTRL signal is set low device goes into Standby mode.

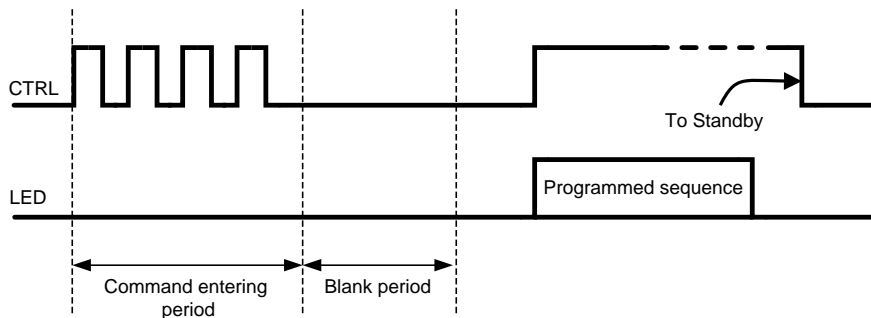


RUN ONCE COMMAND

Programmed blinking sequence is performed once after Run Once command. Four rising edges of CTRL signal within command entering period is interpreted as Run Once command. If CTRL is kept high after command entering period the programmed blinking sequence starts right after the blank period has elapsed. CTRL signal must stay high as long as programmed blinking sequence is executed. If CTRL is set low during execution of blinking sequence, device goes to standby and execution of blinking sequence is stopped.



If CTRL signal is low after command entering period, Run Once command is executed once the CTRL is set high.

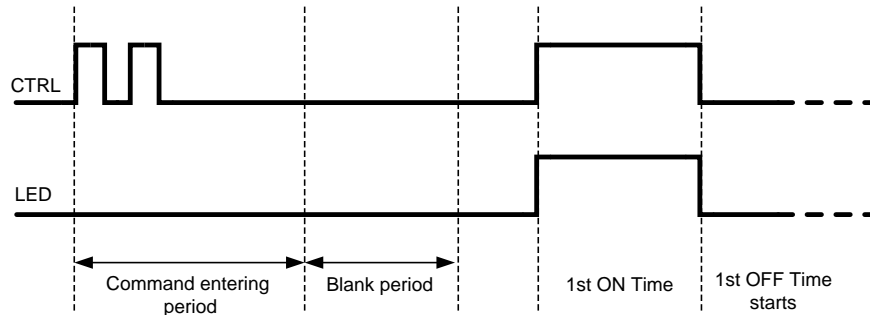


TRAINING START COMMAND

Blinking sequence is programmed into memory in training mode. Blinking sequence is stored into volatile memory, thus removing input voltage V_{IN} resets the memory. Memory can also be reset by giving Training Start and Training End commands without any valid LED ON/OFF times.

LP5522 enters to Training mode after Training Start command. Two rising edges within command entering period is interpreted as the Training Start command. The first LED ON time capturing is started once the rising edge of CTRL signal is detected after the blank period. LED output follows CTRL signal during the programming.

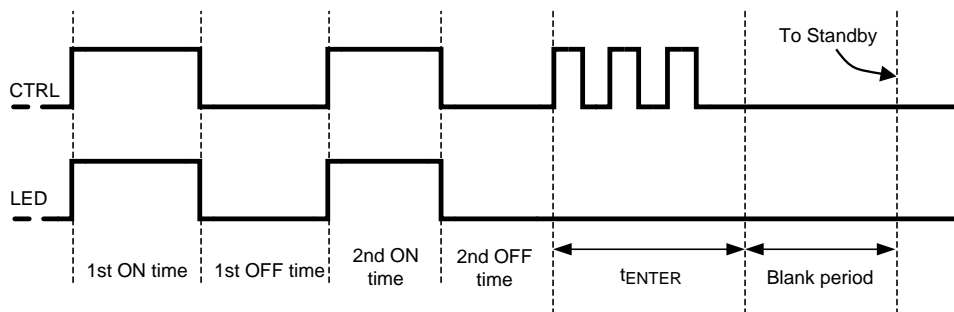
The first LED ON time is recorded once CTRL signal is set low. Same time the first LED OFF time capturing is started. Programmed blinking sequence can have one to three LED ON/OFF times. In order to be programmed correctly, at least one valid LED ON and LED OFF time must be recorded.



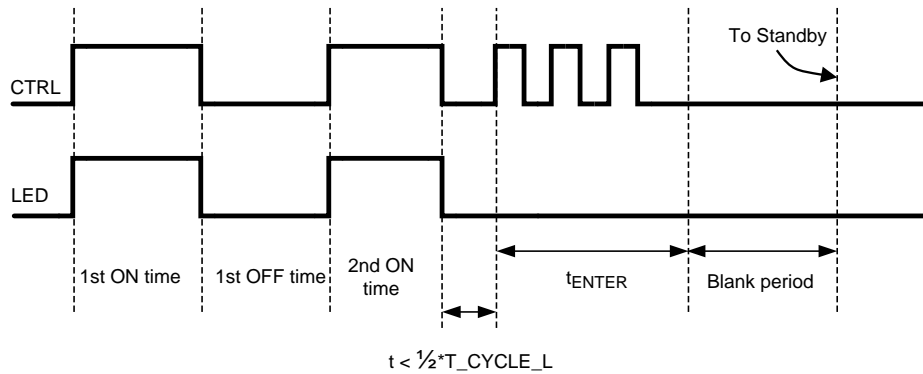
TRAINING END COMMAND

Blinking sequence programming ends once Training End command is introduced. Three rising edges within time period of t_{ENTER} is interpreted as Training End command. Note that blank period is also required after Training End command. During blank period no rising edges are allowed.

When Training End command is introduced during LED OFF time capturing, LED OFF time is recorded and chip goes to standby mode.



If Training End command is introduced during LED ON time capturing, the associated LED ON period is not recorded and hence neither OFF time. Notice that valid OFF time before Training End is longer than half of Minimum LED OFF period (T_{CYCLE_L}).

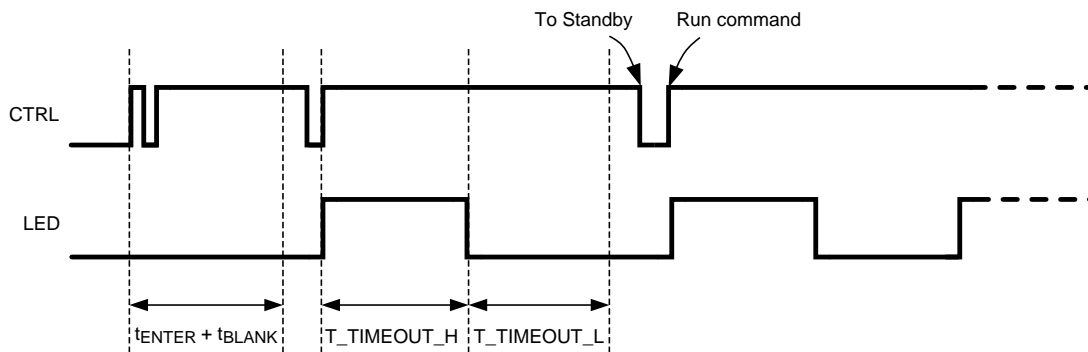


LED TIMEOUT ON/OFF TIMES

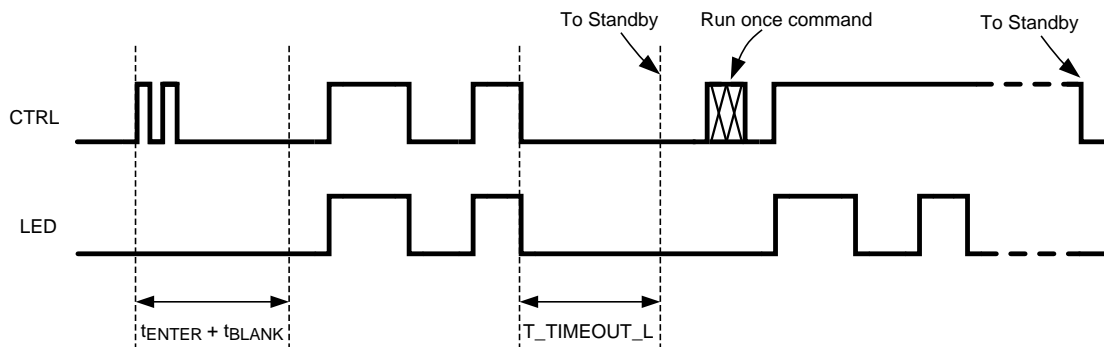
When LP5522 is in training mode and CTRL signal is high longer than LED Timeout ON time, the ON time counter saturates. In this case saturated ON time is recorded and LED OFF time capturing is started. At the same time LED is switched off even if the CTRL signal is still high.

If ON time counter has saturated, LED OFF time recording is terminated either by giving a Train End command or setting the CTRL signal to low and back to high. Setting the CTRL signal back to high records the LED OFF time and starts next ON time capturing.

If anyhow CTRL is still high after the LED Timeout OFF time has been elapsed the OFF time counter saturates and saturated OFF time is recorded. After that chip waits the CTRL signal to go low which cause the chip to go Standby.



LED OFF time counter can saturate also if Training end command is not given or no new ON time has been started. In this case saturated OFF time is recorded and chip goes to Standby.



Recommended External Components

INPUT CAPACITOR, C_{IN}

Although not required for normal operation, a capacitor can be added to V_{IN} to reduce line noise. A surface-mount multi-layer ceramic capacitor (MLCC) is recommended. MLCCs with a X7R or X5R temperature characteristic are preferred.

CURRENT SET RESISTOR, R_{ISET}

If other than 5 mA current is required, R_{ISET} resistor can be used to adjust the current. For 20 mA current 24 k Ω resistor is required. Accuracy of the resistor directly effects to the accuracy of the LED current. 1% or better is recommended.

LED

Forward voltage of LED must be less than minimum input voltage minus minimum headroom voltage (V_{HR}). For example with 2.7V input voltage and 20 mA LED current the maximum LED forward voltage is $2.7V - 100\text{ mV} = 2.6V$.

List of Recommended External Components

Symbol	Symbol Explanation	Value	Unit	Type
C_{IN}	VDD Bypass Capacitor	100	nF	Ceramic, X7R or X5R
R_{ISET}	Current Set Resistor for 20 mA LED Current	24	k Ω	1%
LED		User defined		

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5522TM/NOPB	ACTIVE	DSBGA	YFQ	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	6	Samples
LP5522TMX/NOPB	ACTIVE	DSBGA	YFQ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	6	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

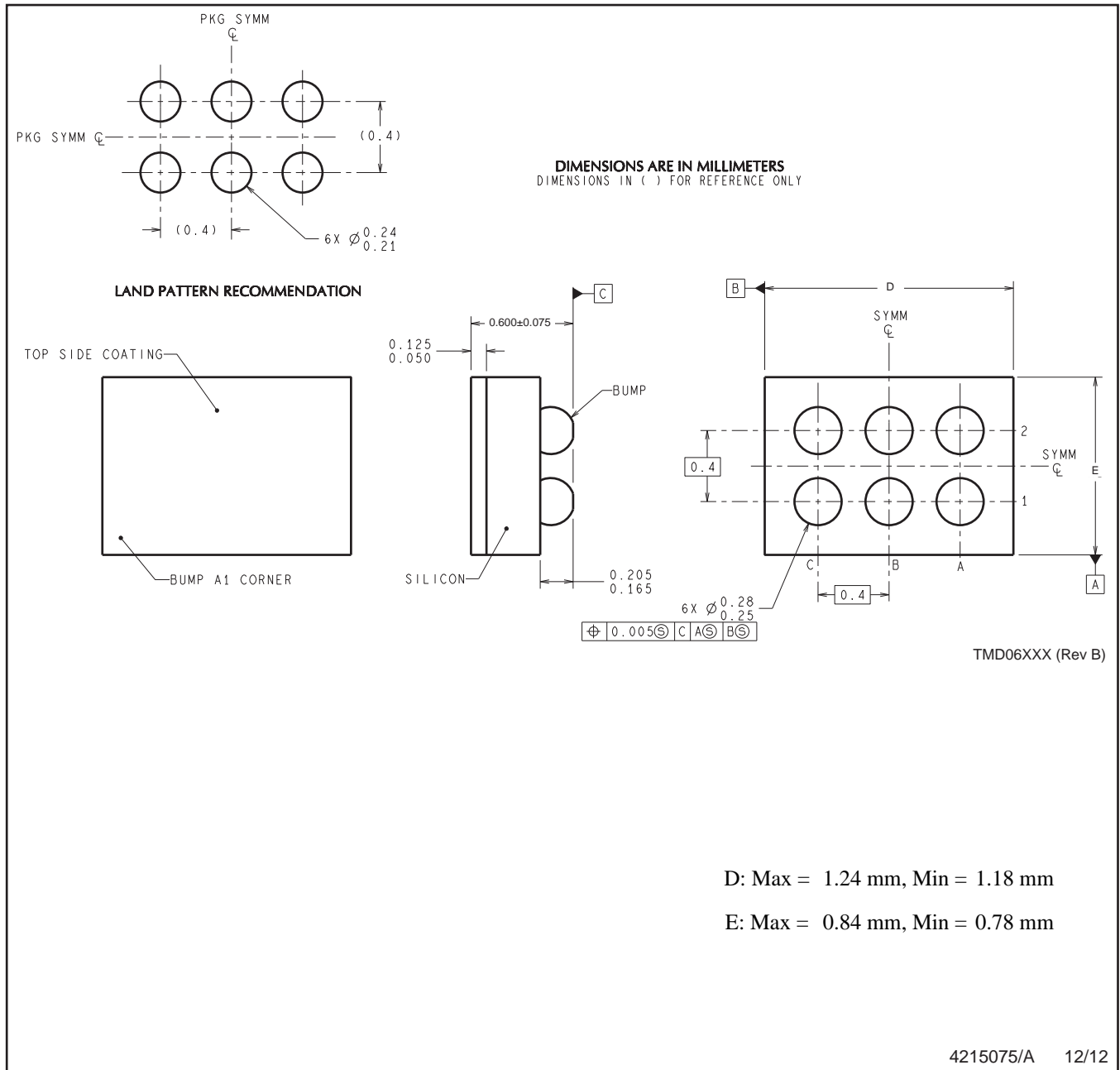
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5522TM/NOPB	DSBGA	YFQ	6	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5522TMX/NOPB	DSBGA	YFQ	6	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5522TM/NOPB	DSBGA	YFQ	6	250	208.0	191.0	35.0
LP5522TMX/NOPB	DSBGA	YFQ	6	3000	208.0	191.0	35.0

YFQ0006



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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