LP8774x Three Buck Converters and 5-V Boost for IWR Radar Sensors

1 Features

- Device operating temperature : –40°C to +125°C ambient
- Input voltage: 3.3 V nominal (3 V to 4 V range)
- Three low-noise step-down DC/DC converters:
  - Output voltage: 0.9 V to 1.9 V, 0.8 V (BUCK3), 0.82 V (BUCK3)
  - Maximum output current: 3 A/ 3 A/ 3 A
  - Switching frequency: 4.4 MHz, 8.8 MHz, and 17.6 MHz
- 5 V boost converter
  - Maximum output current: 350 mA
- 150 mA LDO
  - Output voltage 1.8 V or 3.3 V
- Output short-circuit and overload protection
- Input overvoltage protection (OVP) and undervoltage lockout (UVLO)
- Overtemperature warning and protection
- Serial peripheral interface (SPI)

2 Applications

- Factory automation & control
- Industrial transport (non-car & non-light truck)
- Low ripple, low noise applications

3 Description

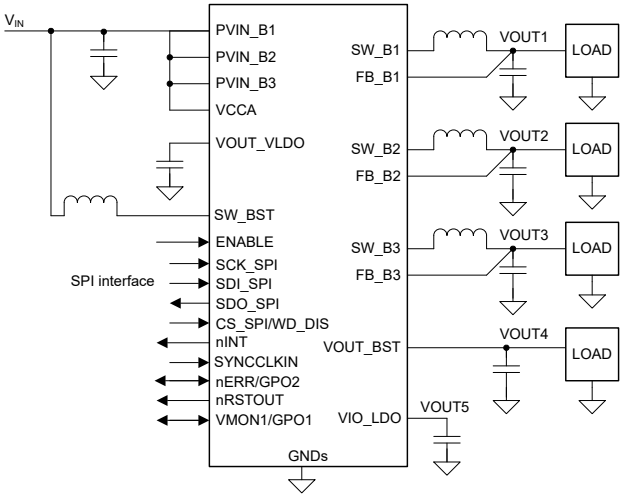
The LP8774x device is designed to meet the power management requirements of the IWR MMICs in various industrial radar applications. The device has three step-down DC/DC converters, a 5-V boost converter and a 1.8 V or 3.3 V LDO. The LDO is powered from the boost and intended for xWR I/O supply. An SPI serial interface and enable signals control the device.

The step-down DC/DC converters support programmable switching frequency of 4.4 MHz, 8.8 MHz, or 17.6 MHz. High switching frequency and low noise across wide frequency range enable LDO-free power solution with minimal or no passive filtering. The high switching frequency improves thermals and transient settling for the MMIC RF rails. The device forces the switching clock into PWM mode for optimal RF performance and can also be synchronized to an external clock. The device supports remote voltage sensing to compensate IR drop between the regulator output and the point-of-load (POL) which improves the accuracy of the output voltage.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)	BODY SIZE (NOM)
LP8774x	RXV (VQFN-HR, 28)	4.50 mm × 5.00 mm	4.50 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

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4 Description (continued)

The LP8774x device supports programmable start-up and shutdown delays and sequences which are synchronized to the ENABLE signal. The sequences can also include GPO signals to control external regulators, load switches, and processor reset. The default settings for the device are programmed into nonvolatile memory (NVM). The device controls the output slew rate to minimize output voltage overshoot and in-rush current during device start-up.

This data sheet applies to the superset device, including all register settings, as was validated and covers the following generic part number LP8774x with orderable part numbers **LP8774xyzzRXVR** where:

LP8774xyzzRXVR

- R: tape and reel (3000 units/reel) (other shipping options may be included in future as this field is not specific to device or functional safety performance)
- RXV: package designator
- zz: OTP part number variant: (A1, A3…etc.) (OTP determines the default register values for OTP based customer configuration registers)
- y = platform (Fsw and BOM/performance optimized options (1, 2, or 3) where
  - 1 : 17.6 MHz + full performance option or BOM/cost optimized option (radar)
  - 2 : 8.8 MHz + full performance option or BOM/cost optimized option (radar)
  - 3 : 4.4 MHz + full performance option (non-radar)
- x = regulator configuration of device version (specified by how many buck, boost and VIO LDO option is supported specific device version)
  - 2: 3 buck regulators, VIO LDO regulator
  - 3: 3 buck regulators
  - 4: 3 buck regulators, boost regulator
  - 5: 3 buck regulators, boost regulator, VIO LDO regulator
- LP8774: device family and base part number

5 Pin Configuration and Functions

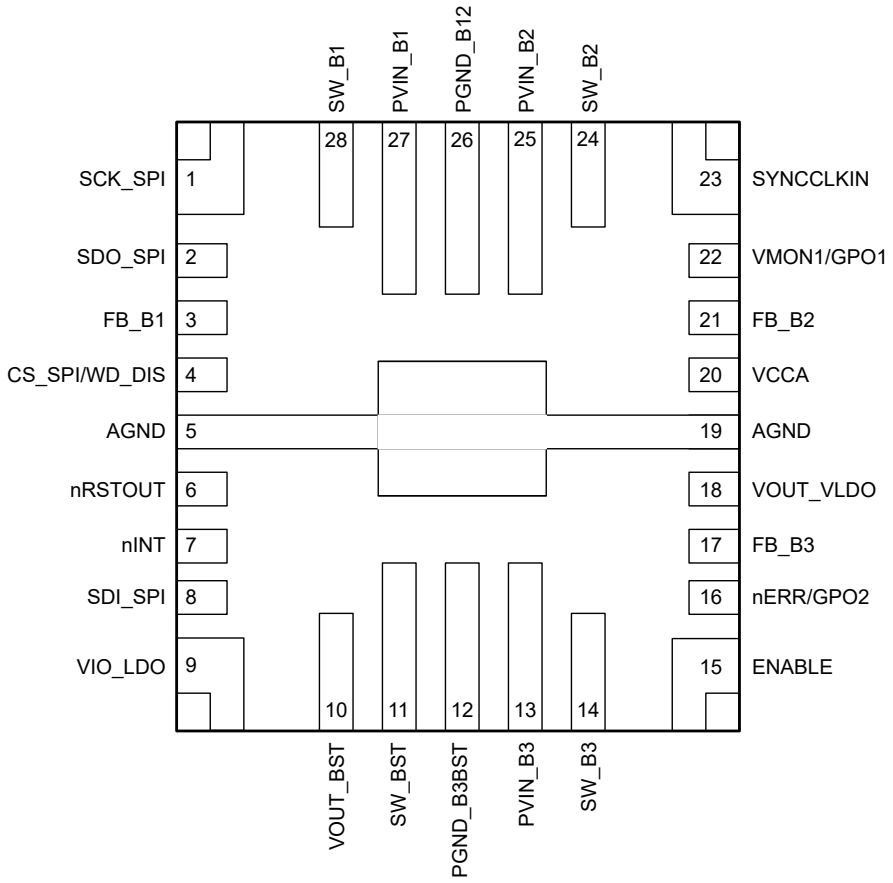

Figure 5-1. RXV Package, 28-Pin VQFN-HR (Top View)

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
SCK_SPI	1	I	Digital	Clock signal for SPI interface.	Ground
SDO_SPI	2	O	Digital	Output data signal for SPI interface.	Floating
FB_B1	3	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground
CS_SPI/ WD_DIS	4	I	Digital	Primary function: Chip select signal for SPI interface.	VCCA
		I	Digital	Alternative programmable function: Watchdog Deactivation Input.	Not applicable
AGND	5	—	Ground	Ground.	Ground
NRSTOUT	6	O	Digital	Reset output.	Floating
nINT	7	O	Digital	Interrupt output and CAN PHY control or both.	Floating
SDI_SPI	8	I	Digital	Input data signal for SPI interface.	Ground
VIO_LDO	9	—	Analog	IO supply from the internal LDO or from external source. LDO active: regulator filter node. LDO inactive: input for connecting to an external IO supply source, with input filtering capacitor placed.	Not applicable
VOUT_BST	10	—	Analog	BOOST active: BOOST output (internally connected as VIO_LDO input). BOOST inactive and VIO_LDO inactive: short with VIO_LDO. BOOST inactive and VIO_LDO active: input for connecting to an external supply used as VIO_LDO input.	External supply
SW_BST	11	—	Analog	When BOOST active: BOOST input. When BOOST inactive: short with VOUT_BST.	VOUT_BST

Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NAME	NO.				
PGND_B3BST	12	—	Ground	Power ground for BUCK3 and BOOST.	Ground
PVIN_B3	13	—	Power	Power input for BUCK3. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B3	14	—	Analog	BUCK3 switch node.	Floating
ENABLE	15	I	Digital	Programmable ENABLE signal.	Not applicable
nERR/GPO2	16	I	Digital	Primary function: System MCU Error Monitoring Input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO2).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT2).	Floating
FB_B3	17	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
VOUT_VLDO	18	—	Power	LDO regulator filter node. LDO is used for internal purposes. No external load allowed.	-
AGND	19	—	Ground	Ground.	Ground
VCCA	20	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bxx pins must be connected together in the application and be locally bypassed.	System supply
FB_B2	21	—	Analog	Output voltage feedback (positive) for BUCK2.	Ground
VMON1/ GPO1	22	—	Analog	Voltage monitoring input.	Ground
		O	Digital	Alternative programmable function: General Purpose Output signal (GPO1).	Floating
		O	Digital	Alternative programmable function: Fault Communication Output signal (FAULT1).	Floating
		O	Digital	Alternative programmable function: CAN PHY control (CAN_DIS).	Floating
SYNCCLKIN	23	I	Digital	External clock input.	Ground
SW_B2	24	—	Analog	BUCK2 switch node.	Floating
PVIN_B2	25	—	Power	Power input for BUCK2. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
PGND_B12	26	—	Ground	Power ground for BUCK1 and BUCK2.	Ground
PVIN_B1	27	—	Power	Power input for BUCK1. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
SW_B1	28	—	Analog	BUCK1 switch node.	Floating

6 Device and Documentation Support

6.1 Documentation Support

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.4 Trademarks

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6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Packaging Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
LP877451A1RXVR	ACTIVE	VQFN-HR	RXV	28	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	LP8774x 51A1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

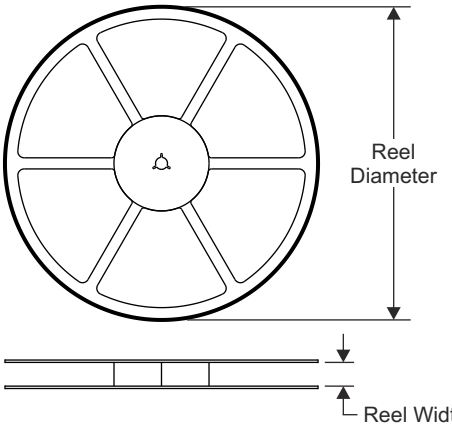
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

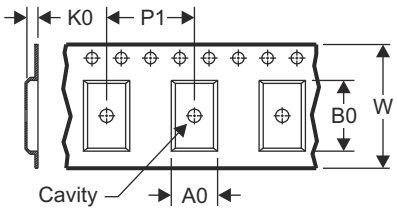
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

8.2 Tape and Reel Information

REEL DIMENSIONS

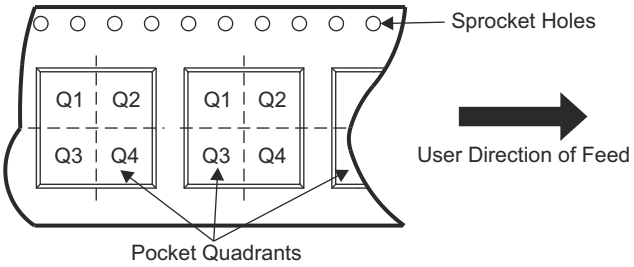


TAPE DIMENSIONS



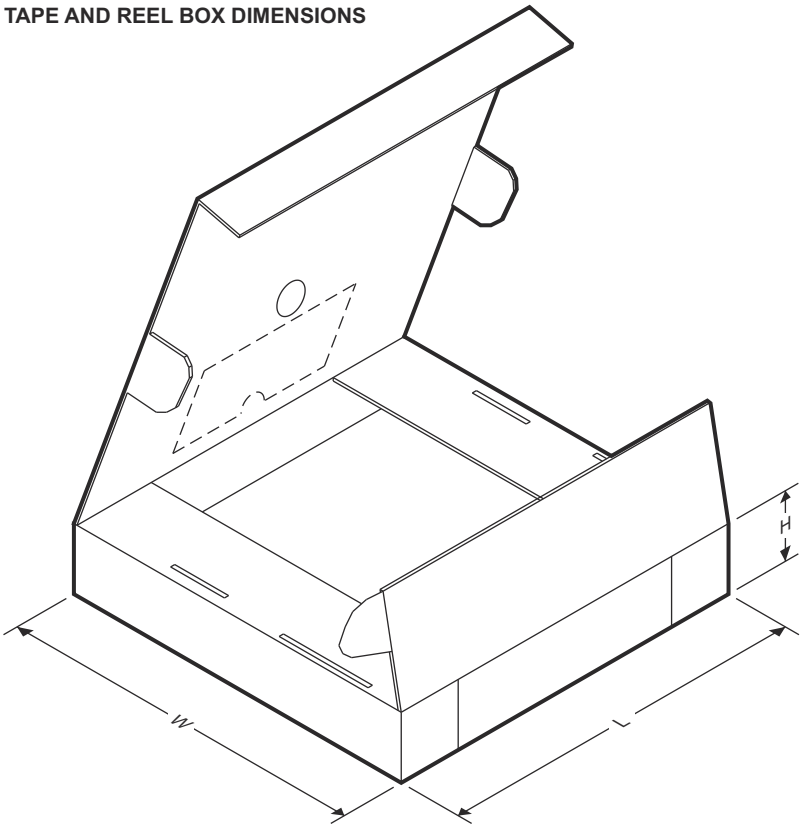
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP877451A1RXVR	VQFN-HR	RXV	28	3000	330	12.4	4.80	5.30	1.10	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



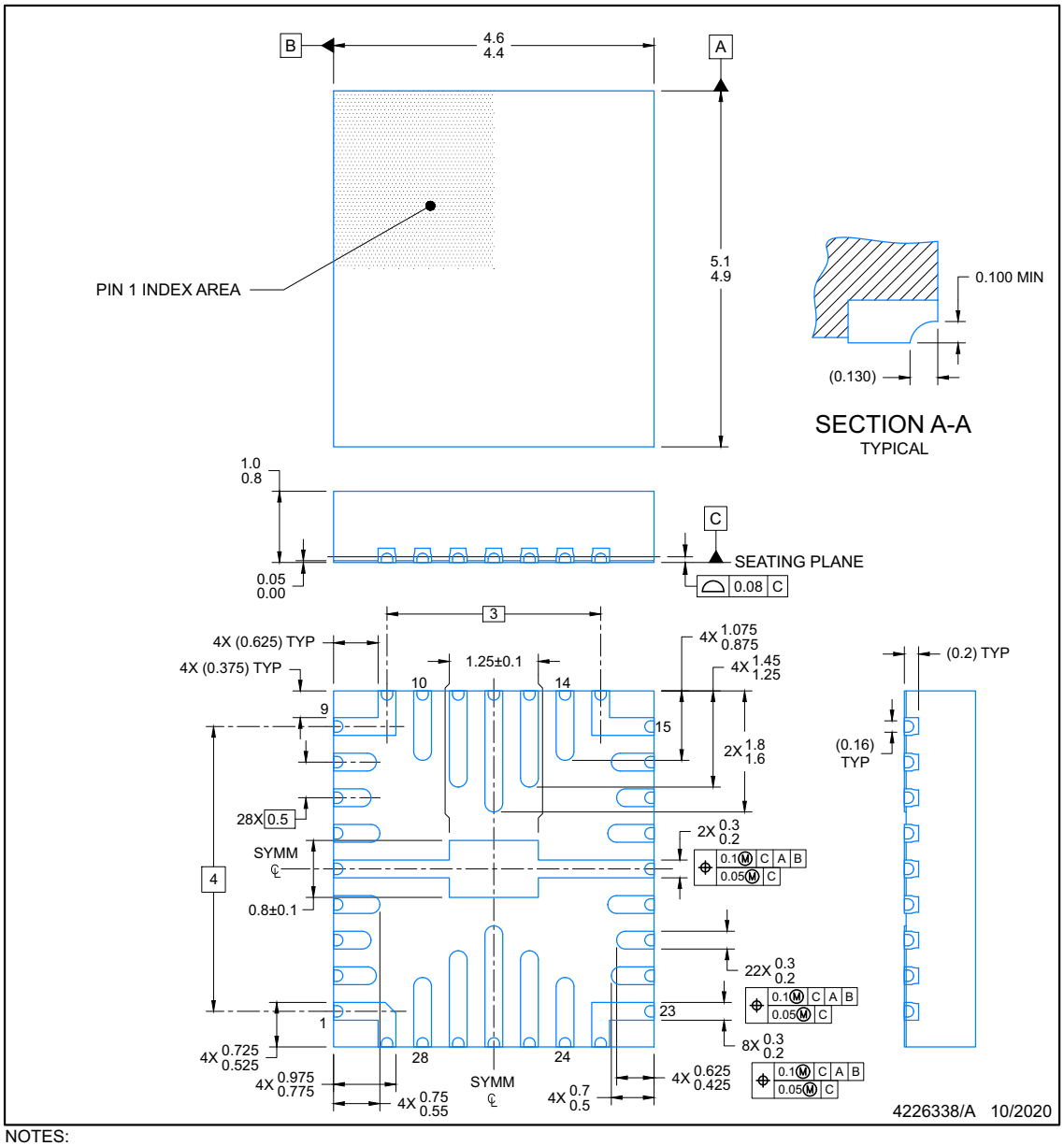
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP877451A1RXVR	VQFN-HR	RXV	28	3000	367	367	38

PACKAGE OUTLINE

RXV0028A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

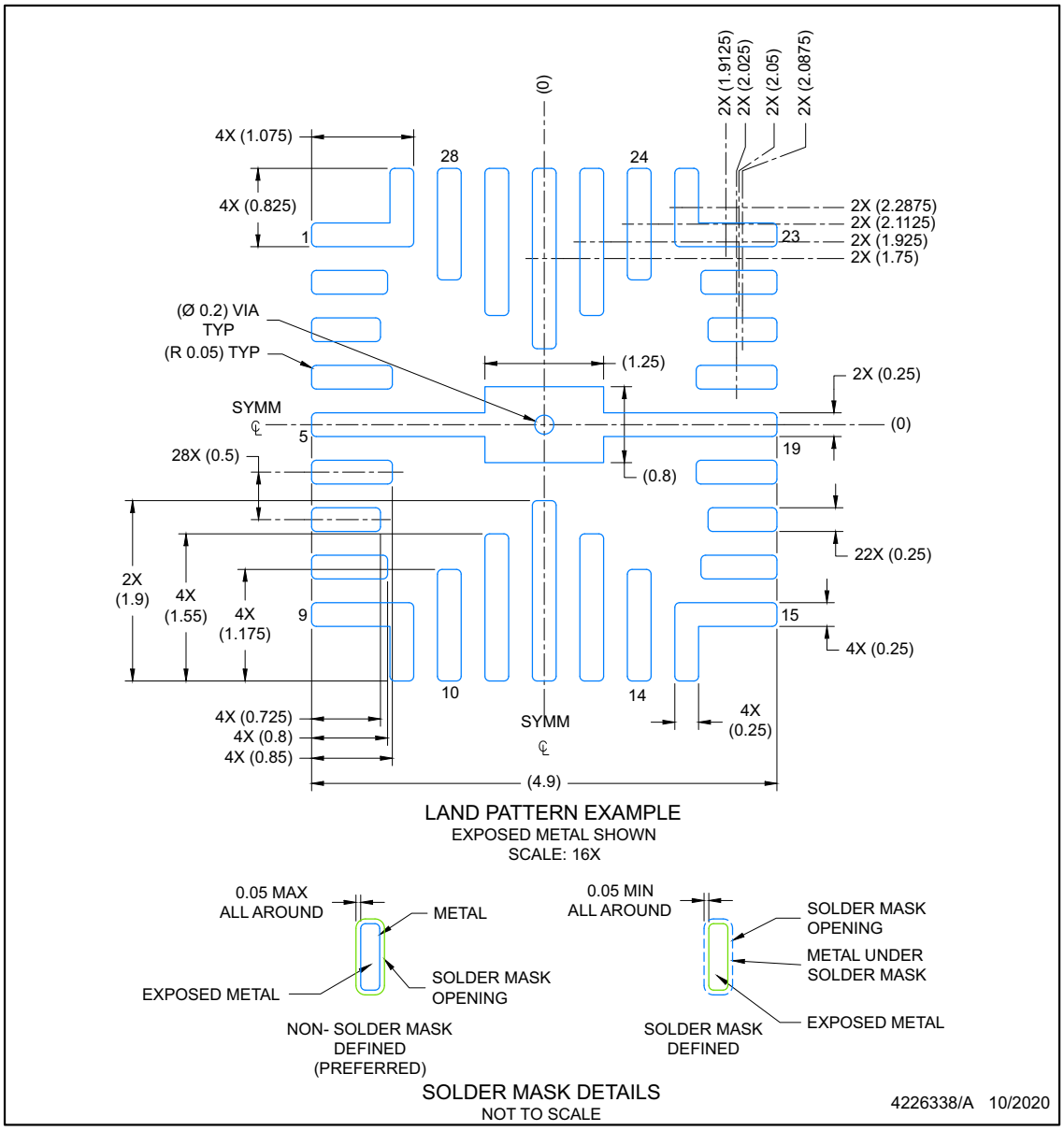
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RXV0028A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

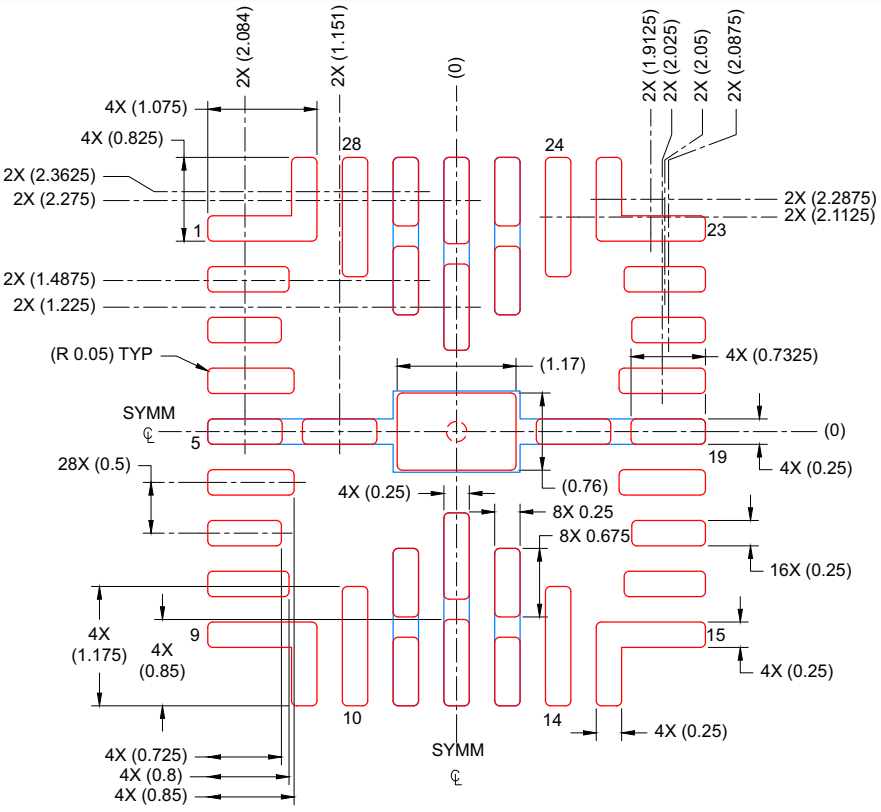
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RXV0028A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
FUSED PAD 5&19: 84%
PADS 11, 13, 25 & 27: 86%
PADS 12 & 26: 89%
SCALE: 16X

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NOTES: (continued)

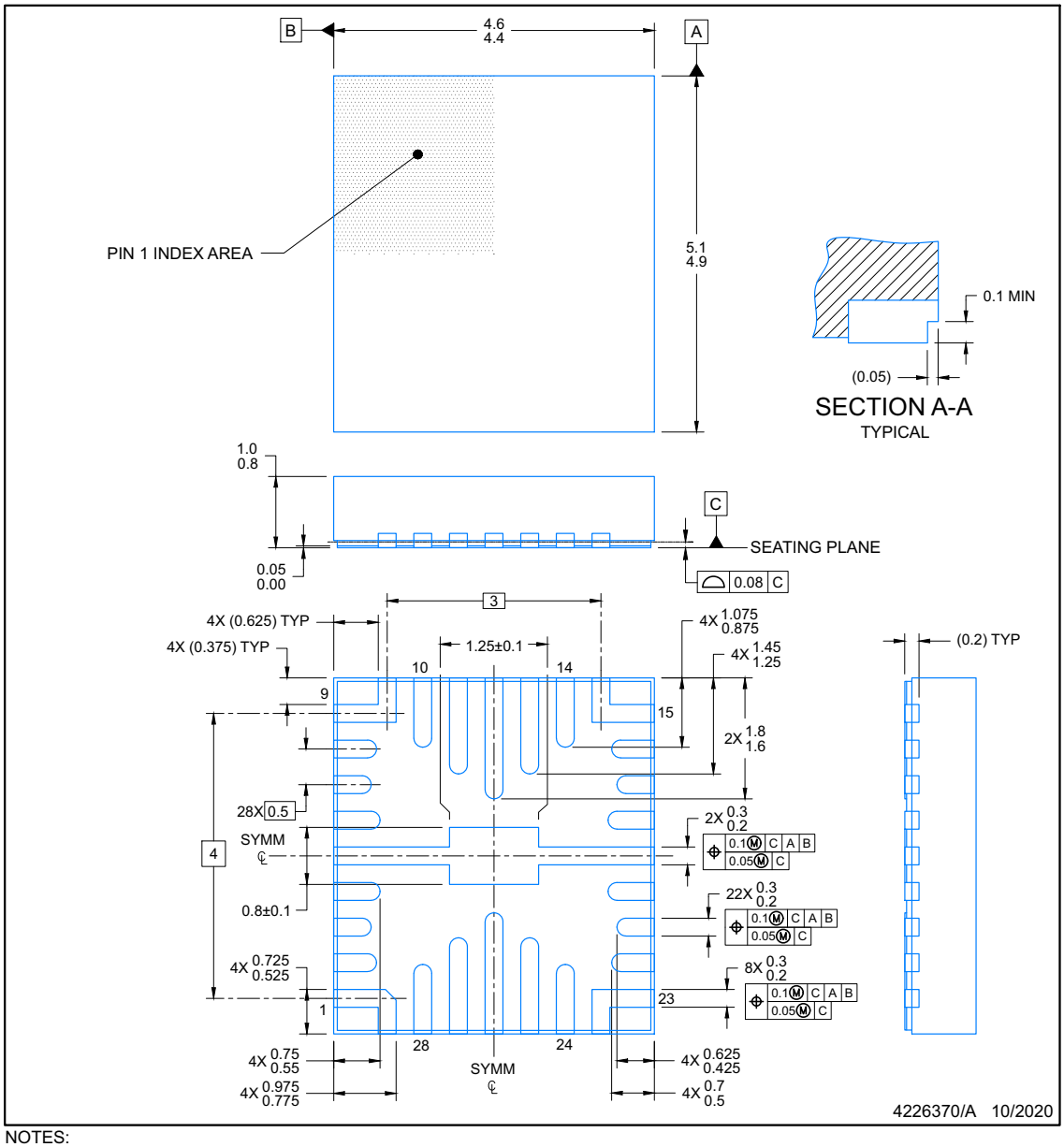
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RXV0028B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

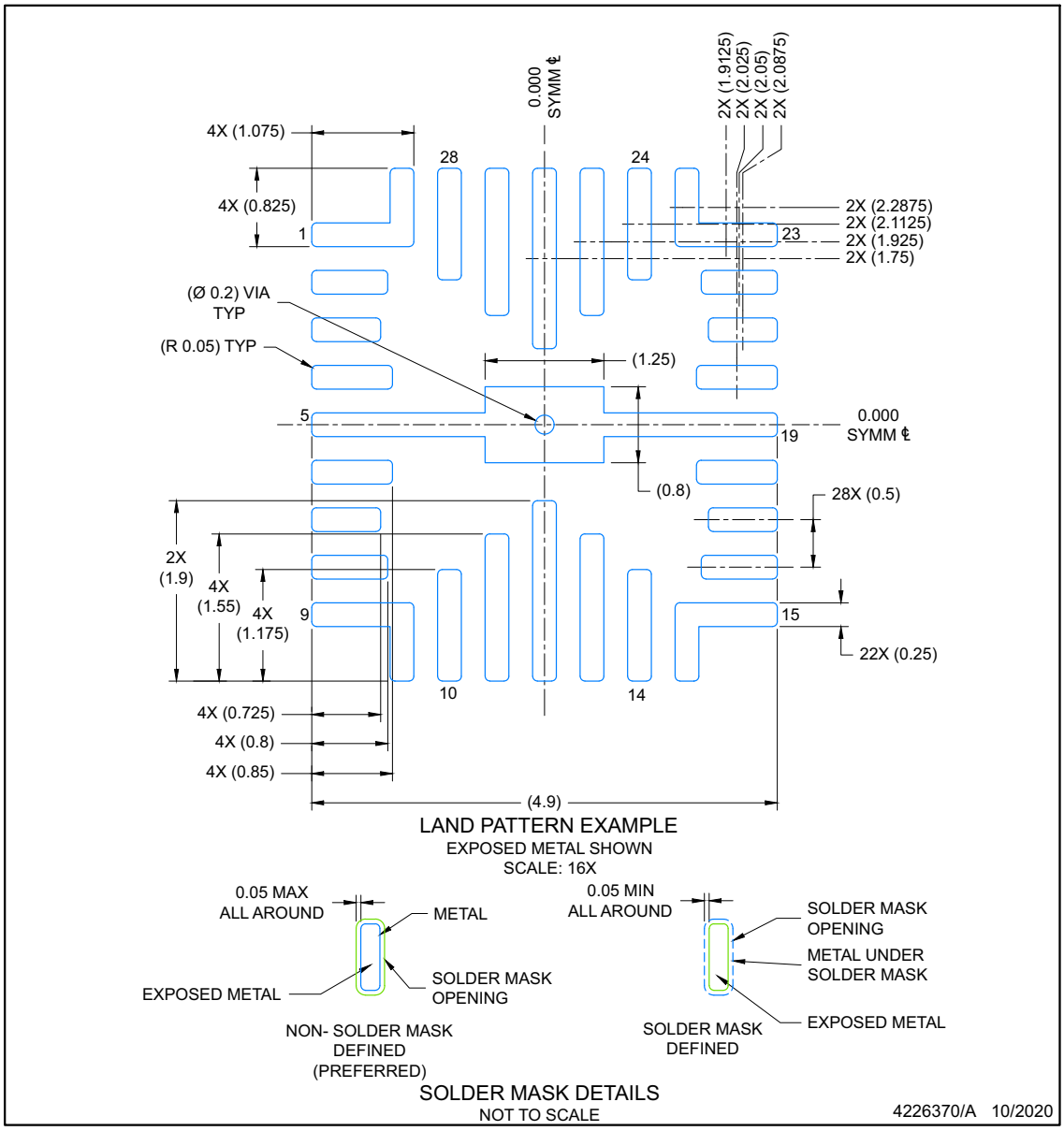
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RXV0028B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

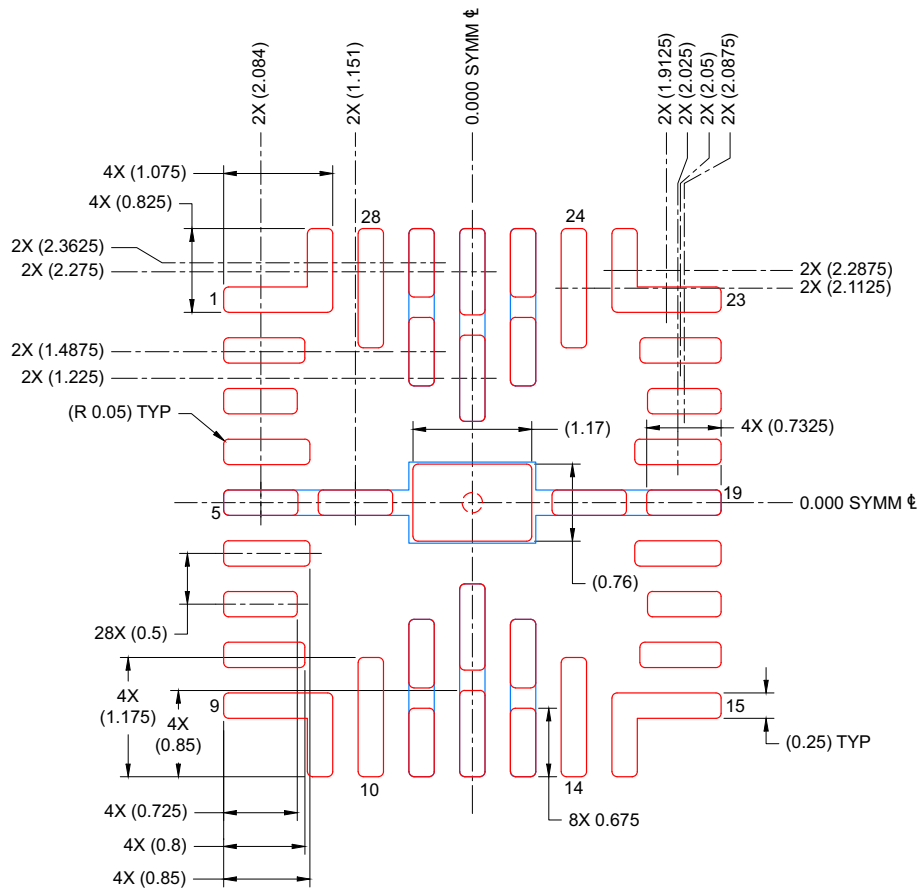
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RXV0028B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
FUSED PAD 5&19: 84%
PADS 11, 13, 25 & 27: 86%
PADS 12 & 26: 89%
SCALE: 16X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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