LT1054 Switched-Capacitor Voltage Converters With Regulators

1 Features
- Output Current, 100 mA
- Low Loss, 1.1 V at 100 mA
- Operating Range, 3.5 V to 15 V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Synchronization
- Devices Can Be Paralleled
- Pin-to-Pin Compatible With the LTC1044/7660

2 Applications
- Industrial Communications (RS232)
- Data Acquisition Supply
- Voltage Inverters
- Voltage Regulators
- Negative Voltage Doublers
- Positive Voltage Doublers

3 Description
The LT1054 device is a bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents.

Total voltage drop at 100-mA output current typically is 1.1 V. This applies to the full supply-voltage range of 3.5 V to 15 V. Quiescent current typically is 2.5 mA.

The LT1054 also provides regulation, a feature previously not available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 can also shut down by grounding the feedback terminal. Supply current in shutdown typically is 100 μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

The LT1054C is characterized for operation over a free-air temperature range of 0°C to 70°C. The LT1054I is characterized for operation over a free-air temperature range of −40°C to 85°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1054</td>
<td>PDIP (8)</td>
<td>9.50 mm × 6.35 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (16)</td>
<td>10.30 mm × 10.30 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2004) to Revision G Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1
5 Pin Configuration and Functions

### P Package
8-Pin PDIP
Top View

- **FB/SD** [1] 
- **CAP+** [2] 
- **GND** [3] 
- **CAP−** [4] 

### DW Package
16-Pin SOIC
Top View

- **FB/SD** [1] 
- **CAP+** [2] 
- **GND** [3] 
- **CAP−** [4] 

NC – No internal connection

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NAME</strong></td>
<td><strong>PDIP</strong></td>
<td><strong>SOIC</strong></td>
</tr>
<tr>
<td>FB/SD</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>CAP+</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>CAP−</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>VOUT</td>
<td>5</td>
<td>11</td>
</tr>
<tr>
<td>VREF</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>OSC</td>
<td>7</td>
<td>13</td>
</tr>
<tr>
<td>V_CC</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>1, 2, 7, 8, 9, 10, 15, 16</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>UI</td>
<td>0</td>
<td>UI</td>
</tr>
<tr>
<td>Tj</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>135</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The absolute maximum supply-voltage rating of 16 V is for unregulated circuits. For regulation-mode circuits with \( V_{OUT} \leq 15 \) V, this rating may be increased to 20 V.

(3) The devices are functional up to the absolute maximum junction temperature.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±500</td>
<td>V</td>
</tr>
<tr>
<td>±3500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>3.5</td>
<td>15 V</td>
</tr>
<tr>
<td>TA</td>
<td>0</td>
<td>70 °C</td>
</tr>
<tr>
<td></td>
<td>-40</td>
<td>85 °C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>LT1054</th>
</tr>
</thead>
<tbody>
<tr>
<td>P (PDIP)</td>
<td></td>
</tr>
<tr>
<td>16 PINS</td>
<td>57 °C/W</td>
</tr>
<tr>
<td>8 PINS</td>
<td>85 °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TA (1)</th>
<th>LT1054C, LT1054I</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VO</td>
<td>Regulated output voltage</td>
<td>VCC = 7 V, TJ = 25°C, RL = 500 Ω (3)</td>
<td>25°C</td>
<td>-4.7 -5 -5.2</td>
</tr>
<tr>
<td></td>
<td>Input regulation</td>
<td>VCC = 7 V to 12 V, RL = 500 Ω (3)</td>
<td>Full range</td>
<td>5 25</td>
</tr>
<tr>
<td></td>
<td>Output regulation</td>
<td>VCC = 7 V, RL = 100 Ω to 500 Ω (3)</td>
<td>Full range</td>
<td>10 50</td>
</tr>
<tr>
<td></td>
<td>Voltage loss, VCC −</td>
<td>VCC = 3.5 V to 15 V</td>
<td>Full range</td>
<td>15 25 35</td>
</tr>
<tr>
<td></td>
<td>VO (4)</td>
<td>C1 = C0 = 100-μF tantalum</td>
<td>I0 = 10 mA</td>
<td>0.35 0.55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I0 = 100 mA</td>
<td>1.1 1.6</td>
</tr>
<tr>
<td></td>
<td>Output resistance</td>
<td>ΔIO = 10 mA to 100 mA</td>
<td>See (5)</td>
<td>10 15</td>
</tr>
<tr>
<td>ref</td>
<td>Reference voltage</td>
<td>VCC = 7 V, RL = 100 Ω to 500 Ω (3)</td>
<td>Full range</td>
<td>2.25 2.75</td>
</tr>
<tr>
<td>ref</td>
<td>Supply current</td>
<td>I0 = 0</td>
<td>VCC = 3.5 V</td>
<td>2.5 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VCC = 15 V</td>
<td>3 200</td>
</tr>
<tr>
<td>ref</td>
<td>Supply current in shutdown</td>
<td>VCC = 0 V</td>
<td>Full range</td>
<td>100</td>
</tr>
<tr>
<td>ref</td>
<td>Voltage loss, VCC −</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ref</td>
<td>Output resistance</td>
<td>ΔIO = 10 mA to 100 mA</td>
<td>See (5)</td>
<td>10 15</td>
</tr>
<tr>
<td>ref</td>
<td>Oscillator frequency</td>
<td>VCC = 3.5 V to 15 V</td>
<td>Full range</td>
<td>15 25 35</td>
</tr>
<tr>
<td>ref</td>
<td>Reference voltage</td>
<td>VCC = 7 V, RL = 100 Ω to 500 Ω (3)</td>
<td>Full range</td>
<td>2.25 2.75</td>
</tr>
<tr>
<td>ref</td>
<td>Supply current</td>
<td>I0 = 0</td>
<td>VCC = 3.5 V</td>
<td>2.5 5</td>
</tr>
<tr>
<td>ref</td>
<td>Supply current in shutdown</td>
<td>VCC = 0 V</td>
<td>Full range</td>
<td>100</td>
</tr>
</tbody>
</table>

(1) Full range is 0°C to 70°C for the LT1054C and −40°C to 85°C for the LT1054I.
(2) All typical values are at TA = 25°C.
(3) All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor CIN = 10 μF (tantalum), external capacitor COUT = 100 μF (tantalum) and C1 = 0.002 μF (see ).
(4) For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. CIN and COUT are external capacitors.
(5) Output resistance is defined as the slope of the curve (ΔVO versus ΔIO) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.
6.6 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature range.

Table 1. Table of Graphs

<table>
<thead>
<tr>
<th>Shutdown threshold voltage</th>
<th>vs Free-air temperature</th>
<th>Figure 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td>vs Input voltage</td>
<td>Figure 2</td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>vs Free-air temperature</td>
<td>Figure 3</td>
</tr>
<tr>
<td>Supply current in shutdown</td>
<td>vs Input voltage</td>
<td>Figure 4</td>
</tr>
<tr>
<td>Average supply current</td>
<td>vs Output current</td>
<td>Figure 5</td>
</tr>
<tr>
<td>Output voltage loss</td>
<td>vs Input capacitance</td>
<td></td>
</tr>
<tr>
<td>Output voltage loss</td>
<td>vs Oscillator frequency (10 µF)</td>
<td>Figure 7</td>
</tr>
<tr>
<td>Output voltage loss</td>
<td>vs Oscillator frequency (100 µF)</td>
<td>Figure 8</td>
</tr>
<tr>
<td>Regulated output voltage</td>
<td>vs Free-air temperature</td>
<td>Figure 9</td>
</tr>
<tr>
<td>Reference voltage change</td>
<td>vs Free-air temperature</td>
<td>Figure 10</td>
</tr>
<tr>
<td>Voltage loss</td>
<td>vs Output current</td>
<td>Figure 17</td>
</tr>
</tbody>
</table>

Figure 1. Shutdown Threshold Voltage vs Free-Air Temperature

Figure 2. Supply Current vs Input Voltage
Figure 9. Regulated Output Voltage vs Free-air Temperature

Figure 10. Reference Voltage Change vs Free-air Temperature
7 Detailed Description

7.1 Overview

LT1054 is a “negative voltage generator” or “negative charge pump” that will output a negative voltage that is proportional to the input voltage (or \(V_{CC}\)). With proper supply voltage, \(V_{OUT}\) will regulate to an unregulated \(V_{OUT}\) that is approximately \(-V_{CC}\) (reduced by a small voltage loss). If a lower absolute voltage is desired, \(V_{OUT}\) can be regulated to that value when proper feedback resistors are applied.

LT1054 regulates up to 100mA with minimal loss and has a shutdown mode that makes this part optimal across a wide range of applications.

7.2 Functional Block Diagram

![Block Diagram of LT1054](image)

† External capacitors

Pin numbers shown are for the P package.

7.3 Feature Description

7.3.1 Reference and Error Amplifier for Regulation

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both \(C_{IN}\) and \(C_{OUT}\) are discharged through the output load. Quiescent current in shutdown drops to approximately 100 µA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (\(C_{OUT}\)) has fully discharged. For most applications, where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (\(C_{OUT}\)) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 11, the restart signal can be either a pulse (\(t_p > 100 \mu s\)) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider \(R3/R4\) shown in Figure 11 should be chosen to provide a signal level at FB/SD of 0.7–1.1 V.

FB/SD also is the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.
7.3.2 External Oscillator Synchronization

This pin can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally Pin 7 is connected to the oscillator timing capacitor (Ct ≈ 150pF) which is alternately charged and discharged by current sources of ±7µA so that the duty cycle is ≈50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be lowered by adding an external capacitor (C1, Figure 12) from Pin 7 to ground. This will increase the charge and discharge times which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C2, Figure 12, in the range of 5pF to 20pF) from Pin 2 to Pin 7. This capacitor will couple charge into CT at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to
Feature Description (continued)

the reference pin (Pin 6). A 20k pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 12. Pulling up Pin 7 to an external voltage is not recommended. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R1/R2 divider allowing Pin 6 to be used as a pullup point for Pin 7.

7.3.3 Output Current and Voltage Loss

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, \( |V_{OUT}| \) referenced to the ground terminal of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler, can provide higher voltages at reduced output currents.

7.3.4 Reference Voltage

Reference Output. This pin provides a 2.5V reference point for use in LT1054-based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60µA. The reference pin will draw ≈100µA when shorted to ground and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

7.4 Device Functional Modes

7.4.1 Main Operation

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 13 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is \( q_1 = C_1 \cdot V_1 \). When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is \( q_2 = C_1 \cdot V_2 \). The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is shown in Equation 1.

\[
\Delta q = q_1 - q_2 = C_1(V_1 - V_2)
\]

If the switch is cycled \( f \) times per second, the charge transfer per unit time (that is, current) is as shown in Equation 2.
\[
I = f \times \frac{\Delta q}{1} = f \times C_1(1 - V_2)
\]

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in Equation 3.
\[
I = \frac{V_1 - V_2}{(1 / f C_1)} = \frac{V_1 - V_2}{R_{EQUIV}}
\]
Device Functional Modes (continued)

A new variable, $R_{\text{EQUIV}}$, is defined as $R_{\text{EQUIV}} = 1 / (f \times C_1)$. The equivalent circuit for the switched-capacitor network is shown in Figure 14. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

![Circuit Diagram](Figure 14. Switched-Capacitor Equivalent Circuit)

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance eventually is dominated by the $1 / (f \times C_1)$ term, and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to operate in the frequency band where voltage losses are at a minimum.

7.4.2 Shutdown

LT1054 can be put into a low quiescent current state by grounding the FB/SD pin. Once FB/SD is pulled low, current being drawn from the supply will be approximately 100 µA.
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The negative voltage converting and regulating ability of the LT1054 make this device optimal across a wide range of applications. As it is a regulator, there are many general design considerations that must be taken into account. Below will describe what to consider for using this device as a basic voltage inverter/regulator. This is the most common application for the LT1054 and the fundamental building block for the applications shown in System Examples.

8.2 Typical Application

![Figure 15. Basic Voltage Inverter/Regulator](image)

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Example Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>3.5V to 15V</td>
</tr>
<tr>
<td>V\text{OUT}</td>
<td>-5V</td>
</tr>
<tr>
<td>I\text{OUT}</td>
<td>100mA</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

When using LT1054 as a basic voltage inverter, determine the following:

- Input Voltage
- Desired output Voltage
- Desired Ripple
- Power Dissipation

8.2.2.1 Output Voltage Programming

The error amplifier of the LT1054 drives the PNP switch to control the voltage across the input capacitor ($C_{IN}$), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. Shows the basic regulator configuration and the formula for calculating the appropriate resistor values. $R_1$ should be $20 \, \Omega$ or greater because the reference current is limited to $\pm 100 \, \mu A$. $R_2$ should be in the range of $100 \, k\Omega$ to $300 \, k\Omega$.

8.2.2.2 Capacitor Selection

While the exact values of $C_{IN}$ and $C_{OUT}$ are noncritical, good-quality low-ESR capacitors, such as solid tantalum, are necessary to minimize voltage losses at high currents. For $C_{IN}$, the effect of the ESR of the capacitor is multiplied by four, because switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with $1 \, \Omega$ of ESR for $C_{IN}$ has the same effect as increasing the output impedance of the LT1054 by $4 \, \Omega$. This represents a significant increase in the voltage losses. $C_{OUT}$ alternately is charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

Frequency compensation is accomplished by adjusting the ratio of $C_{IN}$ to $C_{OUT}$.

For best results, this ratio should be approximately 1:10. Capacitor $C_1$, required for good load regulation, should be 0.002 $\mu F$ for all output voltages.

8.2.2.3 Output Ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as:

$$\Delta V = \frac{I_{OUT}}{2f_{OSC}}$$

where

- $\Delta V$ = peak-to-peak ripple
- $f_{OSC}$ = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$\left(2I_{OUT}\times\text{ESR of } C_{OUT}\right)$$

8.2.2.4 Power Dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction-temperature ratings. The total power dissipation is calculated from two components—the power loss due to voltage drops in the switches, and the power loss due to drive-current losses. The total power dissipated by the LT1054 is calculated as:

$$P = (V_{CC} - V_{OUT}) \times I_{OUT} + (V_{CC})(I_{OUT})(0.2)$$

where

- both $V_{CC}$ and $V_{OUT}$ are referenced to ground
The power dissipation is equivalent to that of a linear regulator. Limited power-handling capability of the LT1054 packages causes limited output-current requirements, or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with \( C_{\text{IN}} \) as shown in Figure 16. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when \( C_{\text{IN}} \) is both charging and discharging, the resistor chosen is as shown:

\[
R_x = \frac{V_x}{4.4 \, I_{\text{OUT}}}
\]

where

- \( V_x = V_{\text{CC}} - [(\text{LT1054 voltage loss})(1.3) + |V_{\text{OUT}}|] \)
- \( I_{\text{OUT}} \) = maximum required output current

The factor of 1.3 allows some operating margin for the LT1054.

When using a 12-V to -5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

\[
P = (12 \, V - | -5 \, V |)(100 \, mA) + (12 \, V)(100 \, mA)(0.2)
P = 700 \, mW + 240 \, mW = 940 \, mW
\] (8)

At \( R_{\text{JA}} \) of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C occurs. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor \( R_x \), determine how much voltage can be dropped across \( R_x \). The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

\[
V_x = 12 \, V - [(1.6 \, V)(1.3) + | -5 \, V |] = 4.9 \, V
\] (9)

and

\[
R_x = \frac{4.9 \, V}{(4.4)(100 \, mA)} = 11 \, \Omega
\] (10)
The resistor reduces the power dissipated by the LT1054 by \((4.9 \text{ V})(100 \text{ mA}) = 490 \text{ mW}\). The total power dissipated by the LT1054 is equal to \((940 \text{ mW} - 490 \text{ mW}) = 450 \text{ mW}\). The junction-temperature rise is \(58^\circ\text{C}\). Although commercial devices are functional up to a junction temperature of \(125^\circ\text{C}\), the specifications are tested to a junction temperature of \(100^\circ\text{C}\). In this example, this means limiting the ambient temperature to \(42^\circ\text{C}\). To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers, with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide printed circuit board traces from the LT1054 leads help remove heat from the device. This is especially true for plastic packages.

### 8.2.3 Application Curve

![Voltage Loss vs Output Current](image.png)

**Figure 17. Voltage Loss vs Output Current**

### 8.3 System Examples

![Motor-Speed Servo](image.png)

**Figure 18. Motor-Speed Servo**

NOTE: Motor-Tach is Canon CKT26-T5-3SAE.

Pin numbers shown are for the P package.
System Examples (continued)

**Figure 19. Negative-Voltage Doubler**

VIN = −3.5 V to −15 V  
VOUT = 2 VIN + (LT1054 Voltage Loss) + (QX Saturation Voltage)

Pin numbers shown are for the P package.

**Figure 20. Positive-Voltage Doubler**

VIN = 3.5 V to 15 V  
VOUT = 2 VIN − (VL + 2 VDiode)  
VL = LT1054 Voltage Loss

Pin numbers shown are for the P package.
System Examples (continued)

**Figure 21. 100-mA Regulating Negative Doubler**

+ $V_{IN} = 3.5 \text{ V to } 15 \text{ V}$
+ $V_{OUT \ MAX} = -2 \ V_{IN} + [LT1054 \ Voltage \ Loss + 2 (V_{Diode})]$

$$R_2 = R_1 \left( \frac{|V_{OUT}|}{V_{REF} - 40 \text{ mV}} + 1 \right) = R_1 \left( \frac{|V_{OUT}|}{1.21 \text{ V}} + 1 \right)$$

Pin numbers shown are for the P package.

**Figure 22. Dual-Output Voltage Doubler**

+ $V_{I} = 3.5 \text{ V to } 15 \text{ V}$
+ $+V_O = 2 \ V_{IN} - (V_L + 2 \ V_{Diode})$  
+ $-V_O = -2 \ V_I + (V_L + 2 \ V_{Diode})$
+ $V_L = LT1054 \ Voltage \ Loss$

Pin numbers shown are for the P package.
System Examples (continued)

Pin numbers shown are for the P package.

Figure 23. 5-V to ±12-V Converter

Pin numbers shown are for the P package.

Figure 24. Strain-Gage Bridge Signal Conditioner
System Examples (continued)

\[ R_2 = R_1 \left( \frac{|V_{\text{OUT}}|}{V_{\text{REF}}/2 - 40 \text{ mV}} + 1 \right) = R_1 \frac{|V_{\text{OUT}}|}{1.21 \text{ V} + 1} \]

Pin numbers shown are for the P package.

Figure 25. 3.5-V to 5-V Regulator
System Examples (continued)

Figure 26. Regulating 200-mA +12-V to −5-V Converter

Figure 27. Digitally Programmable Negative Supply
System Examples (continued)

Pin numbers shown are for the P package.

**Figure 28. Positive Doubler With Regulation (5-V to 8-V Converter)**

Pin numbers shown are for the P package.

**Figure 29. Negative Doubler With Regulator**
9 Power Supply Recommendations

The LT1054 alternately charges $C_{IN}$ to the input voltage when $C_{IN}$ is switched in parallel with the input supply and then transfers charge to $C_{OUT}$ when $C_{IN}$ is switched in parallel with $C_{OUT}$. Switching occurs at the oscillator frequency. During the time that $C_{IN}$ is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that $C_{IN}$ is delivering charge to $C_{OUT}$, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054 and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2µF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example, when the actual input supply is connected to the LT1054 through long leads, or when the pulse current drawn by the LT1054 might affect other circuitry through supply coupling.

In addition to being the output terminal, $V_{OUT}$ is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making $V_{OUT}$ positive with respect to any of the other terminals. For circuits with the output load connected from $V_{CC}$ to $V_{OUT}$ or from some external positive supply voltage to $V_{OUT}$, an external transistor must be added (see Figure 30). This transistor prevents $V_{OUT}$ from being pulled above GND during startup. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{(V_{OUT})^3}{I_{OUT}}$$

(11)

Figure 30. Circuit With Load Connected from $V_{CC}$ to $V_{OUT}$
10 Layout

10.1 Layout Guidelines

- Try to run the feedback trace as far from the noisy power or clocking traces as possible. In the case that the OSC pin is not being used, as in Figure 31, the FB trace can be run on a lower layer under the OSC pin. When OSC is being utilized by a noisy clocking signal, it is recommended to run the FB trace on a lower layer through the Vref pin.
  - Keep the FB trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from EMI and other noise sources is the more critical of the two.
- Keep the external capacitor traces short, specifically on the CAP+ and CAP- nodes that have the fastest rise and fall times.
- Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.

10.2 Layout Example

Figure 31. Basic Inverter/Regulator Layout
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>-40 to 85</td>
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(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**
- Reel Diameter
- Reel Width (W1)

**REEL DIMENSIONS**
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**TAPE DIMENSIONS**
- Pocket Quadrants
- Cavity
- Sprocket Holes
- User Direction of Feed

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

---

**Table: Tape and Reel Information**

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<th>Package Type</th>
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*All dimensions are nominal*
TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
## TUBE

*T - Tube height

*W - Tube width

*B - Alignment groove width

*All dimensions are nominal

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This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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