MAX202 5-V Dual RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- ESD Protection for RS-232 Bus Pins: ±15-kV Human-Body Model
- Operates at 5-V V_{CC} Supply
- Operates Up to 120 kbit/s
- Two Drivers and Two Receivers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications
- Battery-Powered Systems
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

3 Description
The MAX202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of 30-V/\mu s driver output slew rate.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX202CD</td>
<td>SOIC (16)</td>
<td>9.90 mm x 3.91 mm</td>
</tr>
<tr>
<td>MAX202ID</td>
<td>SOIC WIDE (16)</td>
<td>10.30 mm x 7.50 mm</td>
</tr>
<tr>
<td>MAX202CPW</td>
<td>TSSOP (16)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

```
5 V

POWER

DIN 2

TX

2

DOUT

RS-232

120 kbit/s

15 kV HBM

ROUT 2

RX

2

RIN

RS-232
```
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2007) to Revision F

Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .................................................................................. 1

• Removed the Ordering Information table; see POA at the end of the data sheet ................................................................. 1

• Changed values in the Thermal Information table to align with JEDEC standards .......................................................... 4

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# 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1+</td>
<td>—</td>
<td>Positive lead of C1 capacitor</td>
</tr>
<tr>
<td>2</td>
<td>V+</td>
<td>O</td>
<td>Positive charge pump output for storage capacitor only</td>
</tr>
<tr>
<td>3</td>
<td>C1−</td>
<td>—</td>
<td>Negative lead of C1 capacitor</td>
</tr>
<tr>
<td>4</td>
<td>C2+</td>
<td>—</td>
<td>Positive lead of C2 capacitor</td>
</tr>
<tr>
<td>5</td>
<td>C2−</td>
<td>—</td>
<td>Negative lead of C2 capacitor</td>
</tr>
<tr>
<td>6</td>
<td>V−</td>
<td>O</td>
<td>Negative charge pump output for storage capacitor only</td>
</tr>
<tr>
<td>7</td>
<td>DOUT2</td>
<td>O</td>
<td>RS-232 line data output (to remote RS-232 system)</td>
</tr>
<tr>
<td>8</td>
<td>RIN2</td>
<td>I</td>
<td>RS-232 line data input (from remote RS-232 system)</td>
</tr>
<tr>
<td>9</td>
<td>ROUT2</td>
<td>O</td>
<td>Logic data output (to UART)</td>
</tr>
<tr>
<td>10</td>
<td>DIN2</td>
<td>I</td>
<td>Logic data input (from UART)</td>
</tr>
<tr>
<td>11</td>
<td>DIN1</td>
<td>I</td>
<td>Logic data input (from UART)</td>
</tr>
<tr>
<td>12</td>
<td>ROUT1</td>
<td>O</td>
<td>Logic data output (to UART)</td>
</tr>
<tr>
<td>13</td>
<td>RIN1</td>
<td>I</td>
<td>RS-232 line data input (from remote RS-232 system)</td>
</tr>
<tr>
<td>14</td>
<td>DOUT1</td>
<td>O</td>
<td>RS-232 line data output (to remote RS-232 system)</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>—</td>
<td>Supply voltage, connect to external 5-V power supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{CC})(^{(2)})</td>
<td>(-0.3)</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Positive charge pump voltage, (V_+)(^{(2)})</td>
<td>(V_{CC} - 0.3)</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>Negative charge pump voltage, (V_-)(^{(2)})</td>
<td>(-14)</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, (V_I) (Drivers)</td>
<td>(-0.3)</td>
<td>(V_+ + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Receivers)</td>
<td>(\pm 30)</td>
<td></td>
</tr>
<tr>
<td>Output voltage, (V_O) (Drivers)</td>
<td>(V_- - 0.3)</td>
<td>(V_+ + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Receivers)</td>
<td>(-0.3)</td>
<td>(V_{CC} + 0.3)</td>
</tr>
<tr>
<td>Short-circuit duration, (D_{OUT})</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>(-65)</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>Pins 7, 8, 13, and 14</td>
<td>(\pm 15000)</td>
</tr>
<tr>
<td>All other pins</td>
<td>(\pm 2000)</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>(\pm 1500)</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted\(^{(1)}\); see Figure 10)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH}) Driver high-level input voltage ((D_{IN}))</td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{IL}) Driver low-level input voltage ((D_{IN}))</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_I) Driver input voltage ((D_{IN}))</td>
<td></td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Receiver input voltage</td>
<td>(-30)</td>
<td></td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>MAX202C</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>MAX202I</td>
<td>(-40)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Test conditions are \(C1–C4 = 0.1 \mu F\) at \(V_{CC} = 5 V \pm 0.5 V\).

6.4 Thermal Information

| THERMAL METRIC\(^{(1)}\) | MAX202 |
|-------------------------|--------|--------|
| \(R_{JA}\) Junction-to-ambient thermal resistance | 76.2 | 76.8 | 101 | °C/W |
| \(R_{JC(top)}\) Junction-to-case (top) thermal resistance | 36.8 | 39.6 | 36.4 | °C/W |
| \(R_{JB}\) Junction-to-board thermal resistance | 33.9 | 41.5 | 45.9 | °C/W |
| \(\psi_{JT}\) Junction-to-top characterization parameter | 6.7 | 12.6 | 2.7 | °C/W |
| \(\psi_{JB}\) Junction-to-board characterization parameter | 33.6 | 40.9 | 45.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see Figure 10)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(^{(2)})</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I(_{CC})</td>
<td>Supply current</td>
<td>No load, V(_{CC}) = 5 V</td>
<td>8</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td><strong>DRIVER SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{OH})</td>
<td>High-level output voltage</td>
<td>D(_{OUT}) at R(<em>L) = 3 k(\Omega) to GND, D(</em>{IN}) = GND</td>
<td>5</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td>V(_{DL})</td>
<td>Low-level output voltage</td>
<td>D(<em>{OUT}) at R(<em>L) = 3 k(\Omega) to GND, D(</em>{IN}) = V(</em>{CC})</td>
<td>−5</td>
<td>−9</td>
<td>V</td>
</tr>
<tr>
<td>I(_{IH})</td>
<td>High-level input current</td>
<td>V(<em>{I\text{IN}}) = V(</em>{CC})</td>
<td>0</td>
<td>200</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>I(_{IL})</td>
<td>Low-level input current</td>
<td>V(_{I\text{IN}}) at 0 V</td>
<td>0</td>
<td>−200</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>I(_{OS})(^{(3)})</td>
<td>Short-circuit output current</td>
<td>V(<em>{CC}) = 5.5 V, V(</em>{O}) = 0 V</td>
<td>±10</td>
<td>±60</td>
<td>mA</td>
</tr>
<tr>
<td>r(_{O})</td>
<td>Output resistance</td>
<td>V(<em>{CC}), V+, and V− = 0 V, V(</em>{O}) = ±2 V</td>
<td>300</td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td><strong>RECEIVER SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{OH})</td>
<td>High-level output voltage</td>
<td>I(_{OH}) = −1 mA</td>
<td>3.5</td>
<td>V(_{CC}) − 0.4</td>
<td>V</td>
</tr>
<tr>
<td>V(_{DL})</td>
<td>Low-level output voltage</td>
<td>I(_{DL}) = 1.6 mA</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V(_{IT\text{+}})</td>
<td>Positive-going input threshold voltage</td>
<td>V(<em>{CC}) = 5 V, T(</em>{A}) = 25°C</td>
<td>1.7</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>V(_{IT\text{−}})</td>
<td>Negative-going input threshold voltage</td>
<td>V(<em>{CC}) = 5 V, T(</em>{A}) = 25°C</td>
<td>0.8</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>V(_{v\text{sys}})</td>
<td>Input hysteresis (V(<em>{IT\text{+}}) − V(</em>{IT\text{−}}))</td>
<td>0.2</td>
<td>0.5</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>r(_{I})</td>
<td>Input resistance</td>
<td>V(_{I\text{IN}}) at ±3 V to ±25 V</td>
<td>3</td>
<td>5</td>
<td>7</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Test conditions are C\(_{1}\)–C\(_{4}\) = 0.1 \(\mu\)F at V\(_{CC}\) = 5 V ± 0.5 V.
\(^{(2)}\) All typical values are at V\(_{CC}\) = 5 V, and T\(_{A}\) = 25°C.
\(^{(3)}\) Pulse skew is defined as |t\(_{PLH}\) − t\(_{PHL}\)| of each channel of the same device.

6.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see Figure 10)\(^{(1)}\)

| PARAMETER                  | TEST CONDITIONS | MIN | TYP\(^{(2)}\) | MAX | UNIT | |
|---------------------------|-----------------|-----|-------------|-----|------| |
| **DRIVER SECTION**        |                 |     |             |     |      | |
| Maximum data rate         |                 |     |             |     |      | |
| I\(_{PLH\text{(D)}}\)     | Propagation delay time, low- to high-level output | C\(_{L}\) = 50 pF to 1000 pF, R\(_L\) = 3 k\(\Omega\) to 7 k\(\Omega\) one D\(_{OUT}\) switching, see Figure 6 | 120 |      | kbit/s |
| I\(_{PHL\text{(D)}}\)     | Propagation delay time, high- to low-level output | C\(_{L}\) = 2500 pF, R\(_L\) = 3 k\(\Omega\), all drivers loaded, see Figure 6 | 2   |      | \(\mu\)s |
| t\(_{sk(p)}\)\(^{(3)}\)   | Pulse skew     | C\(_{L}\) = 150 to 2500 pF, R\(_L\) = 3 k\(\Omega\) to 7 k\(\Omega\), see Figure 7 | 300 |      | ns   |
| **RECEIVER SECTION**      |                 |     |             |     |      | |
| I\(_{PLH\text{(R)}}\)     | Propagation delay time, low- to high-level output | C\(_{L}\) = 150 pF | 0.5 | 10   | \(\mu\)s |
| I\(_{PHL\text{(R)}}\)     | Propagation delay time, high- to low-level output | C\(_{L}\) = 150 pF | 0.5 | 10   | \(\mu\)s |
| t\(_{sk(p)}\)\(^{(3)}\)   | Pulse skew     | C\(_{L}\) = 150 pF | 300 |      | ns   |

\(^{(1)}\) Test conditions are C\(_{1}\)–C\(_{4}\) = 0.1 \(\mu\)F at V\(_{CC}\) = 5 V ± 0.5 V.
\(^{(2)}\) All typical values are at V\(_{CC}\) = 5 V, and T\(_{A}\) = 25°C.
\(^{(3)}\) Pulse skew is defined as |I\(_{PLH}\) − I\(_{PHL}\)| of each channel of the same device.
6.7 Typical Characteristics
at \( T_A = 25^\circ\text{C} \) (unless otherwise noted)

![Figure 1. Receiver VOL vs Output Current](image1.png)

![Figure 2. Receiver VOH vs Output Current](image2.png)

![Figure 3. Driver VOL vs Output Current](image3.png)

![Figure 4. Driver VOH vs Output Current](image4.png)

![Figure 5. Driver and Receiver Loopback Waveforms](image5.png)
7 Parameter Measurement Information

A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR = 120$ kbit/s, $Z_O = 50 \, \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

**Figure 6. Driver Slew Rate**

A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $PRR = 120$ kbit/s, $Z_O = 50 \, \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

**Figure 7. Driver Pulse Skew**

A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \, \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

**Figure 8. Receiver Propagation Delay Times**
8 Detailed Description

8.1 Overview
The MAX202 device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to ±30-V inputs and decode inputs as low as ±3 V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

8.2 Functional Block Diagram

![Functional Block Diagram](image)

8.3 Feature Description

8.3.1 Power
The power block increases and inverts the 5-V supply for the RS-232 driver using a charge pump that requires four 0.1-µF external capacitors.

8.3.2 RS-232 Driver
Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

8.3.3 RS-232 Receiver
Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-kΩ load to ground. An open input results in a high output on ROUT.

8.4 Device Functional Modes

8.4.1 $V_{CC}$ Powered by 5-V
The device is in normal operation when powered by 5 V.

8.4.2 $V_{CC}$ Unpowered
When MAX202 is unpowered, it can be safely connected to an active remote RS-232 device.
Device Functional Modes (continued)

8.4.3 Truth Tables

Table 1 and Table 2 list the function for each driver and receiver (respectively).

Table 1. Function Table for Each Driver\(^{(1)}\)

<table>
<thead>
<tr>
<th>INPUT DIN</th>
<th>OUTPUT DOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

\(^{(1)}\) H = high level, L = low level

Table 2. Function Table for Each Receiver\(^{(1)}\)

<table>
<thead>
<tr>
<th>INPUT RIN</th>
<th>OUTPUT ROUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Open</td>
<td>H</td>
</tr>
</tbody>
</table>

\(^{(1)}\) H = high level, L = low level, Open = input disconnected or connected driver off

Figure 9. Logic Diagram (Positive Logic)
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
For proper operation, add capacitors as shown in Figure 10. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

9.2 Typical Application

A. C3 can be connected to VCC or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

Figure 10. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements
• VCC minimum is 4.5 V and maximum is 5.5 V.
• Maximum recommended bit rate is 120 kbps.
Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The MAX202 requires 0.1-µF capacitors. Capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V+ and V–.

Bypass VCC to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple VCC to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

9.2.2.2 ESD Protection

MAX202 devices have standard ESD protection structures incorporated on all pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

9.2.2.3 ESD Test Conditions

Stringent ESD testing is performed by TI based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

9.2.2.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 11. Figure 12 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

![Figure 11. HBM ESD Test Circuit](image-url)
Typical Application (continued)

![Waveform Diagram]

**Figure 12. Typical HBM Current Waveform**

9.2.3 Application Curve

![Waveform Diagram]

120 kbit/s, 1-nF load

**Figure 13. Driver and Receiver Loopback Signal**
10 Power Supply Recommendations

The \( V_{CC} \) voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. \( V_{CC} \) must be between 4.5 V and 5.5 V.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. For best ESD performance, make the impedance from MAX202 ground pin to the ground plane of the circuit board as low as possible. Use wide metal and multiple vias on both sides of ground pin.

11.2 Layout Example

![Figure 14. MAX202 Circuit Board Layout](image-url)
12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™ Online Community TI’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
<tr>
<td>MAX202CDW</td>
<td>LIFEBUY</td>
<td>SOIC</td>
<td>DW</td>
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<td>40</td>
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<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>MAX202C</td>
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<td>-40 to 85</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  ≤1000ppm threshold. Antimony trioxide based flame retardants must also meet the  ≤1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
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TAPE AND REEL INFORMATION

**PACKAGE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**TAPE DIMENSIONS**

- **A0**: Cavity
- **B0**: Cavity
- **K0**: Cavity
- **W**: Cavity

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**: Pocket Quadrant
- **Q2**: Pocket Quadrant
- **Q3**: Pocket Quadrant
- **Q4**: Pocket Quadrant

**User Direction of Feed**

*All dimensions are nominal*

<table>
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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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</tbody>
</table>
TUBE

- **T** - Tube length
- **W** - Tube width
- **T** - Tube height
- **B** - Alignment groove width

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
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<th>Package Type</th>
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<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
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<td>506.98</td>
<td>12.7</td>
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<td>6.6</td>
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</tbody>
</table>
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AC.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

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