

## 5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

### FEATURES

- ESD Protection for RS-232 I/O Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V  $V_{CC}$  Supply
- Four Drivers and Four Receivers
- Operates up to 120 kbit/s
- External Capacitors:  $4 \times 0.1 \mu\text{F}$
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

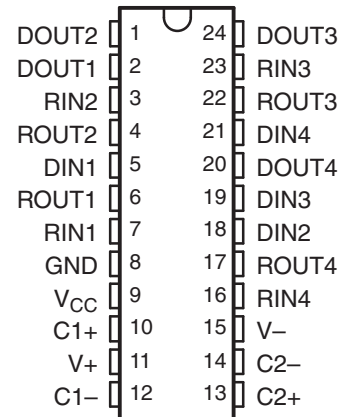
### APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

### DESCRIPTION

The MAX208 device consists of four line drivers, four line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV HBM ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The devices operate at data signaling rates up to 120 kbit/s and a maximum of  $30\text{-V}/\mu\text{s}$  driver output slew rate.

DB OR DW PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	MAX208CDW
		Reel of 2000	MAX208CDWR
	SSOP – DB	Tube of 60	MAX208CDB
		Reel of 2000	MAX208CDBR
–40°C to 85°C	SOIC – DW	Tube of 25	MAX208IDW
		Reel of 2000	MAX208IDWR
	SSOP – DB	Tube of 60	MAX208IDB
		Reel of 2000	MAX208IDBR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE  
EACH DRIVER<sup>(1)</sup>**

INPUT DIN	OUTPUT DOUT
L	H
H	L

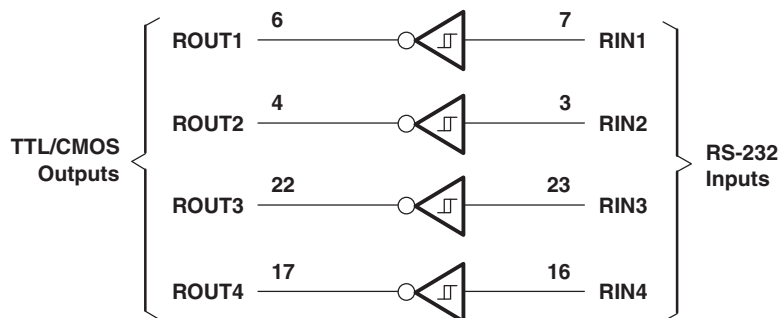
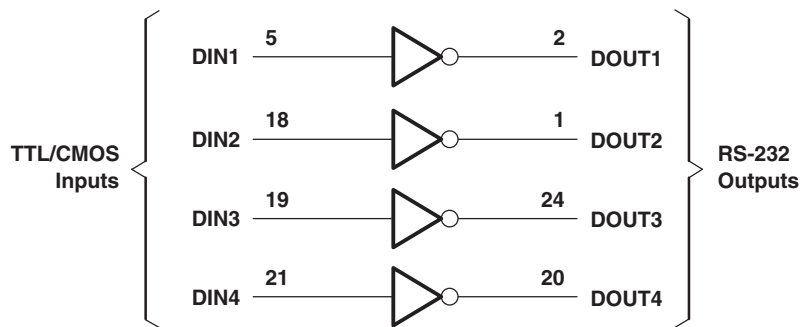
(1) H = high level, L = low level

**FUNCTION TABLE  
EACH RECEIVER<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,  
Open = input disconnected or  
connected driver off

**logic diagram (positive logic)**



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

$V_{CC}$	Supply voltage range <sup>(2)</sup>		–0.3 V to 6 V
V+	Positive charge pump voltage range <sup>(2)</sup>		$V_{CC} - 0.3$ V to 14 V
V–	Negative charge pump voltage range <sup>(2)</sup>		–14 V to 0.3 V
V+ – V–	Supply voltage difference <sup>(2)</sup>		13 V
$V_I$	Input voltage range	Drivers	–0.3 V to V+ + 0.3 V
		Receivers	±30 V
$V_O$	Output voltage range	Drivers	V– – 0.3 V to V+ + 0.3 V
		Receivers	–0.3 V to $V_{CC} + 0.3$ V
	Short-circuit duration on DOUT		Continuous
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>	DB package	63°C/W
		DW package	46°C/W
$T_J$	Operating virtual-junction temperature		150°C
$T_{stg}$	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

(3) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V (see [Figure 4](#))

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$V_{IH}$	Driver high-level input voltage	DIN	2			V
$V_{IL}$	Driver low-level input voltage	DIN			0.8	V
$V_I$	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage		–30		30	
$T_A$	Operating free-air temperature	MAX208C	0		70	°C
		MAX208I	–40		85	

## ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V (see [Figure 4](#)), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}$	Supply current	No load, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$		11	20	mA

## DRIVER SECTION

### ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (see [Figure 4](#)), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = GND	5	9		V
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = $V_{CC}$	-5	-9		V
$I_{IH}$	High-level input current	$V_I = V_{CC}$		15	200	$\mu$ A
$I_{IL}$	Low-level input current	$V_I = 0\text{ V}$		-15	-200	$\mu$ A
$I_{OS}$	Short-circuit output current <sup>(1)</sup>	$V_{CC} = 5.5\text{ V}$ , $V_O = 0\text{ V}$		$\pm 10$	$\pm 60$	mA
$r_o$	Output resistance	$V_{CC}$ , $V_+$ , and $V_- = 0\text{ V}$ , $V_O = \pm 2\text{ V}$	300			$\Omega$

(1) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### SWITCHING CHARACTERISTICS

C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (see [Figure 4](#)), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Maximum data rate	$C_L = 50$ to $1000\text{ pF}$ , One DOUT switching, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See <a href="#">Figure 1</a>	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output $C_L = 2500\text{ pF}$ , All drivers loaded, $R_L = 3\text{ k}\Omega$ , See <a href="#">Figure 1</a>		2		$\mu$ s
$t_{PHL(D)}$	Propagation delay time, high- to low-level output $C_L = 2500\text{ pF}$ , All drivers loaded, $R_L = 3\text{ k}\Omega$ , See <a href="#">Figure 1</a>		2		$\mu$ s
$t_{sk(p)}$	Pulse skew <sup>(2)</sup> $C_L = 150\text{ pF}$ to $2500\text{ pF}$ , See <a href="#">Figure 2</a>		300		ns
SR(tr)	Slew rate, transition region (see <a href="#">Figure 1</a> ) $C_L = 50\text{ pF}$ to $2500\text{ pF}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $V_{CC} = 5\text{ V}$	3	6	30	V/ $\mu$ s

(1) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

### ESD PROTECTION

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	$\pm 15$	kV

## RECEIVER SECTION

### ELECTRICAL CHARACTERISTICS

C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (see [Figure 4](#)), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{ mA}$	3.5			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1.6\text{ mA}$			0.4	V
$V_{IT+}$	Positive-going input threshold voltage	$V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$		1.7	2.4	V
$V_{IT-}$	Negative-going input threshold voltage	$V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$	0.8	1.2		V
$V_{hys}$	Input hysteresis ( $V_{IT+} - V_{IT-}$ )	$V_{CC} = 5\text{ V}$	0.2	0.5	1	V
$r_i$	Input resistance	$V_I = \pm 3\text{ V to } \pm 25\text{ V}, V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$	3	5	7	k $\Omega$

### SWITCHING CHARACTERISTICS

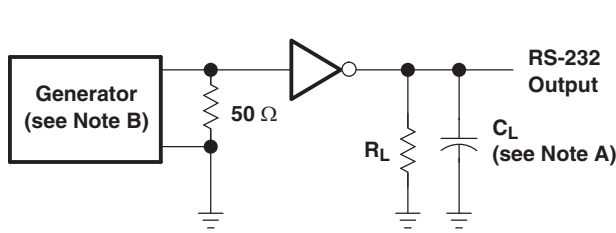
C1 to C4 = 0.1  $\mu$ F at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (see [Figure 4](#)), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	$C_L = 150\text{ pF}$		0.5	10	$\mu$ s
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	$C_L = 150\text{ pF}$		0.5	10	$\mu$ s
$t_{sk(p)}$	Pulse skew <sup>(2)</sup>			300		ns

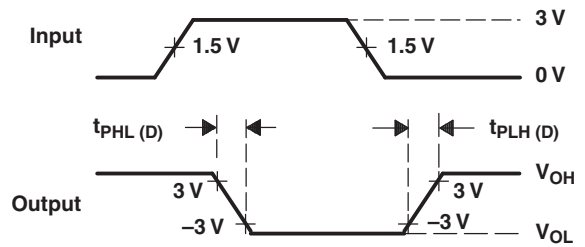
(1) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

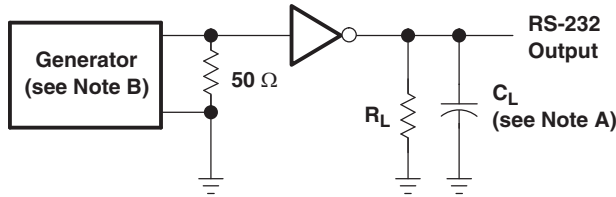


VOLTAGE WAVEFORMS

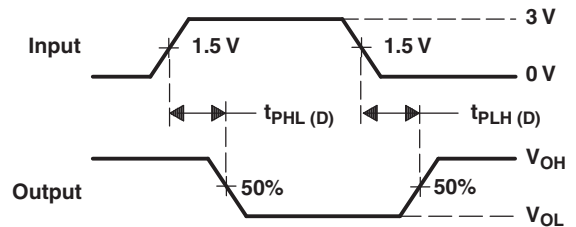
$$SR(tr) = \frac{6\text{ V}}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  
 PRR = 120 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 1. Driver Slew Rate



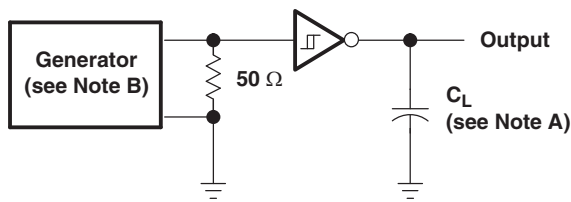
TEST CIRCUIT



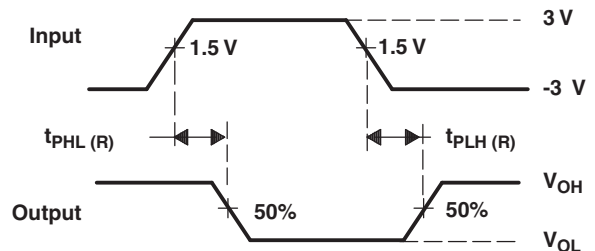
VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  
 PRR = 120 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 2. Driver Pulse Skew



TEST CIRCUIT

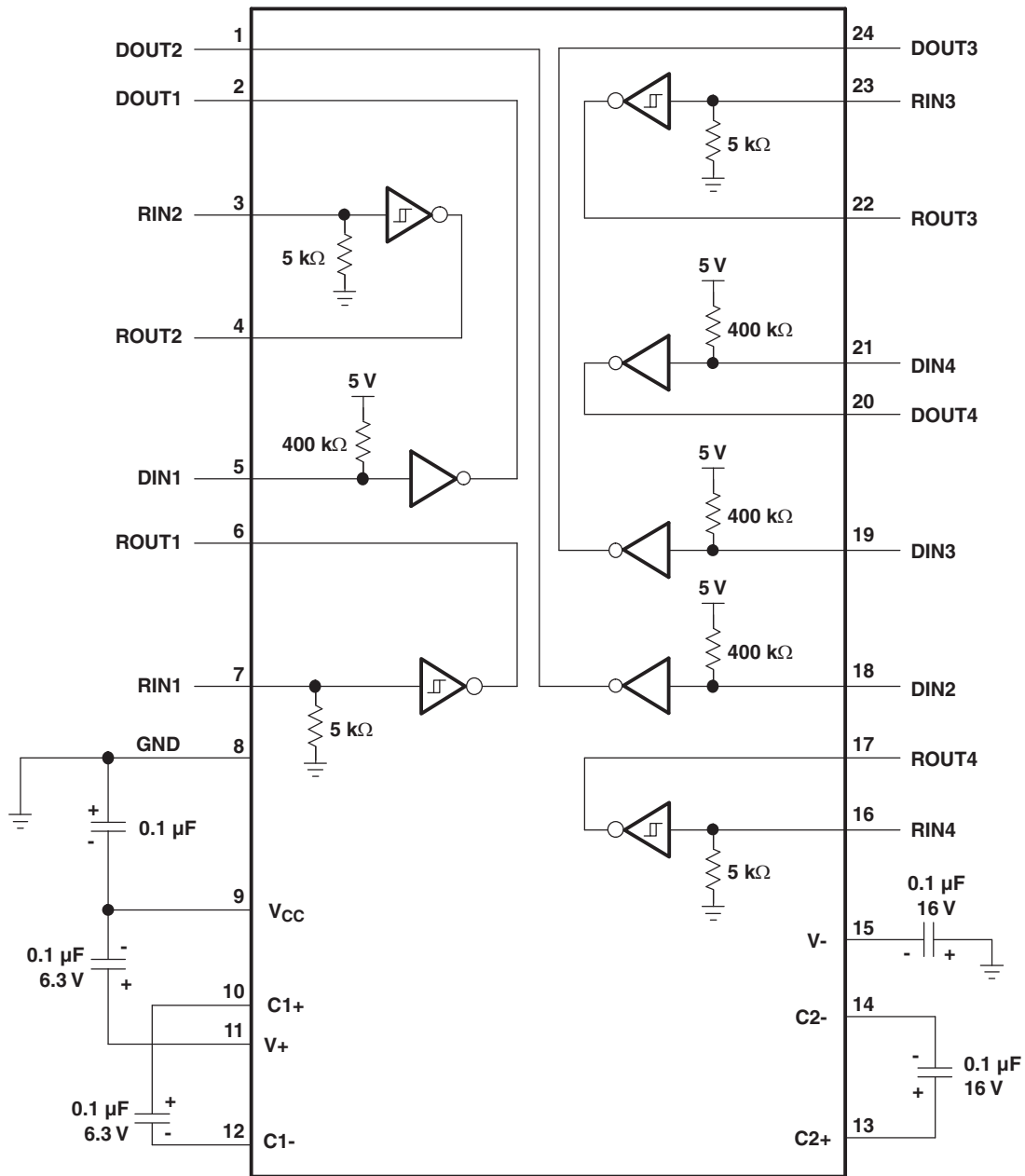


VOLTAGE WAVEFORMS

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



- A. Resistor values shown are nominal.
- B. Non-polarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

## Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX208 requires 0.1- $\mu\text{F}$  capacitors, although capacitors up to 10  $\mu\text{F}$  can be used without harm. Ceramic dielectrics are suggested for the 0.1- $\mu\text{F}$  capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10  $\mu\text{F}$ ) to reduce the output impedance at V+ and V–.

Bypass  $V_{\text{CC}}$  to ground with at least 0.1  $\mu\text{F}$ . In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{\text{CC}}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

## ESD Protection

TI MAX208 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$  kV when powered down.

## ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

## Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5-k $\Omega$  resistor.

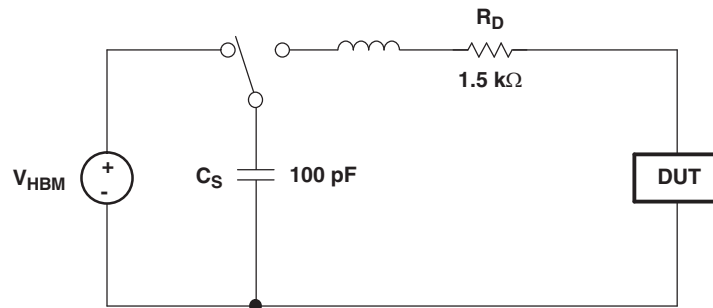
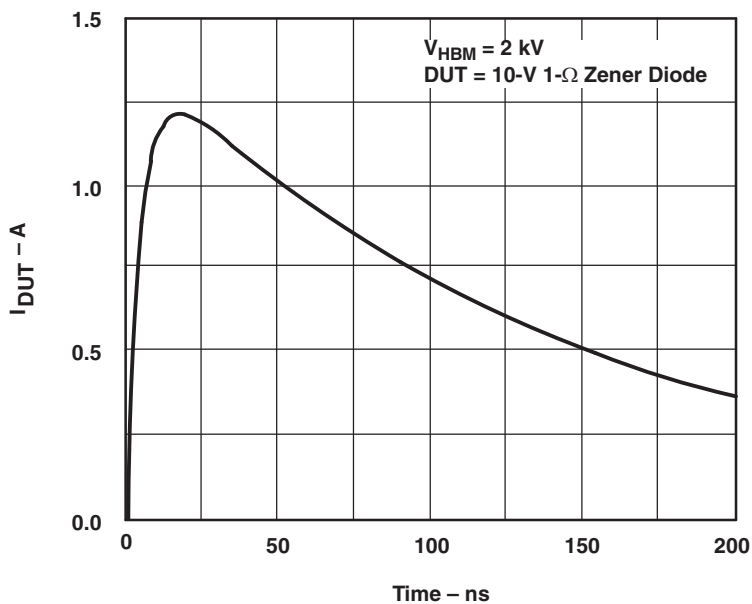


Figure 5. HBM ESD Test Circuit





**Figure 6. Typical HBM Current Waveform**

**Machine Model (MM)**

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">MAX208CDBR</a>	Obsolete	Production	SSOP (DB)   24	-	-	Call TI	Call TI	0 to 70	MA208C
<a href="#">MAX208CDW</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX208C
MAX208CDW.Z	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208C
<a href="#">MAX208CDWR</a>	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX208C
<a href="#">MAX208IDB</a>	Obsolete	Production	SSOP (DB)   24	-	-	Call TI	Call TI	-40 to 85	MB208I
<a href="#">MAX208IDBR</a>	Obsolete	Production	SSOP (DB)   24	-	-	Call TI	Call TI	-40 to 85	MB208I
<a href="#">MAX208IDW</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I
MAX208IDW.Z	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I
<a href="#">MAX208IDWR</a>	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX208I

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX208CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
MAX208IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX208CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
MAX208IDWR	SOIC	DW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX208CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
MAX208CDW.Z	DW	SOIC	24	25	506.98	12.7	4826	6.6
MAX208IDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
MAX208IDW.Z	DW	SOIC	24	25	506.98	12.7	4826	6.6

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.



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