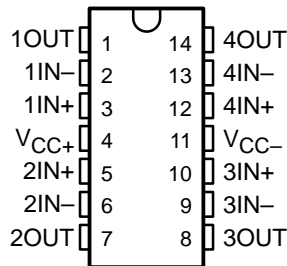


MC3303, MC3403 QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

- Wide Range of Supply Voltages, Single Supply . . . 3 V to 36 V or Dual Supplies
- Class AB Output Stage
- True Differential Input Stage
- Low Input Bias Current
- Internal Frequency Compensation
- Short-Circuit Protection
- Designed to Be Interchangeable With Motorola MC3303, MC3403

MC3303 . . . D, N, OR PW PACKAGE
MC3403 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the μ A741, but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to $V_{CC} - 1.5$ V. Quiescent supply currents are less than one-half those of the μ A741.

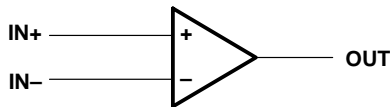
The MC3303 is characterized for operation from -40°C to 85°C , and the MC3403 is characterized for operation from 0°C to 70°C .

AVAILABLE OPTIONS

T_A	$V_{IO\text{MAX}}$ AT 25°C	PACKAGE			
		PLASTIC SMALL OUTLINE (D, NS)	PLASTIC SHRINK SMALL OUTLINE (DB)	PLASTIC DIP (N)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)
0°C to 70°C	10 mV	MC3403D MC3403NS	MC3403DB	MC3403N	MC3403PW
-40°C to 85°C	8 mV	MC3303D	—	MC3303N	MC3303PW

The D package is available taped and reeled. Add R suffix to the device type (e.g., MC3403DR). The DB, NS, and PW packages are only available taped and reeled.

logic diagram (each amplifier)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

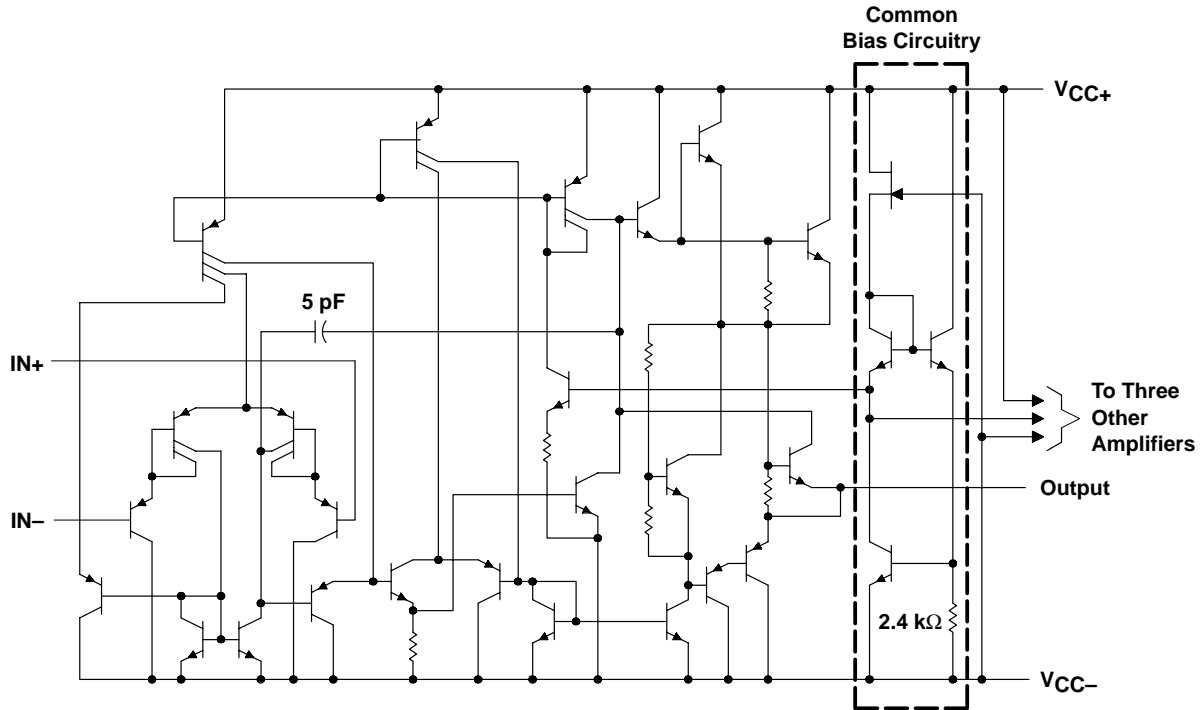
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

MC3303, MC3403 QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}	18 V
V_{CC-}	-18 V
Supply voltage, V_{CC+} with respect to V_{CC-}	36 V
Differential input voltage (see Note 2)	± 36 V
Input voltage (see Notes 1 and 3)	± 18 V
Package thermal impedance, θ_{JA} (see Note 4):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-} .
 4. The package thermal impedance is calculated in accordance with JESD 51-7.

MC3303, MC3403

QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

recommended operating conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	5	30	V	
Dual-supply voltage		V _{CC+}	2.5	15	V
		V _{CC-}	-2.5	-15	V
T _A	Operating free-air temperature	MC3303	-40	85	°C
		MC3403	0	70	

electrical characteristics at specified free-air temperature, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303, V_{CC±} = ±15 V for MC3403 (unless otherwise noted)

PARAMETER	TEST CONDITION†	MC3303			MC3403			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
V _{IO}	Input offset voltage	See Note 5	25°C	2	8	2	10	mV		
				Full range	10	12				
α _{VIO}	Temperature coefficient of input offset voltage	See Note 5	Full range	10	10	10	10	μV/°C		
I _{IO}	Input offset current	See Note 5	25°C	30	75	30	50	nA		
				Full range	250	200				
α _{IIO}	Temperature coefficient of input offset current	See Note 5	Full range	50	50	50	50	pA/C		
I _{IB}	Input bias current	See Note 5	25°C	-0.2	-0.5	-0.2	-0.5	μA		
				Full range	-1	-0.8				
V _{ICR}	Common-mode input voltage range‡		25°C	V _{CC-} to 12	V _{CC-} to 12.5	V _{CC-} to 13	V _{CC-} to 13.5	V		
V _{OM}	Peak output voltage swing	R _L = 10 kΩ	25°C	12	12.5	±12	±13.5	V		
			25°C	10	12	±10	±13			
			Full range	10	±10					
A _{VD}	Large-signal differential voltage amplification	V _O = ±10 V, R _L = 2 kΩ	25°C	20	200	20	200	V/mV		
			Full range	15	15					
B _{OM}	Maximum-output-swing bandwidth	V _{OPP} = 20 V, A _{VD} = 1, THD ≤ 5%, R _L = 2 kΩ	25°C	9	9	9	9	kHz		
B ₁	Unity-gain bandwidth	V _O = 50 mV, R _L = 10 kΩ	25°C	1	1	1	1	MHz		
φ _m	Phase margin	C _L = 200 pF, R _L = 2 kΩ	25°C	60°	60°	60°	60°			
r _i	Input resistance	f = 20 Hz	25°C	0.3	1	0.3	1	MΩ		
r _o	Output resistance	f = 20 Hz	25°C	75	75	75	75	Ω		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	25°C	70	90	70	90	dB		
k _{SVS}	Supply voltage sensitivity (ΔV _{IO} /ΔV _{CC})	V _{CC±} = ±2.5 to ±15 V	25°C	30	150	30	150	μV/V		
I _{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I _{CC}	Total supply current	No load, See Note 5	25°C	2.8	7	2.8	7	mA		

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is -40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡ The V_{ICR} limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V_{CC+}.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 5: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403 and V_O = 7 V for MC3303.



MC3303, MC3403 QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MC3303			MC3403			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input offset voltage	$V_O = 2.5\text{ V}$			10	2	10	mV	
I_{IO}	Input offset current	$V_O = 2.5\text{ V}$			75	30	50	nA	
I_{IB}	Input bias current	$V_O = 2.5\text{ V}$			-0.5	-0.2	-0.5	μA	
V_{OM}	Peak output voltage swing‡	$R_L = 10\text{ k}\Omega$			3.3	3.5	3.3	3.5	V
		$R_L = 10\text{ k}\Omega$, $V_{CC+} = 5\text{ V to }30\text{ V}$			$V_{CC+} - 1.7$		$V_{CC+} - 1.7$		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1.7\text{ V to }3.3\text{ V}$, $R_L = 2\text{ k}\Omega$			20	200	20	200	V/mV
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$			150			$\mu\text{V/V}$	
I_{CC}	Supply current	$V_O = 2.5\text{ V}$, No load			2.5	7	2.5	7	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$f = 1\text{ kHz to }20\text{ kHz}$			120		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Output will swing essentially to ground.

operating characteristics, $V_{CC+} = 14\text{ V}$, $V_{CC-} = 0\text{ V}$ for MC3303, $V_{CC\pm} = \pm 15\text{ V}$ for MC3403, $T_A = 25^\circ\text{C}$, $A_{VD} = 1$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP	UNIT	
SR	Slew rate at unity gain	$V_I = \pm 10\text{ V}$,	$C_L = 100\text{ pF}$,	$R_L = 2\text{ k}\Omega$,	See Figure 1	0.6	V/ μs
t_r	Rise time	$\Delta V_O = 50\text{ mV}$,	$C_L = 100\text{ pF}$,	$R_L = 10\text{ k}\Omega$,	See Figure 1	0.35	μs
t_f	Fall time	$\Delta V_O = 50\text{ mV}$,	$C_L = 100\text{ pF}$,	$R_L = 10\text{ k}\Omega$,	See Figure 1	0.35	μs
	Overshoot factor	$\Delta V_O = 50\text{ mV}$,	$C_L = 100\text{ pF}$,	$R_L = 10\text{ k}\Omega$,	See Figure 1	20	%
	Crossover distortion	$V_I(PP) = 30\text{ mV}$,	$V_{OPP} = 2\text{ V}$,	$f = 10\text{ kHz}$		1	%

PARAMETER MEASUREMENT INFORMATION

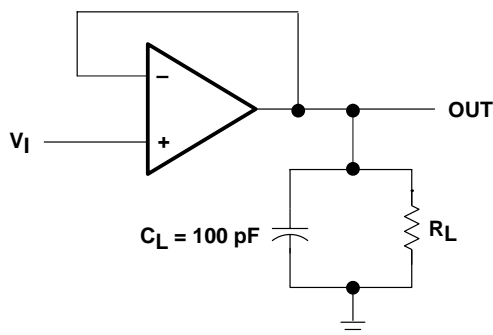


Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

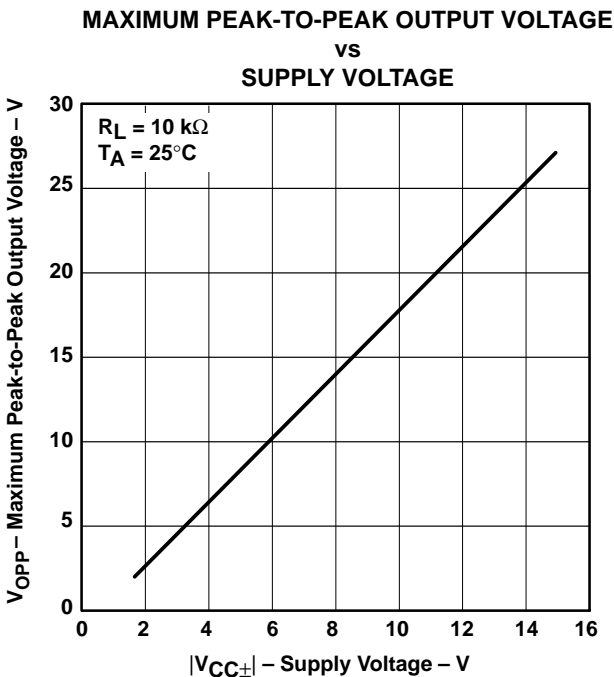


Figure 2

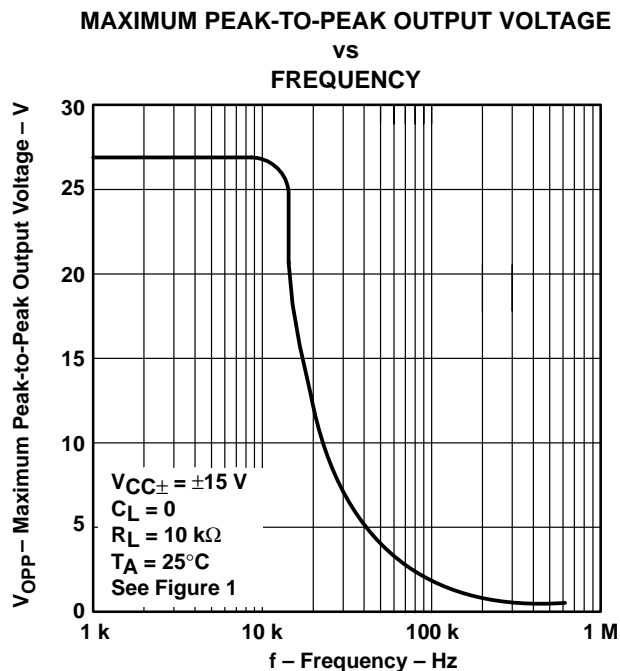


Figure 3

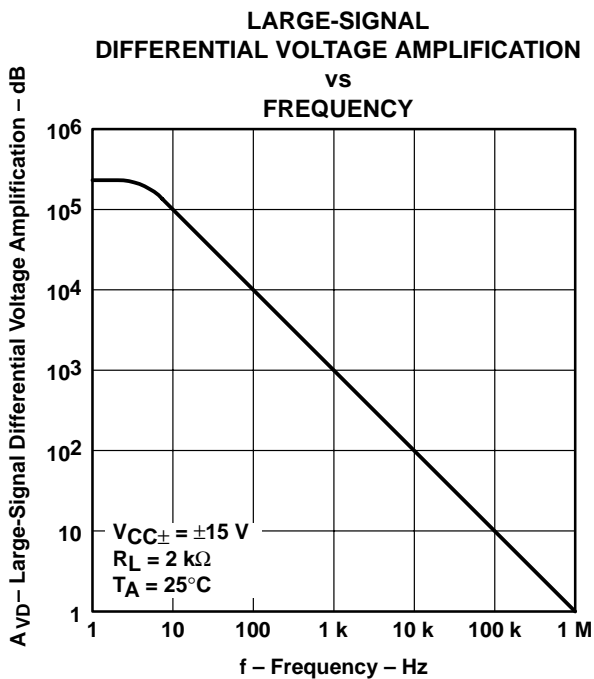


Figure 4

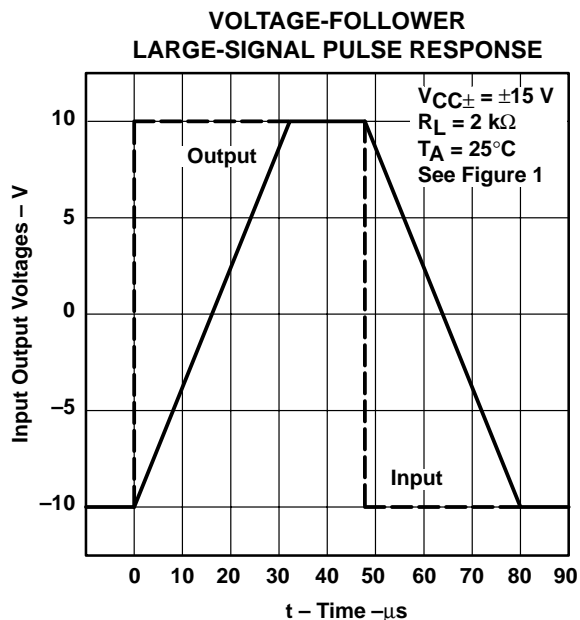


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

MC3303, MC3403 QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

TYPICAL CHARACTERISTICS†

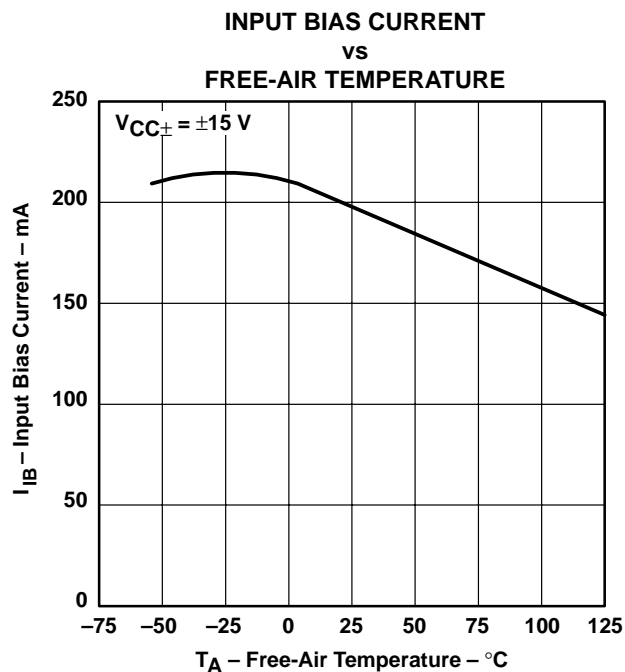


Figure 6

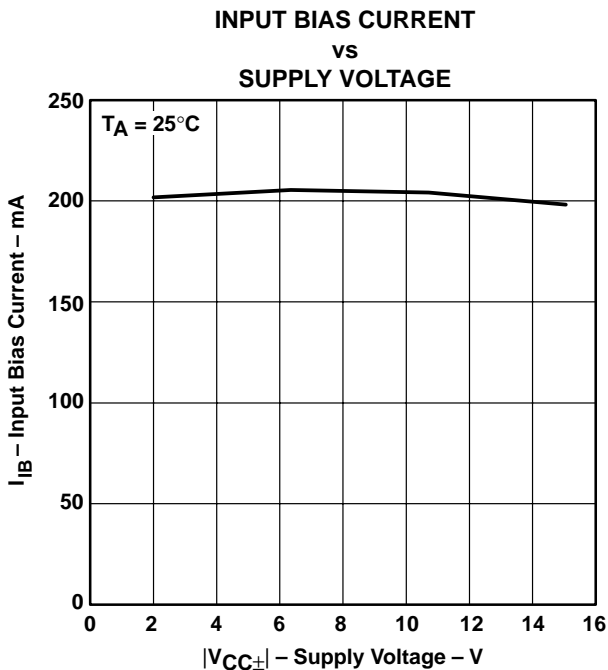


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3303D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	MC3303	
MC3303DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MC3303	Samples
MC3303N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	MC3303N	Samples
MC3303PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	M3303	
MC3303PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M3303	Samples
MC3403D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	MC3403	
MC3403DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3403	Samples
MC3403N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3403N	Samples
MC3403NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3403	Samples
MC3403PWR	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	M3403	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3303DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3303PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MC3403DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3403NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3303DR	SOIC	D	14	2500	356.0	356.0	35.0
MC3303PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
MC3403DR	SOIC	D	14	2500	353.0	353.0	32.0
MC3403NSR	SO	NS	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MC3303N	N	PDIP	14	25	506	13.97	11230	4.32
MC3403N	N	PDIP	14	25	506	13.97	11230	4.32

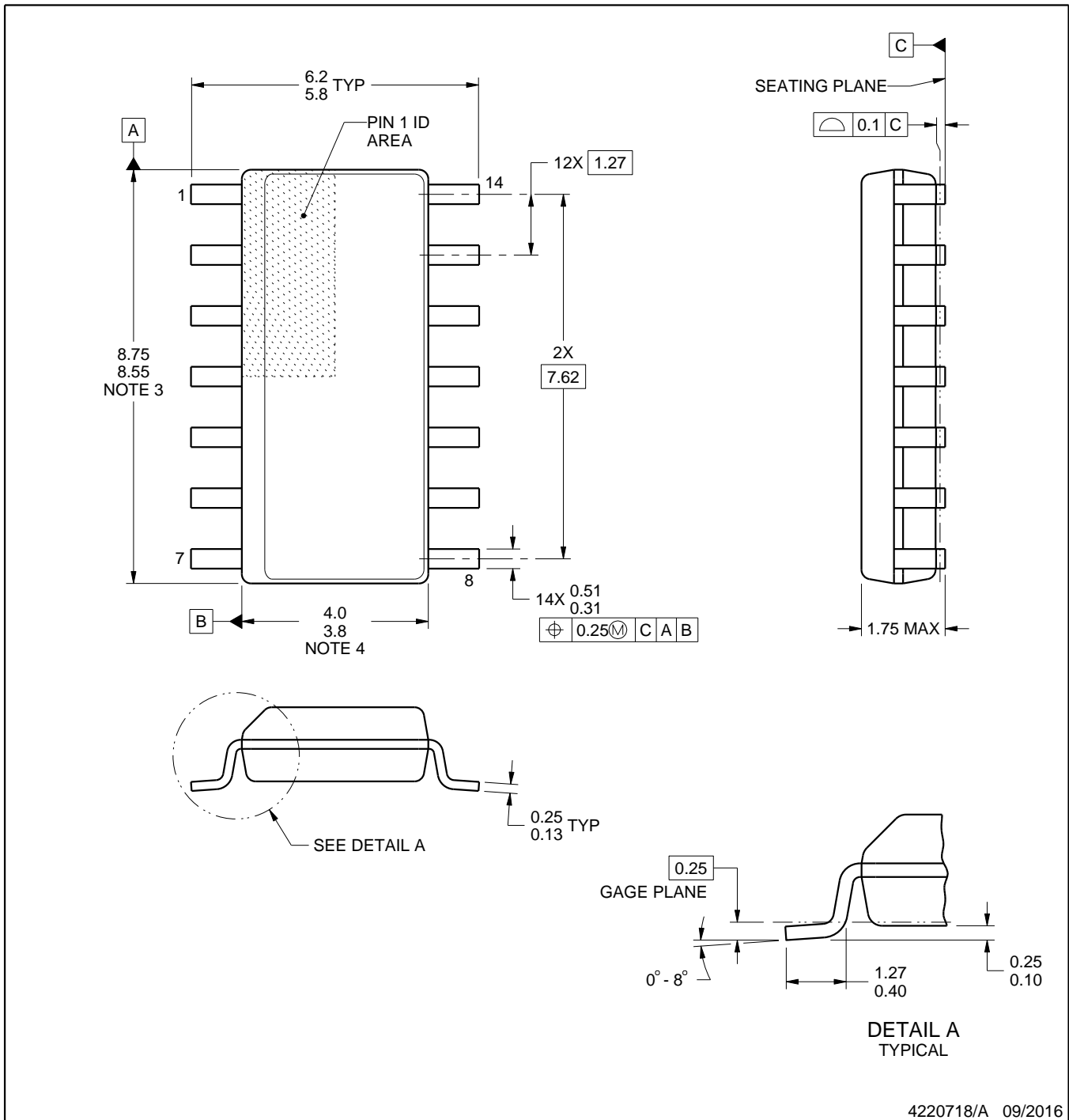
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

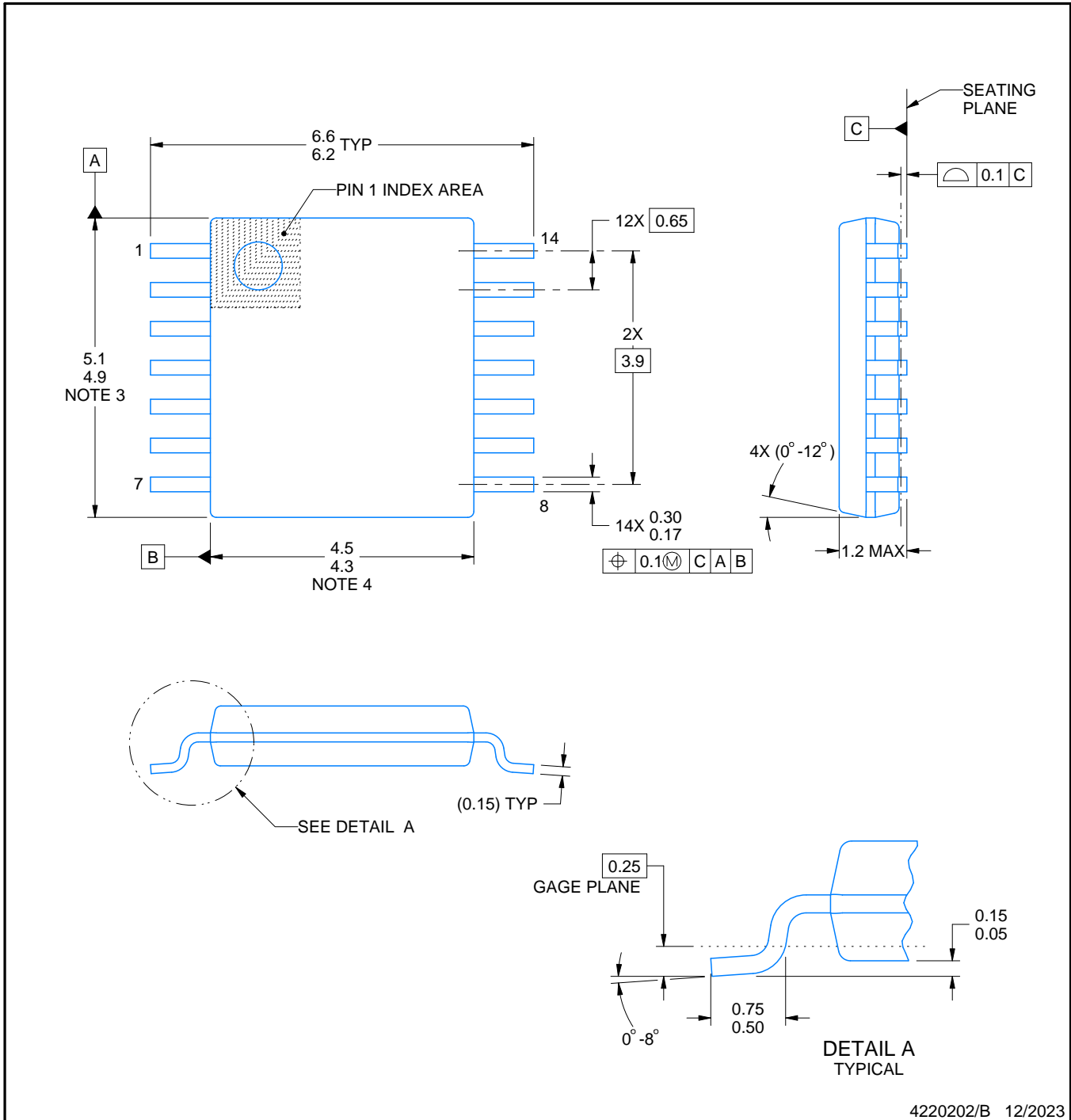
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

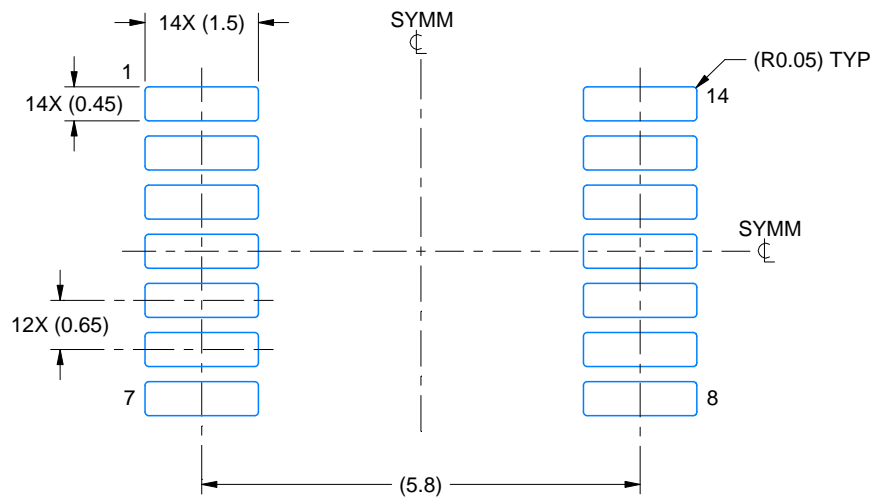
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

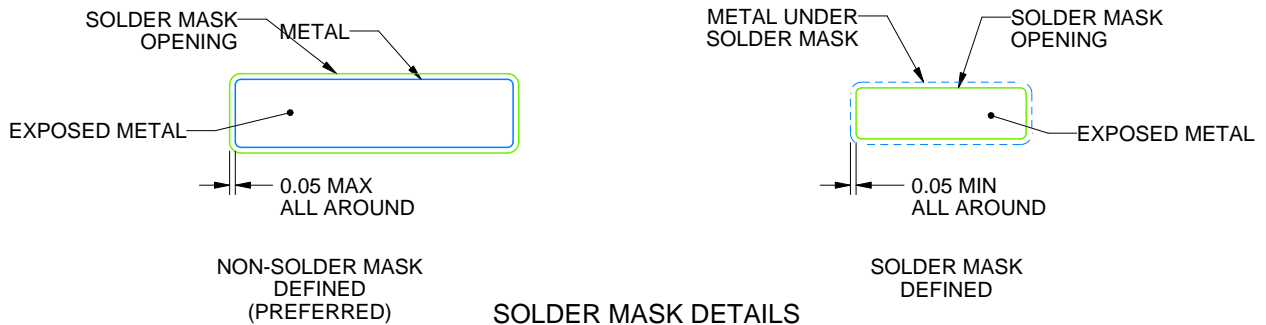
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

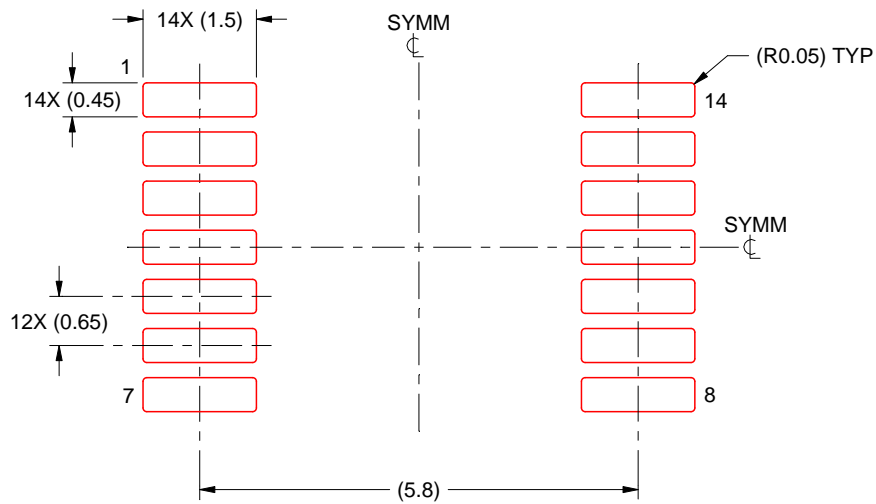
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated